Data Sheet | December 8, 2008 | FN6775.0

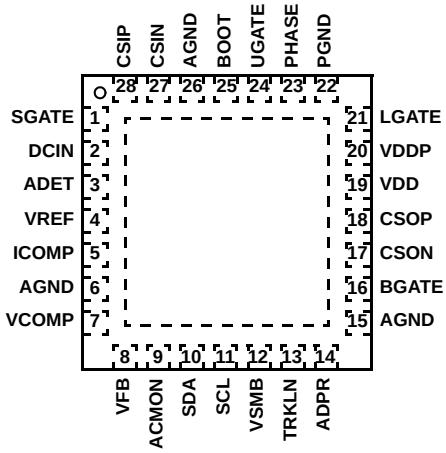
Narrow VDC Regulator/Charger with SMBus Interface

The ISL9518, ISL9518A are highly integrated Narrow VDC system voltage regulators and battery charger controllers. Operating parameters are programmable over the System Management Bus (SMBus). The ISL9518, ISL9518A are designed for applications where the system power source is either the battery pack or the output of the regulator/charger. This makes the max voltage to the system equal to the max battery voltage instead of the max adapter voltage. The ISL9518, ISL9518A also include a system to control trickle charging deeply discharged batteries while maintaining system voltage at a user defined minimum. High efficiency is achieved with a DC/DC synchronous-rectifier buck converter, equipped with diode emulation for enhanced light load efficiency and AC-adapter boosting prevention. The ISL9518, ISL9518A can charge two to four series connected Lithium-ion cells, at up to 8A charge current. The ISL9518 has default settings for 2-cell systems and the ISL9518A has default settings for 3-cell systems. Integrated MOSFET drivers and bootstrap diode result in fewer components and smaller implementation area. Low offset current-sense amplifiers provide high accuracy.

The ISL9518, ISL9518A provide two open drain digital outputs that indicate the presence of the AC adapter and trickle charge state. Trickle charge state and AC adapter present indicators are also available via SMBus. The ISL9518, ISL9518A also provide two analog outputs that indicate the adapter current and battery discharge current with 4% accuracy.

Pinout

ISL9518, ISL9518A
(28 LD TQFN)
TOP VIEW



Features

- ±0.5% System Voltage Accuracy (-10°C to +100°C)
- ±3% Accurate Input Current Limit
- ±3% Accurate Battery Charge Current Limit
- Switching Frequency can be Reduced via SMBus for Higher Efficiency at Light Load Conditions
- Trickle Charge System for Deeply Discharged Batteries
  - Automatic Trickle Charge Current (256mA)
  - Holds Minimum Voltage to System
- SMBus 2-Wire Serial Interface
- Battery Short Circuit Protection
- Fast System-Load Transient Response
- Monitor Outputs
  - Adapter Current (2.5% Accuracy)
  - Trickle Charge Mode Indicator
  - AC-Adapter Present Indicator
- 11-Bit Max System Voltage Setting
- 7-Bit Min System Voltage Setting
- 6-Bit Charge Current Setting
- 6-Bit Adapter Current Setting
- Over 8A Battery Charger Current
- Over 8A Maximum Adapter Current
- +8V to +22V Adapter Voltage Range
- Pb-Free (RoHS Compliant)

Applications

- Notebook Computers
- Tablet PCs
- Portable Equipment with Rechargeable Batteries

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9518HRTZ*	951 8HRTZ	-10 to +100	28 Ld 4x4 TQFN	L28.4x4A
ISL9518AHRTZ*	951 8AHRTZ	-10 to +100	28 Ld 4x4 TQFN	L28.4x4A

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

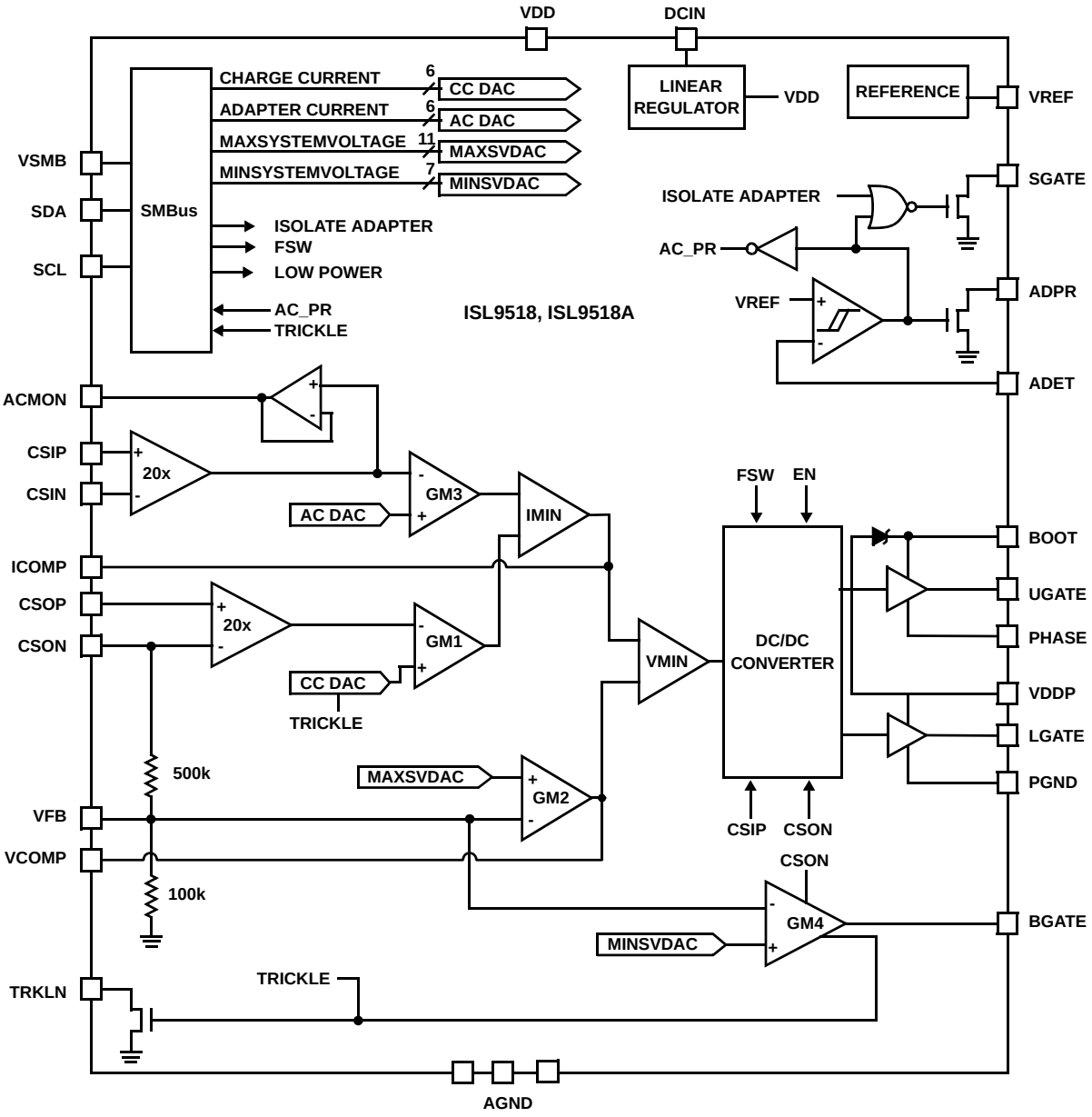


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

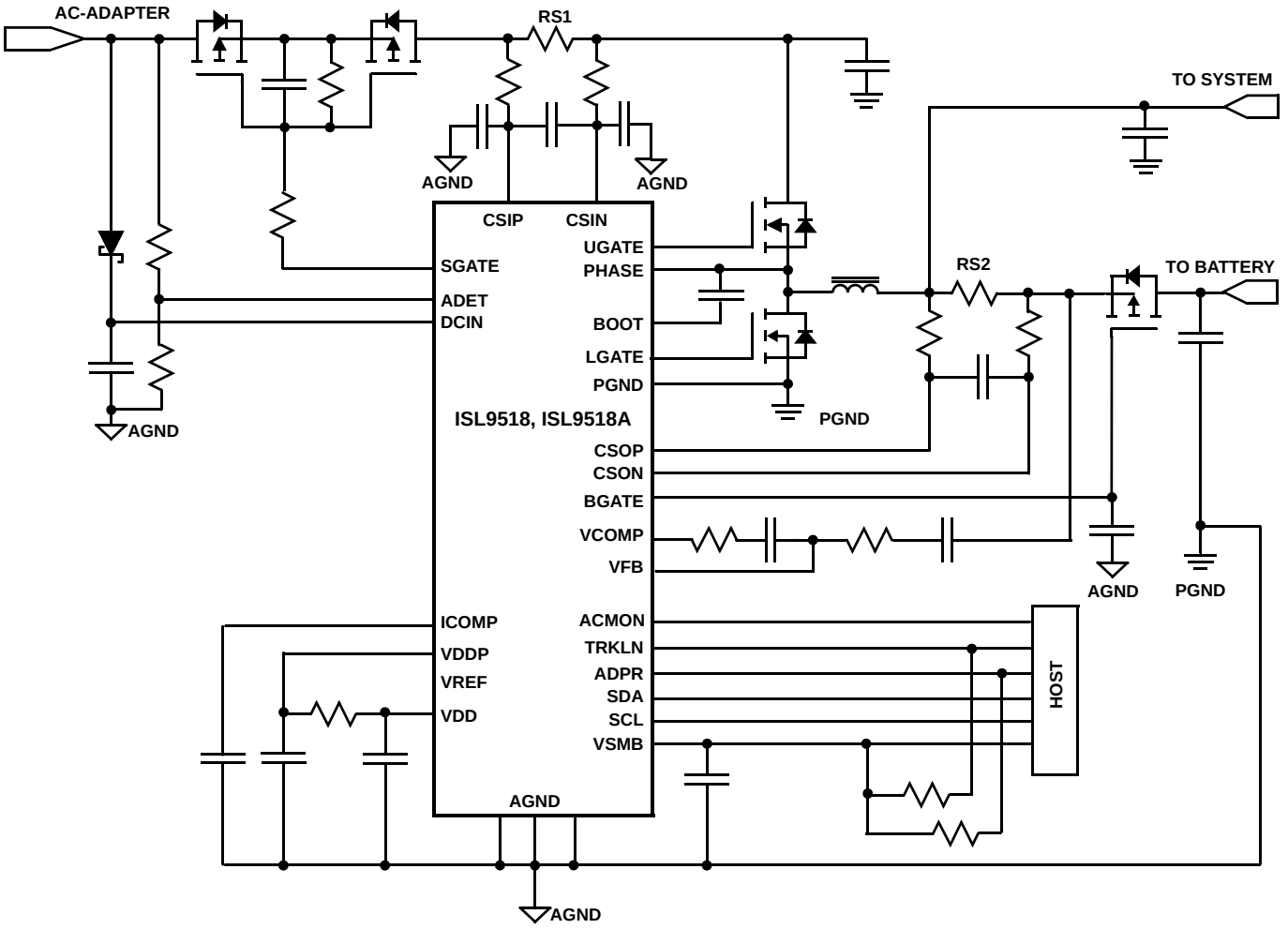


FIGURE 2. TYPICAL APPLICATION CIRCUIT

Absolute Maximum Ratings

DCIN, CSIP, CSON, SGATE . . . . . -0.3V to +28V
CSIP-CSIN, CSOP-CSON, PGND-AGND . . . . . -0.3V to +0.3V
PHASE . . . . . -6V to +30V
BOOT . . . . . -0.3V to +33V
BOOT to PHASE . . . . . -0.3V to +6V
BOOT to VDDP . . . . . PGND - 1.5V to 28V
UGATE . . . . . PHASE - 0.3V to BOOT + 0.3V
LGATE . . . . . PGND - 0.3V to VDDP + 0.3V
ACMON, ICOMP, VCOMP, VREF, VFB . . . . . -0.3V to VDD + 0.3V
VSMB, SCL, SDA, ADET, ADPR, TRKLN . . . . . -0.3V to +6V
VDDP, VDD to AGND, VDDP to PGND . . . . . -0.3V to +6V
BGATE . . . . . AGND - 0.3V to CSON + 0.3V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld TQFN Package	39	3

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -10°C to +100°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5.0V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM VOLTAGE REGULATION					
Maximum System Voltage Accuracy	MaxSystemVoltage = 0x41A0	16.699	16.8	16.901	V
		-0.6		0.6	%
	MaxSystemVoltage = 0x3130	12.529	12.592	12.655	V
		-0.5		0.5	%
	MaxSystemVoltage = 0x20D0	8.350	8.4	8.450	V
		-0.5		0.5	%
Minimum System Voltage Accuracy	MinSystemVoltage = 0x2F00	11.791	12.032	12.273	V
		-2		2	%
	MinSystemVoltage = 0x2300	8.691	8.96	9.229	V
		-3		3	%
	MinSystemVoltage = 0x1800	5.898	6.144	6.390	V
		-4		4	%
CHARGE CURRENT REGULATION					
Charge Current and Accuracy	RS2 = 10mΩ (see Figure 2) ChargingCurrent = 0x1f80	7.822	8.064	8.306	A
		-3		3	%
	RS2 = 10mΩ (see Figure 2) ChargingCurrent = 0x1000	3.932	4.096	4.260	A
		-4		4	%
	RS2 = 10mΩ (see Figure 2) ChargingCurrent = 0x0100	128	256	384	mA
Trickle Charge Current	RS2 = 10mΩ (see Figure 2) CSON-BGATE<4.3V	128	256	384	mA
Trickle Charge Threshold	CSON-BGATE	4.0	4.5	5.0	V
Battery Quiescent Current	$I_{CSOP} + I_{CSON} + I_{PHASE} + I_{CSIP} + I_{CSIN} + I_{SGATE}$ $V_{PHASE} = V_{BOOT} = V_{CSON} = V_{CSOP} = V_{CSIN} = V_{CSIP} = V_{SGATE}$ = 12.6V, V_{DCIN} = VDD = VDDP = 0V		14	25	µA

Electrical Specifications DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5.0V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CURRENT REGULATION					
Input Current Accuracy	RS1 = 20mΩ (see Figure 2) Adapter Current = 512mA	-7		7	%
	RS1 = 20mΩ (see Figure 2) Adapter Current = 4096mA or 8064mA	-3		3	%
CSIP/CSIN Input Voltage Range		5		26	V
ACMON Accuracy Ideal ACMON = 20*(CSIP-CSIN)	$V_{CSIP-CSIN}$ = 161.28mV, ACMON load < 1µA	-2.5		2.5	%
	$V_{CSIP-CSIN}$ = 81.92mV ACMON load < 1µA	-4		4	%
	$V_{CSIP-CSIN}$ = 10.24mV, ACMON load < 1µA	-20		20	%
	$V_{CSIP-CSIN}$ = 5.12mV, ACMON load < 1µA	-40		40	%
ACMON Min Output Voltage	$V_{CSIP-CSIN}$ = 0.0V, ACMON load < 1µA		30	80	mV
ACMON Max Source Current	$V_{CSIP-CSIN}$ = 161.28mV, V_{ACMON} = 0V	25	40	60	µA
ACMON Max Sink Current	$V_{CSIP-CSIN}$ = 0.0V, V_{ACMON} = 2V	25	40	60	µA
SUPPLY AND LINEAR REGULATOR					
DCIN, Input Voltage Range		8		26	V
DCIN Quiescent Current	$V_{ADAPTER}$ = 8V to 26V, $V_{BATTERY}$ 4V to 16.8V		2	5	mA
VDD Output Voltage	8.0V < V_{DCIN} < 26V, no load	4.975	5.1	5.23	V
VDD Load Regulation	0 < I_{VDDP} < 30mA		35	80	mV
VDD UVLO Rising		4.5	4.7	4.85	V
VDD UVLO Hysteresis		350	470	600	mV
VSMB Range		2.7		5.5	V
VSMB UVLO Rising		2.35	2.475	2.6	V
VSMB UVLO Hysteresis		80	100	120	mV
VSMB Quiescent Current	VSMB = SCL = SDA = 3.42V		80	150	µA
VSMB Quiescent Current	VSMB = SCL = SDA = 3.42V, LOW POWER BIT= 1		55	75	µA
V REFERENCE					
VREF Output Voltage	0 < I_{VREF} < 300µA	3.158	3.2	3.232	V
ADPR					
Sink Current	V_{ADPR} = 0.4V, ADET = 3.7V	2	8		mA
Leakage Current	V_{ADPR} = 5.5V, ADET = 2.7V			1	µA
TRKLN					
Sink Current	$V_{CSON-BGATE}$ = 6V	2	7		mA
Leakage Current	$V_{CSON-BGATE}$ = 4V			1	µA

Electrical Specifications DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5.0V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SGATE					
Sink Current	V_{ADET} > 3.5V, SGATE = 0.4V	1	2.3		mA
Leakage Current	V_{ADET} = 0V, SGATE = 26V			1	µA
ADET					
ADET Rising Threshold		3.15	3.2	3.25	V
ADET Threshold Hysteresis		40	60	90	mV
ADET Input Leakage Current				1	µA
SWITCHING REGULATOR					
Frequency 400kHz	Register 0x3D = xxxxxx00b	330	400	440	kHz
Frequency 100kHz	Register 0x3D = xxxxxx01b	80	100	125	kHz
Frequency 50kHz	Register 0x3D = xxxxxx11b	35	50	70	kHz
UGATE ON-Resistance Low	I_{UGATE} = -100mA (Note 3)		0.9	1.6	Ω
UGATE ON-Resistance High	I_{UGATE} = +100mA (Note 3)		2	3.1	Ω
LGATE ON-Resistance High	I_{LGATE} = +100mA (Note 3)		2	3.1	Ω
LGATE ON-Resistance Low	I_{LGATE} = -100mA (Note 3)		0.9	1.6	Ω
Dead Time	Falling UGATE to rising LGATE or Falling LGATE to rising UGATE 50% to 50%. Load = 100Ω and 10pF	25	50	75	ns
ERROR AMPLIFIERS					
gm2 Amplifier Transconductance	Transconductance from VFB to VCOMP	200	250	300	µA/V
gm1 Amplifier Transconductance	Transconductance from (CSOP-CSON) to ICOMP	40	50	60	µA/V
gm3 Amplifier Transconductance	Transconductance from (CSIP-CSIN) to ICOMP	40	50	60	µA/V
gm4 Amplifier Transconductance	Transconductance from VFB to BGATE	50	100	150	µA/V
gm1/gm3 Saturation Current		15	21	25	µA
gm2 Saturation Current		10	17	25	µA
ICOMP, VCOMP Clamp Voltage	Max Voltage between V_{VCOMP} and V_{ICOMP}	200	300	400	mV
LOGIC LEVELS					
SDA/SCL Input Low Voltage	VSMB = 2.7V to 5.5V			0.8	V
SDA/SCL Input High Voltage	VSMB = 2.7V to 5.5V	2			V
SDA/SCL Input Bias Current	VSMB = 2.7V to 5.5V			1	µA
SDA, Output Sink Current	V_{SDA} = 0.4V	4	12		mA

SMB Timing Specification

VSMB = 2.7V to 5.5V; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Frequency	FSMB		10		100	kHz
Bus Free Time	TBUF		4.7			µs
Start Condition Hold Time from SCL	THD:STA		4			µs
Start Condition Set-up Time from SCL	TSU:STA		4.7			µs
Stop Condition Set-up Time from SCL	TSU:STO		4			µs
SDA Hold Time from SCL	THD:DAT		300			ns
SDA Set-up Time from SCL	TSU:DAT		250			ns
SCL Low Period	TLOW		4.7			µs
SCL High Period	THIGH		4			µs
SMBus Inactivity Time-out		Maximum Charging Period Without a SMBus Write to MaxSystemVoltage or ChargeCurrent Register	120	180	250	s

NOTE:

3. Limits should be considered typical and are not production tested.

Typical Operating Performance

DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted.

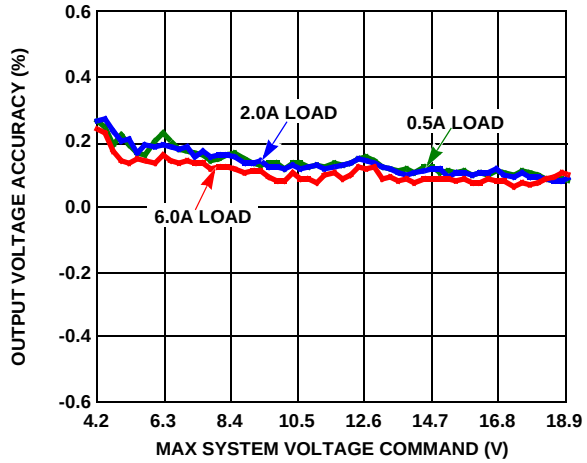


FIGURE 3. MAXIMUM SYSTEM VOLTAGE ACCURACY

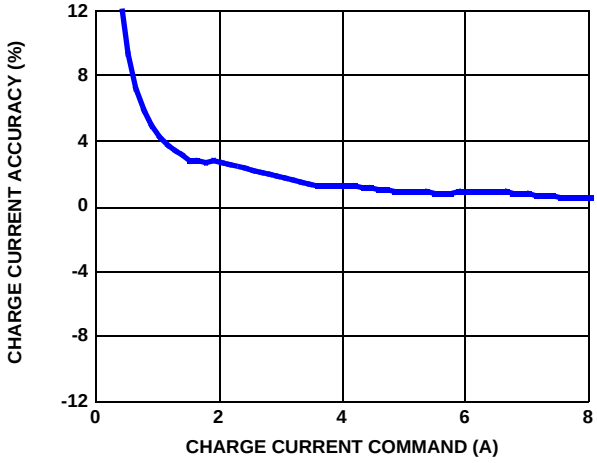


FIGURE 4. CHARGE CURRENT ACCURACY

Typical Operating Performance

DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

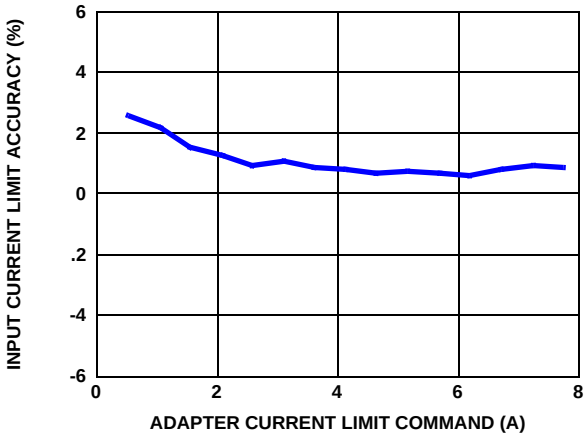


FIGURE 5. INPUT CURRENT LIMIT ACCURACY

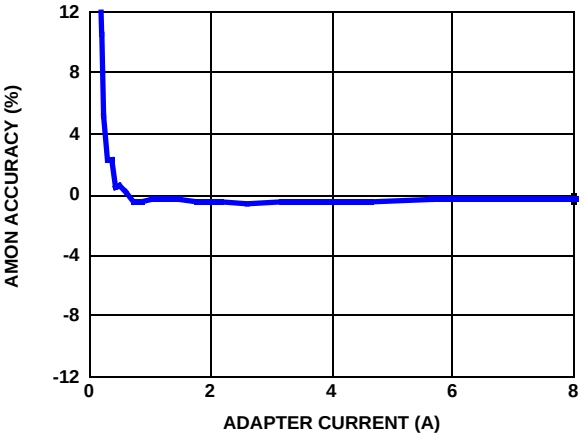


FIGURE 6. AMON ACCURACY

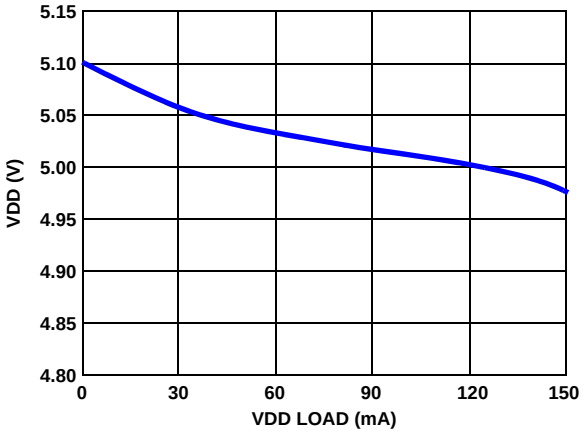


FIGURE 7. VDD LOAD REGULATION

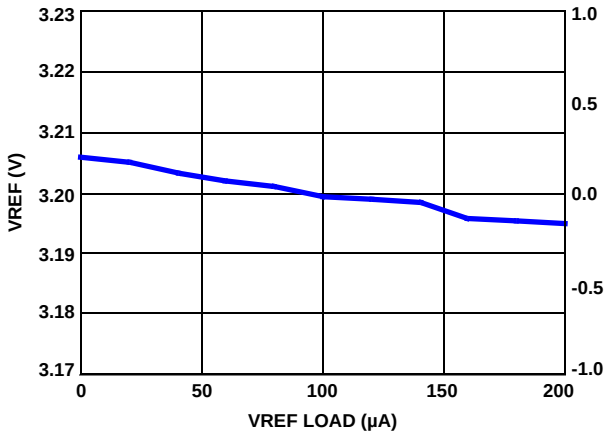


FIGURE 8. VREF LOAD REGULATION

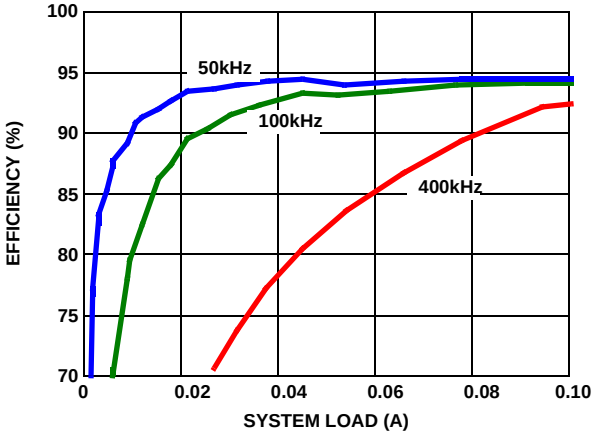


FIGURE 9. LIGHT LOAD EFFICIENCY

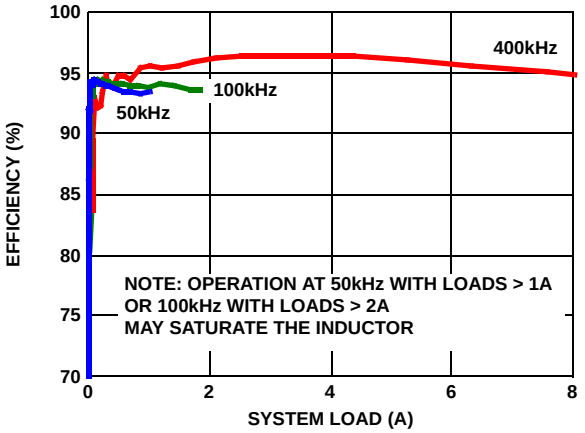


FIGURE 10. EFFICIENCY

Typical Operating Performance

DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

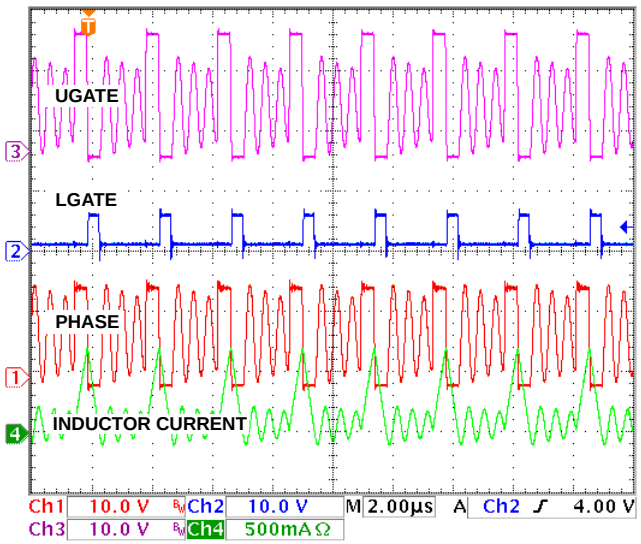


FIGURE 11. SWITCHING WAVEFORMS IN DISCONTINUOUS CONDUCTION MODE

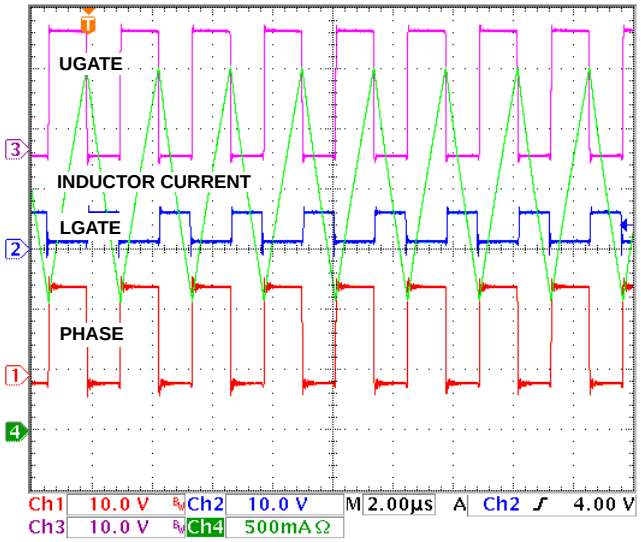


FIGURE 12. SWITCHING WAVEFORMS IN CONTINUOUS CONDUCTION MODE

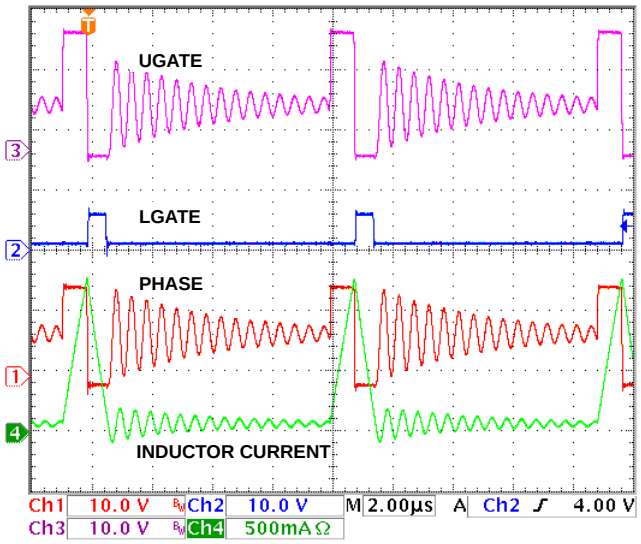


FIGURE 13. 100kHz SWITCHING WAVEFORMS

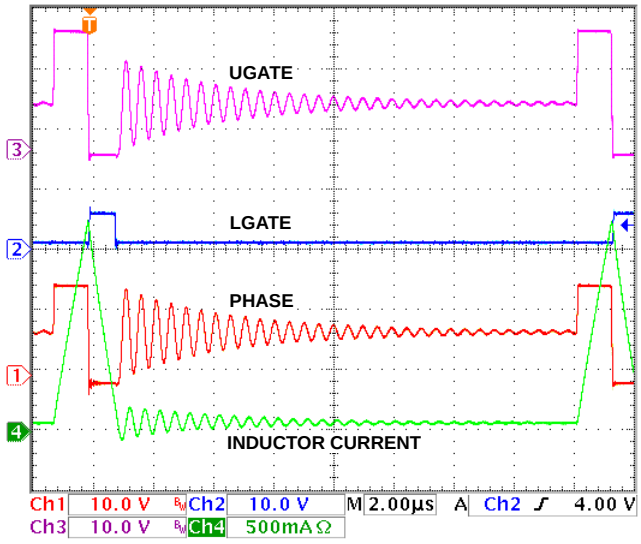


FIGURE 14. 50kHz SWITCHING WAVEFORMS

Functional Pin Descriptions

BOOT

High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BOOT to PHASE.

UGATE

High-Side Power MOSFET Driver Output. Connect to the high-side N-Channel MOSFET gate.

LGATE

Low-Side Power MOSFET Driver Output. Connect to low-side N-Channel MOSFET. LGATE drives between VDDP and PGND.

PHASE

High-Side Power MOSFET Driver Source Connection. Connect to the source of the high-side N-Channel MOSFET.

PGND

Power Ground. Connect PGND to the source of the low side MOSFET.

CSOP

Charge Current-Sense Positive Input.

CSON

Charge Current-Sense Negative Input and system voltage feedback.

CSIP

Input Current-Sense Positive Input.

CSIN

Input Current-Sense Negative Input.

DCIN

Charger Bias Supply Input. Bypass DCIN with a 0.1µF capacitor to AGND.

ADET

AC Adapter Detection Input. Connect to a resistor divider from the AC-adapter output.

ADPR

Adapter Present Output. This open drain output is high impedance when ADET is greater than 3.2V. The ADPR output remains low when the ISL9518 is powered down. Connect a 10k pull-up resistor from ADPR to VSMB.

ACMON

Input Current Monitor Output. ACMON voltage equals $20 \times (V_{CSIP} - V_{CSIN})$.

VDD

Linear Regulator Output. VDD is the output of the 5.1V linear regulator supplied from DCIN. VDD supplies regulated power input for internal analog circuits. Connect a 4.7Ω resistor from VDD to VDDP and a 1µF ceramic capacitor from VDD to AGND.

VDDP

VDDP directly supplies the LGATE driver and the BOOT strap diode. Bypass with a 1µF ceramic capacitor from VDDP to PGND.

ICOMP

Output of the Current Control error amplifier. See “Loop Compensation Design” on page 20 for details on selecting compensation components.

VCOMP

Output of the Voltage loop error amplifier. See “Loop Compensation Design” on page 20 for details on selecting compensation components.

VFB

Negative input to the Min System Voltage and Max System Voltage control error amplifier.

VREF

Output of an internal precision voltage reference.

TRKLN

Open drain out that goes low when the charger is in trickle-charge mode.

BGATE

Gate drive for the battery connection PFET. This pin can go high to disconnect the battery, low to connect the battery or operate in a linear mode to regulate minimum system voltage during trickle charge. It is also the compensation point for the Min System Voltage regulation loop.

SGATE

SGATE is the AC adapter power source select output. The SGATE pin drives back to back external P-MOSFETs used to connect and disconnect the AC adapter to the NVDC charger input. SGATE is controlled by the SMBus and the ADET state.

VSMB

SMBus interface Supply Voltage Input. Bypass with a 0.1µF capacitor to AGND.

SDA

SMBus Data I/O. Open-drain Output. Connect an external pull-up resistor according to SMBus specifications.

SCL

SMBus Clock Input. Connect an external pull-up resistor according to SMBus specifications.

AGND

Analog Ground. Connect to PGND close to the output capacitor.

Backside Paddle

Connects the backside paddle to AGND.

Theory of Operation

Introduction

The ISL9518 differs from the ISL9518A only in the default states of the internal registers at power-up. ISL9518 defaults are for systems with an 8.4V (2-cell) battery and ISL9518A defaults are for systems with a 12.6V battery (3-cell). Unless otherwise noted, all specifications and descriptions of ISL9518 refer to both the ISL9518 and ISL9518A.

A high efficiency synchronous buck converter is used to control the system voltage up to 19.2V and charging current up to 8A. The ISL9518 also has input current limiting up to 8.064A (or higher with lower values of sense resistor). The Input current limit, charge current limit, minimum and maximum system voltage are set by internal registers written with SMBus. The ISL9518 “Typical Application Circuit” is shown in Figure 2.

The ISL9518 charges the battery with constant charge current, set by the ChargeCurrent register, until the battery voltage rises to a voltage set by the MaxSystemVoltage register. The charger will then operate at a constant voltage. The adapter current is monitored and if the adapter current rises to the limit set by the InputCurrent register, system voltage and battery charge current are reduced to limit adapter current. If battery voltage is below the min system voltage, the trickle charge system is activated.

The ISL9518 features two voltage regulation loops and two current regulation loops. The max system voltage loop controls the voltage at CSON with a precision voltage divider to the voltage error amplifier GM2. The min system voltage prevents the system voltage from dropping below a minimum value even if a deeply discharged battery is inserted that is below the minimum. The Charge Current regulation loop limits the battery charging current delivered to the battery to ensure that it never exceeds the current set by the ChargeCurrent register. The Input Current regulation loop limits the current drawn from the AC-adapter to ensure that it never exceeds the limit set by the InputCurrent register to prevent adapter overload.

PWM Control

The ISL9518 employs a fixed frequency pulse width modulator (PWM) with feed forward. The switching frequency can be reduced with an SMBus command for improved light load efficiency

AC-adapter Detection

AC-adapter voltage is connected through a resistor divider to ADET to detect when AC power is available, as shown in Figure 2. ADPR is an open-drain output and is active low when ADET is less than $V_{th,fall}$, and high Z when ADET is above $V_{th,rise}$. The ADET rising threshold is 3.2V (typ) with 57mV hysteresis. ADET must be above the threshold to Enable the output voltage.

Current Measurement

ACMON is an output voltage that is proportional to the adapter current being sensed across CSIP and CSIN. The output voltage range is 0.1V to 3.2V. The voltage of ACMON is given by Equation 1:

$$ACMON = 20 \cdot I_{INPUT} \cdot R_{S1} \quad \text{(EQ. 1)}$$

where I_{INPUT} is the DC current drawn from the AC-adapter. A capacitor is required at the ACMON output to stabilize the ACMON amplifier and to minimize switching noise.

VDD Regulator

VDD provides a 5.1V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of continuous current. VDD also supplies power to VDDP through a low pass filter as shown in the “Typical Application Circuit” in Figure 2. The MOSFET drivers are powered by VDDP. Bypass VDDP and VDD with a 1µF capacitor.

VSMB Supply

The VSMB input provides power to the SMBus interface. Connect an external supply to VSMB to keep the SMBus interface active while the supply to DCIN is removed. When VSMB is biased, the internal registers are maintained. Bypass VSMB to AGND with a 0.1µF or greater ceramic capacitor.

SGATE Function

If ADET > 3.2V and VDD > 4.5V and ISOLATE_ADAPTER bit is 0 (default state) then SGATE will be ON (meaning SGATE will be driven to ground turning on the inrush limit and the adapter isolation FETs ON). In all other cases, SGATE is OFF (meaning the chip will not pull-down SGATE and the off chip resistor will pull the gates of the in-rush limit and adapter isolation FETs to their sources, turning them OFF).

BGATE Function

The BGATE pin drives the gate of an external PFET to control the minimum system voltage. If a battery is connected that is discharged below the value set in the MinSystemVoltage register, BGATE controls the system voltage at the value set in the MinSystemVoltage register.

Trickle Charging

If a battery that is discharged below the value set in the MinSystemVoltage register is connected to the system, the trickle charge system is activated. In trickle charge mode, the charge current is reduced to 256mA. The value in the ChargeCurrent register is not changed. The BGATE FET is controlled in a linear mode to regulate the system voltage at min system voltage and to drop voltage between the min system voltage and the battery. This state is communicated to the host system by the trickle bit in the control register and a low state on the TRKLN pin.

When the battery is charged to the min system voltage, the BGATE FET becomes fully enhanced and BGATE is pulled more than 5V below the system voltage. This changes the

charge mode from trickle to fast charge. The charge current is increased to the value in the ChargeCurrent register. The TRKLN output goes hi and the trickle bit in the control register goes low.

Short Circuit Protection and 0V Battery Charging

If a battery is connected that is completely discharged or a short circuit, the trickle charge system is activated. The Charge Current is reduced to 256mA and BGATE controls the BGATE FET to maintain system voltage at the value in the MinSystemVoltage register.

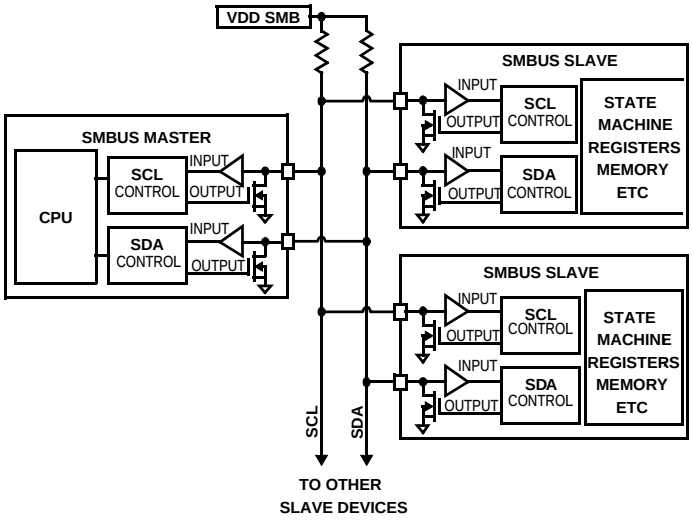
Over-Temperature Protection

If the die temp exceeds +150°C, it turns both of the synchronous buck FETs off. The system bus and the battery charging are disabled. Once the die temp drops below +125°C, system bus regulation and battery charging will start-up again.

The System Management Bus

The System Management Bus (SMBus) is a 2-wire bus that supports bidirectional communications. The protocol is described briefly here. More detail is available from http://www.smbus.org/.

General SMBus Architecture



Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 15.

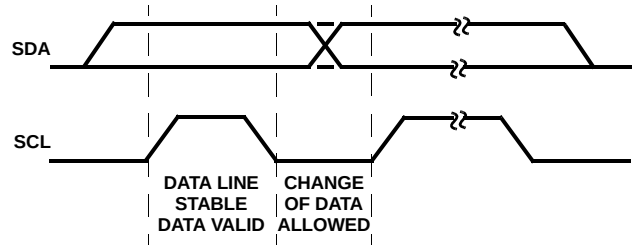


FIGURE 15. DATA VALIDITY

START and STOP Conditions

As shown in Figure 16, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

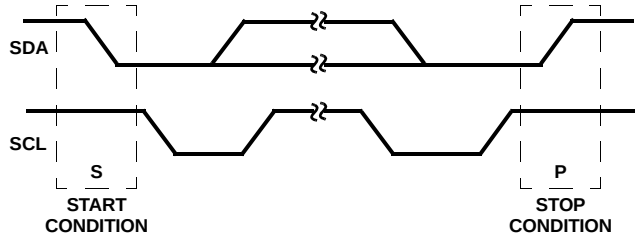


FIGURE 16. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/$\overline{W}$ bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 17). The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

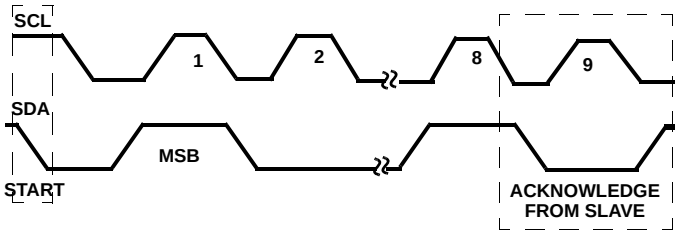


FIGURE 17. ACKNOWLEDGE ON THE I^2C BUS

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7 bits of slave address (0001001 for the ISL9518) followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the SMBus bus recognize their address, they will acknowledge by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition.

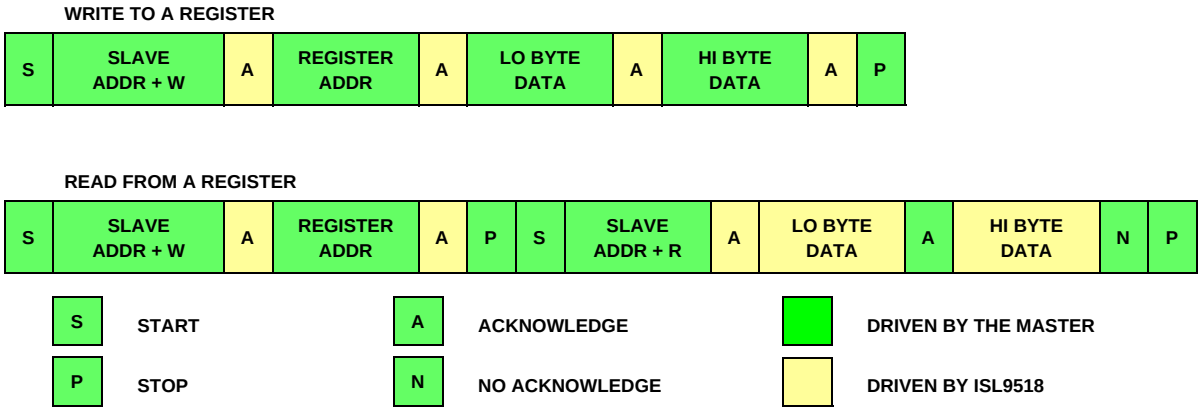


FIGURE 18. SMBus/ISL9518 READ AND WRITE PROTOCOL

Once the control byte is sent, and the ISL9518 acknowledges it, the 2nd byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9518 which register the master will write or read. See Table 1 for details of the registers. Once the ISL9518 receives a register address byte, it responds with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB). The LO BYTE data is transferred before the HI BYTE data.

ISL9518 and SMBus

The ISL9518 receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols, as documented in the System Management Bus Specification V1.1, which can be downloaded from http://www.smbus.org/. The ISL9518 uses the SMBus Read-Word and Write-Word protocols (Figure 18) to communicate with the host system and a smart battery. The ISL9518 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ (0x12).

Read address = 0b00010011 and

Write address = 0b00010010.

In addition, the ISL9518 has two identification (ID) registers: a 16-bit device ID register (0xFF) and a 16-bit manufacturer ID register (0xFE).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications. The ISL9518 is controlled by the data written to the registers described in Table 1.

SMBus Registers

The ISL9518 supports 7 internal registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. ManufacturerID and DeviceID are “read only” registers and can be used to identify the ISL9518. On the ISL9518, ManufacturerID always returns 0x0049 (ASCII code for “I” for Intersil) and DeviceID always returns 0x0002.

TABLE 1. ISL9518 AND ISL9518A REGISTER SUMMARY

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	ISL9518 (2-CELL) POR STATE	ISL9518A (3-CELL) POR STATE
0x14	ChargeCurrent	Read or Write	6-Bit Charge Current Setting	0x0000 = 0A	0x0000 = 0A
0x15	MaxSystemVoltage	Read or Write	11-Bit MaxSystemVoltage Setting	0x2000 = 8.192V	0x3000 = 12.288V
0x3D	Control	Read or Write	8-Bit Control bit register	0x0000	0x0000
0x3E	MinSystemVoltage	Read or Write	7-Bit MinSystemVoltage setting	0x1800 = 6.144V	0x2400 = 9.216V
0x3F	InputCurrent	Read or Write	6-Bit Input Current Setting	0x0C00 = 3.072A	0x0E00 = 3.584A
0xFE	ManufacturerID	Read Only	Manufacturer ID	0x0049	0x0049
0xFF	DeviceID	Read Only	Device ID	0x0002	0x0002

Setting Max System Voltage

Max system voltage is set by writing a valid 16-bit number to the 16-bit MaxSystemVoltage register. The ISL9518 ignores the first 4 LSBs and uses the next 11 bits to set the voltage DAC. The max system voltage range of the ISL9518 is 1.024V to 19.200V. Numbers requesting max system voltage greater than 19.200V result in a max system voltage of 19.200V. All numbers requesting max system voltage below 1.024V result in a voltage set point of zero, which turns off the regulator. The trickle charge system is activated when CSON-BGATE < 5V. If the MaxSystemVoltage register is set below 6.144V, it may not be possible to get CSON-BGATE > 5V. In this case, the regulator will stay in trickle charge mode.

Upon initial power-up of the VSMB supply, the MaxSystemVoltage register is reset to the POR value in Table 1. Use the Write-Word protocol (Figure 18) to write to the MaxSystemVoltage register. The register address for MaxSystemVoltage is 0x15. The 16-bit binary number formed by D15–D0 represents the max system voltage set point in mV. However, the resolution of the ISL9518 is 16mV because the D0–D3 bits are ignored, as shown in Table 2. The D15 bit is also ignored because it is not needed to span the 1.024V to 19.2V range. Table 2 shows the mapping between the 16-bit number written to the MaxSystemVoltage register and max system voltage set point. The MaxSystemVoltage register can be read back to verify its contents.

Smart Battery Registers

The MaxSystemVoltage and ChargeCurrent registers use addresses and the format defined in the Smart Battery Charger Specification (Level 2) for ChargeVoltage and ChargeCurrent. In some systems, the Smart Battery Pack may write commands to these registers in ISL9518. If a Smart Battery is used with ISL9518; please refer to the Smart Battery Charger Specification for details

TABLE 2. MaxSystemVoltage (REGISTER 0x15)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4	MaxSystemVoltage, MAXSVDAC 0	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 16mV of charger voltage.
5	MaxSystemVoltage, MAXSVDAC 1	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 32mV of charger voltage.
6	MaxSystemVoltage, MAXSVDAC 2	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 64mV of charger voltage.
7	MaxSystemVoltage, MAXSVDAC 3	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 128mV of charger voltage.
8	MaxSystemVoltage, MAXSVDAC 4	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 256mV of charger voltage.
9	MaxSystemVoltage, MAXSVDAC 5	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 512mV of charger voltage.
10	MaxSystemVoltage, MAXSVDAC 6	0 = Adds 0mA of charger voltage. 1 = Adds 1024mV of charger voltage.
11	MaxSystemVoltage, MAXSVDAC 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	MaxSystemVoltage, MAXSVDAC 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	MaxSystemVoltage, MAXSVDAC 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	MaxSystemVoltage, MAXSVDAC 10	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage, 19200mV maximum
15		Not used. Normally a 32768mV weight.

Setting Minimum System Voltage

Minimum System Voltage is set by writing a valid 16-bit number to the MinSystemVoltage register. This 16-bit number translates to a 65.535V full-scale voltage. The ISL9518 ignores the first 8 LSBs and uses the next 7 bits to set the MinSystemVoltage DAC. The min system voltage range of the ISL9518 is 0V to 19.2V. Numbers requesting min system voltage greater than 19.2V result in a min system voltage of 19.2V. Although min system voltage can be set to 0.00V, the min system voltage cannot go below the Vgs of the BGATE FET. Min system voltage below 6.144V is not recommended.

Upon initial power-up of the VSMB supply, the MinSystemVoltage register is reset to the POR value in Table 1. Use the Write-Word protocol (Figure 18) to write to the MinSystemVoltage register. The register address for MinSystemVoltage is 0x3E. The 16-bit binary number formed by D15–D0 represents the min system voltage set point in mV. However, the resolution of the ISL9518 is 256mV because the D0–D7 bits are ignored as shown in Table 3. The D15 bit is also ignored because it is not needed to span the 0V to 19.2V range. Table 3 shows the mapping between the 16-bit number written to the MinSystemVoltage register and the min system voltage set point. The MinSystemVoltage register can be read back to verify its contents.

Setting Charge Current

ISL9518 has a 16-bit ChargeCurrent register that sets the battery charging current. ISL9518 controls the charge current by controlling the CSOP-CSON voltage. The register's LSB translates to 10µV at CSON-CSOP. With a 10mΩ charge current R_{SENSE} resistor (RS2 in "Typical Application Circuit" on page 3), the LSB translates to 1mA charge current. The ISL9518 ignores the first 7 LSBs and uses the next 6 bits to control the current DAC. The charge-current range of the ISL9518 is 0A to 8.064A (using a 10mΩ current-sense resistor). All numbers requesting charge current above 8.064A result in a current setting of 8.064A. All numbers requesting charge current between 0mA to 128mA result in a current setting of 0mA. After initial power-up of VSMB, the ChargeCurrent register is reset to 0x0000, BGATE is high (BGATE FET is OFF) and charging is disabled. To charge the battery, write a valid, non-zero number to the ChargeCurrent register. The ChargeCurrent register uses the Write-Word protocol (Figure 18). The register code for ChargeCurrent is 0x14 (0b00010100). Table 4 shows the mapping between the 16-bit ChargeCurrent number and the charge current set point. The ChargeCurrent register can be read back to verify its contents.

TABLE 3. MinSystemVoltage (REGISTER 0x3E)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7		Not used.
8	MinSystemVoltage, MINSVDAC 0	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 256mV of charger voltage.
9	MinSystemVoltage, MINSVDAC 1	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 512mV of charger voltage.
10	MinSystemVoltage, MINSVDAC 2	0 = Adds 0mA of charger voltage. 1 = Adds 1024mV of charger voltage.
11	MinSystemVoltage, MINSVDAC 3	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	MinSystemVoltage, MINSVDAC 4	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	MinSystemVoltage, MINSVDAC 5	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	MinSystemVoltage, MINSVDAC 6	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage, 19200mV maximum
15		Not used.

TABLE 4. ChargeCurrent (REGISTER 0x14) (10mΩ SENSE RESISTOR, RS2)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7	Charge Current, CCDAC 0	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
8	Charge Current, CCDAC 1	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
9	Charge Current, CCDAC 2	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
10	Charge Current, CCDAC 3	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
11	Charge Current, CCDAC 4	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
12	Charge Current, CCDAC 5	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current, 8064mA maximum
13		Not used.
14		Not used.
15		Not used.

Smart Battery Registers

The MaxSystemVoltage and ChargeCurrent registers use addresses and the format defined in the Smart Battery Charger specification (Level 2) for ChargeVoltage and ChargeCurrent. In some systems the Smart Battery Pack may write commands to these registers in ISL9518. If a Smart Battery is used with ISL9518, please refer to the Smart Battery Charger Specification for details.

Setting Input Current Limit

When the input current exceeds the set input current limit, the ISL9518 decreases the charge current to provide priority to system load current. As the system load rises, the available charge current drops linearly to zero. Higher system loads can be drawn from the battery. If the battery is not present, the system voltage is reduced to supply more system current at the same input current. The total input current can increase to the limit of the AC-adapter.

The internal amplifier compares the differential voltage between CSIP and CSIN to a scaled voltage set by the InputCurrent register. The total input current is a function of battery charge current, system load current, V_{OUT}, V_{IN} and efficiency. The total input current can be estimated by Equation 2:

$$I_{INPUT} = (I_{SYSTEM} + I_{BATTERY}) \times V_{SYSTEM} / (\eta \times V_{INPUT}) \quad \text{(EQ. 2)}$$

Where η is the efficiency of the DC/DC converter (typically 90% to 95%).

The ISL9518 has a 16-bit InputCurrent register that translates to a 1mA LSB and a 65.53A full scale current using a 20mΩ current-sense resistor (RS1 in Figure 2). Equivalently, the 16-bit Input Current number sets the voltage across CSIP and CSIN inputs in 20µV per LSB increments. To set the input current limit, use the SMBus to write a 16-bit InputCurrent register using the data format listed in Table 5. The InputCurrent register uses the Write-Word protocol (see Figure 18). The register code for InputCurrent is 0x3F (0b00111111). The InputCurrent register can be read back to verify its contents.

The ISL9518 ignores the first 7 LSBs and uses the next 6-bits to control the input current DAC. The input current range of the ISL9518 is from 128mA to 8.064A. All 16-bit numbers requesting input current above 8.064A result in an input-current setting of 8.064A. The default input current limit setting at power on of VSMB is the POR value in Table 1.

TABLE 5. INPUT CURRENT (REGISTER 0x3F) (20mΩ SENSE RESISTOR, RS1)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7	Input Current, ACDAC 0	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.
8	Input Current, ACDAC 1	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
9	Input Current, ACDAC 2	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
10	Input Current, ACDAC 3	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
11	Input Current, ACDAC 4	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
12	Input Current, ACDAC 5	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current, 8064mA maximum
13		Not used.
14		Not used.
15		Not used.

TABLE 6. CONTROL REGISTER (REGISTER 0x3D)

BIT	BIT NAME	DESCRIPTION
0	100kHz	100kHz = 1 Changes the switching frequency to100kHz. Default 0
1	50kHz	50kHz = 1 AND 100kHz = 1 Changes the switching frequency to 50kHz. Default 0
2	Isolate Adapter	Isolate Adapter = 1 disconnects the adapter from the charger by making the SGATE pin HI Z. Default 0
3	Spare	Spare Default 0
4	LowPower	LowPower = 1 removes power from the battery discharge monitor circuits to reduce power consumption. Default 0
5	Spare	Spare Default 0
6	AC_OK	Read only. The chip indicates the state. Default 0. read only
7	Trickle	Read only. The chip indicates the state. Default 0. Read only
8		Not used.
9		Not used.
10		Not used.
11		Not used.
12		Not used.
13		Not used.
14		Not used.
15		Not used.

Control Register

Each bit in the control register has a different function. Table 6 describes the actions of each bit. The register can be read or written. Bits 6 and 7 are controlled internally and are read only. Writing to bits 7 and 6 does not change their value or the function of ISL9518.

The register returns to its default values on power-up of VSMB (see Table 1).

Charger Timeout

The ISL9518 includes a timer to insure the SMBus master is active and to prevent over charging the battery. If the adapter is present and if ISL9518 does not receive a write to the MaxSystemVoltage or ChargeCurrent register within 175s, ISL9518 will terminate charging by turning the BGATE FET OFF. If a time-out occurs, either the MaxSystemVoltage or the ChargeCurrent register must be written to re-enable charging. ISL9518 will continue to regulate the system voltage even if an SMBus time-out occurs. If the adapter is not present, ISL9518 turns the BGATE FET ON to supply system voltage from the battery.

ISL9518 Data Byte Order

Each register in ISL9518 contains 16 bits or two 8-bit bytes. All data sent on the SMBus is in 8-bit bytes and 2 bytes must be written or read from each register in ISL9518. The order in which these bytes are transmitted appears reversed from the way they are normally written. The LO BYTE is sent first and the HI BYTE is sent second. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is sent second. See Figure 18.

Writing to the Internal Registers

In order to set the ChargeCurrent, InputCurrent, MaxSystemVoltage, MinSystemVoltage or the Control registers, valid 16-bit numbers must be written to ISL9518's internal registers via the SMBus.

To write to a register in the ISL9518, the master sends a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. If it receives an Acknowledge from the ISL9518, it sends a register address byte setting the register to be written (i.e. 0x14 for the ChargeCurrent register). The ISL9518 will respond with an Acknowledge. The master then sends the lower data byte to be written into the desired register. The ISL9518 will respond with an Acknowledge. The master then sends the higher data byte to be written into the desired register. The ISL9518 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL9518 that the current transaction is complete. Once this transaction completes, the ISL9518 will begin operating at the new current or voltage. See Figure 18.

ISL9518 does not support writing more than one register per transaction.

Reading from the Internal Registers

The ISL9518 has the ability to read from 7 internal registers. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the registers address byte. This process begins by the master sending a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. Once it receives an acknowledge from the ISL9518, it sends a register address byte representing the internal register it wants to read. The ISL9518 will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition, the master follows with a new Start condition, then sends a new control byte with the ISL9518 slave address and the R/$\overline{W}$ bit set to 1, indicating a read. The ISL9518 will Acknowledge then send the lower byte stored in that register. After receiving the byte, the master Acknowledges by holding SDA low during the 9th clock pulse. ISL9518 then sends the higher byte stored in the register. After the second byte, neither device holds SDA low (No Acknowledge). The master will then produce a Stop condition to end the read transaction. See Figure 18.

ISL9518 does not support reading more than 1 register per transaction.

Application Information

The following battery charger design refers to the "Typical Application Circuit" in Figure 2. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size, crossover frequency and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher AC losses in the magnetic core and the windings, which decreases the system efficiency. Higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (DC resistance of the inductor) loss, lower saturation current and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±15% to ±20% of the maximum operating DC current at maximum input voltage. Maximum ripple is at 50% duty cycle or $V_{BAT} = V_{IN,MAX}/2$. The required inductance for ±15% ripple current can be calculated from Equation 3:

$$L = \frac{V_{IN,MAX}}{4 \cdot F_{SW} \cdot 0.3 \cdot I_{OUT,MAX}} \quad \text{(EQ. 3)}$$

Where $V_{IN,MAX}$ is the maximum input voltage, F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the max DC current required by the system.

For $V_{IN,MAX}$ = 20V, V_{BAT} = 12.6V, $I_{BAT,MAX}$ = 4.5A, and f_S = 400kHz, the calculated inductance is 9.3µH. Choosing the closest standard value gives L = 10µH. Ferrite cores are often the best choice since they are optimized at 400kHz to

600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak} in Equation 4:

$$I_{PEAK} = I_{OUT,MAX} + \frac{1}{2} \cdot I_{RIPPLE} \quad \text{(EQ. 4)}$$

Inductor saturation can lead to cascade failures due to very high currents. Conservative design limits the peak current in the inductor to less than 90% of the rated saturation current.

Crossover frequency is heavily dependent on the inductor value. F_{CO} should be less than 20% of the switching frequency and a conservative design has F_{CO} less than 10% of the switching frequency. The highest F_{CO} is in voltage control mode with the battery removed and may be calculated (approximately) from Equation 5:

$$F_{CO} = \frac{5 \cdot 11 \cdot R_{SENSE}}{2\pi \cdot L} \quad \text{(EQ. 5)}$$

Output Capacitor Selection

In Narrow VDC systems, one or more capacitors are connected at the charger output (CSON) and a large number of capacitors are connected to the system voltage output. Most of the system voltage capacitors are placed near the inputs to the system and core regulators. Some capacitance (on the order of 20µF to 100µF) with low ESR should be placed near the inductor and FETs to provide a path for switching currents that is short and has a small area.

A combination of 0.1µF, 10µF ceramic capacitors and organic polymer capacitors is a good choice for capacitors near the ISL9518 and the inputs to the other system regulators. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of the buck regulator.

MOSFET Selection

The Notebook battery charger synchronous buck converter has the input voltage from the AC-adapter output. The maximum AC-adapter output voltage does not exceed 25V. Therefore, 30V logic MOSFET should be used.

The high side MOSFET must be able to dissipate the conduction losses plus the switching losses. For the battery charger application, the input voltage of the synchronous buck converter is equal to the AC-adapter output voltage, which is relatively constant. The maximum efficiency is achieved by selecting a high side MOSFET that has the conduction losses equal to the switching losses. Switching losses in the low-side FET are very small. The choice of low-side FET is a trade-off between conduction losses ($r_{DS(ON)}$) and cost. A good rule of thumb for the $r_{DS(ON)}$ of the low-side FET is 2x the $r_{DS(ON)}$ of the high-side FET.

The LGATE gate driver can drive sufficient gate current to switch most MOSFETs efficiently. However, some FETs may exhibit cross conduction (or shoot-through) due to current injected into the drain-to-source parasitic capacitor (C_{gd}) by the high dV/dt rising edge at the phase node when the high side MOSFET turns on. Although LGATE sink current (1.8A typical) is more than enough to switch the FET off quickly, voltage drops across parasitic impedances between LGATE and the MOSFET can allow the gate to rise during the fast rising edge of voltage on the drain. MOSFETs with low threshold voltage (<1.5V) and low ratio of C_{gs}/C_{gd} (<5) and high gate resistance (>4Ω) may be turned on for a few ns by the high dV/dt (rising edge) on their drain. This can be avoided with higher threshold voltage and C_{gs}/C_{gd} ratio.

For the high-side MOSFET, the worst-case conduction losses occur at the minimum input voltage, as shown in Equation 6:

$$P_{Q1,conduction} = \frac{V_{OUT}}{V_{IN}} \cdot (I_{SYS} + I_{BAT})^2 \cdot r_{DS(ON)} \quad \text{(EQ. 6)}$$

The optimum efficiency occurs when the switching losses equal the conduction losses. However, it is difficult to calculate the switching losses in the high-side MOSFET since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the MOSFET internal gate resistance, gate charge, threshold voltage, stray inductance and the pull-up and pull-down resistance of the gate driver.

The following switching loss calculation (Equation 7) provides a rough estimate.

$$P_{Q1,Switching} = \frac{1}{2} V_{IN} I_{LV} f_{sw} \left(\frac{Q_{gd}}{I_{g,source}} \right) + \frac{1}{2} V_{IN} I_{LP} f_{sw} \left(\frac{Q_{gd}}{I_{g,sink}} \right) + Q_{rr} V_{IN} f_{sw} \quad \text{(EQ. 7)}$$

where the following are the peak gate-drive source/sink current of Q_1, respectively:

- Q_{gd}: drain-to-gate charge,
- Q_{rr}: total reverse recovery charge of the body-diode in low-side MOSFET,
- I_{LV}: inductor valley current,
- I_{LP}: Inductor peak current,
- $I_{g,sink}$
- $I_{g,source}$

Low switching loss requires low drain-to-gate charge Q_{gd}. Generally, the lower the drain-to-gate charge, the higher the ON-resistance. Therefore, there is a trade-off between the ON-resistance and drain-to-gate charge. Good MOSFET selection is based on the Figure of Merit (FOM), which is a product of the total gate charge and ON-resistance. Usually, the smaller the value of FOM, the higher the efficiency for the same application.

For the low-side MOSFET, the worst-case power dissipation occurs at minimum battery voltage and maximum input voltage (Equation 8):

$$P_{Q2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot I_{BAT}^{2} \cdot r_{DS(ON)} \quad \text{(EQ. 8)}$$

Choose a low-side MOSFET that has the lowest possible ON-resistance with a moderate-sized package like the SO-8 and is reasonably priced. The switching losses are not an issue for the low-side MOSFET because it operates at zero-voltage-switching.

Ensure that the required total gate drive current for the selected MOSFETs should be less than 24mA. So, the total gate charge for the high-side and low-side MOSFETs is limited by Equation 9:

$$Q_{GATE} \leq \frac{I_{GATE}}{f_{sw}} \quad \text{(EQ. 9)}$$

Where I_{GATE} is the total gate drive current and should be less than 24mA. Substituting I_{GATE} = 24mA and f_S = 400kHz into Equation 9 yields that the total gate charge should be less than 80nC. Therefore, the ISL9518 easily drives the battery charge current up to 8A.

Snubber Design

ISL9518's buck regulator operates in discontinuous current mode (DCM) when the load current is less than half the peak-to-peak current in the inductor. After the low-side FET turns off, the phase voltage rings due to the high impedance with both FETs off. This can be seen in Figure 11. Adding a snubber (resistor in series with a capacitor) from the phase node to ground can greatly reduce the ringing. In some situations a snubber can improve output ripple and regulation.

The snubber capacitor should be approximately twice the parasitic capacitance of the phase node. This can be estimated by operating at very low load current (100mA) and measuring the ringing frequency. Other capacitor values can be used but smaller values will allow some ringing and larger values will increase the power dissipated in the snubber resistor.

C_{SNUB} and R_{SNUB} can be calculated from Equations 10 and 11:

$$C_{SNUB} = \frac{2}{(2\pi F_{ring})^{2} \cdot L} \quad \text{(EQ. 10)}$$

$$R_{SNUB} = \sqrt{\frac{2 \cdot L}{C_{SNUB}}} \quad \text{(EQ. 11)}$$

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by Equation 12:

$$I_{RMS} = I_{BAT} \cdot \frac{\sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(EQ. 12)}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC-adapter is plugged into the battery charger. For Notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Loop Compensation Design

ISL9518 has four closed loop control modes. One controls the output voltage when the battery is fully charged or absent. A second controls the current into the battery when charging, the third limits current drawn from the adapter and the fourth controls the minimum system voltage. The charge current and input current control loops are compensated by a single capacitor on the ICOMP pin. The voltage control loops are compensated by a network shown in Figure 21. Descriptions of these control loops and guidelines for selecting compensation components will be given in the following sections. Which loop controls the switching regulator is determined by the minimum current buffer and the minimum voltage buffer (IMIN and VMIN in Figure 1). These four loops will be described separately.

Transconductance Amplifiers gm1, gm2, gm3 and gm4

ISL9518 uses several transconductance amplifiers (also known as gm amps). Most commercially available op amps are voltage controlled voltage sources with gain expressed as $A = V_{OUT}/V_{IN}$. gm amps are voltage controlled current sources with gain expressed as $gm = I_{OUT}/V_{IN}$. gm will appear in some of the equations for poles and zeros in the compensation.

PWM Gain F_m

The Pulse Width Modulator in the ISL9518 converts voltage at VCOMP (or ICOMP) to a duty cycle by comparing VCOMP to a triangle wave (duty = $VCOMP/V_{P\text{-}P\ RAMP}$). The low-pass filter formed by L and C_O convert the duty cycle to a DC output voltage ($V_{OUT} = V_{DCIN}$*duty). In ISL9518, the triangle wave amplitude is proportional to V_{DCIN}. Making the ramp amplitude proportional to DCIN makes the gain from VCOMP to the PHASE output a constant 11 and is independent of DCIN.

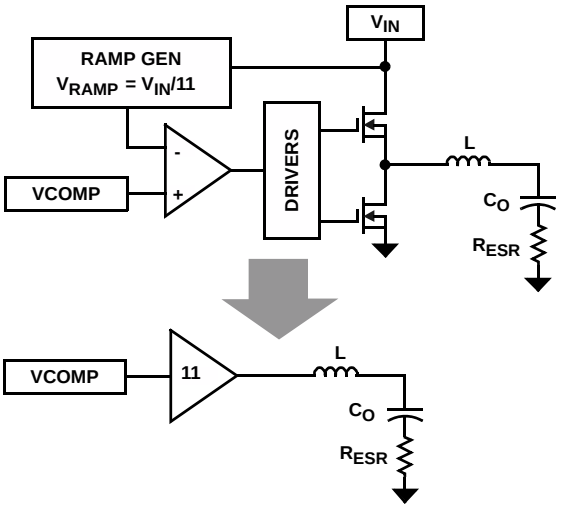


FIGURE 19. FOR SMALL SIGNAL AC ANALYSIS, THE PWM AND POWER STAGE CAN BE MODELED AS A SIMPLE GAIN OF 11

Output LC Filter Transfer Functions

The gain from the phase node to the system output and battery depend entirely on external components. Transfer function $A_{LC}(s)$ is shown in Equations 13 and 14:

$$A_{LC} = \frac{\left(1 - \frac{s}{\omega_{ESR}}\right)}{\left(\frac{s^2}{\omega_{DP}} + \frac{s}{(\omega_{DP} \cdot Q)} + 1\right)} \quad \text{(EQ. 13)}$$

$$\omega_{DP} = \frac{1}{(\sqrt{L \cdot C_o})}$$

$$\omega_{ESR} = \frac{1}{(R_{ESR} \cdot C_o)} \quad \text{(EQ. 14)}$$

$$Q = R_o \cdot \sqrt{\frac{L}{C_o}}$$

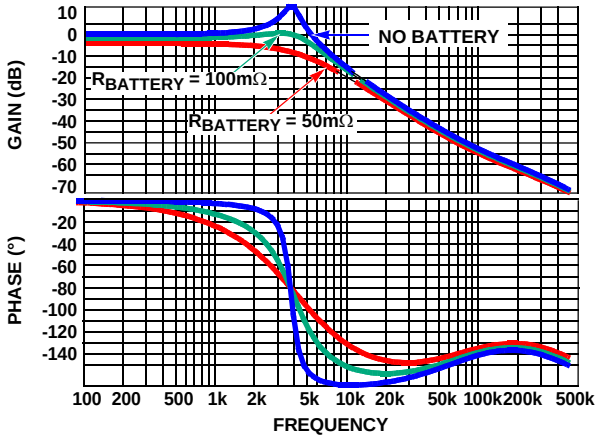


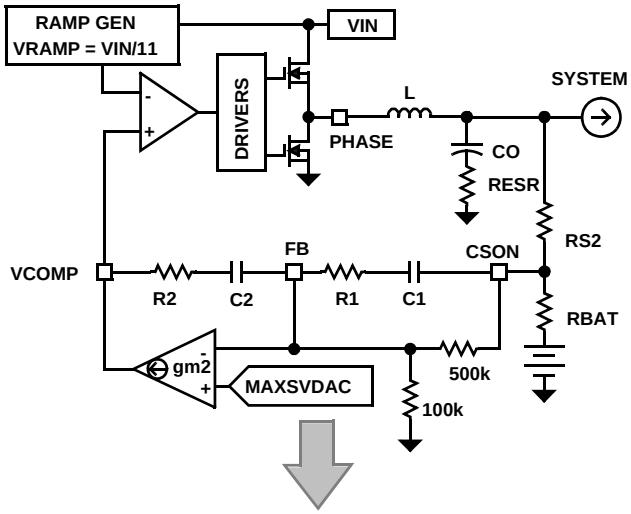
FIGURE 20. FREQUENCY RESPONSE OF THE LC OUTPUT FILTER

The load resistance R_O is a combination of MOSFET $r_{DS(ON)}$, inductor DCR and the internal resistance of the battery (normally between 50mΩ and 200mΩ) in parallel with the system. The system load may be modeled as a current sink in parallel with a resistance. For AC analysis of the voltage control loop, this may be treated as a very high resistance or an open circuit. The worst case for voltage mode control is when the battery is absent. This results in the highest Q of the LC filter and the lowest phase margin.

When the battery is present, the Q is very low (typically 0.1). With very low Q, the double pole from the LC filter split into two separate poles, one at frequency below ω_{DP} and one at a frequency above ω_{DP}.

Max System Voltage Control Loop

The max system voltage error amplifier controls the output when the input current is below the limit and the battery is charged to the value in the MaxSystemVoltage register. Under these conditions, VCOMP controls the charger's output because the 2 current error amplifiers (gm1 and gm3) output their maximum current and charge the capacitor on ICOMP to its maximum voltage (clamped to 0.3V above VCOMP). With ICOMP higher than VCOMP, the minimum voltage buffer output equals the voltage on VCOMP. The max system voltage control loop is shown in Figure 21.



FOR SMALL SIGNAL AC ANALYSIS, VOLTAGE SOURCES ARE SHORT CIRCUITS AND CURRENT SOURCES ARE OPEN CIRCUITS.

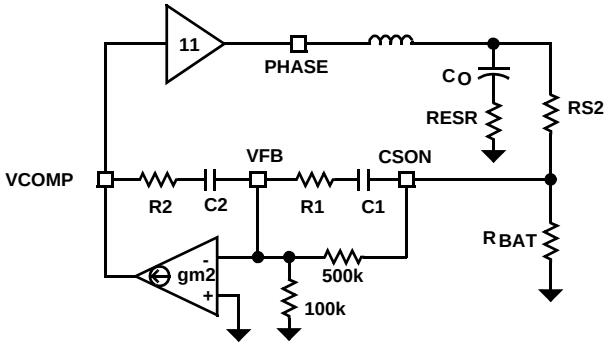


FIGURE 21. MAX SYSTEM VOLTAGE LOOP COMPENSATOR

The compensation network consists of the max system voltage error amplifier gm2 and the compensation network R_1, C_1, R_2 and C_2. Equations 15 through 20 relate to the compensation network's poles, zeros and gain to the components in Figure 21. Figure 22 shows an asymptotic bode plot of the DC/DC converter's gain vs frequency. It is strongly recommended that F_{Z1} is approximately 1/4*F_{DP} and F_{Z2} is approximately 1/2*F_{DP}.

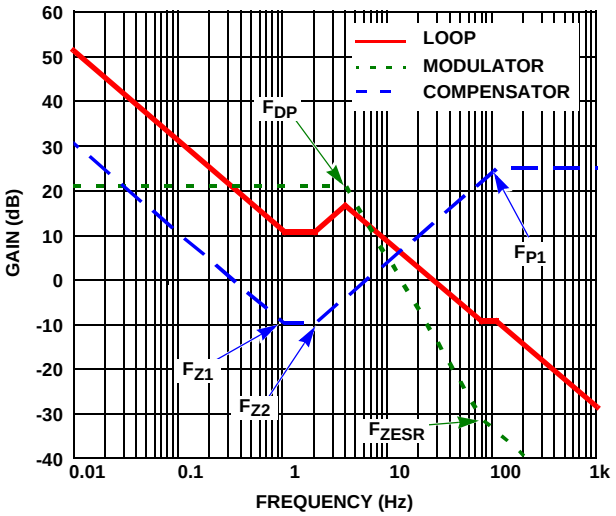


FIGURE 22. ASYMPTOTIC BODE PLOT OF THE MAX SYSTEM VOLTAGE CONTROL LOOP GAIN

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{(2\pi \cdot C_1 \cdot (R_1 + R_3))} \quad \text{(EQ. 15)}$$

$$F_{Z2} = \frac{1}{\left(2\pi \cdot C_2 \cdot \left\{R_2 - \frac{1}{gm2}\right\}\right)} \quad \text{(EQ. 16)}$$

$$\frac{1}{gm2} = 4000\Omega \quad \text{(EQ. 17)}$$

$$F_{DP} = \frac{1}{(2\pi \sqrt{L \cdot C_o})} \quad \text{(EQ. 18)}$$

$$F_{P1} = \frac{1}{(2\pi \cdot R_1 \cdot C_1)} \quad \text{(EQ. 19)}$$

$$F_{ESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 20)}$$

Charge Current Control Loop

When the battery voltage is less than the programmed max system voltage, the max system voltage error amplifier goes to it's maximum output (limited to 0.3V above ICOMP) and the ICOMP voltage controls the loop through the minimum voltage buffer. Figure 23 shows the charge current control loop.

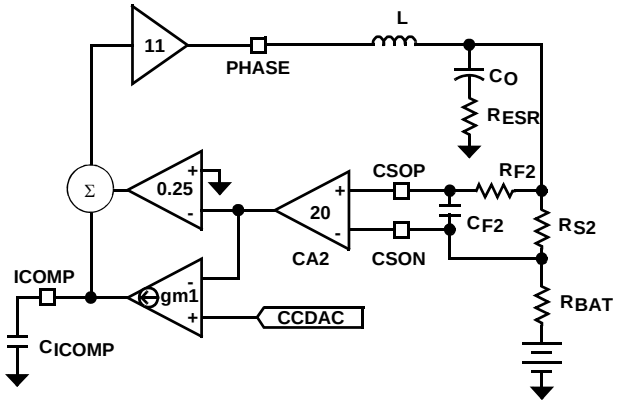


FIGURE 23. CHARGE CURRENT LIMIT LOOP

The compensation capacitor (C_{ICOMP}) gives the error amplifier (gm1) a pole at a very low frequency (<<1Hz) and a a zero at F_{Z1}. F_{Z1} is created by the 0.25*CA2 output added to ICOMP. The loop response has another zero due to the output capacitor's ESR.

A filter should be added between R_{S2} and CSOP and CSON to reduce switching noise. The filter roll off frequency should be between the crossover frequency and the switching frequency (~100kHz). R_{F2} should be small (<2Ω) to minimize offsets due to leakage current into CSOP.

$$F_{DP} = \frac{1}{(2\pi \sqrt{L \cdot C_o})} \quad \text{(EQ. 21)}$$

$$F_{ZESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 22)}$$

$$F_{Z1} = \frac{4 \cdot gm1}{(2\pi \cdot C_{ICOMP})} \quad \text{(EQ. 23)}$$

$$gm1 = 50\mu A/V \quad \text{(EQ. 24)}$$

$$F_{FILTER} = \frac{1}{(2\pi \cdot C_{F2} \cdot R_{F2})} \quad \text{(EQ. 25)}$$

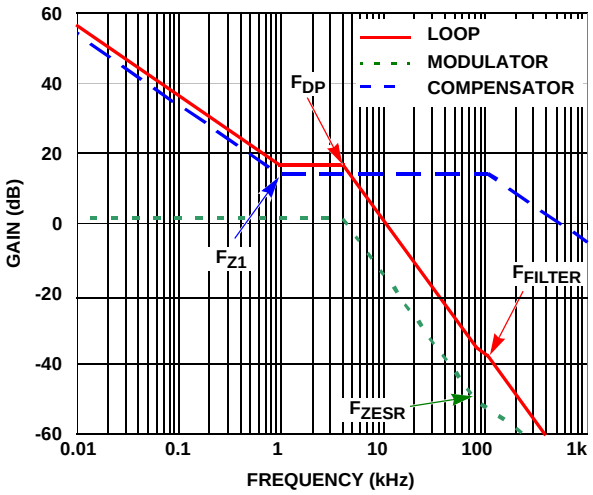


FIGURE 24. CHARGE CURRENT LOOP BODE PLOTS

C_{ICOMP} should be chosen using Equation 26 to set $F_{Z1} = F_{DP}/10$. The crossover frequency will be approximately $2.5*F_{DP}$. The phase margin will be between +10° and +40° depending on F_{ZESR}.

$$C_{ICOMP} = \frac{4 \cdot gm1}{2\pi \cdot F_{DP}/10} \quad \text{(EQ. 26)}$$

Adapter Current Limit Control Loop

If the combined battery charge current and system load current results in adapter current that equals the programmed adapter current limit, ISL9518 will reduce the current to the battery and/or reduce the output voltage to hold the adapter current at the limit. Above the adapter current limit, the minimum current buffer equals the output of gm3 and ICOMP controls the charger output.

A filter should be added between R_{S1} and CSIP and CSIN to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz).

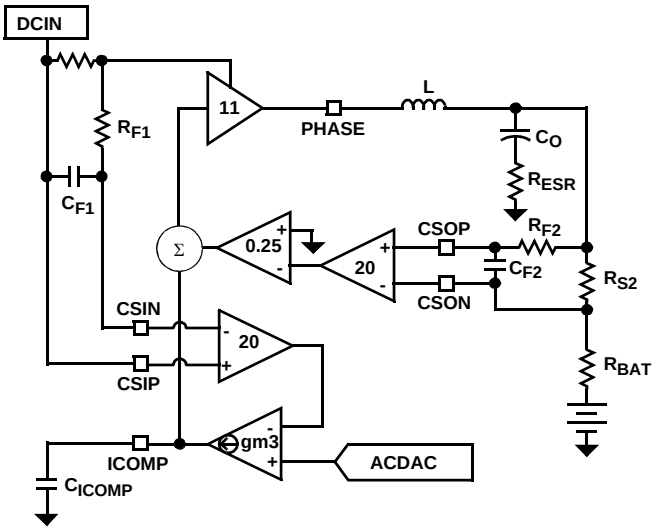


FIGURE 25. ADAPTER CURRENT LIMIT LOOP

The loop response equations, bode plots and the selection of C_{ICOMP} are the same as the charge current control loop with loop gain reduced by the duty cycle. In other words, if the duty cycle D = 50%, the loop gain will be 6dB lower than the loop gain in Figure 24. This gives lower crossover frequency and higher phase margin in this mode.

The current control loops can have the same gain if the Input current sense resistor is larger than the charge current sense resistor by the same ratio that input voltage is larger than output voltage.

Min System Voltage Control Loop

The min system voltage control loop is only active when a battery is connected that is discharged to a voltage below the voltage in the MinSystemVoltage register. When it is active, the ISL9518 reduces the charge current to 256mA and controls the BGATE FET in the linear range to hold the min system voltage on the system output. The reduced charge current and active BGATE control are referred to in this document as “Trickle Charge Mode”.

When the battery voltage is higher than min system voltage, BGATE goes approximately 7V below the system voltage (at CSON) to fully enhance the BGATE FET.

When the battery voltage is less than the min system voltage, the min system voltage loop controls the voltage on BGATE to hold the system voltage at the programmed min system voltage. The difference between the min system voltage and the battery voltage drops across the BGATE FET.

Component Placement

The power MOSFET should be close to the IC so that the gate drive signal, the LGATE, UGATE, PHASE, and BOOT, traces can be short.

Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Signal Ground and Power Ground Connection

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, should be used as signal ground beneath the IC. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each side, where there is little noise; a noisy trace beneath the IC is not recommended.

AGND and VDD Pins

At least one high quality ceramic decoupling capacitor should be used to cross these two pins. The decoupling capacitor can be put close to the IC.

LGATE Pin

This is the gate drive signal for the bottom MOSFET of the buck converter. The signal going through this trace has both high dv/dt and high di/dt, and the peak charging and discharging current is very high. These two traces should be

short, wide, and away from other traces. There should be no other traces in parallel with these traces on any layer.

PGND Pin

PGND pin should be laid out to the source of the lower NMOS.The negative side of the output capacitor must be close to the source node of the bottom MOSFET. This trace is the return path of LGATE.

PHASE Pin

This trace should be short, and positioned away from other weak signal traces. This node has a very high dv/dt with a voltage swing from the input voltage to ground. No trace should be in parallel with it. This trace is also the return path for UGATE. Connect this pin to the high-side MOSFET source.

UGATE Pin

This pin has a square shape waveform with high dV/dt. It provides the gate drive current to charge and discharge the top MOSFET with high di/dt. This trace should be wide, short, and away from other traces, similar to the LGATE.

BOOT Pin

This pin's di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

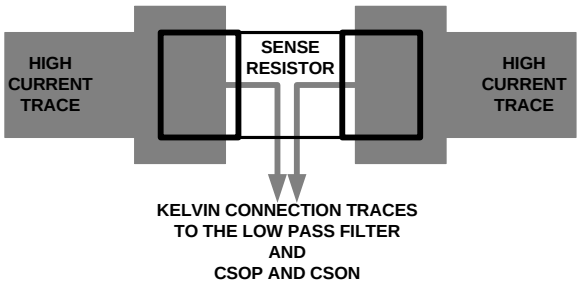


FIGURE 26. CURRENT SENSE RESISTOR LAYOUT

CSOP, CSON, CSIP and CSIN Pins

Accurate charge current and adapter current sensing is critical for good performance. The current sense resistor connects to the CSON and the CSOP pins through a low pass filter with the filter capacitor very near the IC (see Figure 2). Traces from the sense resistor should start at the pads of the sense resistor and should be routed close together through the low pass filter and to the CSOP and CSON pins (see Figure 26). The CSON pin is also used as the system voltage feedback. The traces should be routed away from the high dV/dt and di/dt pins like PHASE, BOOT pins. In general, the current sense resistor should be close to the IC. These guidelines should also be followed for the adapter current sense resistor and CSIP and CSIN. Other layout arrangements should be adjusted accordingly.

DCIN Pin

This pin connects to AC adapter output voltage, and should be less noise sensitive.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

Identify the Power and Signal Ground

The input and output capacitors of the converters (the source terminal of the bottom switching MOSFET PGND) should connect to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at one point.

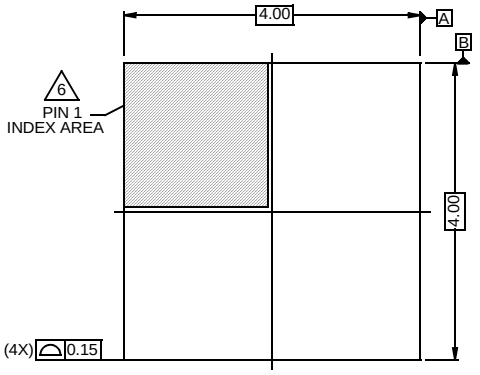
Clamping Capacitor for Switching MOSFET

It is recommended that ceramic capacitors be used closely connected to the drain of the high-side MOSFET, and the source of the low-side MOSFET. This capacitor reduces the noise and the power loss of the MOSFET.

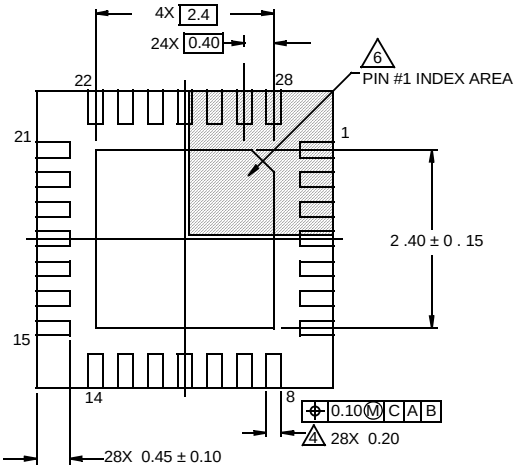
Package Outline Drawing

L28.4x4A

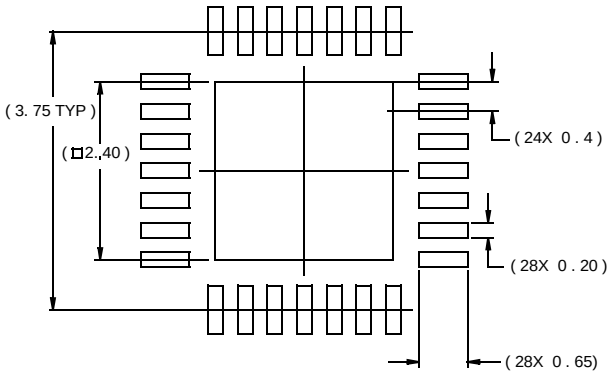
28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 12/08



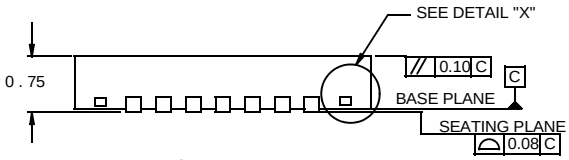
TOP VIEW



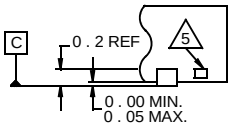
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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