Fiber Channel/Ethernet Clock Generator IC, 7 Clock Outputs

AD9572

FEATURES

Fully integrated dual VCO/PLL cores
- **0.22 ps rms jitter from 0.637 MHz to 10 MHz at 106.25 MHz**
- **0.19 ps rms jitter from 1.875 MHz to 20 MHz at 156.25 MHz**
- **0.42 ps rms jitter from 12 kHz to 20 MHz at 125 MHz**
- **Input crystal or clock frequency of 25 MHz**

Preset divide ratios for 106.25 MHz, 156.25 MHz, 33.33 MHz, 100 MHz, and 125 MHz
Choice of LVPECL or LVDS output format
Integrated loop filters
Copy of reference clock output
Rates configured via strapping pins
0.71 W power dissipation (LVDS operation)
1.07 W power dissipation (LVPECL operation)
3.3 V operation
Space saving, 6 mm × 6 mm, 40-lead LFCSP

APPLICATIONS

Fiber channel line cards, switches, and routers
Gigabit Ethernet/PCIe support included
Low jitter, low phase noise clock generation

FUNCTIONAL BLOCK DIAGRAM

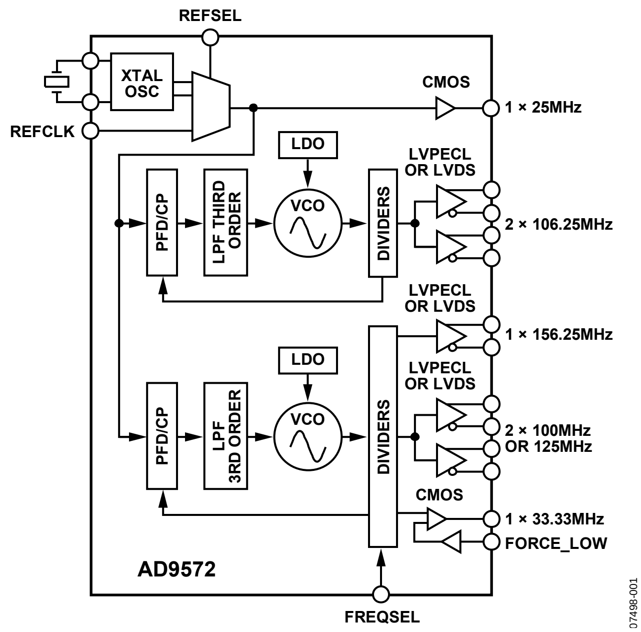

Figure 1.

GENERAL DESCRIPTION

The AD9572 provides a multioutput clock generator function along with two on-chip PLL cores, optimized for fiber channel line card applications that include an Ethernet interface. The integer-N PLL design is based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize network performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a low noise phase frequency detector (PFD), a precision charge pump (CP), a low phase noise voltage controlled oscillator (VCO), and a preprogrammed feedback divider and output divider. By connecting an external crystal or reference clock to the REFCLK pin, frequencies up to 156.25 MHz can be locked to the input reference. Each output divider and feedback divider ratio is preprogrammed for the required output rates.

A second PLL also operates as an integer-N synthesizer and drives two LVPECL or LVDS output buffers for 106.25 MHz operation. No external loop filter components are required, thus conserving valuable design time and board space.

The AD9572 is available in a 40-lead, 6 mm × 6 mm lead frame chip scale package (LFCSP) and can be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

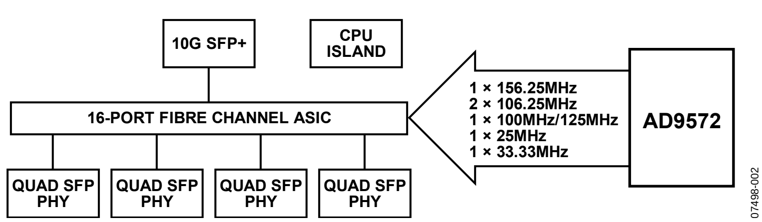

Figure 2. Typical Application

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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SPECIFICATIONS

PLL CHARACTERISTICS

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE NOISE CHARACTERISTICS					
PLL Noise (106.25 MHz LVDS Output)					
At 1 kHz		−123		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−129		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−152		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−153		dBc/Hz	33.33 MHz output disabled
PLL Noise (156.25 MHz LVDS Output)					
At 1 kHz		−118		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−125		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−126		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−145		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−151		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−151		dBc/Hz	33.33 MHz output disabled
PLL Noise (125 MHz LVDS Output)					
At 1 kHz		−119		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−147		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−151		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−152		dBc/Hz	33.33 MHz output disabled
PLL Noise (100 MHz LVDS Output)					
At 1 kHz		−121		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−130		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−147		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−150		dBc/Hz	33.33 MHz output disabled
PLL Noise (106.25 MHz LVPECL Output)					
At 1 kHz		−121		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−129		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−151		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−154		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−155		dBc/Hz	33.33 MHz output disabled
PLL Noise (156.25 MHz LVPECL Output)					
At 1 kHz		−119		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−125		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−126		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−147		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−152		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−153		dBc/Hz	33.33 MHz output disabled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Noise (125 MHz LVPECL Output)					
At 1 kHz		−122		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−148		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−152		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−153		dBc/Hz	33.33 MHz output disabled
PLL Noise (100 MHz LVPECL Output)					
At 1 kHz		−122		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−130		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−148		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−151		dBc/Hz	33.33 MHz output disabled
PLL Noise (33.33 MHz CMOS Output)					
At 1 kHz		−130		dBc/Hz	
At 10 kHz		−138		dBc/Hz	
At 100 kHz		−139		dBc/Hz	
At 1 MHz		−152		dBc/Hz	
At 5 MHz		−152		dBc/Hz	
Phase Noise (25 MHz CMOS Output)					
At 1 kHz		−133		dBc/Hz	
At 10 kHz		−142		dBc/Hz	
At 100 kHz		−148		dBc/Hz	
At 1 MHz		−148		dBc/Hz	
At 5 MHz		−148		dBc/Hz	
Spurious Content[1]		−70		dBc	Dominant amplitude, all outputs active
PLL Figure of Merit		−217.5		dBc/Hz	

[1] When the 33.33 MHz, 100 MHz, and 125 MHz clocks are enabled simultaneously, a worst-case −50 dBc spurious content might be presented on Pin 21 and Pin 22 only.

LVDS CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 2.

Jitter Integration Bandwidth (Typ)	100 MHz	106.25 MHz	125 MHz 33M = Off/On[1]	156.25 MHz	Unit	Test Conditions/Comments
12 kHz to 20 MHz	0.51	0.44	0.42/0.88	0.42	ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
1.875 MHz to 20 MHz				0.19	ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
637 kHz to 10 MHz		0.22			ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
200 kHz to 10 MHz	0.32		0.25/0.78		ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz			0.50 (off only)		ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 2 × 125 MHz, 2 × 106.25 MHz

[1] The typical 125 MHz rms jitter data is collected from the differential pair, Pin 21 and Pin 22, unless otherwise noted.

LVPECL CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 3.

Jitter Integration Bandwidth (Typ)	100 MHz	106.25 MHz	125 MHz 33M = Off/On	156.25 MHz	Unit	Test Conditions/Comments
12 kHz to 20 MHz (Typ)	0.61	0.45	0.44/2.2	0.46	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 20 MHz (Max)	0.87	0.81	0.56 (off only)	0.56	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
1.875 MHz to 20 MHz (Typ)				0.28	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
637 kHz to 10 MHz (Typ)		0.23			ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
200 kHz to 10 MHz (Typ)	0.38		0.24/2.2		ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz (Typ)			0.52 (off only)		ps rms	LVPECL output frequency combinations are 156.25 MHz unterminated, 2 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz (Max)			0.66 (off only)		ps rms	LVPECL output frequency combinations are 156.25 MHz unterminated, 2 × 125 MHz, 2 × 106.25 MHz

CMOS CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 4.

Jitter Integration Bandwidth	25 MHz	33.3 MHz	Unit	Test Conditions/Comments
12 kHz to 5 MHz (Typ)	0.78	0.41	ps rms	
12 kHz to 5 MHz (Max)	1.1	N/A	ps rms	
200 kHz to 5 MHz (Typ)	0.76	0.52	ps rms	
200 kHz to 5 MHz (Max)	1.0	N/A	ps rms	

REFERENCE INPUT

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (REFCLK)					
Input Frequency		25		MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Current	−1.0		+1.0	µA	
Input Capacitance		2		pF	

CLOCK OUTPUTS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					
Output Frequency			156.25	MHz	
Output High Voltage (V_{OH})	V_S − 1.24	V_S − 1.05	V_S − 0.83	V	
Output Low Voltage (V_{OL})	V_S − 2.07	V_S − 1.87	V_S − 1.62	V	
Output Differential Voltage (V_{OD})	700	825	950	mV	
Duty Cycle	45		55	%	
LVDS CLOCK OUTPUTS					
Output Frequency			156.25	MHz	
Differential Output Voltage (V_{OD})	250	350	475	mV	
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.25	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
Duty Cycle	45		55	%	
CMOS CLOCK OUTPUTS					
Output Frequency			33.33	MHz	
Output High Voltage (V_{OH})	V_S − 0.1			V	Sourcing 1.0 mA current
Output Low Voltage (V_{OL})			0.1	V	Sinking 1.0 mA current
Duty Cycle	42		58	%	

TIMING CHARACTERISTICS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 200 Ω to 0 V; C_{LOAD} = 0 pF; C_{AC} = 100 nF; oscilloscope set to 50 Ω termination
Output Rise Time, t_{RP}	480	625	810	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}	480	625	810	ps	80% to 20%, measured differentially
LVDS					Termination = 100 Ω differential; C_{LOAD} = 0 pF; C_{AC} = 100 nF; oscilloscope set to 50 Ω termination
Output Rise Time, t_{RL}	160	350	540	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	160	350	540	ps	80% to 20%, measured differentially
CMOS					
Output Rise Time, t_{RC}	0.25	0.50	2.5	ns	20% to 80%; termination = 50 Ω to 0 V; C_{LOAD} = 5 pF; C_{AC} = 100 nF
Output Fall Time, t_{FC}	0.25	0.70	2.5	ns	80% to 20%; termination = 50 Ω to 0 V; C_{LOAD} = 5 pF; C_{AC} = 100 nF
Output Rise Time, t_{RC2}	1.3	2.1	2.6	ns	20% to 80%; active probe measurement, C_{probe} = 1 pF, R_{probe}=20 kΩ, C_{LOAD} = 3.9 pF
Output Fall Time, t_{FC2}	1.4	2.3	3.0	ns	80% to 20%; active probe measurement, C_{probe} = 1 pF, R_{probe}=20 kΩ, C_{LOAD} = 3.9 pF

CONTROL PINS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
REFSEL Pin					REFSEL has a 30 kΩ pull-up resistor.
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			1.0	µA	
Logic 0 Current			155	µA	
FREQSEL Pin					FREQSEL has a 150 kΩ pull-up resistor and a 100 kΩ pull-down resistor.
Logic 1 Voltage	2/3(V_S) + 0.2			V	
Logic 0 Voltage			1/3(V_S) − 0.2	V	
Logic 1 Current			45	µA	
Logic 0 Current			30	µA	
FORCE_LOW Pin					FORCE_LOW has a 16 kΩ pull-down resistor.
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			240	µA	
Logic 0 Current			2.0	µA	

POWER

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Supply	3.0	3.3	3.6	V	
LVDS Power Dissipation		715	870	mW	
LVPECL Power Dissipation		1075	1305	mW	

CRYSTAL OSCILLATOR

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL SPECIFICATION					Fundamental mode
Frequency		25		MHz	
ESR			50	Ω	
Load Capacitance		14		pF	
Phase Noise		−135		dBc/Hz	At 1 kHz offset
Stability	−30		+30	ppm	

TIMING DIAGRAMS

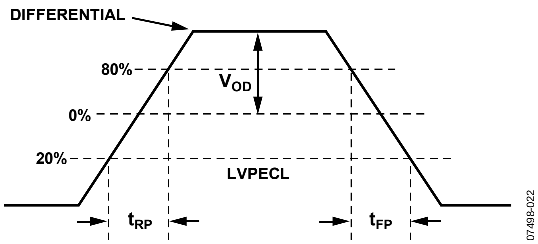

Figure 3. LVPECL Timing, Differential

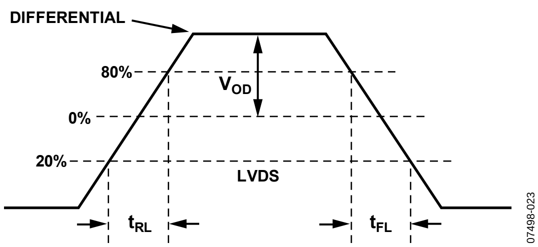

Figure 4. LVDS Timing, Differential

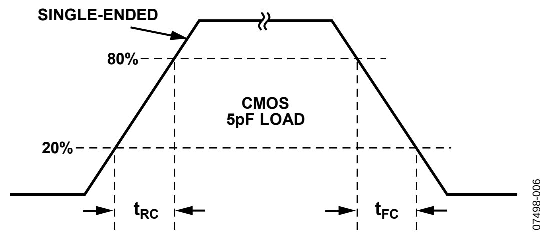

Figure 5. CMOS Timing, Single-Ended, 5 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter	Rating
VS to GND	−0.3 V to +3.6 V
REFCLK to GND	−0.3 V to VS + 0.3 V
BYPASSx to GND	−0.3 V to VS + 0.3 V
XO to GND	−0.3 V to VS + 0.3 V
FREQSEL, FORCE_LOW, and REFSEL to GND	−0.3 V to VS + 0.3 V
25M, 33M, 100M/125M, 106M, and 156M to GND	−0.3 V to VS + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C

[1] See Table 12 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

Table 12. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead LFCSP	27.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

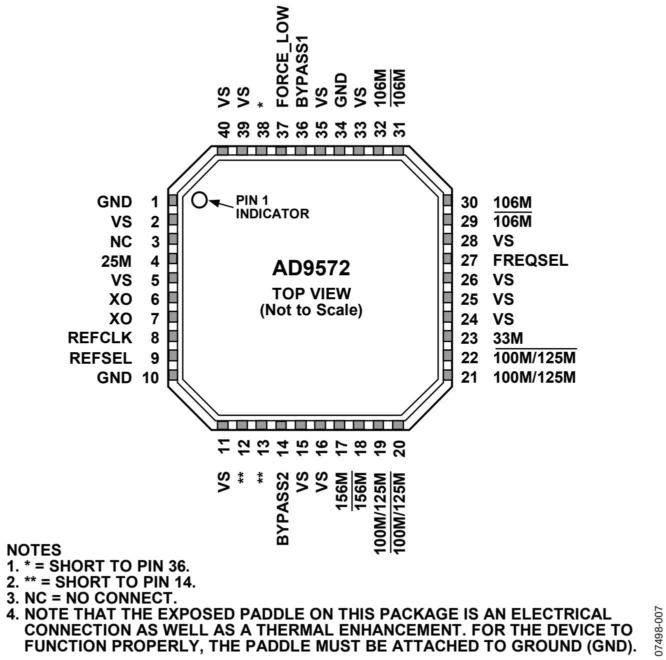

Figure 6. Pin Configuration

Table 13. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1, 10, 34	GND	Ground. Includes external paddle (EPAD).
2	VS	Power Supply Connection for the 25M CMOS Buffer.
3	NC	No Connect. This pin should be left floating.
4	25M	CMOS 25 MHz Output.
5	VS	Power Supply Connection for the Crystal Oscillator.
6, 7	XO	External 25 MHz Crystal.
8	REFCLK	25 MHz Reference Clock Input. Tie low when not in use.
9	REFSEL	Logic Input. Used to select the reference source.
11	VS	Power Supply Connection for the GbE PLL.
12, 13	N/A	Short to Pin 14.
14, 36	BYPASS2, BYPASS1	These pins are for bypassing each LDO to ground with a 220 nF capacitor.
15	VS	Power Supply Connection for the GbE VCO.
16	VS	Power Supply Connection for the 156M LVDS Output Buffer and Output Dividers.
17	156M	LVPECL/LVDS Output at 156.25 MHz.
18	$\overline{\text{156M}}$	Complementary LVPECL/LVDS Output at 156.25 MHz.
19, 21	100M/125M	LVPECL/LVDS Output at 100 MHz or 125 MHz. Selected by FREQSEL pin strapping.
20, 22	$\overline{\text{100M}}$/$\overline{\text{125M}}$	Complementary LVPECL/LVDS Output at 100 MHz or 125 MHz.
23	33M	CMOS 33.33 MHz Output.
24	VS	Power Supply Connection for the 33M CMOS Output Buffer and Output Dividers.
25	VS	Power Supply Connection for the 100M/125M LVDS Output Buffer and Output Dividers.
26	VS	Power Supply Connection for the GbE PLL Feedback Divider.
27	FREQSEL	Logic Input. Used to configure output drivers.
28	VS	Power Supply Connection for the FC PLL Feedback Divider.
29, 31	$\overline{\text{106M}}$	LVPECL/LVDS Output at 106.25 MHz.
30, 32	106M	Complementary LVPECL/LVDS Output at 106.25 MHz.

Pin No.	Mnemonic	Description
33	VS	Power Supply Connection for the 106.25 MHz LVDS Output Buffer and Output Dividers.
35	VS	Power Supply Connection for the FC VCO.
37	FORCE_LOW	Forces the 33.33 MHz output into a low state.
38	N/A	Short to Pin 36.
39	VS	Power Supply Connection for the FC PLL.
40	VS	Power Supply Connection for Miscellaneous Logic.

[1] The exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground (GND).

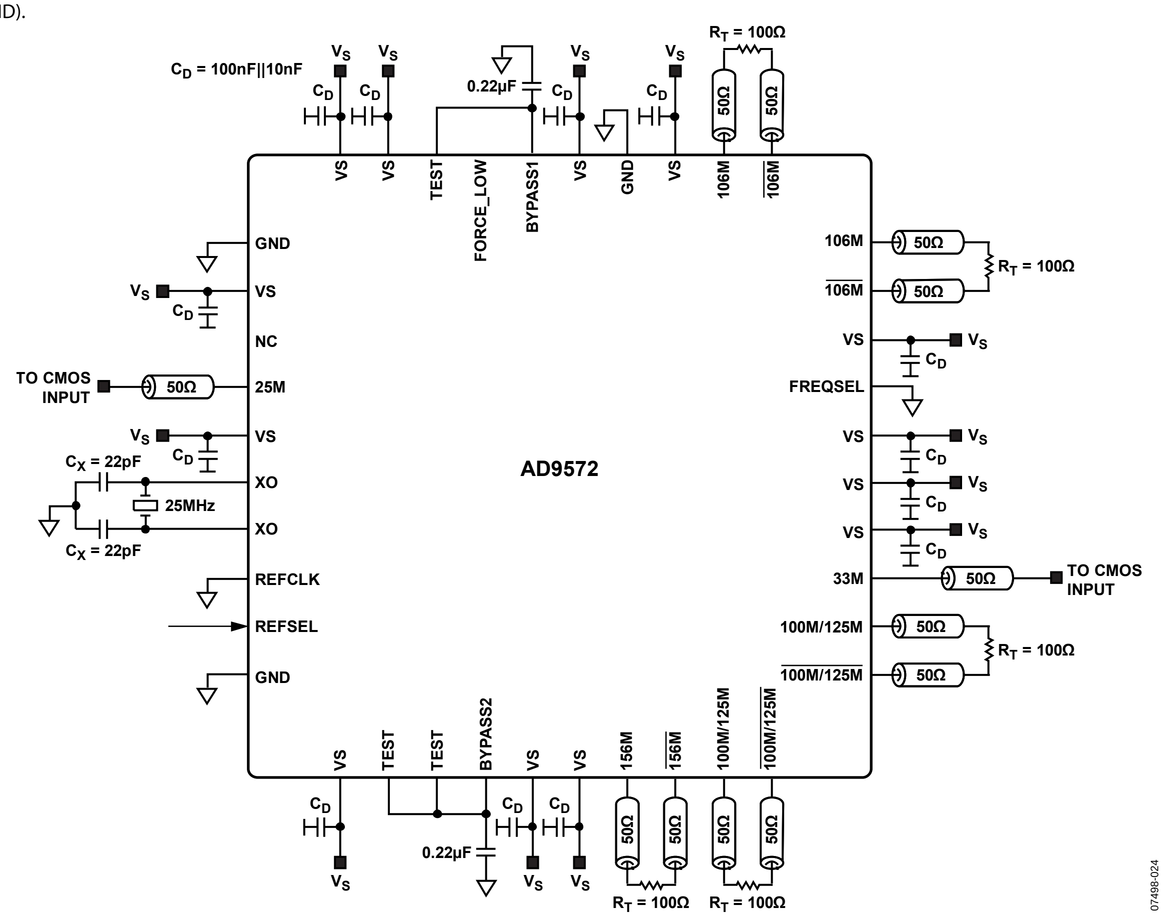

Figure 7. Typical Application Schematic, LVDS Format Outputs, 1 × 25 MHz, 1 × 156.25 MHz, 2 × 125 MHz, and 2 × 106.25 MHz

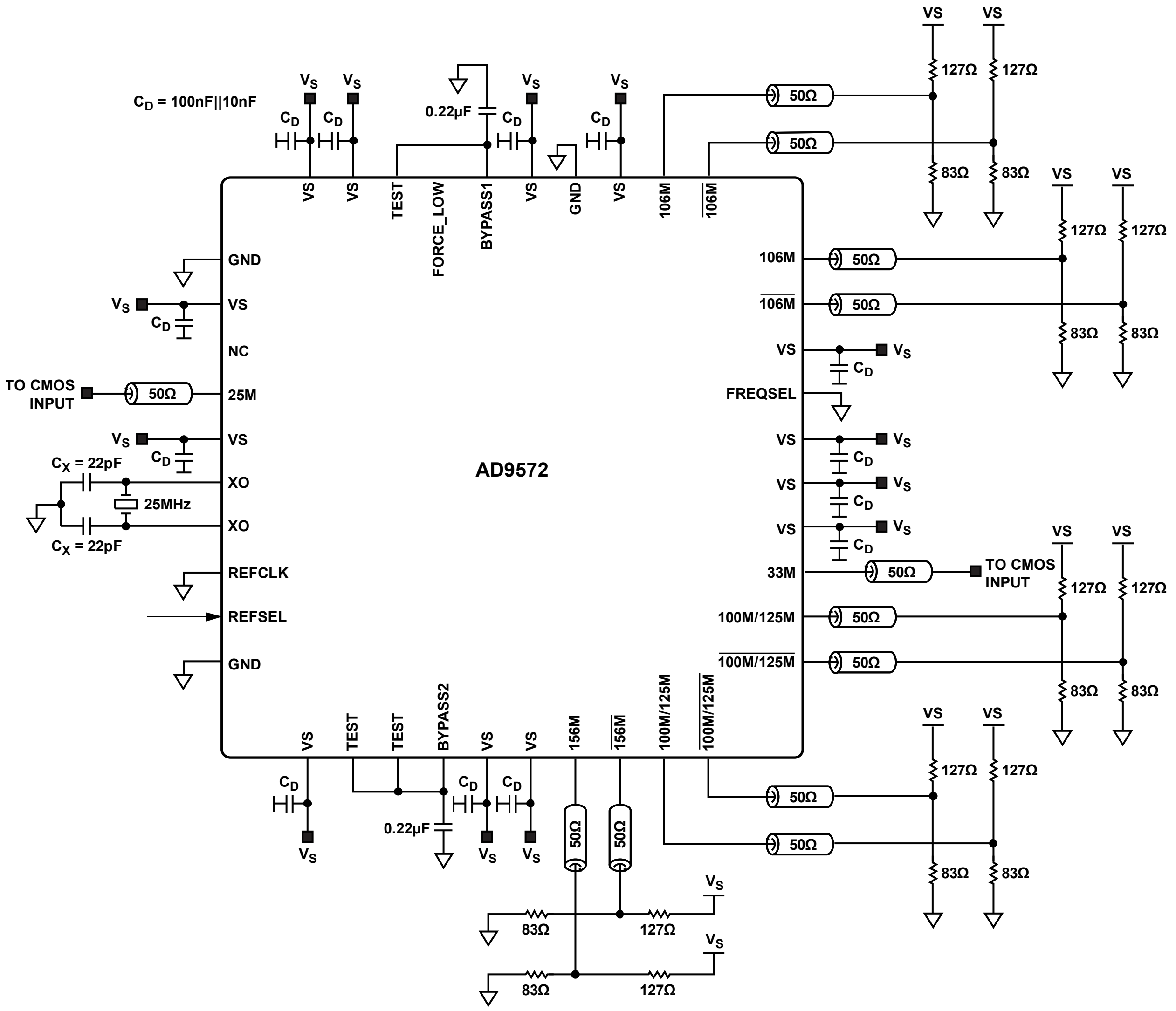

Figure 8. Typical Application Schematic, LPECL Format Outputs, 1 × 25 MHz, 1 × 156.25 MHz, 2 × 125 MHz, and 2 × 106.25 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

Phase noise plots taken with 100 MHz and 125 MHz outputs enabled; 33.3 MHz output disabled.

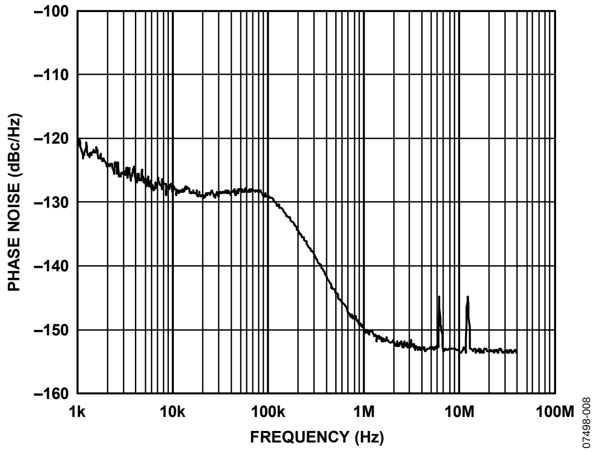

Figure 9. 106.25 MHz Phase Noise

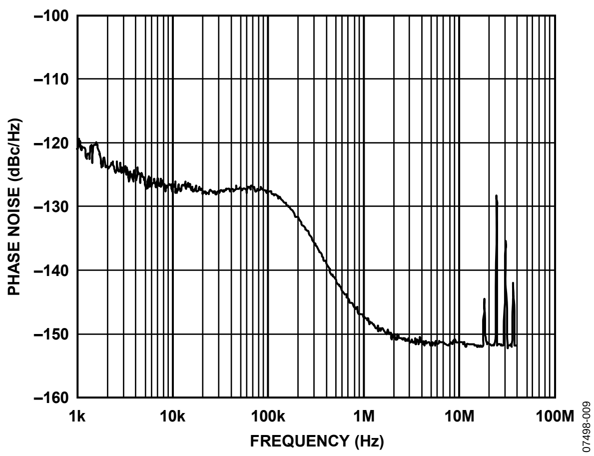

Figure 10. 125 MHz Phase Noise

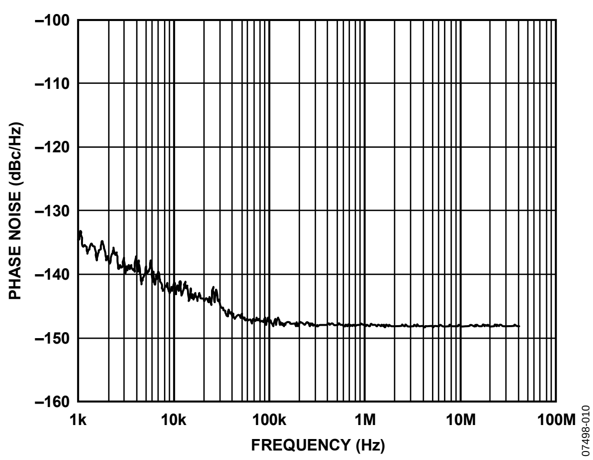

Figure 11. 25 MHz Phase Noise

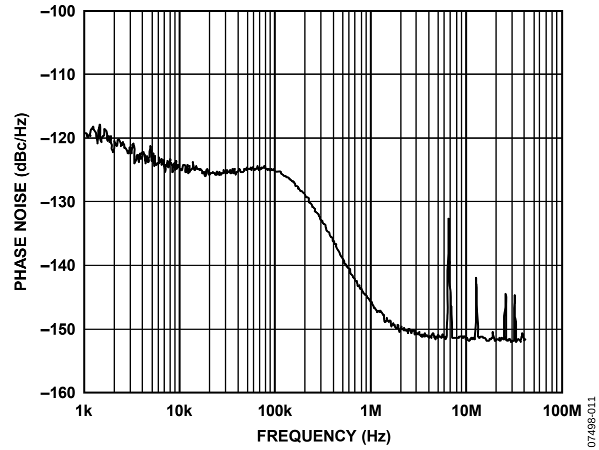

Figure 12. 156.25 MHz Phase Noise

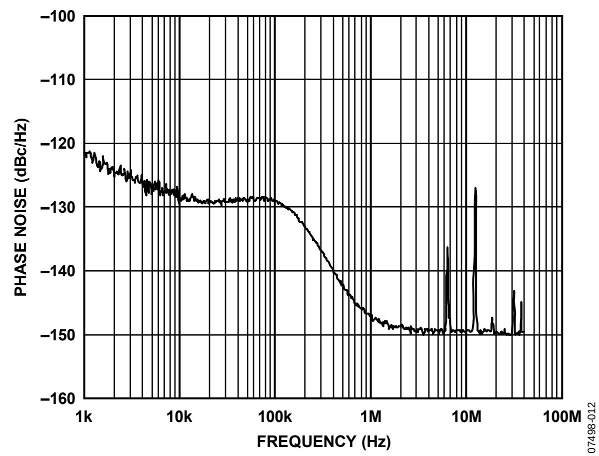

Figure 13. 100 MHz Phase Noise

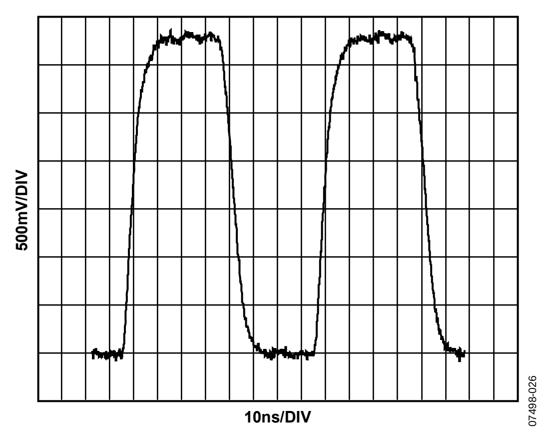

Figure 14. 25 MHz CMOS Output, 3.9 pF Load Capacitance on Evaluation Board, Active-Probe Measurement, R_{probe}=20 kΩ, C_{probe}=1 pF

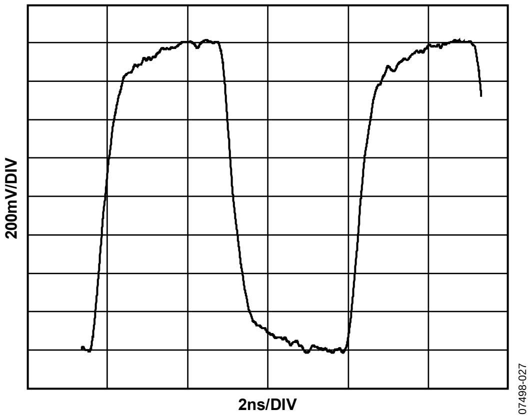

Figure 15. 156.25 MHz LVPECL Output, Differential Plot, 200 Ω Termination to GND on Evaluation Board, AC-Coupled via 0.1 μF Capacitors to Oscilloscope Set to 50 Ω Input Termination

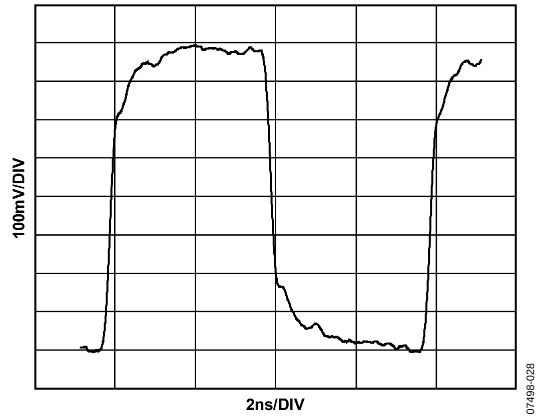

Figure 16. 125 MHz LVDS Output, Differential Plot, AC-Coupled via 0.1 μF Capacitors to Oscilloscope Set to 50 Ω Input Termination

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from the ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise

When the total power contained within some interval of offset frequencies (for example, 12 kHz to 20 MHz) is integrated, it is called the integrated phase noise over that frequency offset interval, and it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on error rate performance by increasing eye closure at the transmitter output and reducing the jitter tolerance/sensitivity of the receiver.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillator or clock source has been subtracted. This makes it possible to predict the degree to which the device will impact the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

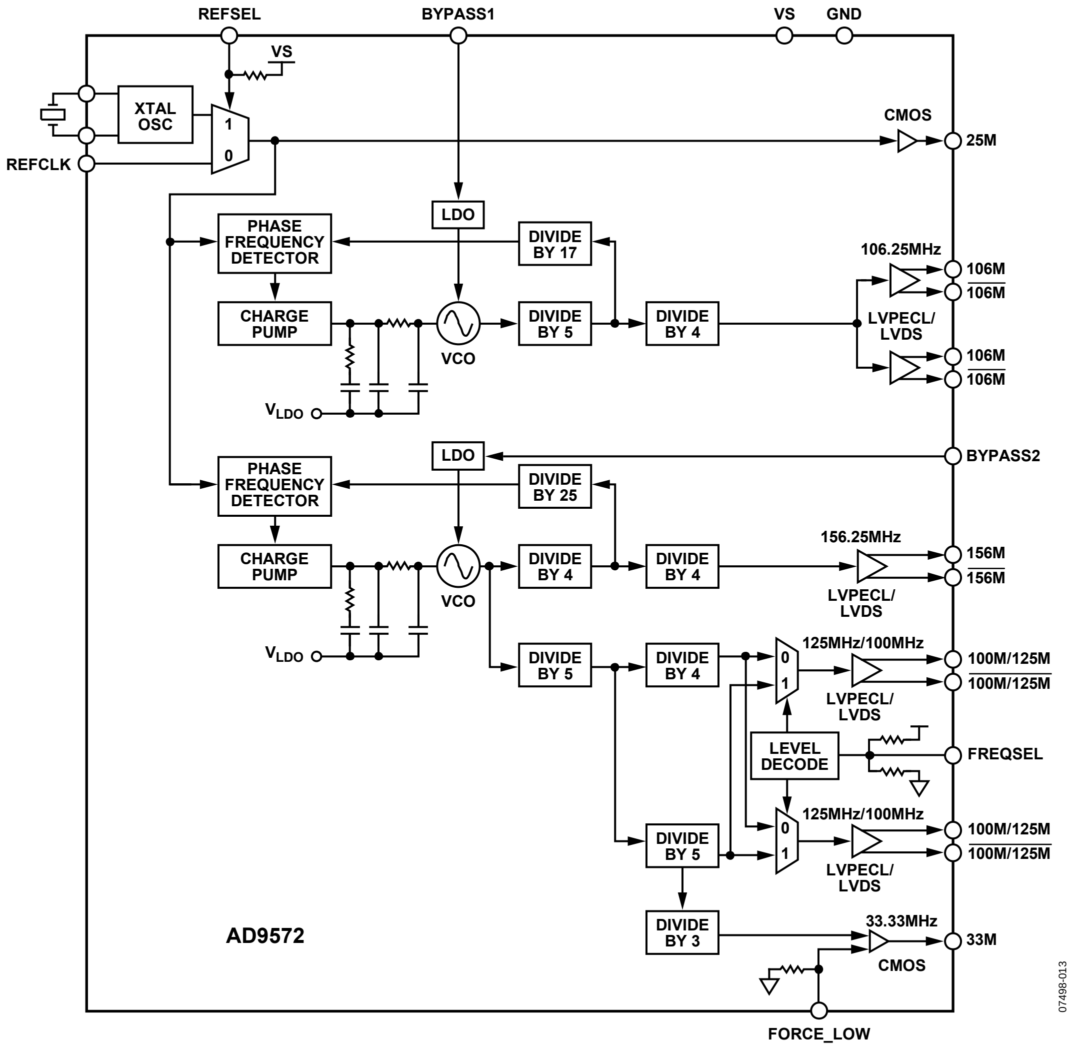

Figure 17. Detailed Block Diagram

Figure 17 shows a block diagram of the AD9572. The chip combines dual PLL cores, which are configured to generate the specific clock frequencies required for networking applications without any user programming. This PLL is based on proven Analog Devices synthesizer technology, noted for its exceptional phase noise performance. The AD9572 is highly integrated and includes loop filters, regulators for supply noise immunity, all the necessary dividers with multiple output buffers in a choice of formats, and a crystal oscillator. A user need only supply a 25 MHz reference clock or an external crystal to implement an entire line card clocking solution that does not require any processor intervention. A copy of the 25 MHz reference source is also available.

OUTPUTS

Table 14 provides a summary of the outputs available.

Table 14. Output Formats

Frequency	Format	Copies
25 MHz	CMOS	1
106.25 MHz	LVPECL/LVDS	2
156.25 MHz	LVPECL/LVDS	1
100 MHz or 125 MHz	LVPECL/LVDS	2
33.33 MHz	CMOS	1

Note that the pins labeled 100M/125M can provide 100 MHz or 125 MHz by strapping the FREQSEL pin as shown in Table 15.

Table 15. FREQSEL (Pin 27) Definition

FREQSEL	Frequency Available from Pin 19 and Pin 20 (MHZ)	Frequency Available from Pin 21 and Pin 22 (MHZ)
0	125	125
1	100	100
NC	125	100

The simplified equivalent circuits of the LVDS and LVPECL outputs are shown in Figure 18 and Figure 19.

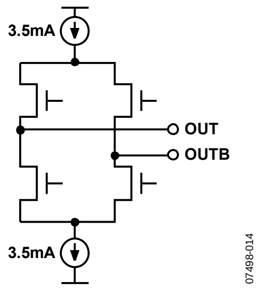

Figure 18. LVDS Output Simplified Equivalent Circuit

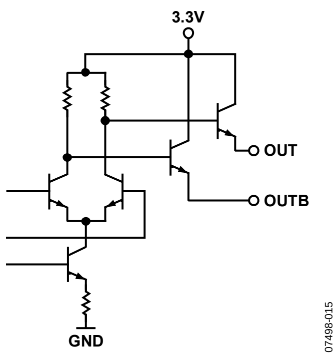

Figure 19. LVPECL Output Simplified Equivalent Circuit

The differential outputs are factory programmed to either LVPECL or LVDS format, and either option can be sampled on request.

CMOS drivers tend to generate more noise than differential outputs and, as a result, the proximity of the 33.33 MHz output to Pin 21 and Pin 22 does affect the jitter performance when FREQSEL = 0 (that is, when the differential output is generating 125 MHz). For this reason, the 33 MHz pin can be forced to a low state by asserting the FORCE_LOW signal on Pin 37 (see Table 16). An internal pull-down enables the 33.33 MHz output if the pin is not connected.

Table 16. FORCE_LOW (Pin 37) Definition

FORCE_LOW	33.33 MHz Output (Pin 23)
0 or NC	33.33 MHz
1	0

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the reference clock and feedback divider to produce an output proportional to the phase and frequency difference between them. Figure 20 shows a simplified schematic.

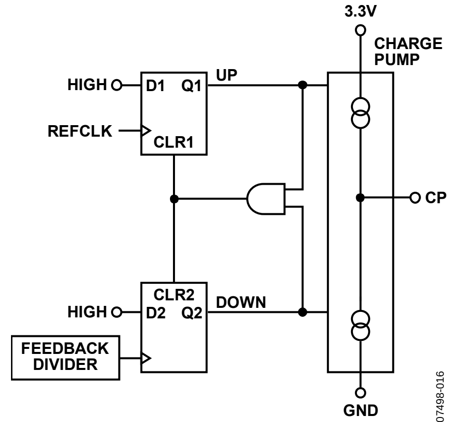

Figure 20. PFD Simplified Schematic

POWER SUPPLY

The AD9572 requires a 3.3 V ± 10% power supply for V_S. The tables in the Specifications section give the performance expected from the AD9572 with the power supply voltage within this range. The absolute maximum range of −0.3 V to +3.6 V, with respect to GND, must never be exceeded on the VS pin.

Good engineering practice should be followed in the layout of power supply traces and the ground plane of the PCB. The power supply should be bypassed on the PCB with adequate capacitance (>10 µF). The AD9572 should be bypassed with adequate capacitors (0.1 µF) at all power pins as close as possible to the part. The layout of the AD9572 evaluation board is a good example.

The exposed metal paddle on the AD9572 package is an electrical connection, as well as a thermal enhancement. For the device to function properly, the paddle must be properly attached to ground (GND). The PCB acts as a heat sink for the AD9572; therefore, this GND connection should provide a good thermal path to a larger dissipation area, such as a ground plane on the PCB.

CMOS CLOCK DISTRIBUTION

The AD9572 provides two CMOS clock outputs (one 25 MHz and one 33.33 MHz) that are dedicated CMOS levels. Whenever single-ended CMOS clocking is used, some of the following general guidelines should be followed.

Point-to-point nets should be designed such that a driver has one receiver only on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. CMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 6 inches are recommended to preserve signal rise/fall times and signal integrity.

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the AD9572 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 21. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

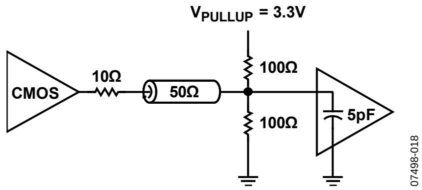

Figure 21. CMOS Output with Far-End Termination

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs, which are open emitter, require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 19 shows the LVPECL output stage.

In most applications, a standard LVPECL far-end termination is recommended, as shown in Figure 22. The resistor network is designed to match the transmission line impedance (50 Ω) and establish a dc bias of (V_{CC} – 2 V). An alternative dc-coupled LVPECL termination network with a reduced number of components is also possible as shown in Figure 23.

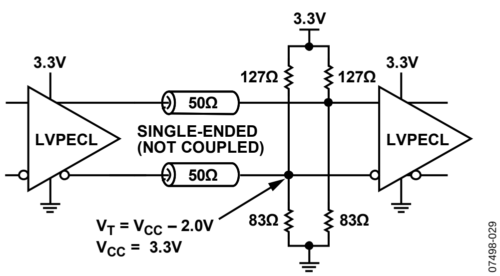

Figure 22. LVPECL Far-End Termination

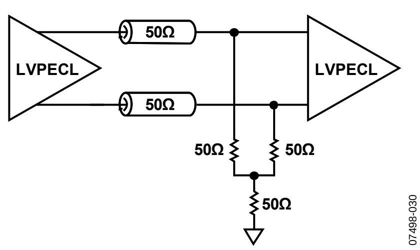

Figure 23. LVPECL Y Termination

An ac- coupled LVPECL termination scheme is shown in Figure 24.

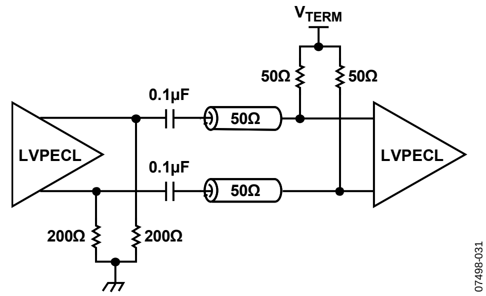

Figure 24. LVPECL AC- Coupled Termination

LVDS CLOCK DISTRIBUTION

The AD9572 is also available with low voltage differential signaling (LVDS) outputs. LVDS uses a current mode output stage with a factory programmed current level. The normal value (default) for this current is 3.5 mA, which yields a 350 mV output swing across a 100 Ω resistor. The LVDS outputs meet or exceed all ANSI/TIA/EIA-644 specifications.

A recommended termination circuit for the LVDS outputs is shown in Figure 25.

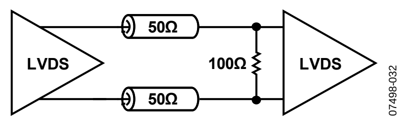

Figure 25. LVDS Output Termination

See the AN-586 Application Note on the Analog Devices website at www.analog.com for more information about LVDS.

REFERENCE INPUT

By default, the crystal oscillator is enabled and used as the reference source, which requires the connection of an external 25 MHz crystal cut to resonate in fundamental mode. The total load capacitance presented to the oscillator should sum to 14 pF. In the example shown in Figure 26, parasitic trace capacitance of 1.5 pF, and an AD9572 input pin capacitance of 1.5 pF are assumed, with the series combination of the two 22 pF capacitances providing a further 11 pF. The REFSEL pin is pulled high internally by about 30 kΩ to support default operation.

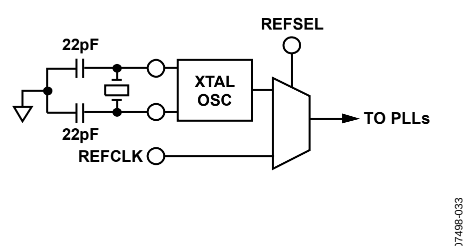

Figure 26. Reference Input section

When REFSEL is tied low, the crystal oscillator is powered down, and the REFCLK pin must provide a good quality 25 MHz reference clock instead. This single-ended input can be driven by either a dc-coupled LVCMOS level signal or an ac-coupled sine wave or square wave, provided that an external divider is used to bias the input at $V_S/2$.

Table 17. REFSEL (Pin 9) Definition

REFSEL	Reference Source
0	REFCLK input
1	Internal crystal oscillator

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as for power supply bypassing and grounding to ensure optimum performance. Each power supply pin should have independent decoupling and connections to the power supply plane. It is recommended that the device exposed paddle be directly connected to the ground plane by a grid of at least nine vias. Care should be taken to ensure that the output traces cannot couple onto the reference or crystal input circuitry. Traces should not be routed under the crystal. Output signal traces should be kept on the top PCB layer; these traces have very high edge rates, and the use of PCB vias will result in signal integrity problems.

OUTLINE DIMENSIONS

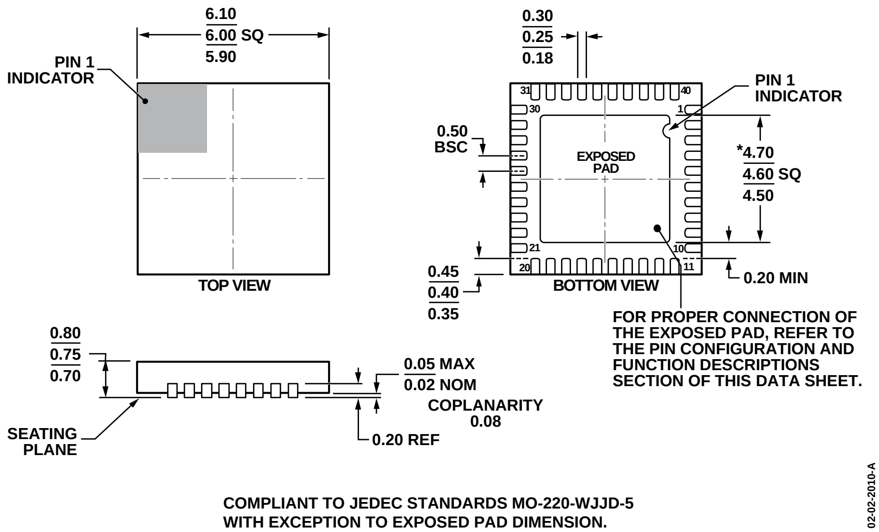

Figure 27. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
AD9572ACPZLVD	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-7
AD9572ACPZLVD-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 13" Tape and Reel, 2,500 Pieces	CP-40-7
AD9572ACPZLVD-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7" Tape and Reel, 750 Pieces	CP-40-7
AD9572ACPZPEC	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-7
AD9572ACPZPEC-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 13" Tape and Reel, 2,500 Pieces	CP-40-7
AD9572ACPZPEC-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7" Tape and Reel, 750 Pieces	CP-40-7
AD9572-EVALZ-LVD		Evaluation Board	
AD9572-EVALZ-PEC		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] LVD indicates LVDS-compliant, differential clock outputs.
[3] PEC indicates LVPECL-compliant, differential clock outputs.

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