



MICROCHIP

PIC16C63 → PIC16C63A Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note: Even though compatible devices are specified to be tested to the same electrical specification, the characteristics of the devices may be different from each other (due to process difference). For systems that were designed to the device specifications, these process differences should not cause any issues in the application. For systems that did not tightly meet the electrical specifications, the process differences may cause the device to behave differently in the application.

Note: While there are no functional or electrical changes to the device oscillator specifications, the user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C63 to the PIC16C63A.

TABLE 1: PIC16C63 → PIC16C63A DIFFERENCES

Functional Differences due to Errata or Module Update					
No.	Module	Difference	H/W	S/W	Prog.
1	CCP	CCP Special Event Trigger clears Timer1.	—	✓	—
2		Compare mode drives pin correctly.	—	✓	—
3	Timers	Reading or writing TMR1H or TMR1L may affect TMR1H or TMR1L unexpectedly.	—	✓	—
4		WDT/TMR0 prescaler assignment changes do not affect TMR0 count.	—	✓	—
5	SSP	TMR2 SPI™ clock synchronized to start of SPI Transmission.	—	✓	—
6		Can now transmit multiple words in SPI mode.	—	✓	—
7		Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023A).	—	✓	—
8		I ² C™ no longer generates ACK pulses when module is enabled.	—	✓	—
9	USART	Async receive errors due to BRGH setting corrected.	—	✓	—
10	Oscillator	TOST delay may be skipped when waking from SLEEP.	—	✓	—
11	RESET	Short MCLR pulses may cause improper operation on the PIC16C63A.	✓	—	—
12		Operating voltage and frequency ranges have been redefined.	✓	—	—
H/W - Issues may exist with regard to the application circuits. S/W - Issues may exist with regard to the user program. Prog. - Issues may exist when writing the program to the controller.					

TABLE 2: ELECTRICAL SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic	PIC16C63			PIC16C63A			Unit	
			Min	Typ†	Max	Min	Typ†	Max		
Core										
D001 D001A	VDD	Supply Voltage XT, LP and RC mode HS mode BOR enabled (Note 1)	4.0 4.5 —	— — —	6.0 5.5 —	4.0 4.0 VBOR	— — —	5.5 5.5 5.5	V V V	
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.3	3.65	—	4.35	V	
D150	VOD	Open-Drain High Voltage on RA4	—	—	14.0	—	—	8.5	V	
SSP in SPI mode										
71 71A	Tsch	SCK input high time (slave mode)	Continuous Single Byte	Tcy+20	—	—	1.25Tcy + 30 40	— —	— —	ns ns
72 72A	TscL	SCK input low time (slave mode)	Continuous Single Byte	Tcy+20	—	—	1.25Tcy + 30 40	— —	— —	ns ns
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge		50	—	—	100	—	—	ns
73A (Note 2)	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		—	—	—	1.5Tcy + 40	—	—	ns
74	Tsch2diL TscL2diL	Hold time of SDI data input to SCK edge		50	—	—	100	—	—	ns
75	TdoR	SDO data output rise time	PIC16CXX PIC16LCXX	—	10	25	— —	10 20	25 45	ns ns
78	TscR	SCK output rise time (master mode)	PIC16CXX PIC16LCXX	—	10	25	— —	10 20	25 45	ns ns
80	Tsch2doV TscL2doV	SDO data output valid after SCK edge	PIC16CXX PIC16LCXX	—	—	50	— —	— —	50 100	ns ns
83	Tsch2ssH TscL2ssH	SS ↑ after SCK edge		—	—	—	1.5Tcy + 40	—	—	ns

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate until VDD drops below VBOR.

2: Specification 73A is only required if specifications 71A and 72A are used.

NOTES:



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-786-7200 Fax: 480-786-7277
Technical Support: 480-786-7627
Web Address: <http://www.microchip.com>

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc.
2 LAN Drive, Suite 120
Westford, MA 01886
Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc.
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Microchip Technology Inc.
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

AMERICAS (continued)

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

China - Beijing

Microchip Technology, Beijing
Unit 915, 6 Chaoyangmen Bei Dajie
Dong Erhuan Road, Dongcheng District
New China Hong Kong Manhattan Building
Beijing, 100027, P.R.C.
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai

Microchip Technology
Unit B701, Far East International Plaza,
No. 317, Xianxia Road
Shanghai, 200051, P.R.C.
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong

Microchip Asia Pacific
Unit 2101, Tower 2
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
I Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 027, India
Tel: 91-80-207-2165 Fax: 91-80-207-2171

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 München, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

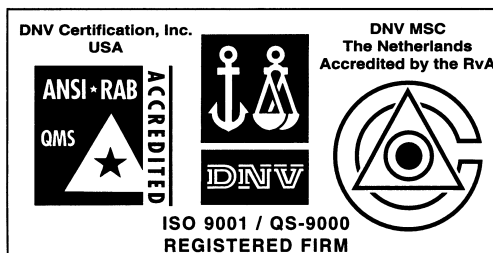
Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5858 Fax: 44-118 921-5835

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