Sympol™ Transceiver

This manual describes the SN65HVD96 Evaluation Module (EVM). This EVM helps designers evaluate the device performance under wire-fault and common-mode conditions, thus supporting the fast development and analysis of data transmission systems using SN65HVD96 transceivers.

Contents

List of Figures

Sympol is a trademark of Texas Instruments.

1 Overview

The SN65HVD96 is designed for error-free data transmission under wire-fault conditions. The receiver provides correct output data whether the bus wires are connected normally or cross-wired. This feature is known as symmetric-polarity (Sympol™) and is auto-detected internally, so no intervention from the controller or the operator is required (see Figure 1).
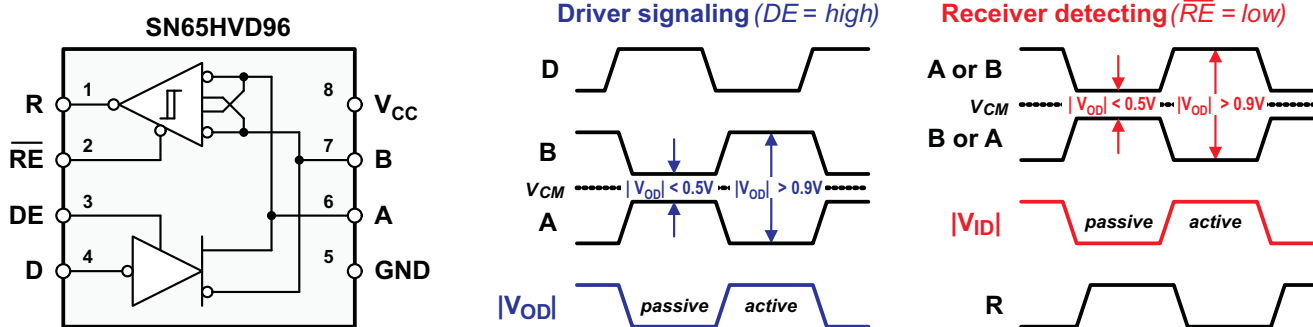

Figure 1. Block Diagram and Sympol™ Signal States

Figure 1 shows that Sympol™ signaling is similar but not identical to CAN-bus signaling. Sympol™ transceivers only look at the magnitude of the differential bus voltage, $|V_A - V_B|$, not its actual polarity. At a driver output, this voltage is called $|V_{OD}|$, at a remote receiver input, it becomes $|V_{ID}|$.

A Sympol™ bus state is known as passive when $|V_A - V_B| < 0.5V$, and it is active when $|V_A - V_B| > 0.9V$.

Similar to RS-485, Sympol™ transceivers can be used for point-to-point, multi-drop, or multi-point networks. Current-limited differential outputs protect in case of driver contention on a "party-line" bus. High receiver input impedance allows the connection of at least 32 nodes. The pin-out is identical to the industry-standard SN75176 transceiver, thus allowing for a direct upgrade from RS-485 to Sympol™.

Note that Sympol™ signaling does not support the operation of Sympol™ transceivers together with RS-485 or CAN transceivers in a mixed-transceiver type of network. Only Sympol™ transceivers are able to communicate between another. However, it is possible to replace an entire RS-485 transceiver network with Sympol™ transceivers while maintaining the same high-level network protocol without the need for software changes.

2 EVM Set-up and Precautions

Figure 2 shows the schematic of the SNHVD96 EVM. The board mounts 13 BergStik headers from JMP1 to JMP14 (JMP5 is omitted) and two 3-pin terminal blocks, TB1 and TB2, supporting the device evaluation for a wide range of system configurations.

- Pin 1 (EARTH) is a second ground pin that allows applying an external voltage between GND and EARTH to simulate common-mode voltage conditions.
- Pin 2 (GND) shall be connected to the negative output or ground terminal of the PSU. This pin represents the ground potential of the device-under-test and the entire EVM. It also connects to various jumpers on the board.
- Pin 3 (VCC) shall be connected to the positive output of a regulated 5V power supply unit (PSU) as it represents the positive supply voltage of the device-under-test and also connects to various jumpers on the board.
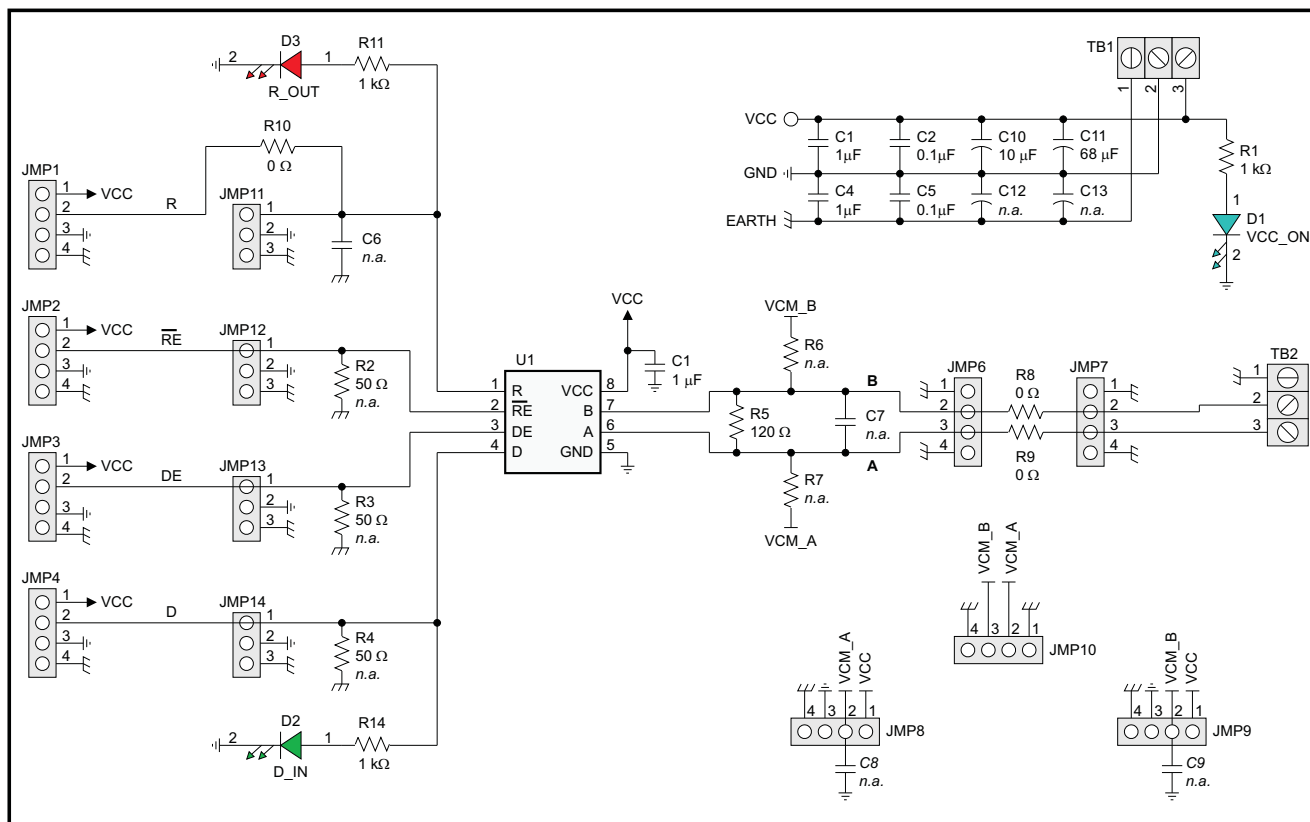
Figure 2. EVM Schematic

For the first measurements, ignore the common-mode simulation and connect EARTH to GND through a wire-bridge between pin 1 and pin 2 of TB1.
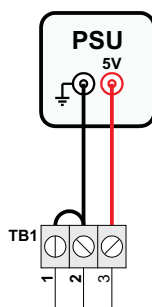

Figure 3. Bridging DUT_GND with EART_GND

While JMP2 to JMP4 are stimulation points, or headers through which the control and data signals for the SN65HVD96 are applied, JMP1, and JMP11 to JMP14 are probe points, or headers at which these signal can be measured.

Note that the 50 Ω resistors, R2, R3, and R4, have the index *n.a.*, indicating that these components are *not assembled*. Because signal generators have a typical source impedance of 50 Ω, their output is twice the required signal voltage, assuming that the on-board 50 Ω resistors divide this voltage down to the correct signal level.

Without these resistors; however, this voltage divider action is not given, and the generator output voltage must be reduced to 5 V to avoid damaging the transceiver inputs.
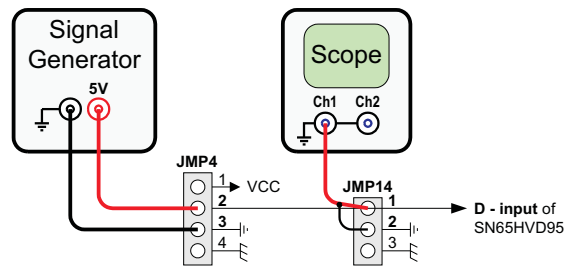
Figure 4. Example for Stimulus and Probe Points with JMP4 and JMP14

Figure 4 gives an example for entering a data signal into the driver section of the Sympol™ transceiver. The signal output of the generator is adjusted to 5V. The generator's ground terminal is connected with pin 3, and the signal output terminal with pin 2 of JMP4. The data signal is measured via an oscilloscope with its signal input connected to pin 1 and its ground wire connected to pin 2 and of JMP14.

The same set-up applies to the DE and $\overline{RE}$ inputs via their corresponding headers JMP2 and 12 and JMP3 and 13. JMP1 however, must not receive a signal stimulus. Like JMP11, it represents the receiver output, R, of the SN65HVD96.

Instead of using signal generators, the EVM can directly interface to micro controller I/O. Then the non-assembled 50 Ω resistors are of no concern. However, for proper operation, it must be assured that the high-level input voltage $V_{IH} \geq 2$ V and the low-level input voltage $V_{IL} \leq 0.8$ V.

3   Powering up the EVM and Taking Measurements

The generally recommended procedure for taking measurements is listed:

1. Install the ground connections required.
2. Connect the oscilloscope with the respective probe points you want to measure.
3. Adjust the power-supply to 5 V.
4. Adjust the generator outputs for a 5 V maximum output signal level, or check the logic switching levels of the controller I/O.
5. Connect the power supply conductor with pin 3 of TB1 and observe the blue LED (D1) turning on.
6. Connect signal conductors from the controller or the generator with their corresponding EVM inputs at JMP2 to JMP4.
7. Logic high at the receiver output, R, will turn on the red LED (D3), and logic high at the driver input, D, turns on the green LED (D2). If D is left open, an internal 100 kΩ pull-up resistor provides logic high instead. However, due to the small input current, D2 will remain off.

3.1   Measurement Examples

Each of the following measurement examples shows the equivalent circuit diagram and the corresponding EVM set-up. Only the measurement relevant headers and terminal blocks are shown, and not necessarily at their exact location on the EVM.

1. Standard Transceiver Configuration

    Normal transceiver operation requires both, the driver and the receiver sections being active. Therefore, the receiver enable pin ($\overline{RE}$) must be at logic low potential and the driver enable pin (DE) at logic high.

    Transmit data entering at the D-input terminal appear as the differential output voltage ($V_{OD} = V_A - V_B$) on the bus wires, A and B. Via the active receiver, it is possible to sense the data traffic in transmit direction.
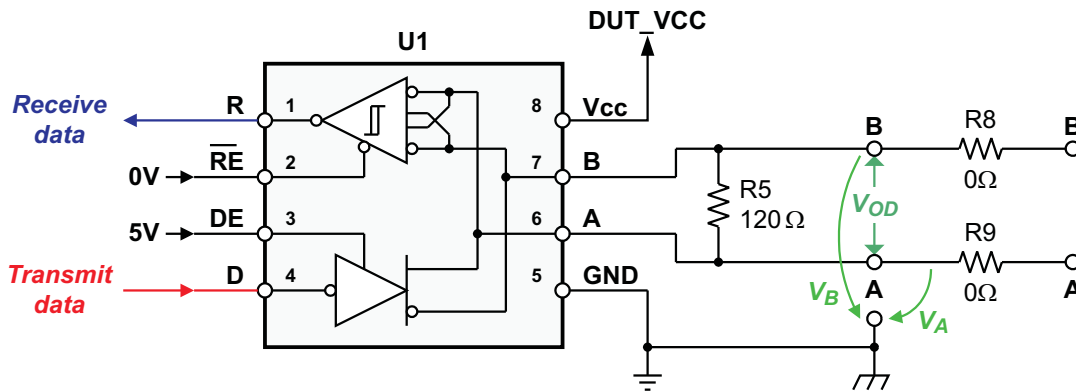
Figure 5. Transceiver Configuration for Normal Operation

Figure 6 shows the corresponding EVM set-up. Earth and ground receive the same reference potential, PSU-ground, through the wire-bridge from pin 1 to pin 2 at the terminal block, TB1, while pin 3 (VCC) is connected to the 5 V output of a power-supply unit (PSU).
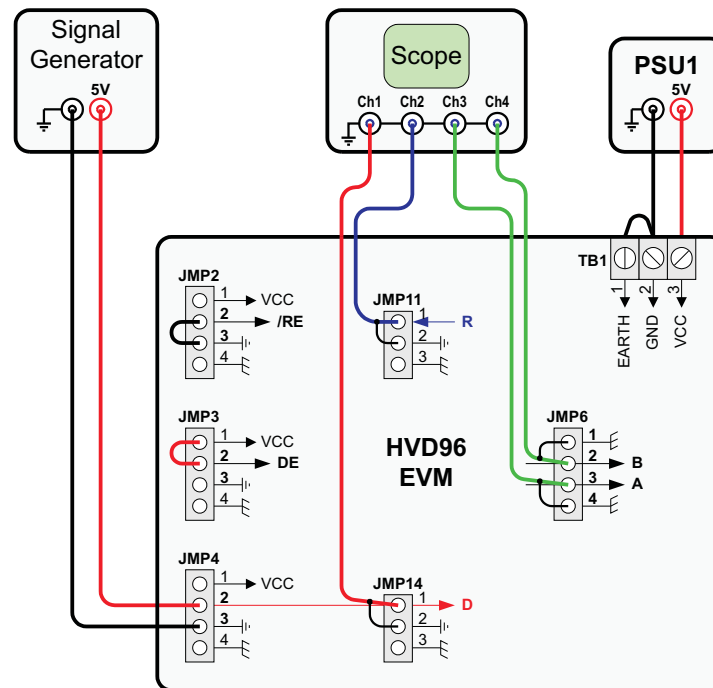

Figure 6. EVM Set-up for Normal Transceiver Operation

The low potential for $\overline{RE}$ is provided by the wire-bridge from pin 2 to pin 3 at JMP2, and the high potential for DE through a wire-bridge from pin 2 to pin 1 at JMP3. Data from the signal generator enter the board at pin 2 and pin 3 of JMP4. This data is measured via channel 1, which is connected to pin 1 and pin 2 of JMP14. Channel 2 measures the receive data at JMP11, and channels 3 and 4 the bus voltages, V_A and V_B, at JMP6.

2. Operation Under Maximum Load

EIA-485 (RS-485) specifies three maximum load parameters: a maximum differential load of 60 Ω, a maximum common-mode load of 375 Ω for each bus wire, and a receiver common-mode voltage range from –7 V to +12 V. Figure 7 reflects these requirements through R5, R8, R9, and V_{CM}. Note that under maximum load conditions the transceiver must be capable of sourcing and sinking bus currents of up to 55 mA. The purpose of this test is to show the robustness of V_{OD} over the entire common-mode voltage range at maximum load.
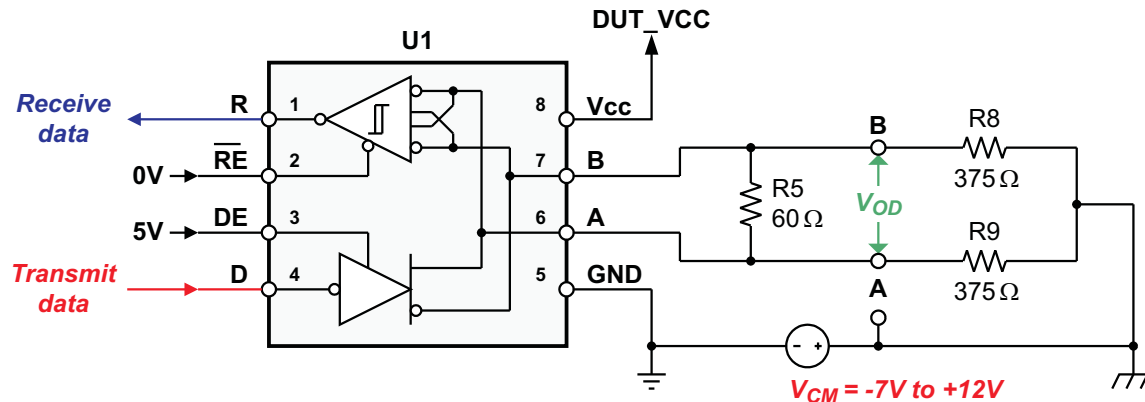
Figure 7. Configuration for Maximum Loading

While the cable connections of the signal generator and the oscilloscope remain the same as in the previous example, the following board changes need to be implemented to reflect maximum load conditions:

- replace R5 (120 Ω default) with 60 Ω
- replace R8 and R9 (0 Ω default) with 375 Ω
- connect pin 2 of JMP7 with pin 1 and pin 3 with pin 4
- replace the previous wire-bridge at TB1 with a second power supply unit (PSU2) and connect the ground terminals of both, PSU1 and PSU2 with a wire-bridge, as shown in Figure 8.
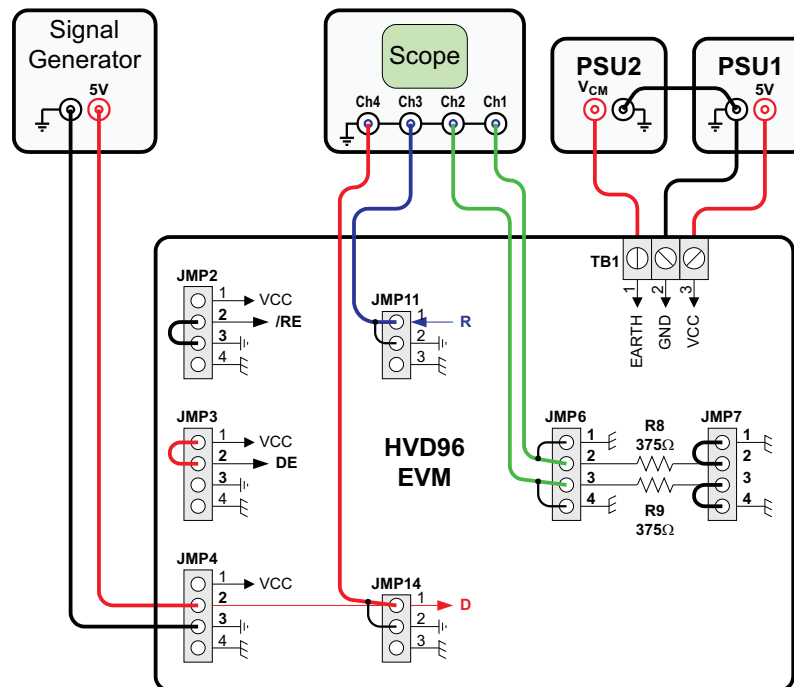

Figure 8. EVM Set-up for Maximum Loading

Note that Figure 8 only shows the wiring of PSU2 for positive common-mode voltages. For negative V_{CM}, connect the ground terminal of PSU2 with pin 1 of TB1 (Earth), and the V_{CM}-output of PSU2 with the ground terminal of PSU1.

3. Wire-fault Condition

   Simulating a wire-fault condition is easily accomplished by using two evaluation modules, one configured as the driving, the other one as the receiving EVM. Figure 9 shows the equivalent circuit using two EVMs with default component values.
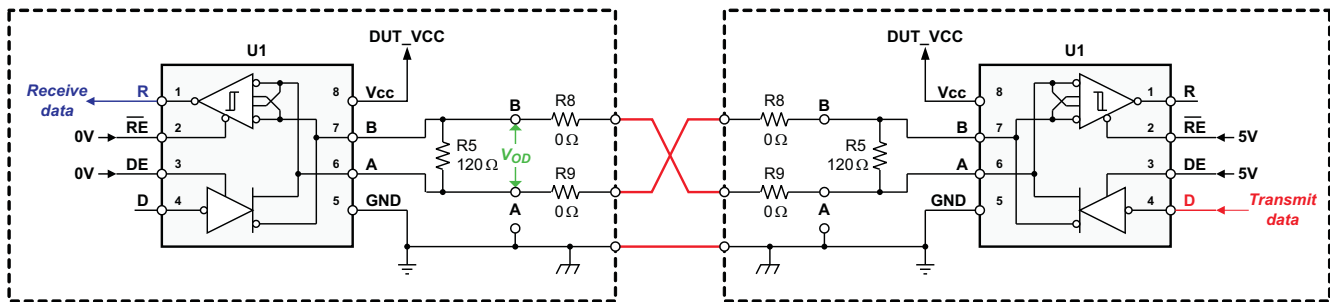
Figure 9. Wire-fault Simulation Using two EVMs

Figure 10 illustrates the EVM configurations and the measurement set-up. The right evaluation module (EVM2) is configured as the driver. Both, driver and receiver enable inputs, DE and $\overline{RE}$, receive high potential through the wire-bridges to VCC at JMP3 and JMP2. *Note that EVM2 is turned by 180°.* EVM1 on the left is configured as the receiver. Here, the driver and receiver enable inputs receive low potential through the wire-bridges to GND at JMP3 and JMP2.
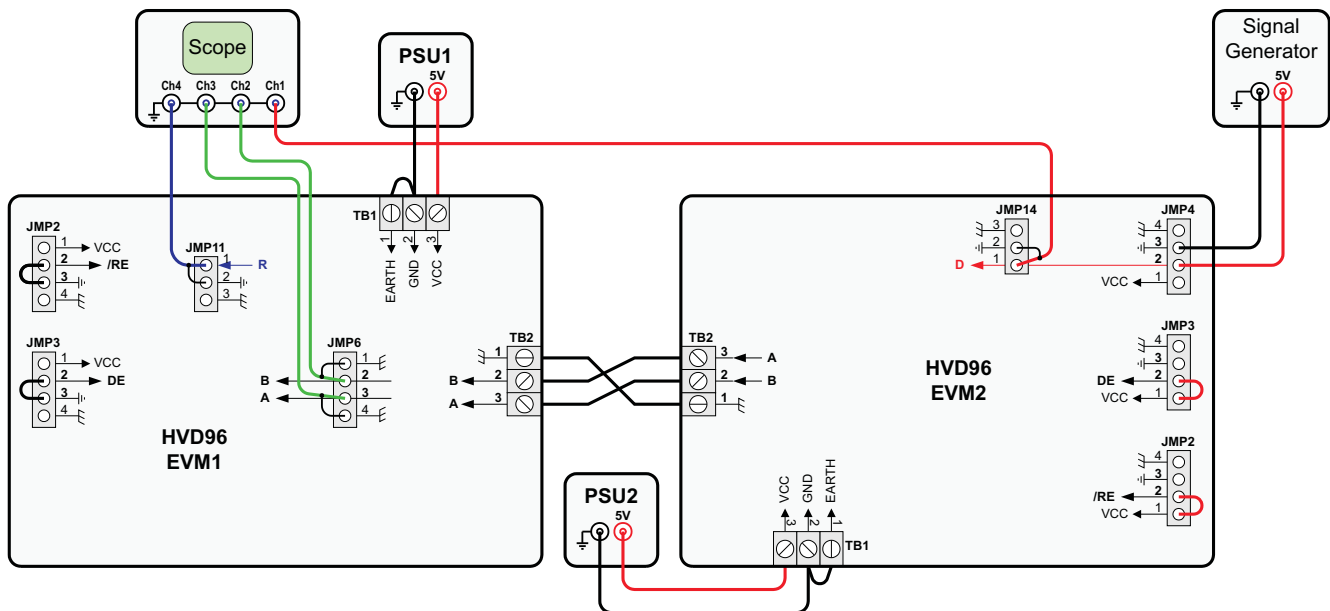

Figure 10. EVM Configurations: Left as Receiver EVM, Right as Transmitter EVM

The input data signal entering EVM2 at JMP4 is measured on scope channel 1, probing the signal at the D-input pin of JMP14. The cross-wiring of the bus wires occurs at the EVM interlink, between the two TB2 terminal blocks. To proof wire-fault robustness, the differential receiver input and the single-ended receiver output signals are measured after the cross-wiring. Channels 2 and 3 measure the bus voltages, V_A and V_B, at pin 2 and pin 3 of JMP6, while the receiver output is taken from pin 1 at JMP11. Note that both 5 V power supplies, PSU1 and PSU2 have their ground terminals connected to the ground and Earth terminals of their respective EVMs.

The scope pictures for the individual examples are shown in Figure 11, Figure 12, and Figure 13. Figure 14 and Figure 15 show the top and bottom view of the SN65HVD96 EVM.
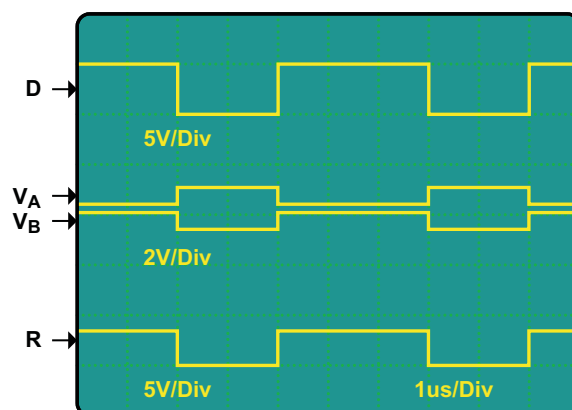
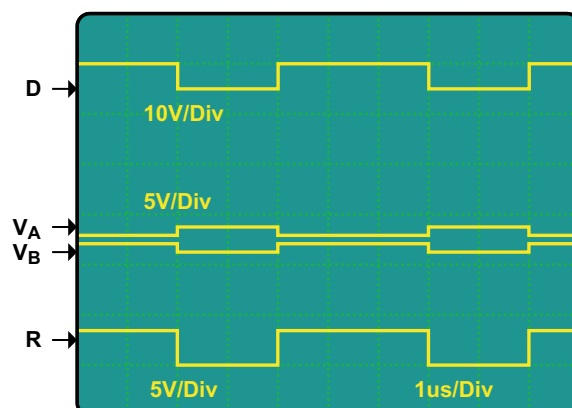**Figure 11. Sympol™ Signaling at 500 kbps Over 1 Meter Cable**

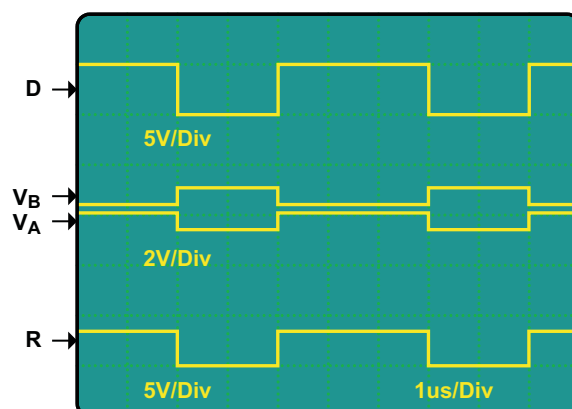**Figure 12. Sympol™ Signaling is Unaffected by Common-Mode Voltage**

Figure 13. Sympol™ Signaling is Unaffected by Cross-wire Fault
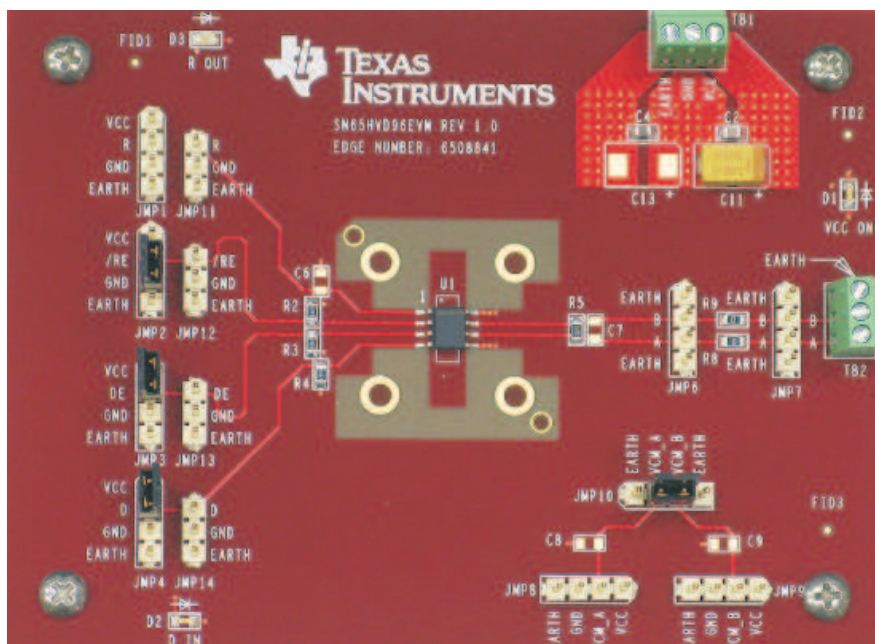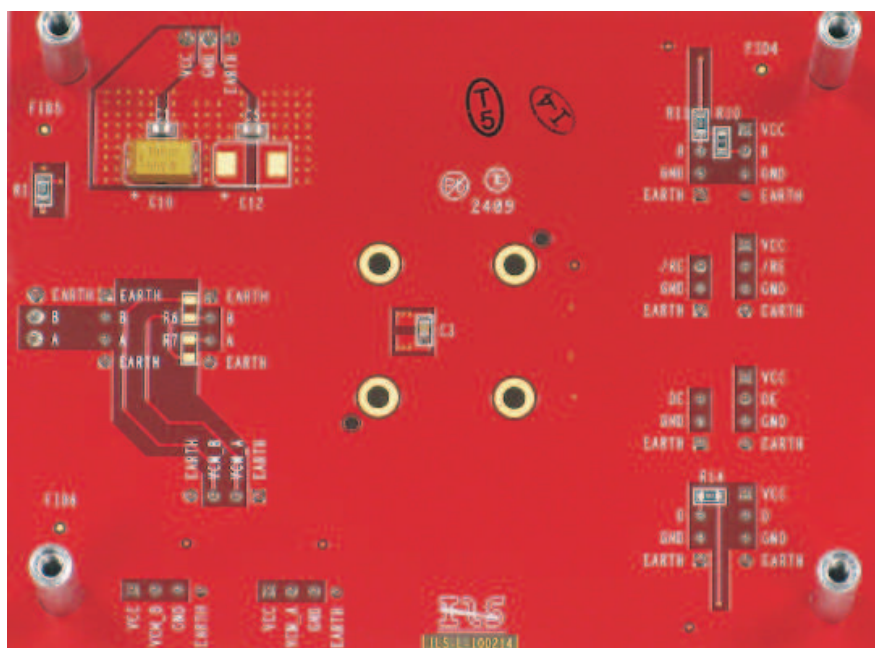
Figure 14. Top View of SN65 HVD96 EVM

Figure 15. Bottom View of SN65 HVD96 EVM

For detailed information on the device parameters see the SN65HVD96 data sheet (Lit.# SLLSE35).

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to 5.25V and the output voltage range of 0V to 5.25V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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