INTERSIL

# IH6216
# 8-Channel Differential CMOS Analog Multiplexer

## FEATURES

- **Pin compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **$r_{DS(on)}$ < 700 ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (3 strobe inputs controls 2 out of 16 channels).**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latch up**
- **Very low leakage $I_{D(off)} \leq$ 100pA**

## GENERAL DESCRIPTION

The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the enable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V) all channels are off. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the enable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

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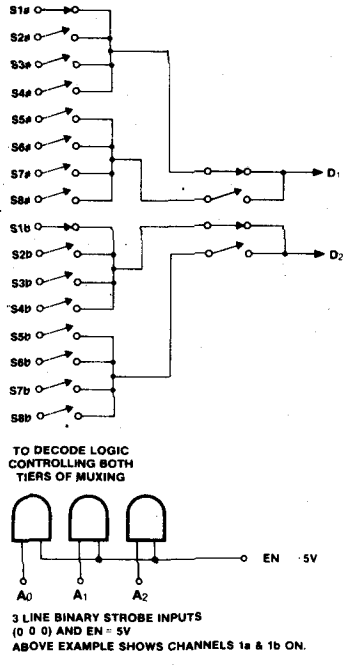
## FUNCTIONAL DIAGRAM

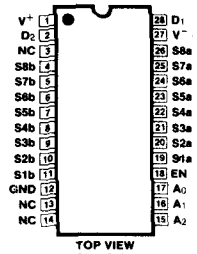



## DECODE TRUTH TABLE

| $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH PAIR |
|---|---|---|---|---|
| X | X | X | 0 | NONE |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

LOGIC "1" = $V_{AH}$ > 3V $V_{ENH}$ > 4.5V
LOGIC "0" = $V_{AL}$ < 0.8V

## PIN CONFIGURATION (Outline drawings DI, PI)




TOP VIEW
$V_-$ COMMON TO SUBSTRATE

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| IH6216MDI | −55°C to +125°C | 28 pin Ceramic DIP |
| IH6216CDI | 0°C to 70°C | 28 pin Ceramic DIP |
| IH6216CPI | 0°C to 70°C | 28 pin Plastic DIP |

## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$ (A, EN) to Ground ..... −15V, $V_1$
$V_S$ or $V_D$ to $V^+$ ..... 0, −32V
$V_S$ or $V_D$ to $V^-$ ..... 0, 32V
$V^+$ to Ground ..... 16V
$V^-$ to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* ..... 1200mW
Lead Temperature (Soldering 10 sec) ..... 300 °C

*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C

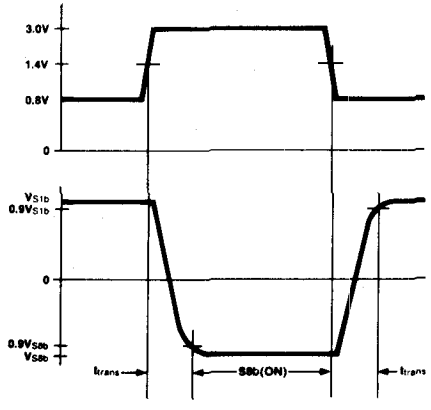
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

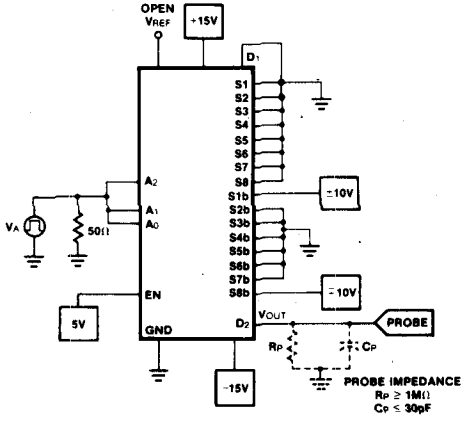
## ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$[1], Ground = 0V, unless otherwise specified.

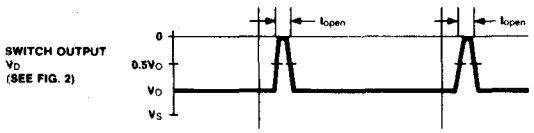
| | CHARACTERISTIC | | MEASURED TERMINAL | NO TESTS PER TEMP | TYP 25°C | MAX LIMITS M SUFFIX −55°C | M SUFFIX 25°C | M SUFFIX 125°C | C SUFFIX 0°C | C SUFFIX 25°C | C SUFFIX 70°C | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SWITCH | $r_{DS(ON)}$ | | S to D | 16 | 480 | 600 | 600 | 700 | 650 | 650 | 750 | Ω | $V_D$ = 10V, $I_S$ = −10mA | Sequence each switch on |
| | | | | 16 | 300 | 600 | 600 | 700 | 650 | 650 | 750 | | $V_D$ = −10V, $I_S$ = 10mA | $V_{AL}$ =0.8V, $V_{AH}$ =3V |
| | $\Delta r_{DS(ON)}$ | | | | 20 | | | | | | | % | $\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg}}$ $V_S$ = ±10V | |
| | $I_{S(OFF)}$ | | S | 16 | 0.01 | | 0.1 | 50 | | 0.2 | 50 | nA | $V_S$ = 10V, $V_D$ = −10V | $V_{EN}$ = 0 |
| | | | | 16 | 0.01 | | 0.1 | 50 | | 0.2 | 50 | | $V_S$ = −10V, $V_D$ = 10V | |
| | $I_{D(OFF)}$ | | D | 2 | 0.1 | | 0.2 | 100 | | 0.4 | 100 | | $V_D$ = 10V, $V_S$ = −10V | |
| | | | | 2 | 0.1 | | 0.2 | 100 | | 0.4 | 100 | | $V_D$ = −10V, $V_S$ = 10V | |
| | $I_{D(ON)}$ | | D | 16 | 0.1 | | 0.2 | 100 | | 0.4 | 100 | | $V_{S(All)}$ = $V_D$ = 10V | Sequence each switch on |
| | | | | 16 | 0.1 | | 0.2 | 100 | | 0.4 | 100 | | $V_{S(All)}$ = $V_D$ = −10V | $V_{AL}$ =0.8V, $V_{AH}$ =3V |
| INPUT | $I_{A(on)}$ or $I_{A(off)}$ | | | 3 | .01 | | −10 | −30 | | −10 | −30 | μA | $V_A$ = 3.0V | |
| | | | | 3 | .01 | | 10 | 30 | | 10 | 30 | | $V_A$ = 15V | |
| | $I_A$ | | $A_0$ $A_1$ $A_2$ $A_3$ | 3 | | | −10 | −30 | | −10 | −30 | | $V_{EN}$ = 5V | All $V_A$ = 0 |
| | | | EN | 1 | | | −10 | −30 | | −10 | −30 | | $V_{EN}$ = 0 | |
| DYNAMIC | $t_{trans}$ | | D | | 0.6 | | 1 | | | | | μs | See Fig. 1 | |
| | $t_{open}$ | | D | | 0.2 | | | | | | | | See Fig. 2 | |
| | $t_{on(En)}$ | | D | | 0.8 | | 1.5 | | | | | | See Fig. 3 | |
| | $t_{off(En)}$ | | D | | 0.3 | | 1 | | | | | | | |
| | "OFF" Isolation | | D | | 60 | | | | | | | dB | $V_{EN}$ = 0, $R_L$ = 200Ω, $C_L$ = 3 pF, $V_S$ = 3 VRMS, f = 500 kHz | |
| | $C_s$ | | S | | 5 | | | | | | | pF | $V_S$ = 0 | |
| | $C_{d(off)}$ | | D | | 20 | | | | | | | | $V_D$ = 0 | $V_{EN}$ = 0, f = 140 kHz to 1 MHz |
| | $C_{ds}$ | | D to S | | 1 | | | | | | | | $V_S$ = 0, $V_D$ = 0 | |
| SUPPLY | Supply Current | + | $I^+$ | 1 | 55 | | 200 | | | 1000 | | μA | $V_{EN}$ = 5V | All $V_A$ = 0 OR 3V |
| | | − | $I^-$ | 1 | 2 | | 100 | | | 1000 | | | | |
| | Standby Current | + | $I^+_{SB}$ | 1 | 1 | | 100 | | | 1000 | | | $V_{EN}$ = 0 | |
| | | − | $I^-_{SB}$ | 1 | 1 | | 100 | | | 1000 | | | | |

**NOTE 1:** See Section V. Enable Input Strobing Levels.

## SWITCHING INFORMATION





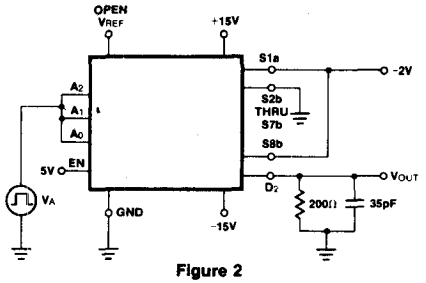
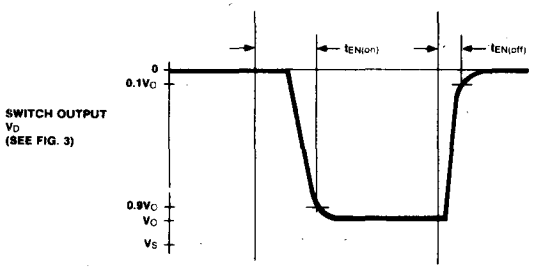




Figure 2



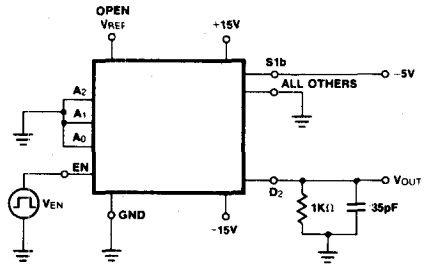




Figure 3

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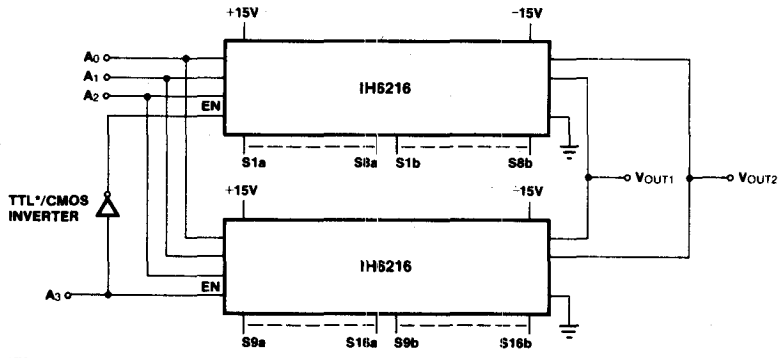
## IH6216 APPLICATIONS

I. 2 out of 32 channel multiplexer using 2 IH6216s.




*TTL gate must have pullup to drive EN

Figure 4

**DECODE TRUTH TABLE**

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | ON SWITCH | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | S1a | |
| 0 | 0 | 0 | 1 | S2a | |
| 0 | 0 | 1 | 0 | S3a | |
| 0 | 0 | 1 | 1 | S4a | |
| 0 | 1 | 0 | 0 | S5a | |
| 0 | 1 | 0 | 1 | S6a | |
| 0 | 1 | 1 | 0 | S7a | |
| 0 | 1 | 1 | 1 | S8a | $V_{OUT1}$ |
| 1 | 0 | 0 | 0 | S9a | |
| 1 | 0 | 0 | 1 | S10a | |
| 1 | 0 | 1 | 0 | S11a | |
| 1 | 0 | 1 | 1 | S12a | |
| 1 | 1 | 0 | 0 | S13a | |
| 1 | 1 | 0 | 1 | S14a | |
| 1 | 1 | 1 | 0 | S15a | |
| 1 | 1 | 1 | 1 | S16a | |

**DECODE TRUTH TABLE**

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | ON SWITCH | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | S1b | |
| 0 | 0 | 0 | 1 | S2b | |
| 0 | 0 | 1 | 0 | S3b | |
| 0 | 0 | 1 | 1 | S4b | |
| 0 | 1 | 0 | 0 | S5b | |
| 0 | 1 | 0 | 1 | S6b | |
| 0 | 1 | 1 | 0 | S7b | |
| 0 | 1 | 1 | 1 | S8b | $V_{OUT2}$ |
| 1 | 0 | 0 | 0 | S9b | |
| 1 | 0 | 0 | 1 | S10b | |
| 1 | 0 | 1 | 0 | S11b | |
| 1 | 0 | 1 | 1 | S12b | |
| 1 | 1 | 0 | 0 | S13b | |
| 1 | 1 | 0 | 1 | S14b | |
| 1 | 1 | 1 | 0 | S15b | |
| 1 | 1 | 1 | 1 | S16b | |

## IH6216 APPLICATIONS

II. 2 out of 32 channel multiplexer using 2 IH6216s; with an IH5043 for submultiplexing.



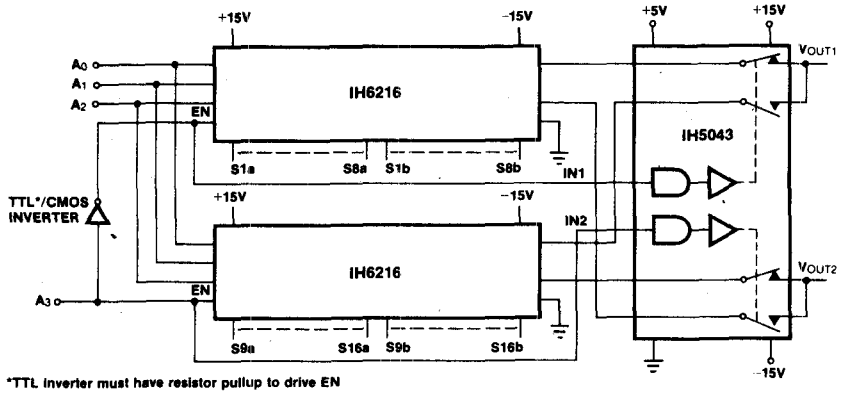



Figure 5

**DECODE TRUTH TABLE**

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | ON SWITCH | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | S1a | |
| 0 | 0 | 0 | 1 | S2a | |
| 0 | 0 | 1 | 0 | S3a | |
| 0 | 0 | 1 | 1 | S4a | |
| 0 | 1 | 0 | 0 | S5a | |
| 0 | 1 | 0 | 1 | S6a | |
| 0 | 1 | 1 | 0 | S7a | |
| 0 | 1 | 1 | 1 | S8a | $V_{OUT1}$ |
| 1 | 0 | 0 | 0 | S9a | |
| 1 | 0 | 0 | 1 | S10a | |
| 1 | 0 | 1 | 0 | S11a | |
| 1 | 0 | 1 | 1 | S12a | |
| 1 | 1 | 0 | 0 | S13a | |
| 1 | 1 | 0 | 1 | S14a | |
| 1 | 1 | 1 | 0 | S15a | |
| 1 | 1 | 1 | 1 | S16a | |

**DECODE TRUTH TABLE**

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | ON SWITCH | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | S1b | |
| 0 | 0 | 0 | 1 | S2b | |
| 0 | 0 | 1 | 0 | S3b | |
| 0 | 0 | 1 | 1 | S4b | |
| 0 | 1 | 0 | 0 | S5b | |
| 0 | 1 | 0 | 1 | S6b | |
| 0 | 1 | 1 | 0 | S7b | |
| 0 | 1 | 1 | 1 | S8b | $V_{OUT2}$ |
| 1 | 0 | 0 | 0 | S9b | |
| 1 | 0 | 0 | 1 | S10b | |
| 1 | 0 | 1 | 0 | S11b | |
| 1 | 0 | 1 | 1 | S12b | |
| 1 | 1 | 0 | 0 | S13b | |
| 1 | 1 | 0 | 1 | S14b | |
| 1 | 1 | 1 | 0 | S15b | |
| 1 | 1 | 1 | 1 | S16b | |

## IH6216 APPLICATIONS

III. 2 out of 64, using 4 IH6216s and 2 IH5043s as submultiplexers.

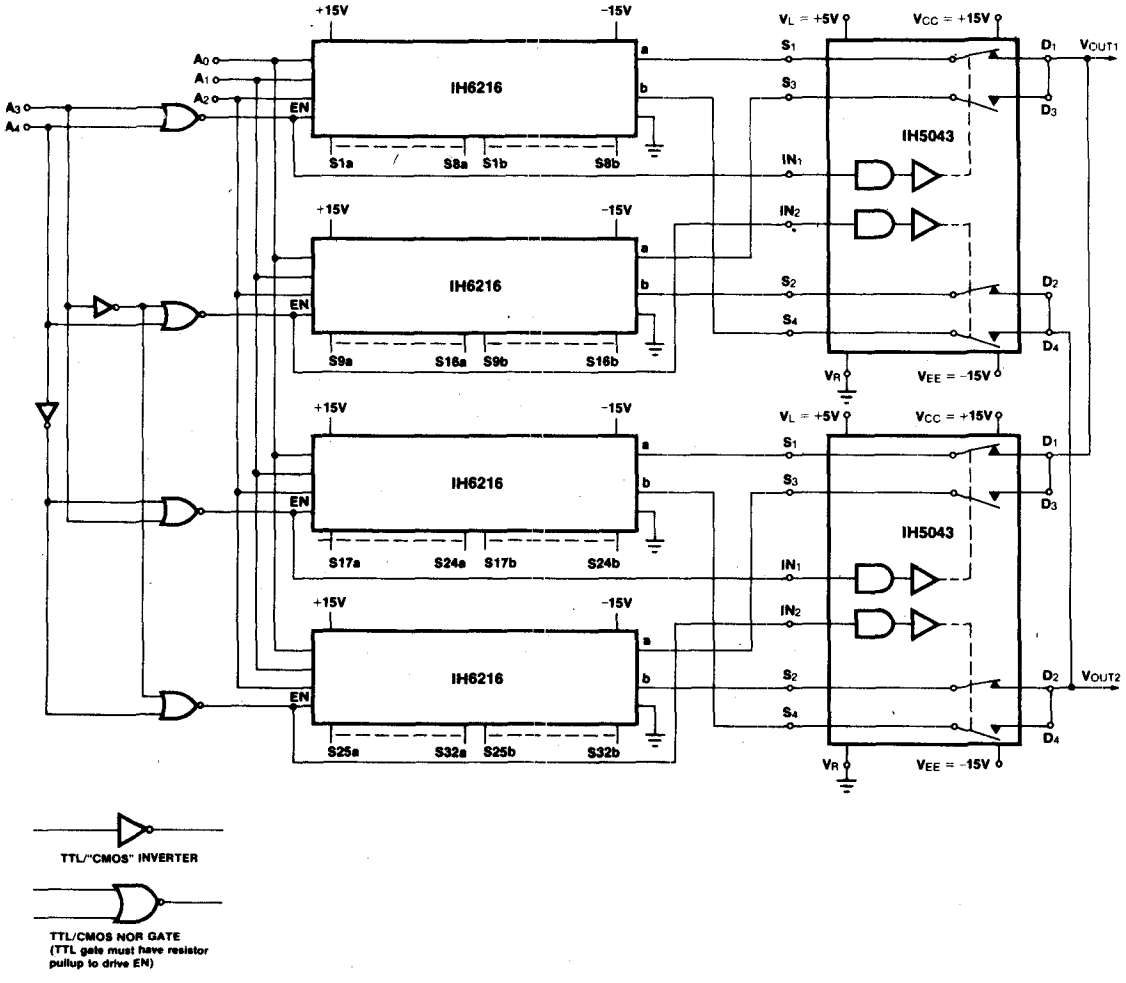



Figure 6

## IV. GENERAL NOTE ON EXPANDABILITY OF IH6216

The IH6216 is a two tier multiplexer where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6216 is expanded.

Figure 4 shows a 2 of 32 multiplexer using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the enable input strobe is used as the $A_3$ input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the $V_{out1}$ and $V_{out2}$ outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA at room temperature. Thruput speed will be typically 0.8$\mu$s for $t_{on}$ and 0.3$\mu$s for $t_{off}$, with thruput channel resistance in the 500$\Omega$ area.

Figure 5 shows the 2 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of 50$\Omega$ (max. is 75$\Omega$) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5$\mu$s for both ON and OFF time, and output leakage is about 0.2 nA.

Figure 6 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5043 is used for the third tier of MUXing. Each $V_{out}$ point will see 3 OFF channels and 1 ON channel at any time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550$\Omega$ area and thruput switching speeds will be about 1.3$\mu$s for ON time and 0.8$\mu$s for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2$\mu$A so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

## V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the $A_3$ input.

For the system to function properly the EN input (pin 18) must go to 5V $\pm$5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1k$\Omega$ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

**NOTE:** This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.