

CMOS 4-Bit Full Adder

With Parallel Carry Out

The RCA-CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A₁ to A₄ and B₁ to B₄, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S₁ and S₄, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units	
				D, F, K, H Packages				E Package					
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25 Typ. Limit		+125	-40	+25 Typ. Limit		+85		
Quiescent Device Current, I _L Max.	—	—	5	5	0.3	5	300	50	0.5	50	700	μA	
	—	—	10	10	0.5	10	600	500	1	100	1400		
	—	—	15	50	1	50	2000	500	5	500	5000		
Output Voltage: Low-Level, V _{OL}	—	0,5	5	0 Typ., 0.05 Max.									V
	—	0,10	10	0 Typ., 0.05 Max.									
	—	0,5	5	4.95 Min.; 5 Typ.									
	—	0,10	10	9.95 Min.; 10 Typ.									
Noise Immunity: Inputs Low, V _{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.									V
	9	—	10	3 Min.; 4.5 Typ.									
	0.8	—	5	1.5 Min.; 2.25 Typ.									
	1	—	10	3 Min.; 4.5 Typ.									
Noise Margin: Inputs Low, V _{NML}	4.5	—	5	1 Min.									V
	9	—	10	1 Min.									
	0.5	—	5	1 Min.									
	1	—	10	1 Min.									
Output Drive Current: n-Channel (Sink), I _{DN} Min.	*	0.5	—	5	0.31	0.5	0.25	0.175	0.155	0.5	0.13	0.105	mA
	*	0.5	—	10	0.93	1.5	0.75	0.53	0.6	1.5	0.5	0.4	
	▲	3	—	5	0.012	0.2	0.01	0.007	0.009	0.2	0.007	0.005	
	▲	3	—	10	0.31	0.5	0.25	0.175	0.24	0.5	0.2	0.16	
	*	4.5	—	5	-0.31	-0.5	-0.25	-0.175	-0.155	-0.5	-0.13	-0.105	
	*	9.5	—	10	-0.93	-1.5	-0.75	-0.53	-0.6	-1.5	-0.5	-0.4	
	▲	2	—	5	-0.012	-0.2	-0.01	-0.007	-0.008	-0.2	-0.007	-0.005	
	▲	7	—	10	-0.185	-0.3	-0.15	-0.105	-0.12	-0.3	-0.1	-0.08	
p-Channel (Source), I _{DP} Min.													
Input Leakage Current, I _{IL} , I _{IH} Max.													
Any Input													
15													
±10 ⁻⁵ Typ.; ±1 Max.													
μA													

* Carry Output

▲ Sum Output

Applications

- Binary addition/arithmetic units

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T _{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
(Voltages referenced to V _{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P _D):	
FOR T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T _A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} + 0.5 V
LEAD TEMPERATURE (DURING SOLDERING)	+265°C
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	

Features:

- 4 sum outputs plus parallel look-ahead carry-output
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T _A = Full Package-Temp. Range)	3	12	V

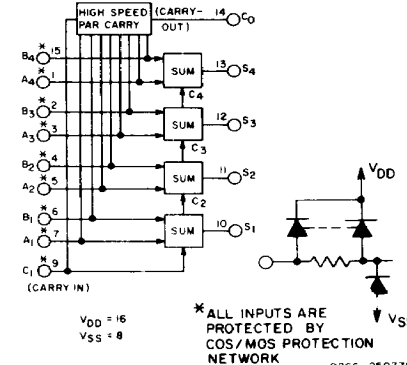


Fig. 1 - CD4008A logic diagram.

TRUTH TABLE

A ₁	B ₁	C ₁	C ₀	SUM
0	0	0	0	0
0	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t _{PHL} , t _{PLH} Sum In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Carry In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Sum In to Carry Out	5	320	600	320	800	ns
	10	120	200	120	240	
Carry In to Carry Out	5	100	175	100	200	ns
	10	45	75	45	90	
Transition Time: t _{THL} , t _{TLH} At Sum Outputs	5	1250	2200	1250	2900	ns
	10	550	900	550	1100	
At Carry Output	5	125	225	125	290	ns
	10	45	75	45	90	
Input Capacitance, C _I (Any Input)	—	10	—	10	—	pF

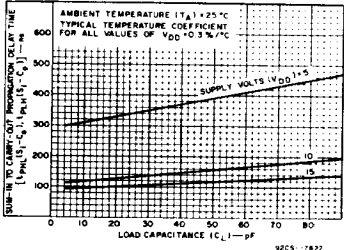


Fig. 2 — Typical sum-in to carry out propagation delay time vs. C_L .

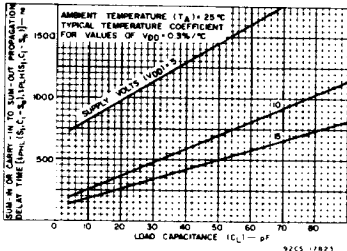


Fig. 3 — Typical sum-in or carry-in to sum-out propagation delay time vs. C_L .

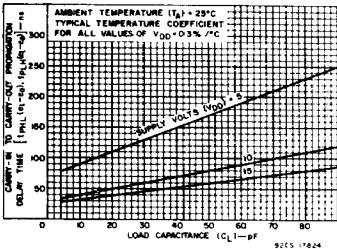


Fig. 4 — Typical carry-in to carry-out propagation delay time vs. C_L .

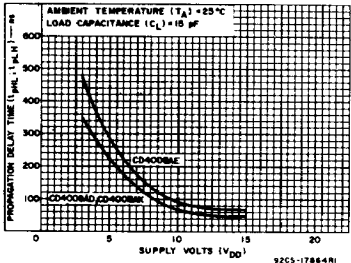


Fig. 5 — Typical maximum propagation delay time vs. V_{DD} for carry-in to carry-out.

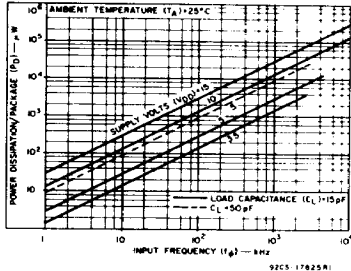


Fig. 6 — Typical dissipation characteristics.

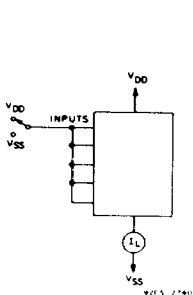


Fig. 7 — Quiescent device current test circuit.

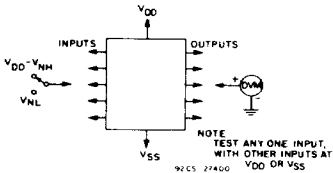


Fig. 8 — Noise immunity test circuit.

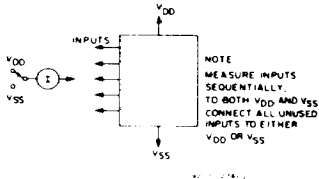


Fig. 9 — Input leakage current test circuit.

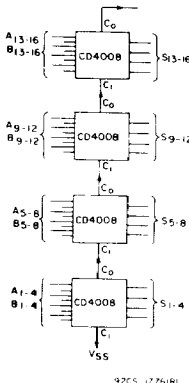


Fig. 10 — Typical connection for a 16-bit adder.