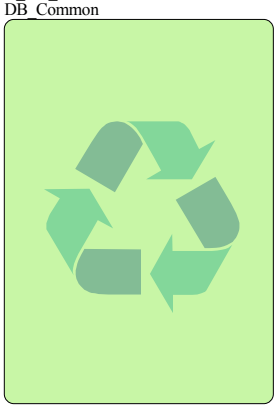
U_DB_Common
DB_Common



U_PSU
PSU.SCHDOC

U_Bypass_Board
DB_Bypass

U_DB41_Hardware_Kit
DB41_Hardware_Kit.SchDoc

Sheet Title	***DB41 Top Level***	
Project Title	***DB41 - Spartan3A/3AN***	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:43 PM	Sheet 1 of 22
File: DB41_Top.SchDoc		

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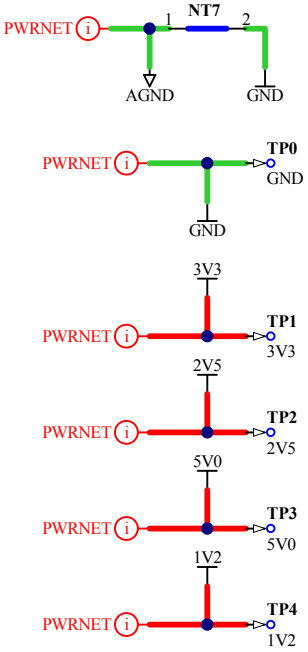

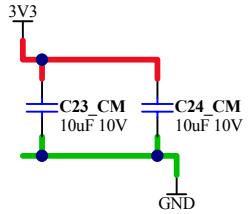

Shared Bypass Caps

U_PSU_MAX1831_1V2_ALT
PSU_MAX1831_1V2_ALT

1V2

Sheet Title	***Power Supply Top Level***		
Project Title	***DB41 - Spartan3A/3AN***		
Size: A4	Assy: D-820-0024	Revision: 01	
Date: 2/12/2008	Time: 1:41:43 PM	Sheet 2 of 22	
File: PSU.SCHDOC			

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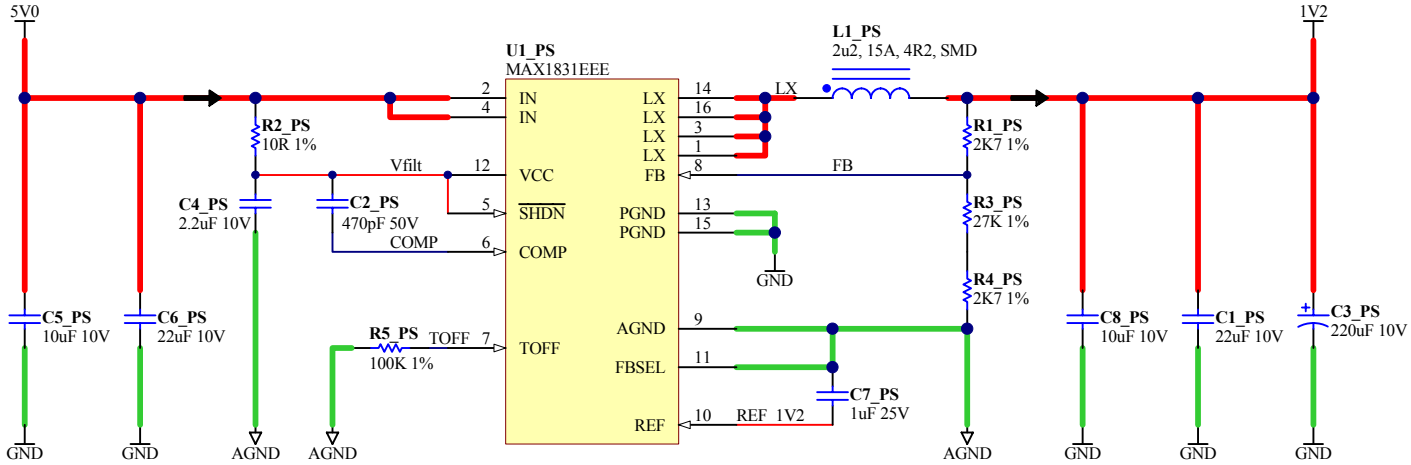

Sheet Title	***Power Supply MAX1831 (1V2)***	
Project Title	***DB41 - Spartan3A/3AN***	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:43 PM	Sheet 3 of 22
File: PSU_MAX1831_1V2_ALT.SchDoc		

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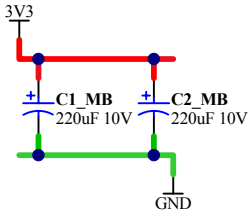

These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title	*Board Bypass Capacitors*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008 Time: 1:41:43 PM	Sheet 4 of 22	
File: DB_Bypass.SchDoc		

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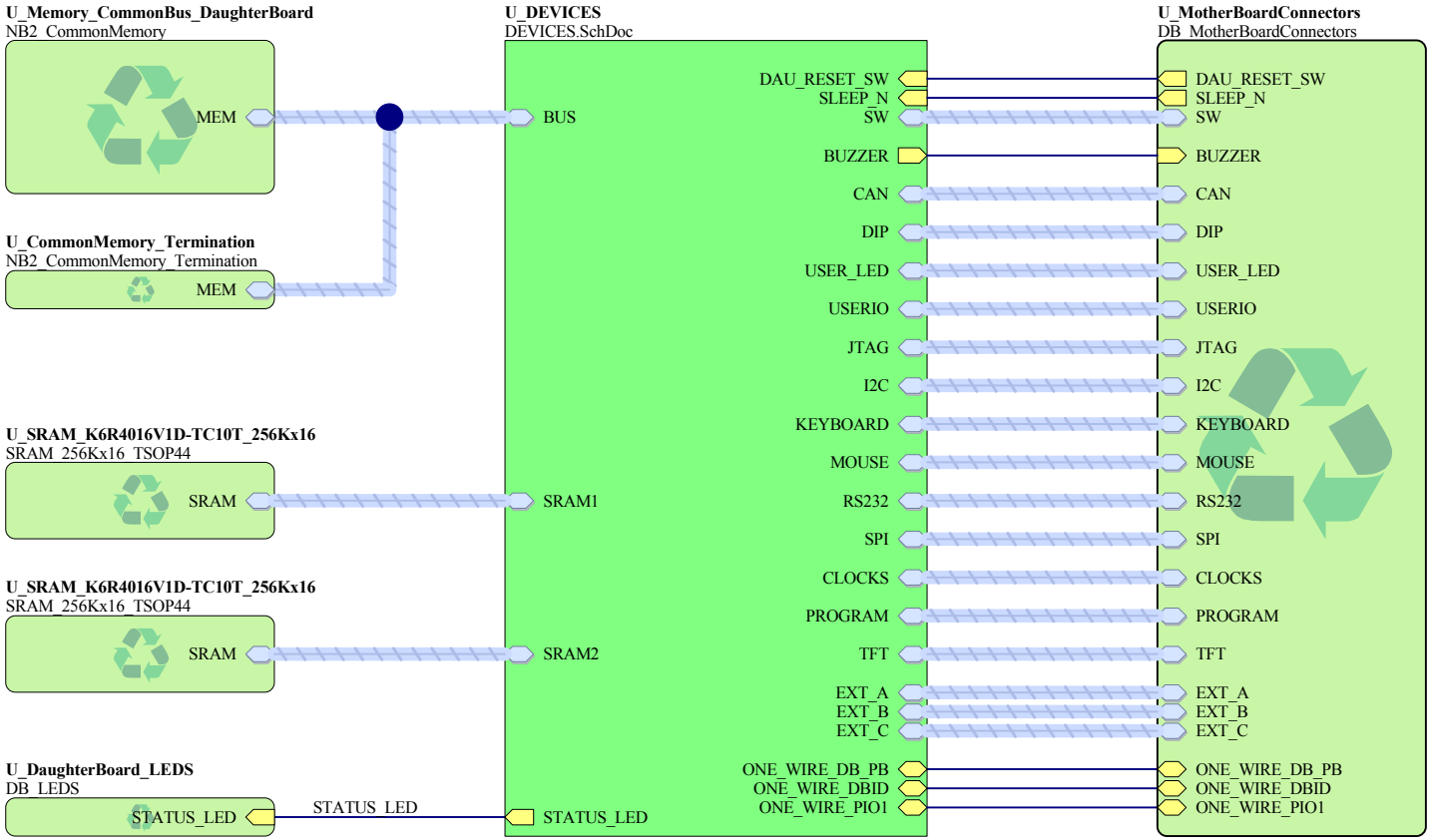
Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU

This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .



Sheet Title	*Daughter Board Top Level*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:43 PM	Sheet 5 of 22
File: DB_Common.SchDoc		

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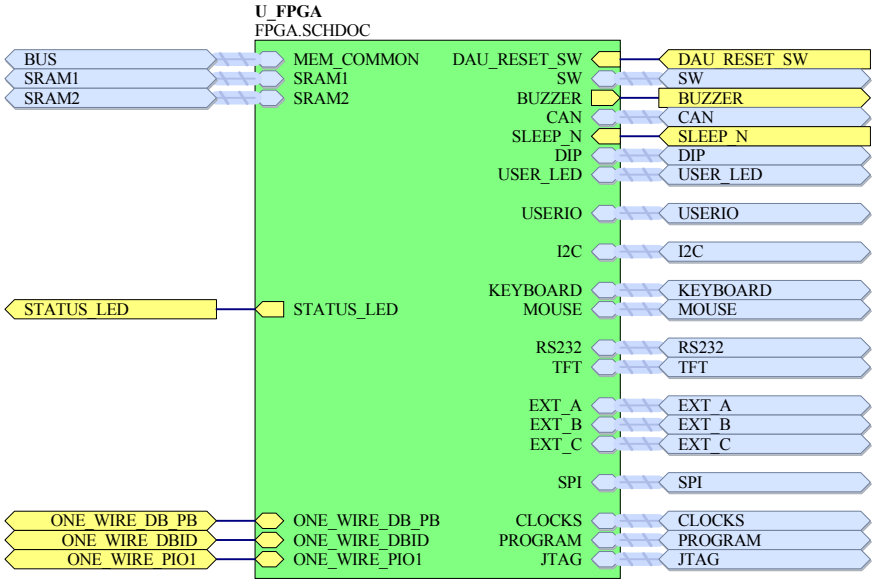

Device Specific Section of Daughter Board Design

This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.

This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

Sheet Title	*FPGA, LEDs and SRAM Memory*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:43 PM	Sheet 6 of 22
File: DEVICES.SchDoc		

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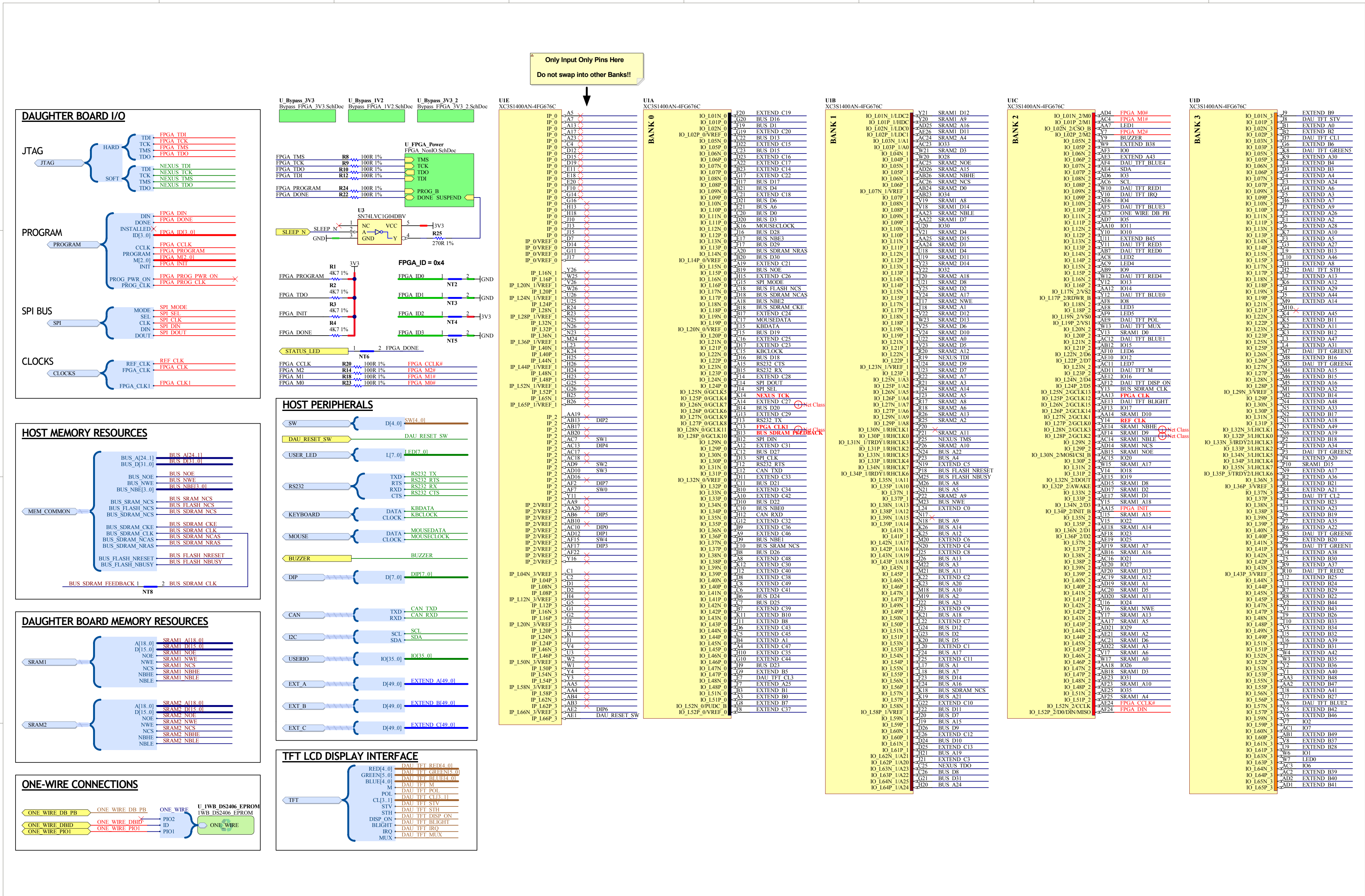

Sheet Title: FPGA Connections

Project Title: DB41 - Spartan3A/3AN

Size: A2 | Assy: D-820-0024 | Revision: 01

Date: 2/12/2008 | Time: 1:41:44 PM | Sheet 7 of 22

File: FPGA.SCHDOC

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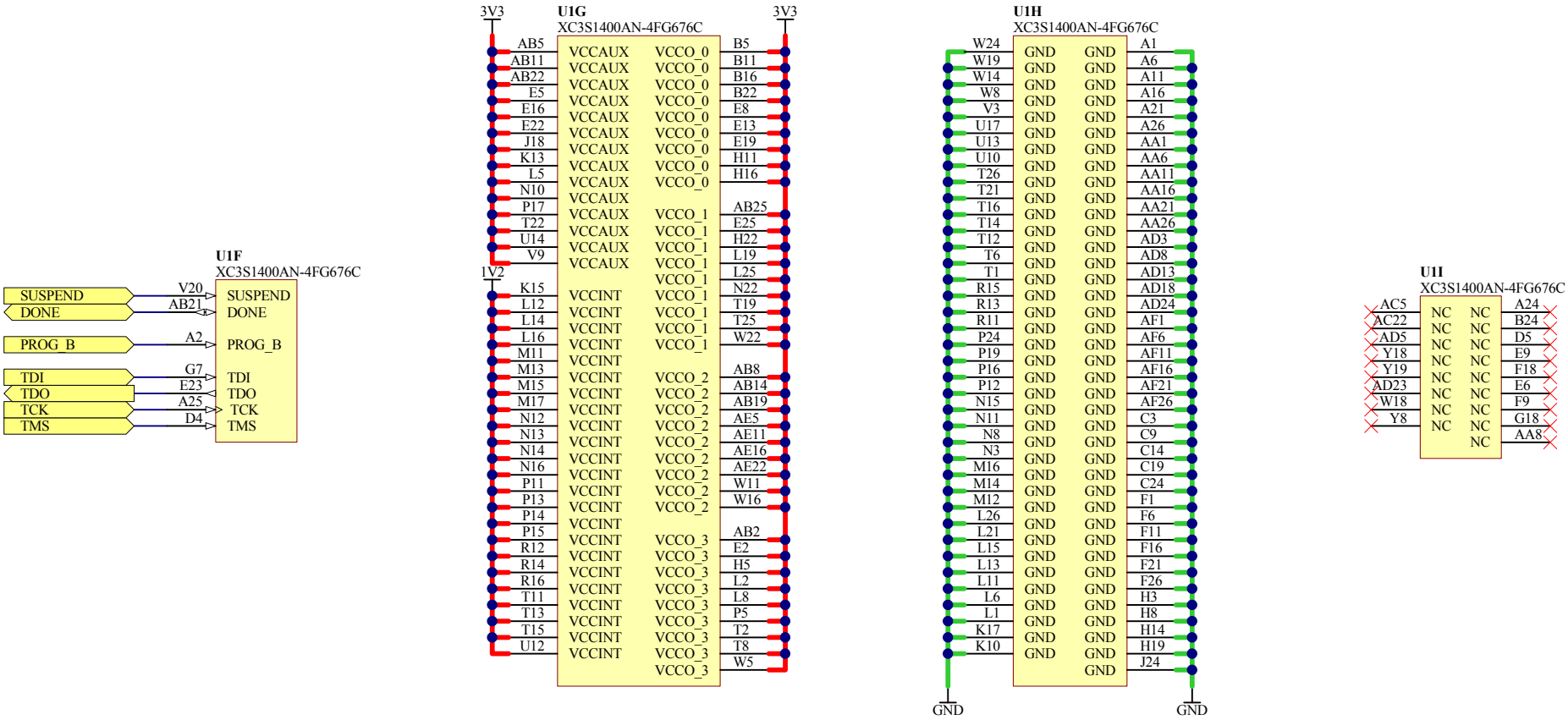

Sheet Title	*FPGA Power and Programming*		
Project Title	*DB41 - Spartan3A/3AN*		
Size: A4	Assy: D-820-0024	Revision: 01	
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 8 of 22	
File: FPGA_NonIO.SchDoc			

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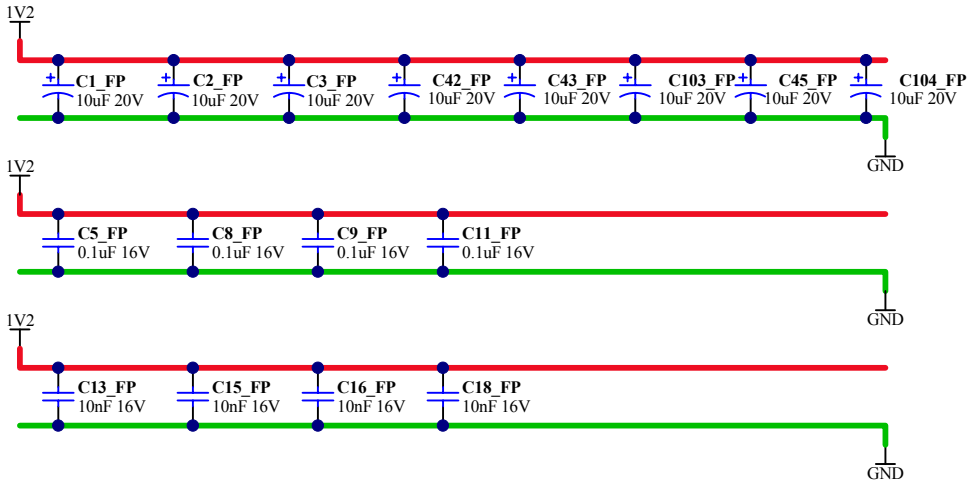

Sheet Title	*FPGA Bypass 1V2*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 9 of 22
File: Bypass_FPGA_1V2.SchDoc		

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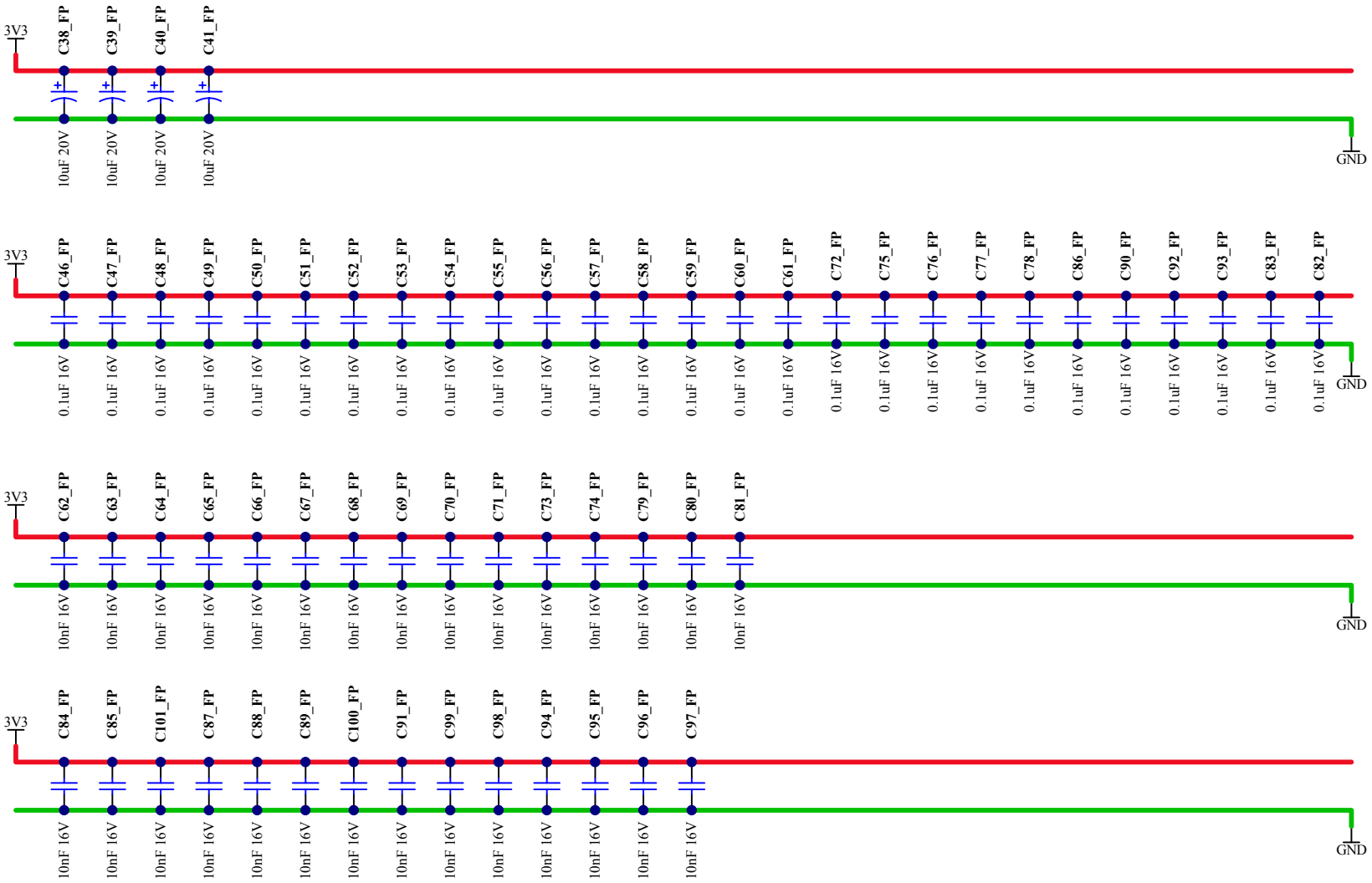

The FPGA bypass capacitors are physically grouped as 10nF and 100nF pairs on all major accessible power pins on the FPGA.

Sheet Title	*FPGA Bypass 3V3*		
Project Title	*DB41 - Spartan3A/3AN*		
Size: A4	Assy: D-820-0024	Revision: 01	
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 10 of 22	
File: Bypass_FPGA_3V3.SchDoc			

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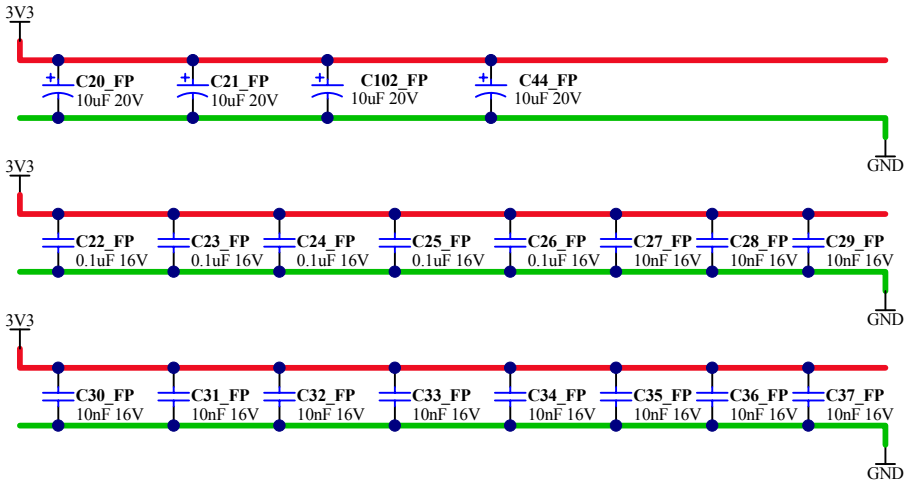

Sheet Title	*FPGA Bypass 3V3*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 11 of 22
File: Bypass_FPGA_3V3_2.SchDoc		

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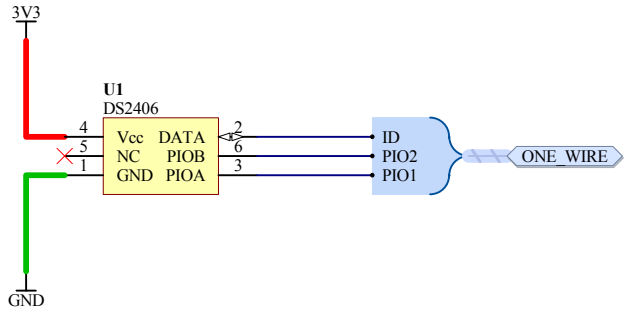

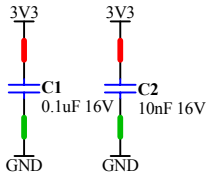

Sheet Title	*1-Wire Bus ID*		
Project Title	*DB41 - Spartan3A/3AN*		
Size: A4	Assy: D-820-0024	Revision: 01	
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 12 of 22	
File: 1WB_DS2406_EPROM.SchDoc			

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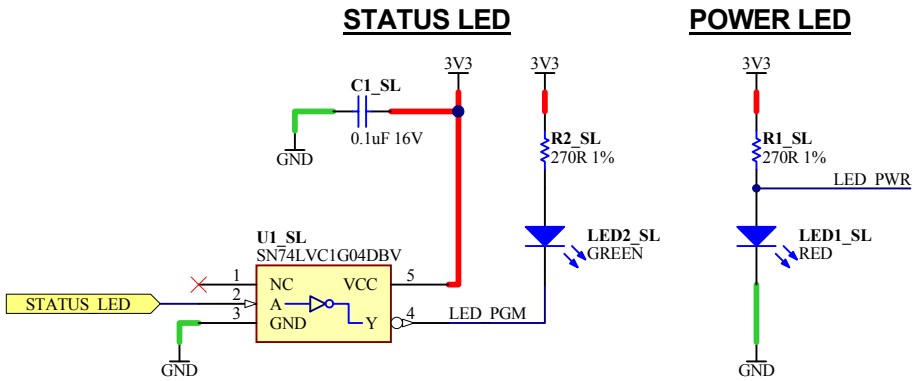

Sheet Title	*Daughter Board LEDs*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 13 of 22
File: DB_LEDS.SchDoc		

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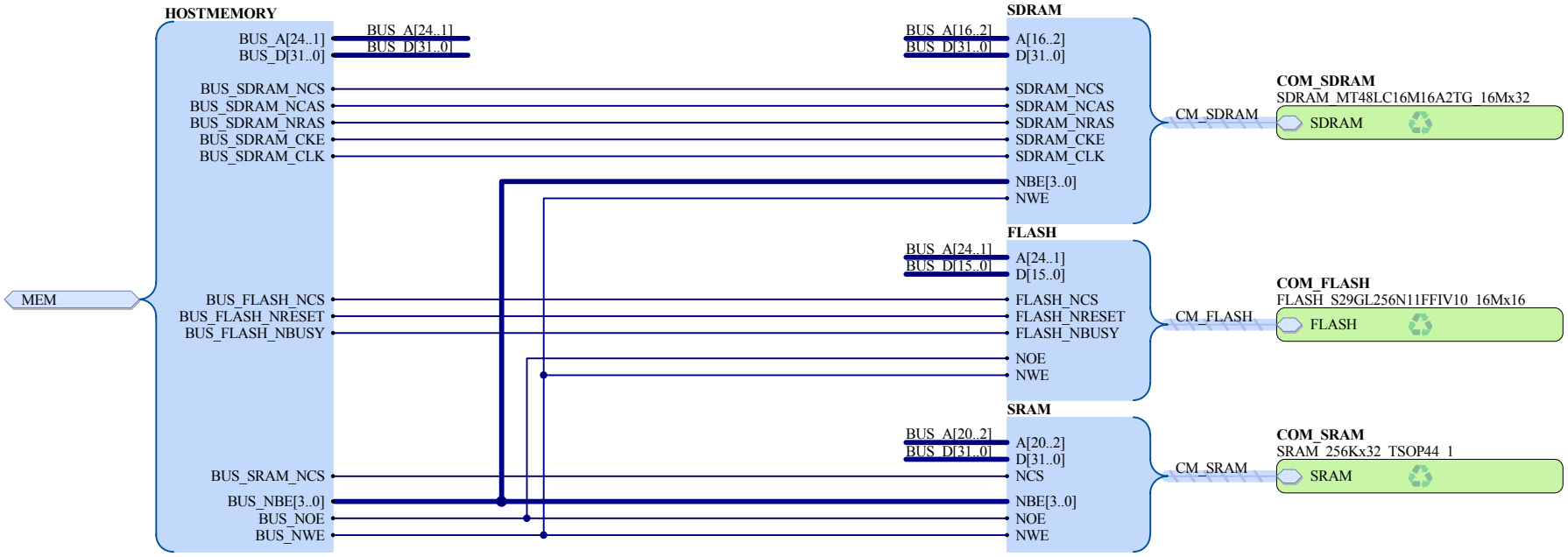

Common-Bus Memory Block

256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)

Sheet Title	*Common-Bus Memory Block*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 14 of 22
File: NB2_CommonMemory.SchDoc		

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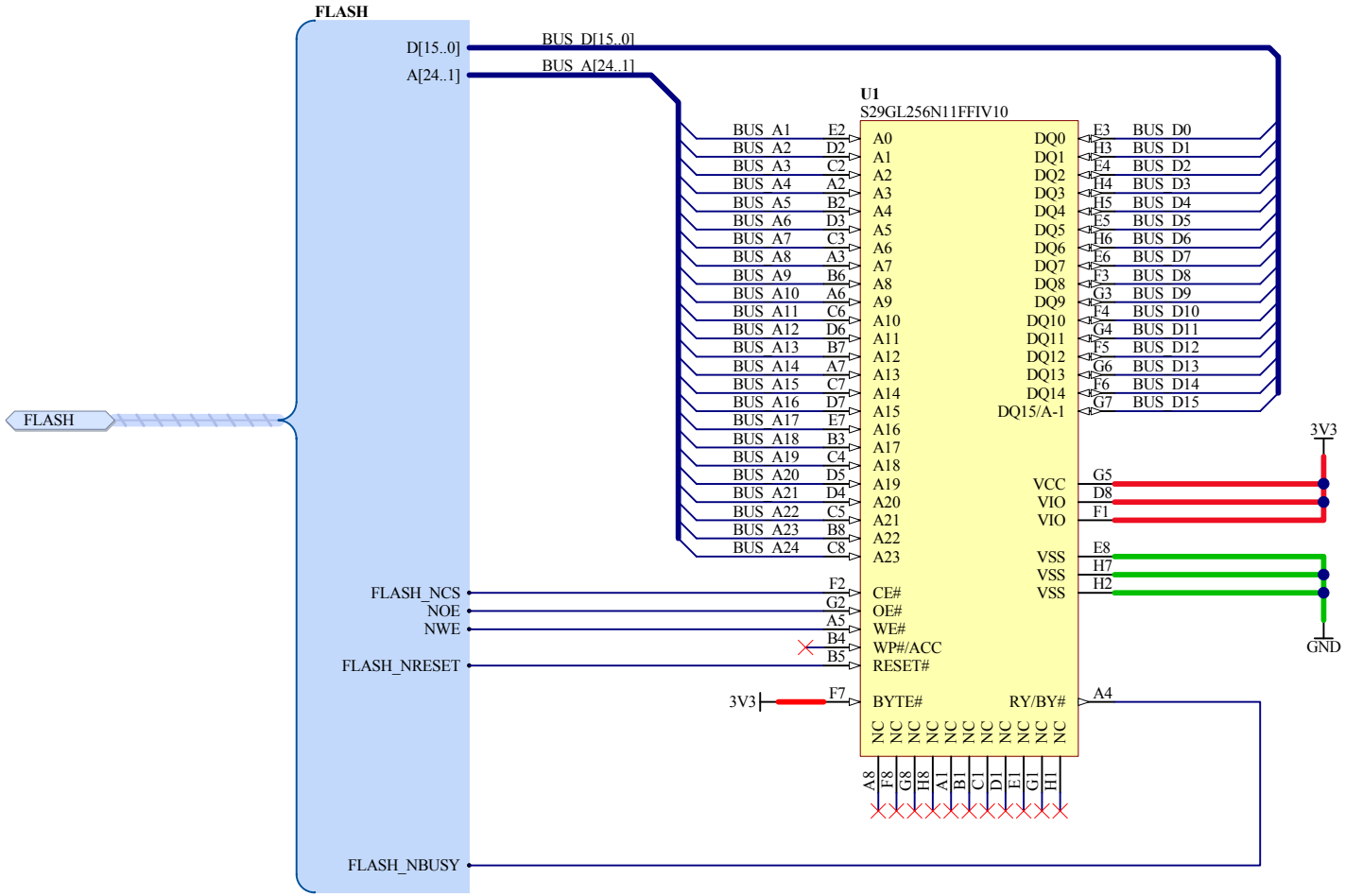

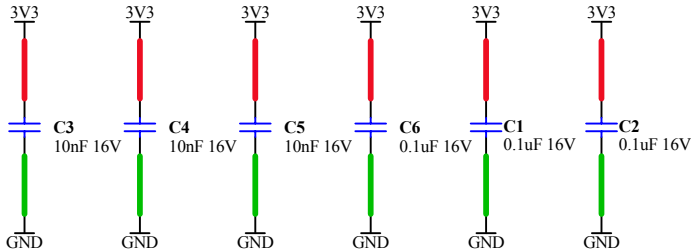

Sheet Title	*16M x 16 Flash Memory (BGA)*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 15 of 22
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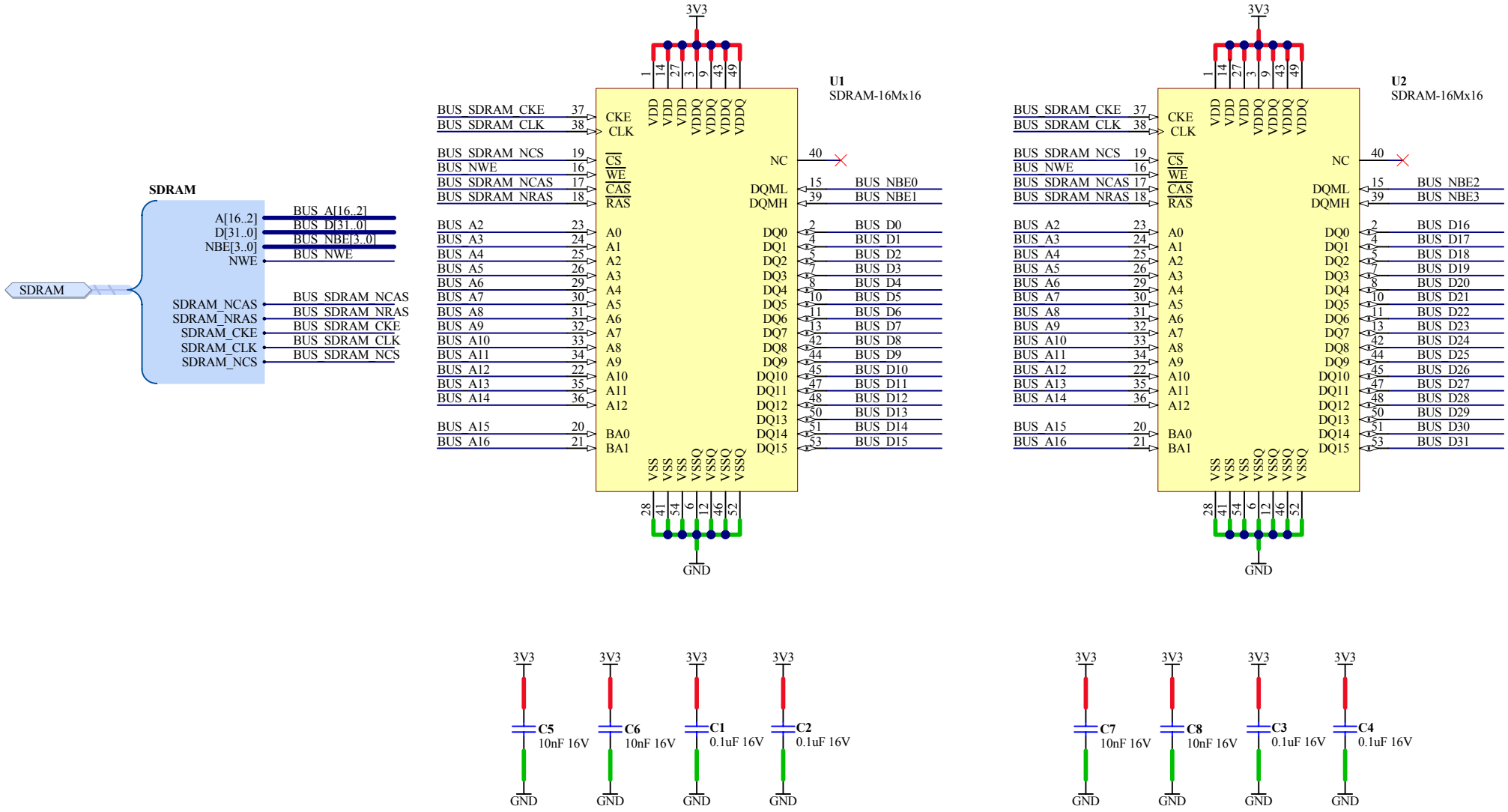

Sheet Title	*16M x 32 SDRAM TSOP54 x 2*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 16 of 22
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc		

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A18 is connected so that 512KBx16 device can be fitted

SRAM

A[20..2] SRAM_A[20..2]
D[31..0] SRAM_D[31..0]
NCS SRAM_NCS
NWE SRAM_NWE
NOE SRAM_NOE
NBE[3..0] SRAM_NBE[3..0]

U1
SRAM-256Kx16

SRAM_A2	1	A0	A17	44	SRAM_A19
SRAM_A3	2	A1	A16	43	SRAM_A18
SRAM_A4	3	A2	A15	42	SRAM_A17
SRAM_A5	4	A3	OE	41	SRAM_NOE
SRAM_A6	5	A4	BHE	40	SRAM_NBE1
SRAM_NCS	6	CS	BLE	39	SRAM_NBE0
SRAM_D0	7	D0	D15	38	SRAM_D15
SRAM_D1	8	D1	D14	37	SRAM_D14
SRAM_D2	9	D2	D13	36	SRAM_D13
SRAM_D3	10	D3	D12	35	SRAM_D12
	11	VDD	VSS	34	
	12	VSS	VDD	33	
SRAM_D4	13	D4	D11	32	SRAM_D11
SRAM_D5	14	D5	D10	31	SRAM_D10
SRAM_D6	15	D6	D9	30	SRAM_D9
SRAM_D7	16	D7	D8	29	SRAM_D8
SRAM_NWE	17	WE	NC	28	SRAM_A20
SRAM_A7	18	A5	A14	27	SRAM_A16
SRAM_A8	19	A6	A13	26	SRAM_A15
SRAM_A9	20	A7	A12	25	SRAM_A14
SRAM_A10	21	A8	A11	24	SRAM_A13
SRAM_A11	22	A9	A10	23	SRAM_A12

3V3 GND GND 3V3

U2
SRAM-256Kx16

SRAM_A2	1	A0	A17	44	SRAM_A19
SRAM_A3	2	A1	A16	43	SRAM_A18
SRAM_A4	3	A2	A15	42	SRAM_A17
SRAM_A5	4	A3	OE	41	SRAM_NOE
SRAM_A6	5	A4	BHE	40	SRAM_NBE3
SRAM_NCS	6	CS	BLE	39	SRAM_NBE2
SRAM_D16	7	D0	D15	38	SRAM_D31
SRAM_D17	8	D1	D14	37	SRAM_D30
SRAM_D18	9	D2	D13	36	SRAM_D29
SRAM_D19	10	D3	D12	35	SRAM_D28
	11	VDD	VSS	34	
	12	VSS	VDD	33	
SRAM_D20	13	D4	D11	32	SRAM_D27
SRAM_D21	14	D5	D10	31	SRAM_D26
SRAM_D22	15	D6	D9	30	SRAM_D25
SRAM_D23	16	D7	D8	29	SRAM_D24
SRAM_NWE	17	WE	NC	28	SRAM_A20
SRAM_A7	18	A5	A14	27	SRAM_A16
SRAM_A8	19	A6	A13	26	SRAM_A15
SRAM_A9	20	A7	A12	25	SRAM_A14
SRAM_A10	21	A8	A11	24	SRAM_A13
SRAM_A11	22	A9	A10	23	SRAM_A12

3V3 GND GND 3V3

3V3 C1 0.1uF 16V GND
3V3 C2 0.1uF 16V GND
3V3 C5 10nF 16V GND
3V3 C6 10nF 16V GND

3V3 C3 0.1uF 16V GND
3V3 C4 0.1uF 16V GND
3V3 C7 10nF 16V GND
3V3 C8 10nF 16V GND

Sheet Title	*256K x 32 SRAM - TSOP44 x 2*		
Project Title	*DB41 - Spartan3A/3AN*		
Size: A4	Assy: D-820-0024	Revision: 01	
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 17 of 22	
File: SRAM_256Kx32_TSOP44_1.SchDoc			

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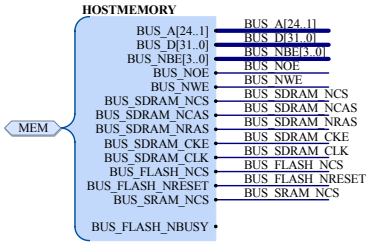
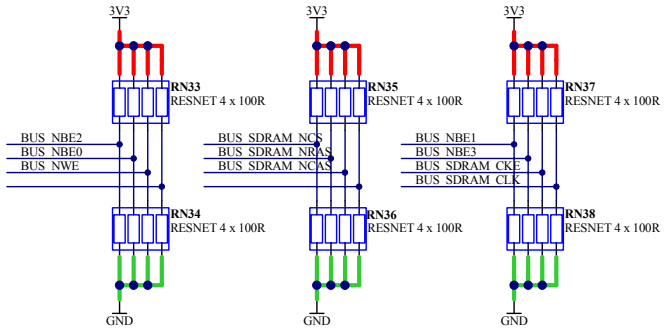


THESE SIGNALS TERMINATE AT THE SDRAM DEVICE



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).
The SRAM should be located next furthest from the source (FPGA).
The SDRAM should be located next furthest from the source (FPGA).
Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.

Sheet Title	*Memory CommonBus Terminations*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A3	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 18 of 22
File: NB2_CommonMemory_Termination.SchDoc		

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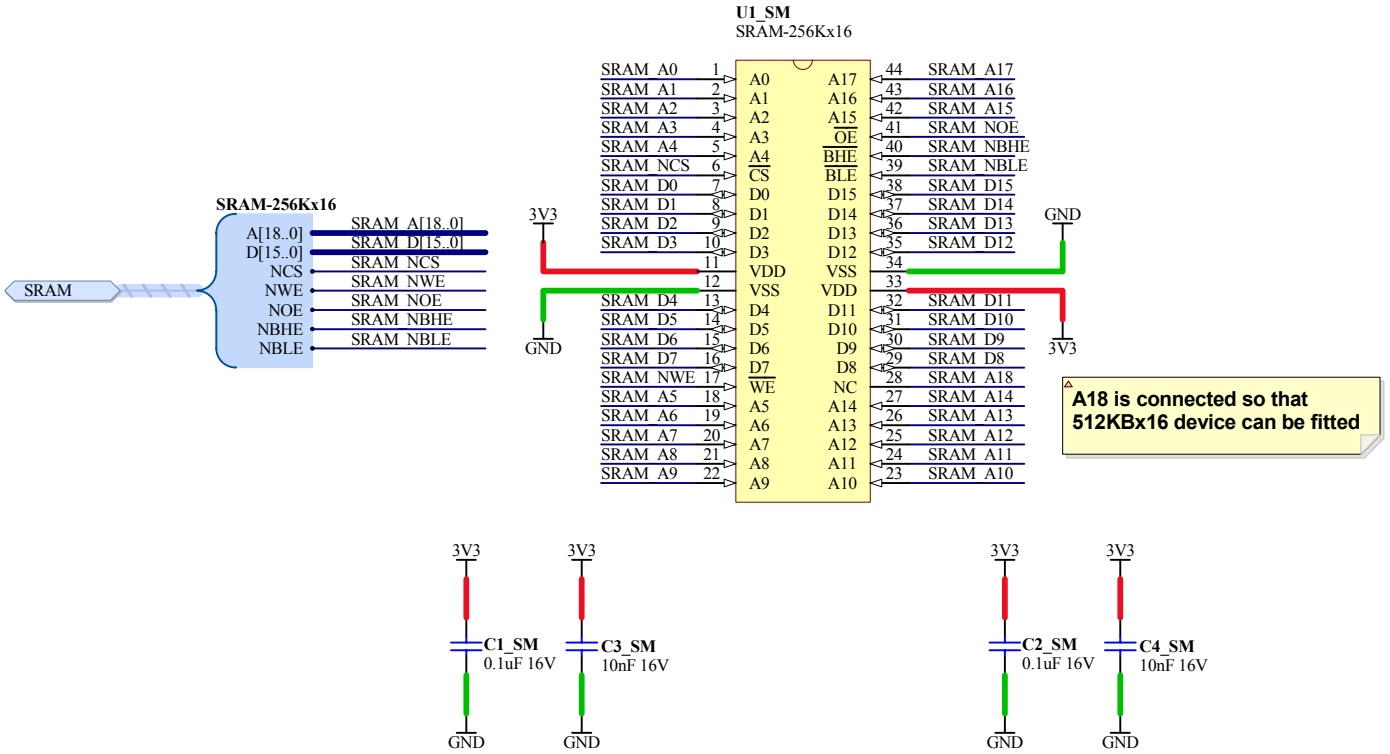

Sheet Title	*256K x 16-Bit SRAM*	
Project Title	*DB41 - Spartan3A/3AN*	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:44 PM	Sheet 19 of 22
File: SRAM_256Kx16_TSOP44.SchDoc		

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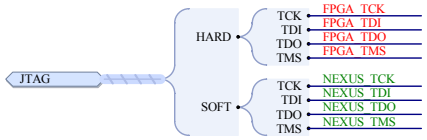
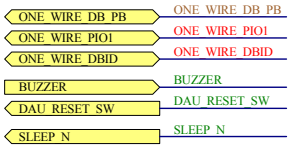
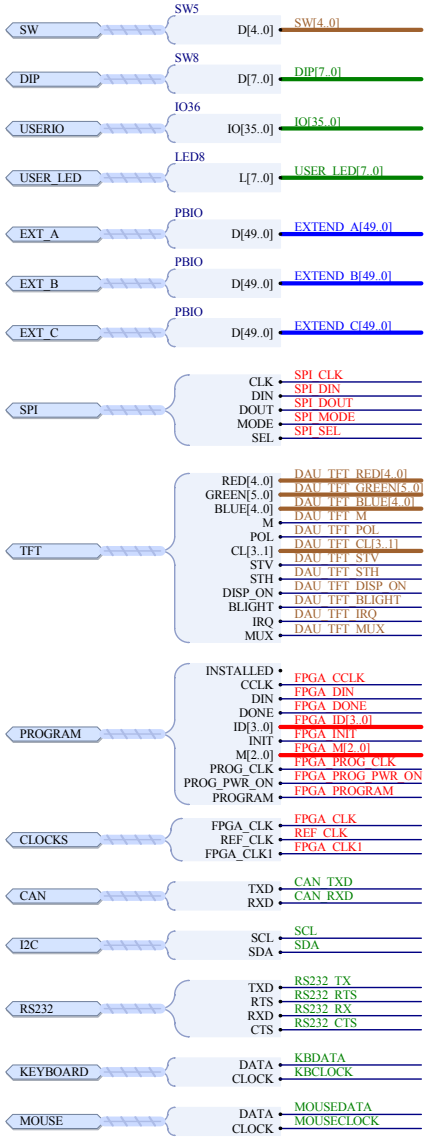
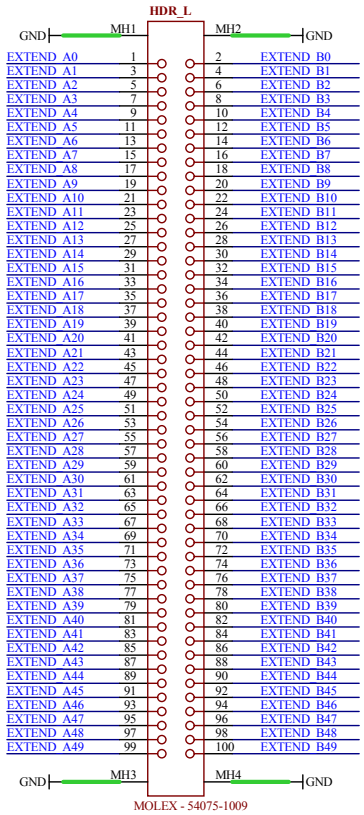
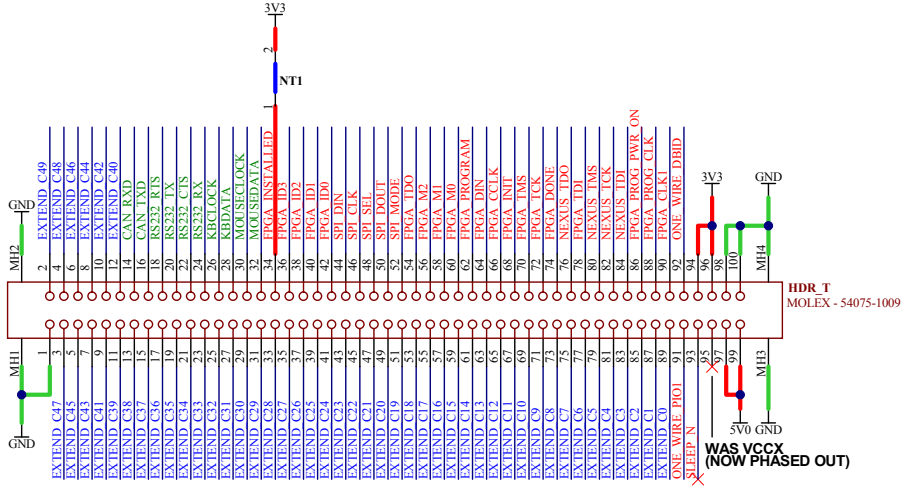




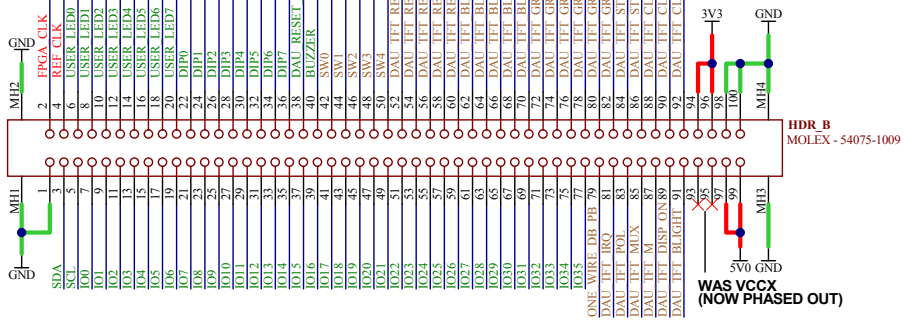






Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the motherboard. These can be changed.

Sheet Title	NB2 to Daughter Board Connectors		
Project Title	DB41 - Spartan3A/3AN		
Size: A3	Assy: D-820-0024	Revision: 01	
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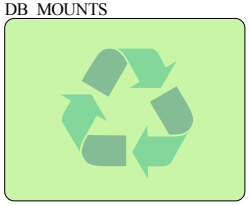
U_MOUNTS
DB_MOUNTS



PCB1
DB41 Blank PCB
Printed Circuit Board (Bare)

Sheet Title	***DB41 Hardware Kit***	
Project Title	***DB41 - Spartan3A/3AN***	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:45 PM	Sheet 21 of 22
File: DB41_Hardware_Kit.SchDoc		

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MH1
MOUNTING HOLE 3MM

MH2
MOUNTING HOLE 3MM

MH3
MOUNTING HOLE 3MM

Altium Logo Top1

Altium Logo Bot1

Sheet Title	***Mounts, Logo & Label***	
Project Title	***DB41 - Spartan3A/3AN***	
Size: A4	Assy: D-820-0024	Revision: 01
Date: 2/12/2008	Time: 1:41:45 PM	Sheet 22 of 22
File: DB_MOUNTS.SchDoc		

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