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HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

Switching Regulator for Chopper Type DC/DC Converter

ADE-204-020A (Z)

Rev.1
Dec. 2000

Description

The HA16114P/FP/FPJ and HA16120FP/FPJ are single-channel PWM switching regulator controller ICs suitable for chopper-type DC/DC converters. Integrated totem-pole output circuits enable these ICs to drive the gate of a power MOSFET directly. The output logic of the HA16120 is designed to control a DC/DC step-up (boost) converter using an N-channel power MOS FET. The output logic of the HA16114 is designed to control a DC/DC step-down (buck) converter or inverting converter using a P-channel power MOS FET.

These ICs can operate synchronously with external pulse, a feature that makes them ideal for power supplies that use a primary-control AC/DC converter to convert commercial AC power to DC, then use one or more DC/DC converters on the secondary side to obtain multiple DC outputs. Synchronization is with the falling edge of the 'sync' pulse, which can be the secondary output pulse from a flyback transformer. Synchronization eliminates the beat interference that can arise from different operating frequencies of the AC/DC and DC/DC converters, and reduces harmonic noise. Synchronization with an AC/DC converter using a forward transformer is also possible, by inverting the 'sync' pulse.

Overcurrent protection features include a pulse-by-pulse current limiter that can reduce the width of individual PWM pulses, and an intermittent operating mode controlled by an on-off timer. Unlike the conventional latched shutdown function, the intermittent operating function turns the IC on and off at controlled intervals when pulse-by-pulse current limiting continues for a programmable time. This results in sharp vertical settling characteristics. Output recovers automatically when the overcurrent condition subsides.

Using these ICs, a compact, highly efficient DC/DC converter can be designed easily, with a reduced number of external components.

Functions

- 2.5 V voltage reference
- Sawtooth oscillator (Triangle wave)
- Overcurrent detection
- External synchronous input
- Totem-pole output

- Undervoltage lockout (UVL)
- Error amplifier
- Vref overvoltage protection (OVP)

Features

- Wide supply voltage range: 3.9 V to 40 V*
- Maximum operating frequency: 600 kHz
- Able to drive a power MOS FET (±1 A maximum peak current) by the built-in totem-pole gate pre-driver circuit
- Can operate in synchronization with an external pulse signal, or with another controller IC
- Pulse-by-pulse overcurrent limiting (OCL)
- Intermittent operation under continuous overcurrent
- Low quiescent current drain when shut off by grounding the ON/$\overline{\text{OFF}}$ pin
  HA16114: I_{OFF} = 10 µA (max)
  HA16120: I_{OFF} = 150 µA (max)
- Externally trimmable reference voltage (Vref): ±0.2 V
- Externally adjustable undervoltage lockout points (with respect to V_{IN})
- Stable oscillator frequency
- Soft start and quick shut function

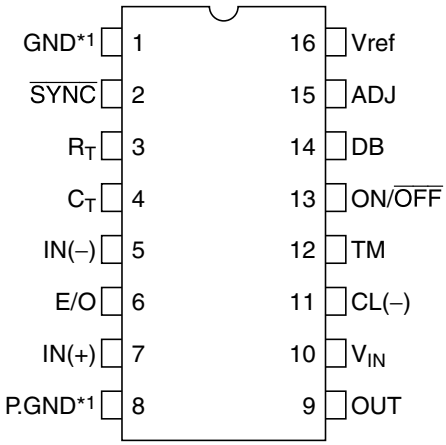
Note: The reference voltage 2.5 V is under the condition of $V_{IN} \geq 4.5$ V.

Ordering Information

Hitachi Control ICs for Chopper-Type DC/DC Converters

Channels	Product Number	Channel No.	Control Functions			Output Circuits	Overcurrent Protection
			Step-Up	Step-Down	Inverting		
Dual	HA17451	Ch 1				Open collector	SCP with timer (latch)
		Ch 2					
Single	HA16114	—	—			Totem pole power MOS FET driver	Pulse-by-pulse current limiter and intermittent operation by on/off timer
	HA16120	—		—	—		
Dual	HA16116	Ch 1	—				
		Ch 2	—		—		
	HA16121	Ch 1	—				
		Ch 2		—	—		

Pin Arrangement



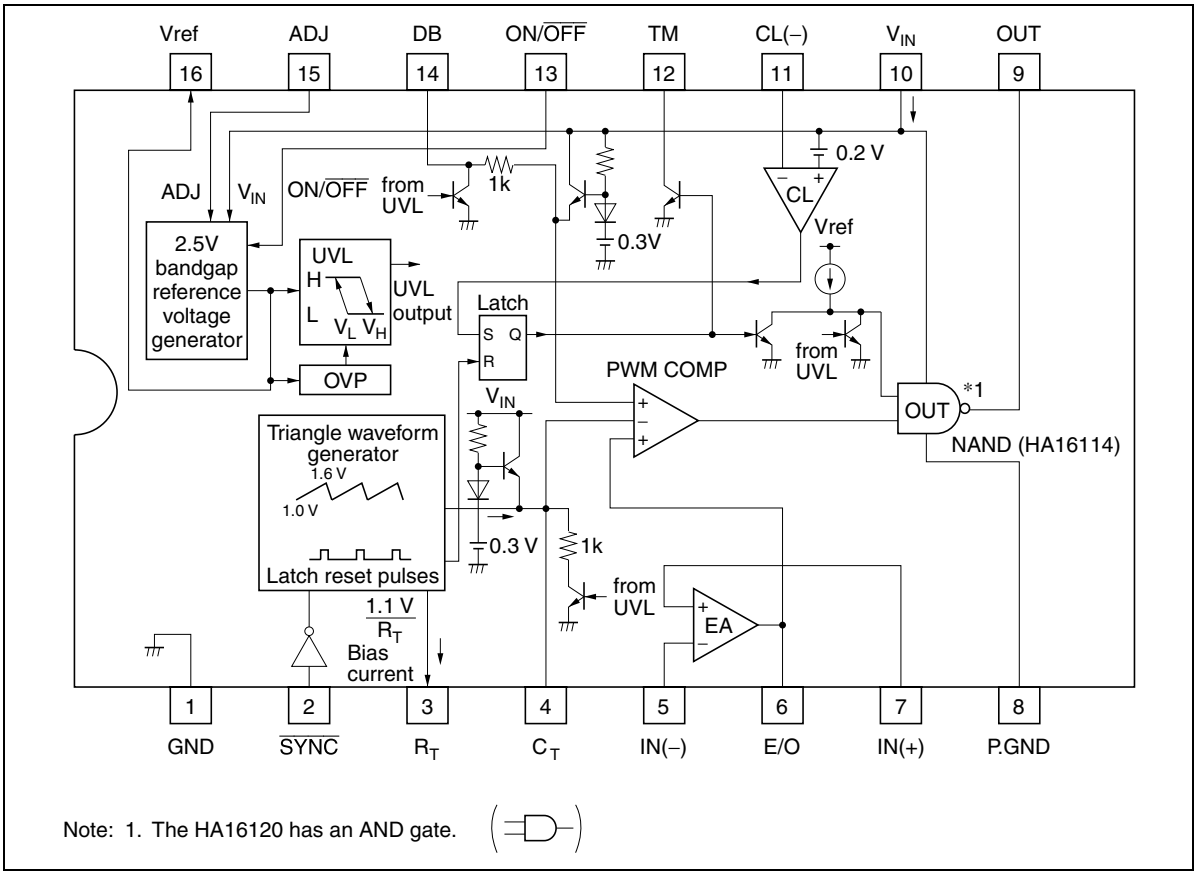
(Top view)

Note: 1. Pin 1 (GND) and Pin 8 (P.GND) must be connected each other with external wire.

Pin Description

Pin No.	Symbol	Function
1	GND	Signal ground
2	$\overline{\text{SYNC}}$	External sync signal input (synchronized with falling edge)
3	R_T	Oscillator timing resistor connection (bias current control)
4	C_T	Oscillator timing capacitor connection (sawtooth voltage output)
5	IN(–)	Inverting input to error amplifier
6	E/O	Error amplifier output
7	IN(+)	Non-inverting input to error amplifier
8	P.GND	Power ground
9	OUT	Output (pulse output to gate of power MOS FET)
10	V_{IN}	Power supply input
11	CL(–)	Inverting input to current limiter
12	TM	Timer setting for intermittent shutdown when overcurrent is detected (sinks timer transistor current)
13	ON/$\overline{\text{OFF}}$	IC on/off control (off below approximately 0.7 V)
14	DB	Dead-band duty cycle control input
15	ADJ	Reference voltage (Vref) adjustment input
16	Vref	2.5 V reference voltage output

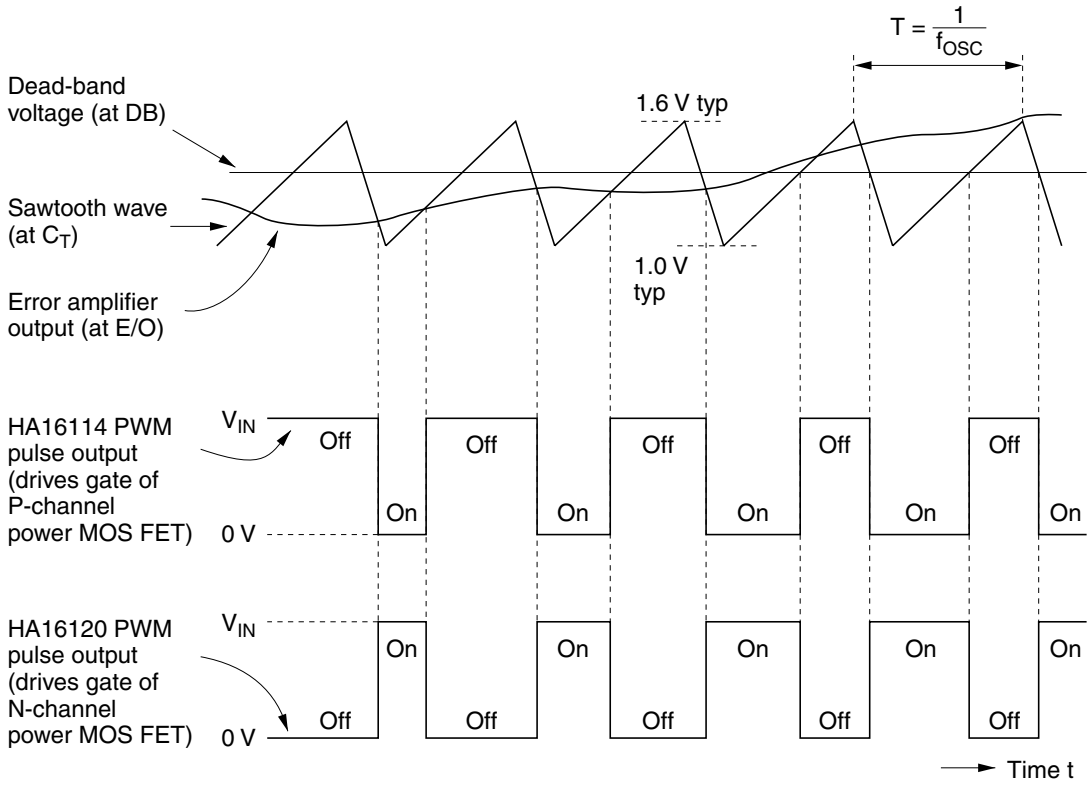
Block Diagram



Note: 1. The HA16120 has an AND gate.

Timing Waveforms

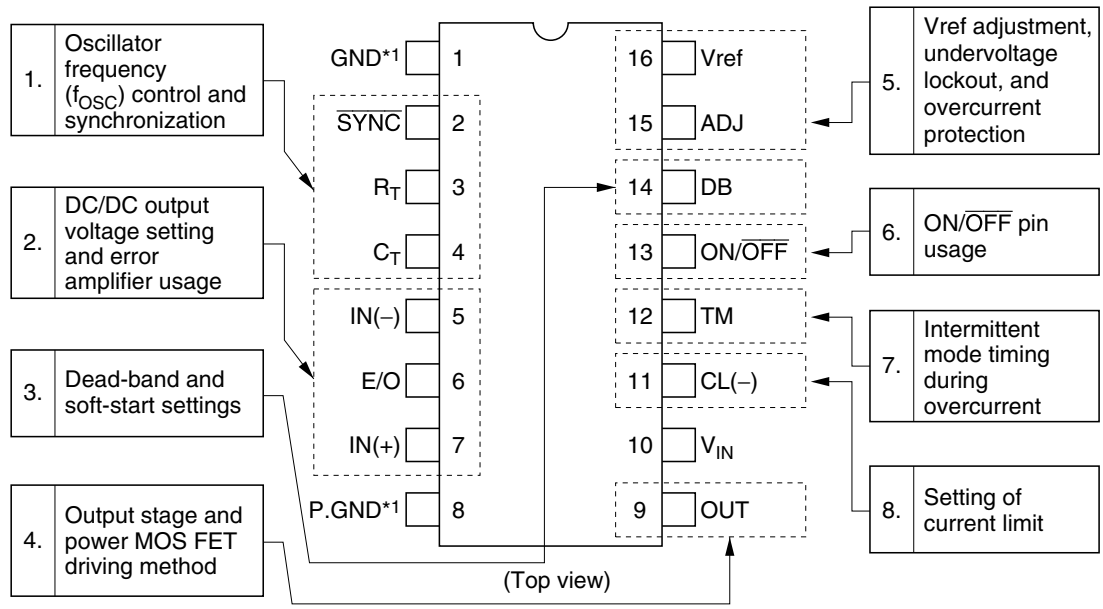
Generation of PWM pulse output from sawtooth wave (during steady-state operation)



Note: On duty = $\frac{t_{ON}}{T}$

Guide to the Functional Description

The description covers the topics indicated below.



Note: 1. P.GND is a high-current (±1 A maximum peak) ground pin connected to the totem-pole output circuit. GND is a low-current ground pin connected to the Vref voltage reference. Both pins must be grounded.

1. Sawtooth Oscillator (Triangle Wave)

1.1 Operation and Frequency Control

The sawtooth wave is a voltage waveform from which the PWM pulses are created (See figure 1). The sawtooth oscillator operates as follows. A constant current I_O determined by an external timing resistor R_T is fed continuously to an external timing capacitor C_T. When the C_T pin voltage exceeds a comparator threshold voltage V_{TH}, the comparator output opens a switching transistor, allowing a $3I_O$ discharge current to flow from C_T. When the C_T pin voltage drops below a threshold voltage V_{TL}, the comparator output closes the switching transistor, stopping the $3I_O$ discharge. Repetition of these operations generates a sawtooth wave.

The value of I_O is 1.1 V/R_T Ω. The I_O current mirror has a limited current capacity, so R_T should be at least 5 kΩ ($I_O \leq 220$ μA).

Internal resistances R_A, R_B, and R_C set the peak and valley voltages V_{TH} and V_{TL} of the sawtooth waveform at approximately 1.6 V and 1.0 V.

The oscillator frequency f_{osc} can be calculated as follows.

$$f_{OSC} = \frac{1}{t_1 + t_2 + t_3}$$

Here, $t_1 = \dfrac{C_T \times (V_H - V_L)}{1.1\ V/R_T}$

$$t_2 = \frac{C_T \times (V_H - V_L)}{3 \times 1.1\ V/R_T}$$

$t_3 \approx 0.8\ \mu s$ (comparator delay time)

Since $V_H - V_L = 0.6\ V$

$$f_{OSC} \approx \frac{1}{0.73 \times C_T \times R_T + 0.8\ (\mu s)}\ (Hz)$$

At high frequencies the comparator delay causes the sawtooth wave to overshoot the 1.6 V threshold and undershoot the 1.0 V threshold, and changes the dead-band thresholds accordingly. Select constants by testing under implementation conditions.

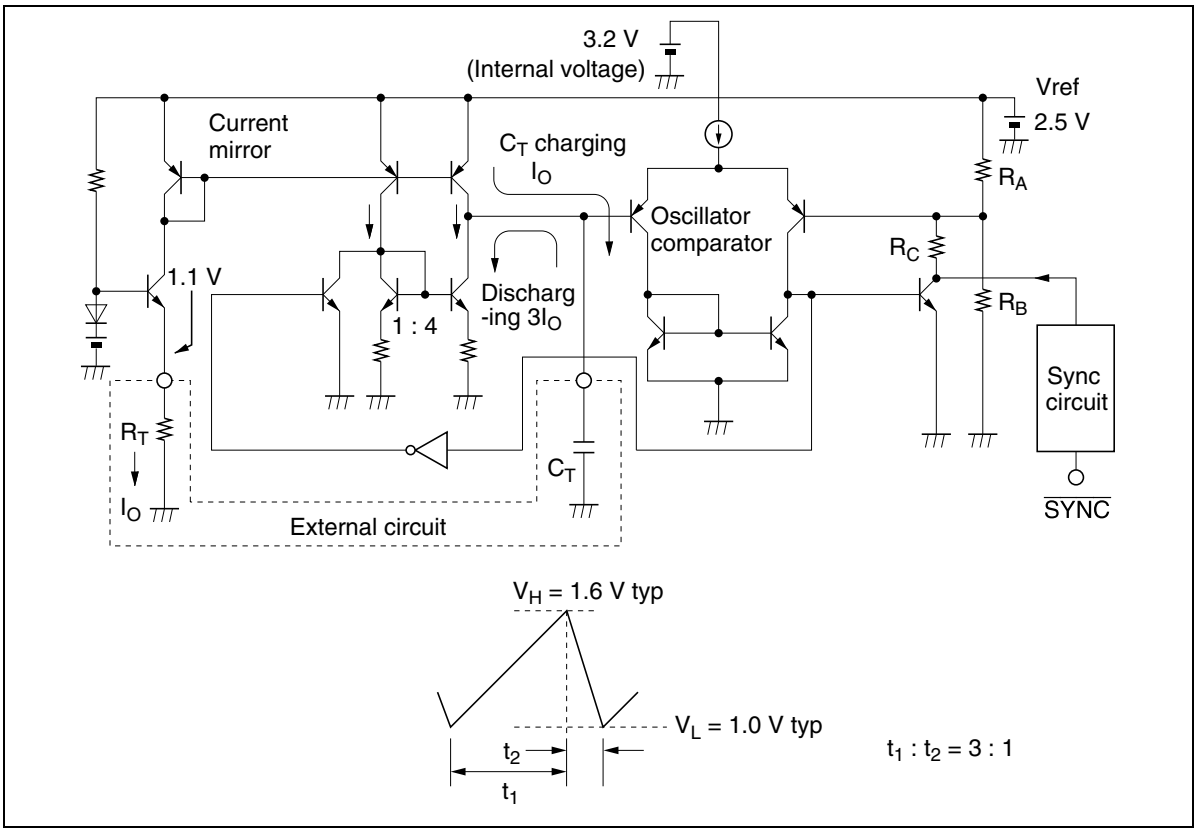


Figure 1.1 Equivalent Circuit of Oscillator

1.2 External Synchronization

These ICs have a sync input pin so that they can be synchronized to a primary-control AC/DC converter. Pulses from the secondary winding of the switching transformer should be dropped through a resistor voltage divider to the sync input pin. Synchronization takes place at the falling edge, which is optimal for multiple-output power supplies that synchronize with a flyback AC/DC converter.

The sync input pin ($\overline{\text{SYNC}}$) is connected internally through a synchronizing circuit to the sawtooth oscillator to synchronize the sawtooth waveform (see figure 1.2).

- Synchronization is with the falling edge of the external sync signal.
- The frequency of the external sync signal must be in the range $f_{OSC} < f_{\overline{SYNC}} < f_{OSC} \times 2$.
- The duty cycle of the external sync signal must be in the range $5\% < t_1/t_2 < 50\%$ (t_1 = 300 ns Min).
- With external synchronization, V_{TH}' can be calculated as follows.

$$V_{TH}' = (V_{TH} - V_{TL}) \times \frac{f_{OSC}}{f_{\overline{SYNC}}} + V_{TL}$$

Note: When not using external synchronization, connect the $\overline{\text{SYNC}}$ pin to the Vref pin.

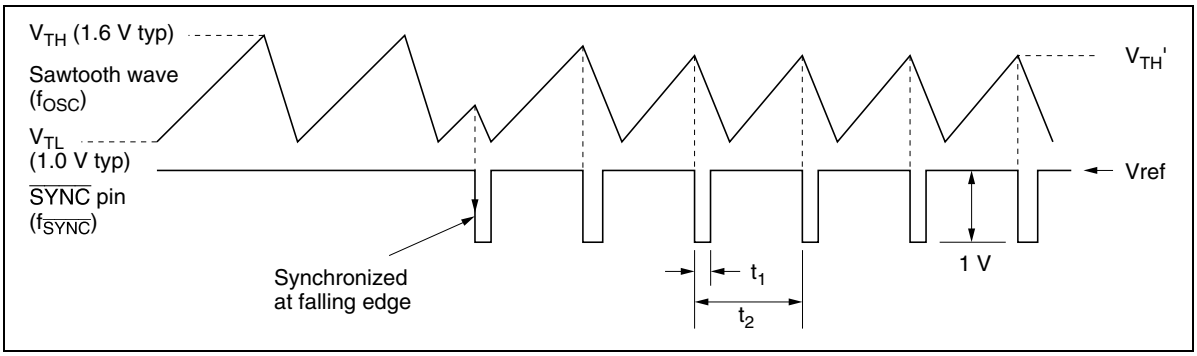


Figure 1.2 External Synchronization

2. DC/DC Output Voltage Setting and Error Amplifier Usage

2.1 DC/DC Output Voltage Setting

1. Positive Output Voltage (V_o > Vref)

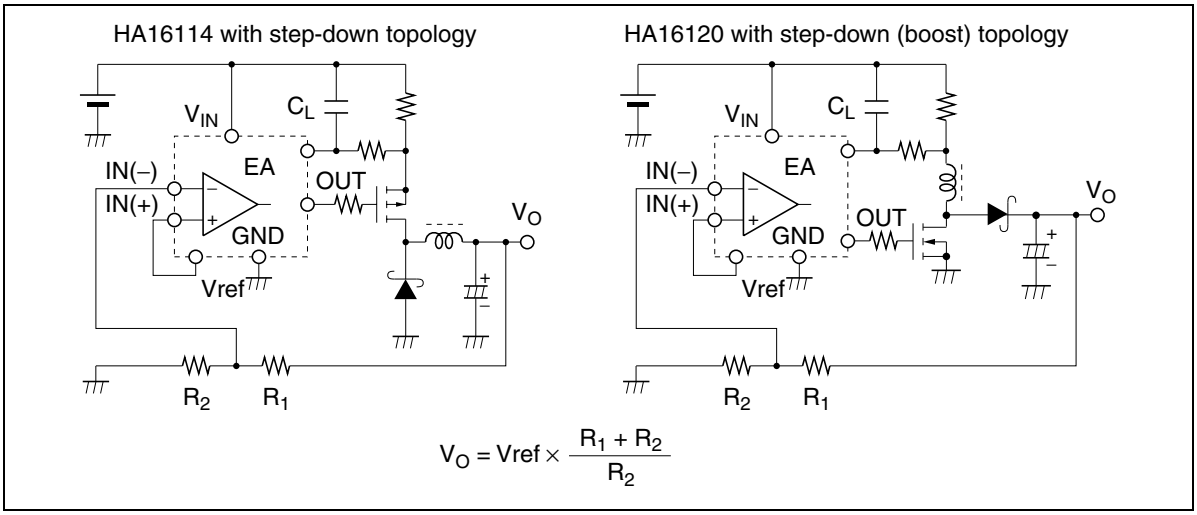


Figure 2.1 Output Voltage Setting (1)

2. Negative Output Voltage (V_o < 0 V)

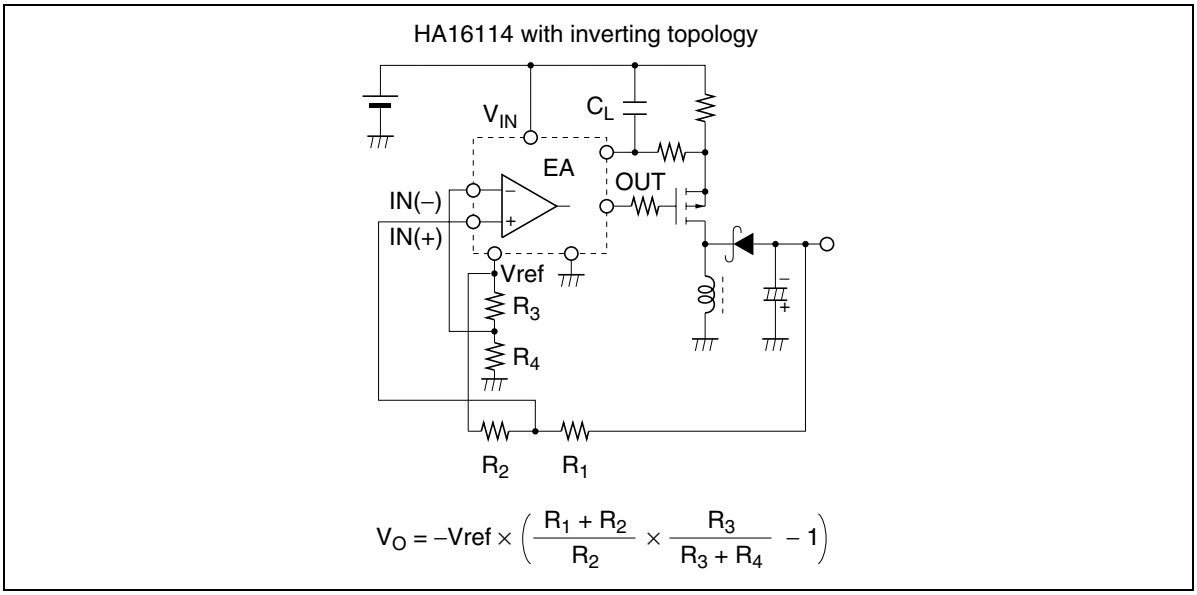


Figure 2.2 Output Voltage Setting (2)

2.2 Error Amplifier Usage

Figure 2.3 shows an equivalent circuit of the error amplifier. The error amplifier in these ICs is a simple NPN-transistor differential amplifier with a constant-current-driven output circuit.

The amplifier combines a wide bandwidth (f_T = 4 MHz) with a low open-loop gain (50 dB Typ), allowing stable feedback to be applied when the power supply is designed. Phase compensation is also easy.

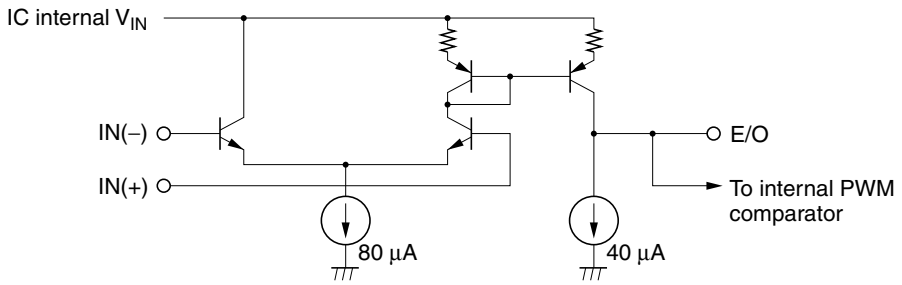


Figure 2.3 Error Amplifier Equivalent Circuit

3. Dead-Band Duty Cycle and Soft-Start Settings

3.1 Dead-Band Duty Cycle Setting

The dead-band duty cycle (the maximum duty cycle of the PWM pulse output) can be programmed by the voltage V_{DB} at the DB pin. A convenient way to obtain V_{DB} is to divide the IC's Vref output by two external resistors. The dead-band duty cycle (DB) and V_{DB} can be calculated as follows.

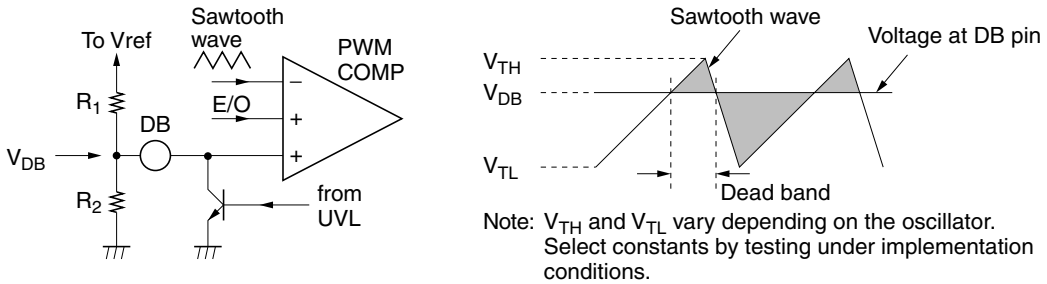
$$DB = \frac{V_{TH} - V_{DB}}{V_{TH} - V_{TL}} \times 100\ (\%) \cdots \text{This applies when } V_{DB} > V_{TL}.$$

If $V_{DB} < V_{TL}$, there is no PWM output.

$$V_{DB} = Vref \times \frac{R_2}{R_1 + R_2}$$

Note: V_{DB} is the voltage at the DB pin.
V_{TH}: 1.6 V (Typ)
V_{TL}: 1.0 V (Typ)

Vref is typically 2.5 V. Select R_1 and R_2 so that 1.0 V ≤ V_{DB} ≤ 1.6 V.



Note: V_{TH} and V_{TL} vary depending on the oscillator. Select constants by testing under implementation conditions.

Figure 3.1 Dead-Band Duty Cycle Setting

3.2 Soft-Start Setting

Soft-start avoids overshoot at power-up by widening the PWM output pulses gradually, so that the converted DC output rises slowly. Soft-start is programmed by connecting a capacitor between the DB pin and ground. The soft-start time is determined by the time constant of this capacitor and the resistors that set the voltage at the DB pin.

$$t_{soft} = -C_1 \times R \times \ln\left(1 - \frac{V_X}{V_{DB}}\right)$$

$$R = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{DB} = Vref \times \frac{R_2}{R_1 + R_2}$$

Note: V_X is the voltage at the DB pin after time t ($V_X < V_{DB}$).

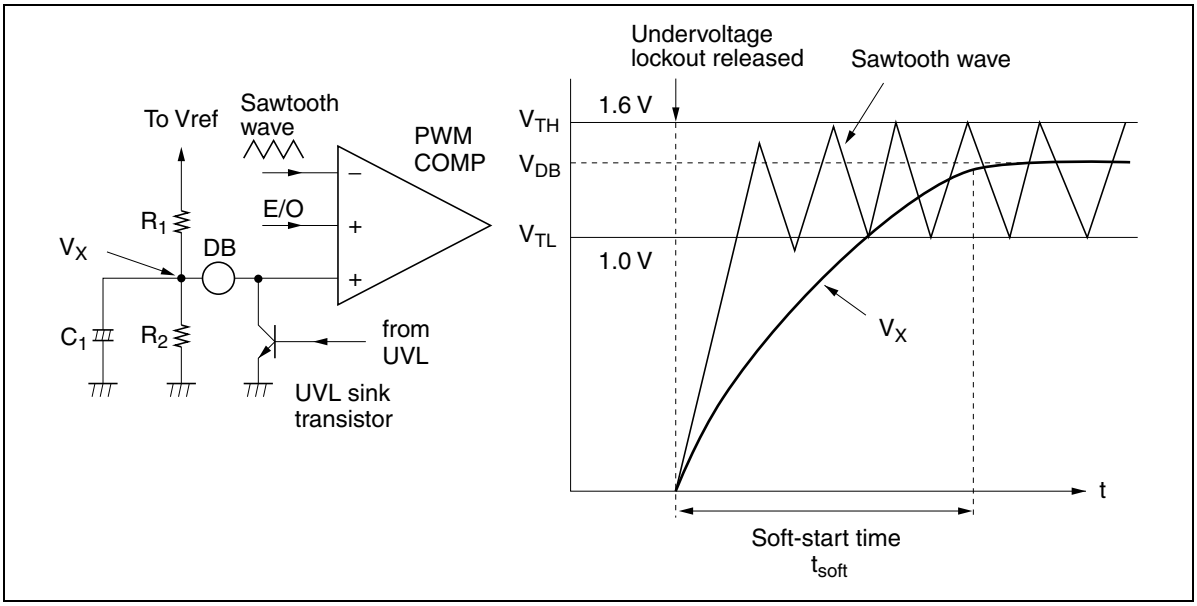


Figure 3.2 Soft-Start Setting

3.3 Quick Shutdown

The quick shutdown function resets the voltages at all pins when the IC is turned off, to assure that PWM pulse output stops quickly. Since the UVL pull-down resistor in the IC remains on even when the IC is turned off, the sawtooth wave output, error amplifier output, and DB pin are all reset to low voltage.

This feature helps in particular to discharge capacitor C_1 in figure 3.2, which has a comparatively large capacitance. In intermittent mode (explained on a separate page), this feature enables the IC to soft-start in each on-off cycle.

4. PWM Output Circuit and Power MOSFET Driving Method

These ICs have built-in totem-pole push-pull drive circuits that can drive a power MOS FET as shown in figure 4.1. The power MOS FET can be driven directly through a gate protection resistor.

If V_{IN} exceeds the gate breakdown voltage of the power MOS FET additional protective measures should be taken, e.g. by adding Zener diodes as shown in figure 4.2.

To drive a bipolar power transistor, the base should be protected by voltage and current dividing resistors as shown in figure 4.3.

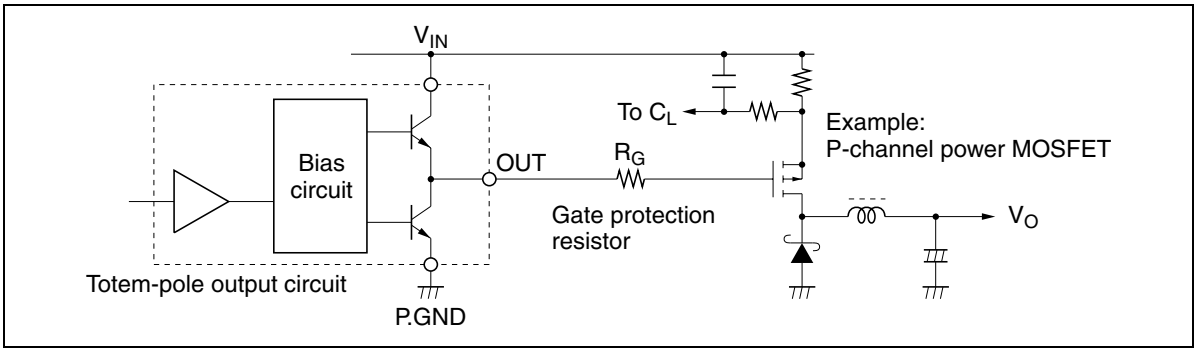


Figure 4.1 Connection of Output Stage to Power MOS FET

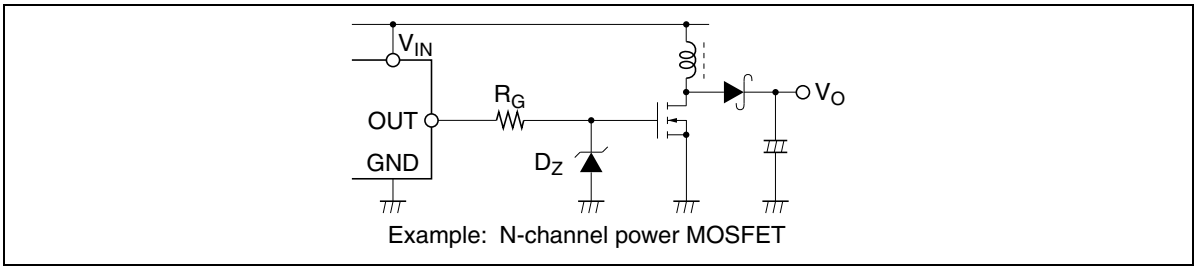


Figure 4.2 Gate Protection by Zener Diodes

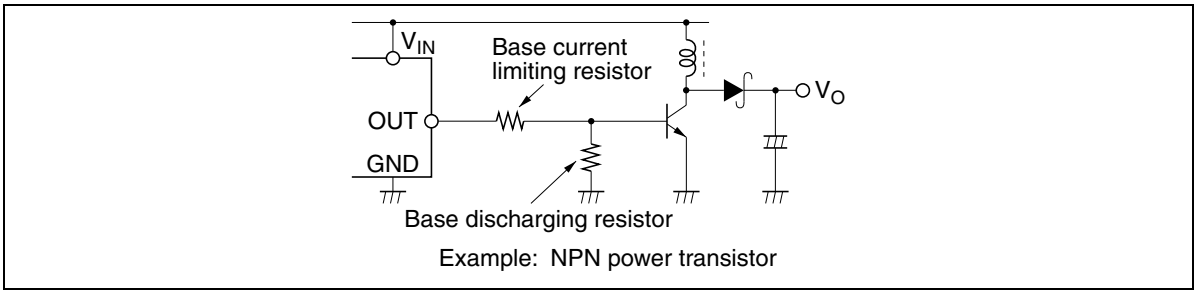


Figure 4.3 Driving a Bipolar Power Transistor

5. Voltage Reference (Vref = 2.5 V)

5.1 Voltage Reference

A bandgap reference built into the IC (see figure 5.1) outputs 2.5 V ± 50 mV. The sawtooth oscillator, PWM comparator, latch, and other internal circuits are powered by this 2.5 V and an internally-generated voltage of approximately 3.2 V.

The voltage reference section shut downs when the IC is turned off at the ON/$\overline{\text{OFF}}$ pin as described later, saving current when the IC is not used and when it operates in intermittent mode during overcurrent.

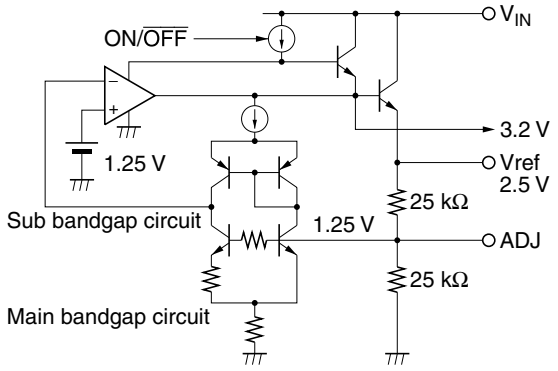


Figure 5.1 Vref Reference Circuit

5.2 Trimming the Reference Voltage (Vref and ADJ pins)

Figure 5.2 shows a simplified circuit equivalent to figure 5.1. The ADJ pin in this circuit is provided for trimming the reference voltage (Vref). The output at the ADJ pin is a voltage V_{ADJ} of 1.25 V (Typ) generated by the bandgap circuit. Vref is determined by V_{ADJ} and the ratio of internal resistors R_1 and R_2 as follows:

$$\text{Vref} = V_{ADJ} \times \frac{R_1 + R_2}{R_2}$$

The design values of R_1 and R_2 are 25 kΩ with a tolerance of ±25%.

If trimming is not performed, the ADJ pin open can be left open.

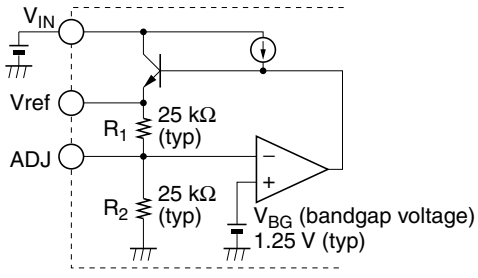


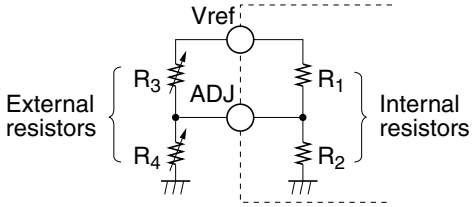
Figure 5.2 Simplified Diagram of Voltage Reference Circuit

The relation between Vref and the ADJ pin enables Vref to be trimmed by inserting one external resistor (R_3) between the Vref and ADJ pins and another (R_4) between the ADJ pin and ground, to change the resistance ratio. Vref is then determined by the combined resistance ratio of the internal R_1 and R_2 and external R_3 and R_4.

$$Vref = V_{ADJ} \times \frac{R_A + R_B}{R_B}$$

Where, R_A: parallel resistance of R_1 and R_3
R_B: parallel resistance of R_2 and R_4

Although Vref can be trimmed by R_3 or R_4 alone, to decrease the temperature dependence of Vref it is better to use two resistors having identical temperature coefficients. Vref can be trimmed in the range of 2.5 V ± 0.2 V. Outside this range, the bandgap circuit will not operate and the IC may shut down.



$$R_A = \frac{R_1 R_3}{R_1 + R_3}$$

$$R_B = \frac{R_2 R_4}{R_2 + R_4}$$

Figure 5.3 Trimming of Reference Voltage

5.3 Vref Undervoltage Lockout and Overvoltage Protection

The undervoltage lockout (UVL) function turns off PWM pulse output when the input voltage (V_{IN}) is low. In these ICs, this is done by monitoring the Vref voltage, which normally stays constant at approximately 2.5 V. The UVL circuit operates with hysteresis: it shuts PWM output off when Vref falls below 1.7 V, and turns PWM output back on when Vref rises above 2.0 V. Undervoltage lockout also provides protection in the event that Vref is shorted to ground.

The overvoltage protection circuit shuts PWM output off when Vref goes above 6.8 V. This provides protection in case the Vref pin is shorted to V_{IN} or another high-voltage source.

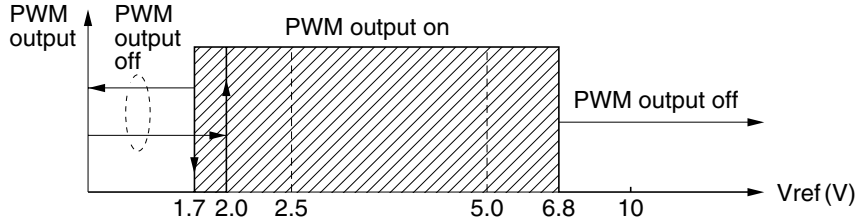


Figure 5.4 Vref Undervoltage Lockout and Overvoltage Protection

UVL Voltage	Vref (V typ)	V_{IN} (V typ)	Description
V_H	2.0 V	3.6 V	V_{IN} increasing: UVL releases; PWM output starts
V_L	1.7 V	3.3 V	V_{IN} decreasing: undervoltage lockout; PWM output stops

6. Usage of ON/$\overline{\text{OFF}}$ Pin

This pin is used for the following purposes:

- To shut down the IC while its input power remains on (power management)
- To externally alter the UVL release voltage
- With the timer (TM) pin, to operate in intermittent mode during overcurrent (see next section)

6.1 Shutdown by ON/$\overline{\text{OFF}}$ Pin Control

The IC can be shut down safely by bringing the voltage at the ON/$\overline{\text{OFF}}$ pin below about 0.7 V (the internal VBE value). This feature can be used in power supply systems to save power. When shut down, the HA16114 draws a maximum current (I_{OFF}) of 10 µA, while the HA16120 draws a maximum 150 µA. The ON/$\overline{\text{OFF}}$ pin sinks 290 µA (Typ) at 5 V, so it can be driven by TTL and other logic ICs. If intermittent mode will also be employed, use a logic IC with an open-collector or open-drain output.

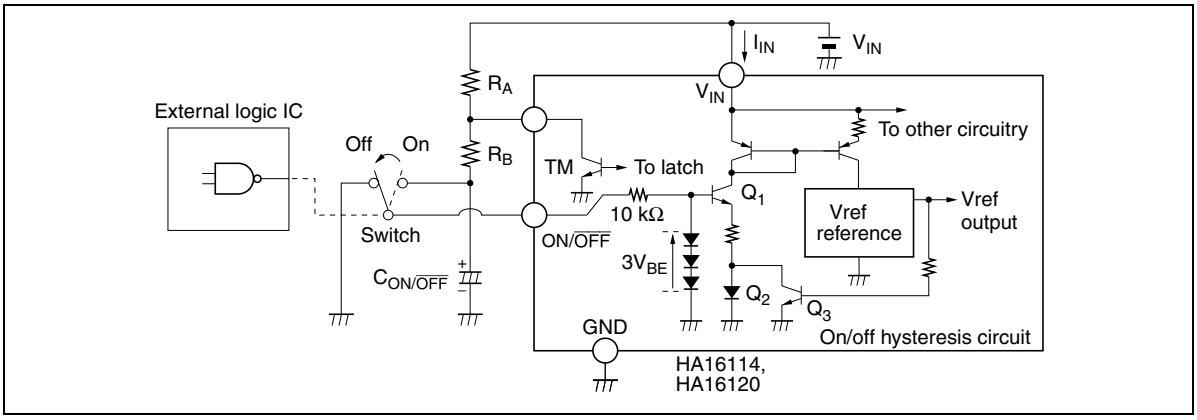


Figure 6.1 Shutdown by ON/$\overline{\text{OFF}}$ Pin Control

6.2 Adjustment of UVL Voltages (when not using intermittent mode)

These ICs permit external adjustment of the undervoltage lockout voltages. The adjustment is made by changing the undervoltage lockout thresholds V_{TH} and V_{TL} relative to V_{IN}, using the relationships shown in the accompanying diagrams.

When the IC is powered up, transistor Q_3 is off, so V_{ON} is $2V_{BE}$, or about 1.4 V. Connection of resistors R_C and R_D in the diagram makes undervoltage lockout release at:

$$V_{IN} = 1.4\ V \times \frac{R_C + R_D}{R_D}$$

This V_{IN} is the supply voltage at which undervoltage lockout is released. At the release point Vref is still below 2.5 V. To obtain Vref = 2.5 V, V_{IN} must be at least about 4.3 V.

Since $V_{ON/\overline{OFF}}$ operates in relation to the base-emitter voltage of internal transistors, V_{ON} has a temperature coefficient of approximately –4 mV/°C. Keep this in mind when designing the power supply unit.

When undervoltage lockout and intermittent mode are both used, the intermittent-mode time constant is shortened, so the constants of external components may have to be altered.

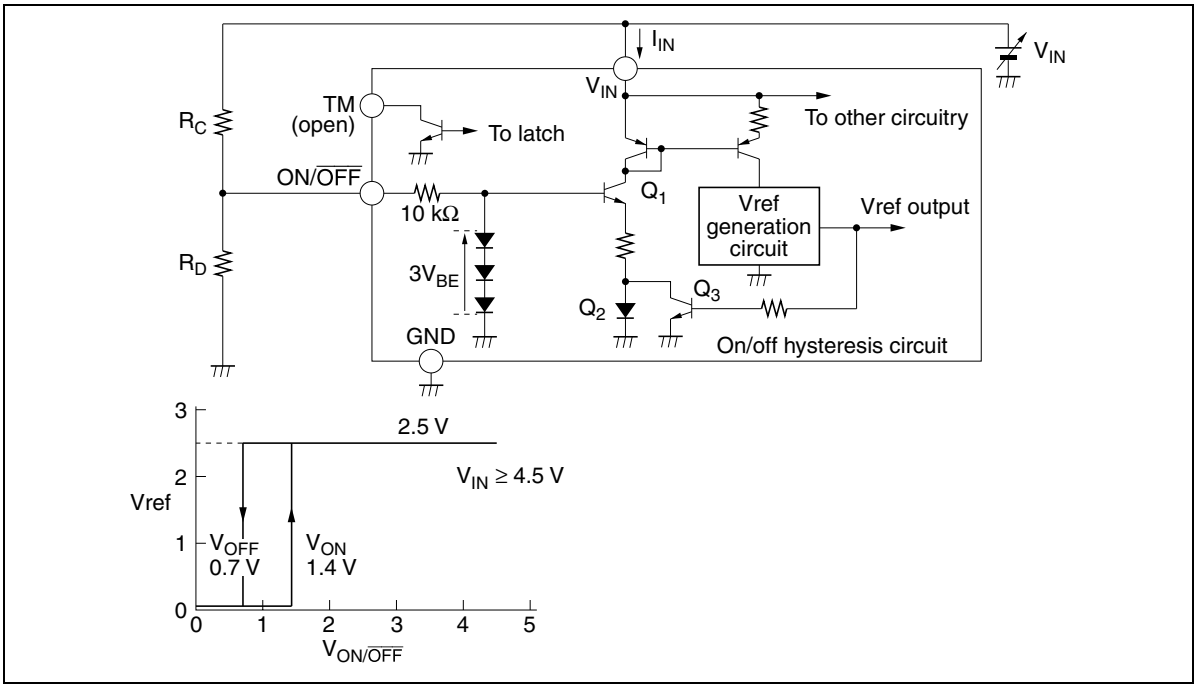


Figure 6.2 Adjustment of UVL Voltages

7. Timing of Intermittent Mode during Overcurrent

7.1 Principle of Operation

These ICs provide pulse-by-pulse overcurrent protection by sensing the current during each pulse and shutting off the pulse if overcurrent is detected. In addition, the TM and ON/$\overline{OFF}$ pins can be used to operate the IC in intermittent mode if the overcurrent state continues. A power supply with sharp settling characteristics can be designed in this way.

Intermittent mode operates by making use of the hysteresis of the ON/$\overline{OFF}$ pin threshold voltages V_{ON} and V_{OFF} ($V_{ON} - V_{OFF} = V_{BE}$). The timing can be programmed as explained below.

When not using intermittent mode, leave the TM pin open, and pull the ON/$\overline{OFF}$ pin up to V_{ON} or higher. The V_{BE} is base emitter voltage of internal transistors.

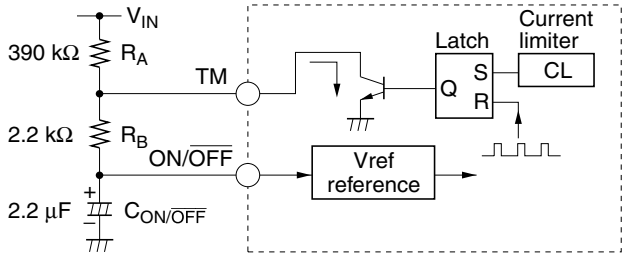
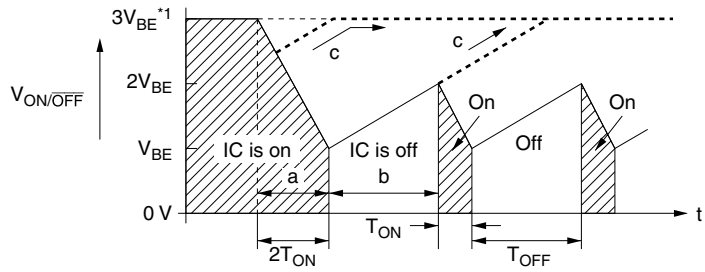


Figure 7.1 Connection Diagram (example)

7.2 Intermittent Mode Timing Diagram ($V_{ON/\overline{OFF}}$ only)



a. Continuous overcurrent is detected
b. Intermittent operation starts (IC is off)
c. Voltage if overcurrent ends (thick dotted line)

Note: 1. V_{BE} is the base-emitter voltage of internal transistors, and is approximately 0.7 V. (See the figure 6.1.)
For details, see the overall waveform timing diagram.

Figure 7.2 Intermittent Mode Timing Diagram ($V_{ON/\overline{OFF}}$ only)

7.3 Calculation of Intermittent Mode Timing

Intermittent mode timing is calculated as follows.

(1) T_{ON} (time until the IC shuts off when continuous overcurrent occurs)

$$T_{ON} = C_{ON/\overline{OFF}} \times R_B \times \ln\left(\frac{2V_{BE}}{V_{BE}}\right) \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

$$= C_{ON/\overline{OFF}} \times R_B \times \ln 2 \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

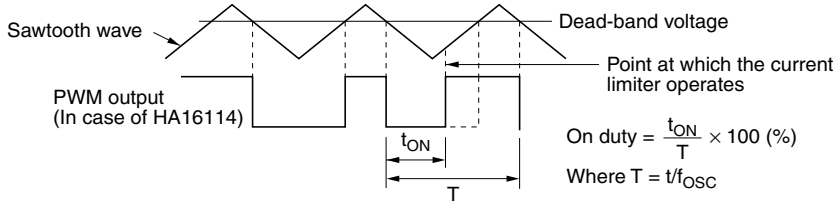
$$\approx 0.69 \times C_{ON/\overline{OFF}} \times R_B \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

(2) T_{OFF} (time from when the IC shuts off until it next turns on)

$$T_{OFF} = C_{ON/\overline{OFF}} \times (R_A + R_B) \times \ln\left(\frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}}\right)$$

Where $V_{BE} \approx 0.7$ V

The greater the overload, the sooner the pulse-by-pulse current limiter operates, the smaller t_{ON} becomes, and from the first equation (1) above, the smaller T_{ON} becomes. From the second equation (2), T_{OFF} depends on V_{IN}. Note that with the connections shown in the diagram, when V_{IN} is switched on the IC does not turn on until T_{OFF} has elapsed.



Note: On duty is the percent of time the IC output is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

Figure 7.3

7.4 Examples of Intermittent Mode Timing (calculated values)

(1) T_{ON}

$T_{ON} = T_1 \times C_{ON/\overline{OFF}} \times R_B$

Here, coefficient

$$T_1 = 0.69 \times \frac{1}{1 - \text{On duty}}$$

from section 7.3 (1) previously.

Example: If $C_{ON/\overline{OFF}}$ = 2.2 µF, R_B = 2.2 kΩ, and the on duty of the current limiter is 75%, then T_{ON} = 13 ms.

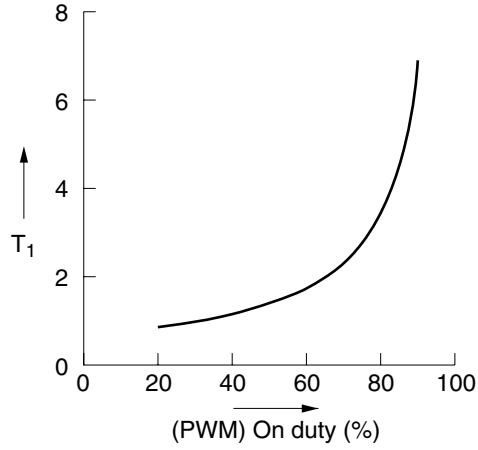


Figure 7.4 Examples of Intermittent Mode Timing (1)

(2) T_{OFF}

$T_{OFF} = T_2 \times C_{ON/\overline{OFF}} \times (R_A + R_B)$

Here, coefficient

$$T_2 = \ln \frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}}$$

from section 7.3 (2) previously.

Example: If $C_{ON/\overline{OFF}}$ = 2.2 µF, R_B = 2.2 kΩ, R_A = 390 kΩ, V_{IN} = 12 V, then T_{OFF} = 55 ms.

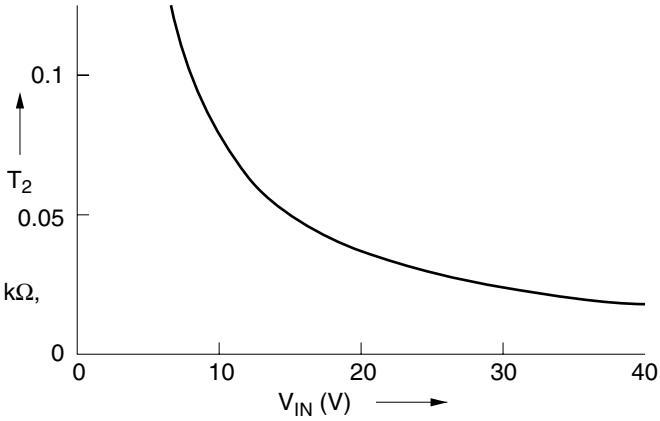


Figure 7.5 Examples of Intermittent Mode Timing (2)

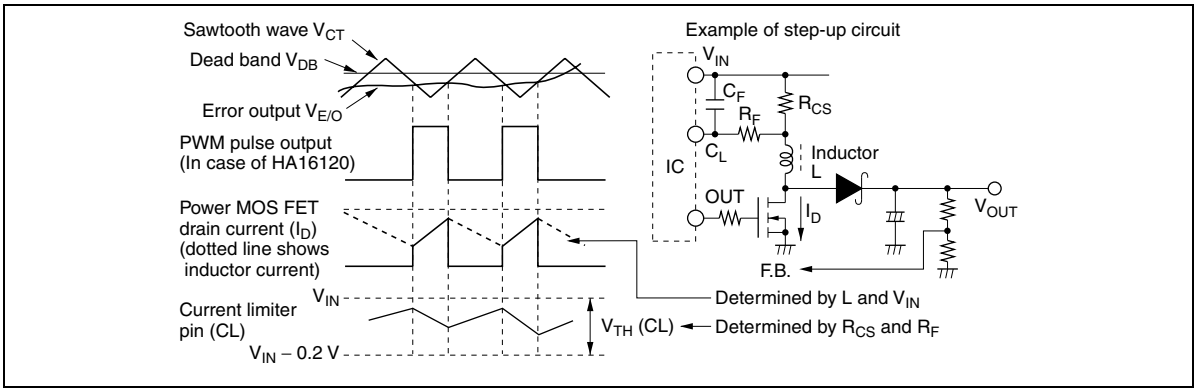


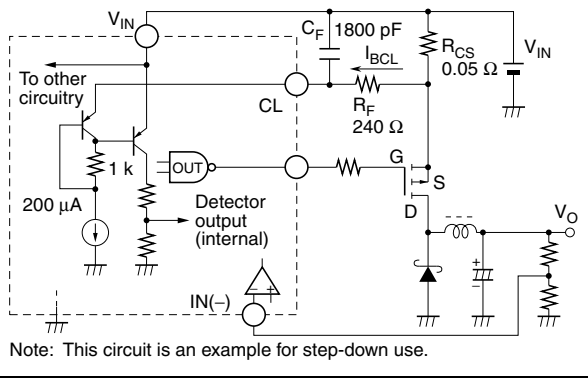
Figure 7.6

8. Setting the Overcurrent Detection Threshold

The voltage drop V_{TH} at which overcurrent is detected in these ICs is typically 0.2 V. The bias current is typically 200 µA. The power MOS FET peak current value before the current limiter goes into operation is given as follows.

$$I_D = \frac{V_{TH} - (R_F + R_{CS}) \times I_{BCL}}{R_{CS}}$$

Where, $V_{TH} = V_{IN} - V_{CL} = 0.2$ V, V_{CL} is a voltage refered on GND.
Note that R_F and C_F form a low-pass filter with a cutoff frequency determined by their RC time constant. This filter prevents incorrect operation due to current spikes when the power MOS FET is switched on or off.



Note: This circuit is an example for step-down use.

Figure 8.1 Example for Step-Down Use

With the values shown in the diagram, the peak current is:

$$I_D = \frac{0.2\ \text{V} - (240\ \Omega + 0.05\ \Omega) \times 200\ \mu\text{A}}{0.05\ \Omega} = 3.04\ \text{A}$$

The filter cutoff frequency is calculated as follows:

$$f_C = \frac{1}{2\pi\, C_F\, R_F} = \frac{1}{6.28 \times 1800\ \text{pF} \times 240\ \Omega} = 370\ \text{kHz}$$

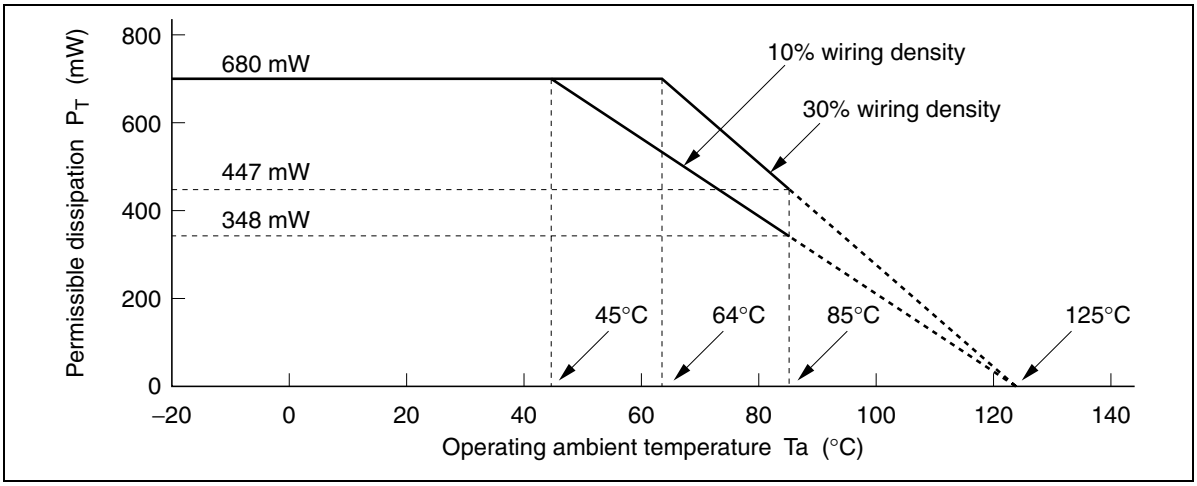
Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating		Unit
		HA16114P/FP, HA16120FP	HA16114PJ/FPJ, HA16120FPJ	
Supply voltage	V_{IN}	40	40	V
Output current (DC)	I_O	±0.1	±0.1	A
Output current (peak)	I_O peak	±1.0	±1.0	A
Current limiter input voltage	V_{CL}	V_{IN}	V_{IN}	V
Error amplifier input voltage	V_{IEA}	V_{IN}	V_{IN}	V
E/O input voltage	$V_{IE/O}$	Vref	Vref	V
RT source current	I_{RT}	500	500	µA
TM sink current	I_{TM}	3	3	mA
$\overline{SYNC}$ voltage	$V_{\overline{SYNC}}$	Vref	Vref	V
$\overline{SYNC}$ current	$I_{\overline{SYNC}}$	±250	±250	µA
Power dissipation	P_T	680*1, *2	680*1, *2	mW
Operating temperature	Topr	–20 to +85	–40 to +85	°C
Junction temperature	TjMax	125	125	°C
Storage temperature	Tstg	–55 to +125	–55 to +125	°C

Notes: 1. This value is for an SOP package (FP) and is based on actual measurements on a 40 × 40 × 1.6 mm glass epoxy circuit board. With a 10% wiring density, this value is permissible up to Ta = 45°C and should be derated by 8.3 mW/°C at higher temperatures. With a 30% wiring density, this value is permissible up to Ta = 64°C and should be derated by 11.1 mW/°C at higher temperatures.

2. For the DILP package.
   This value applies up to Ta = 45°C; at temperatures above this, 8.3 mW/°C derating should be applied.

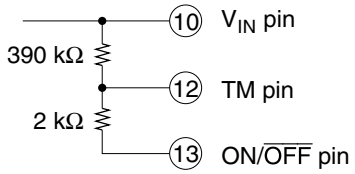


Electrical Characteristics

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Voltage reference section	Output voltage	Vref	2.45	2.50	2.55	V	I_O = 1 mA	
	Line regulation	Line	—	2	60	mV	4.5 V ≤ V_{IN} ≤ 40V	1
	Load regulation	Load	—	30	60	mV	0 ≤ I_O ≤ 10 mA	
	Short-circuit output current	I_{OS}	10	24	—	mA	Vref = 0 V	
	Vref overvoltage protection threshold	Vrovp	6.2	6.8	7.4	V		
	Temperature stability of output voltage	ΔVref/ΔTa	—	100	—	ppm/°C		
	Vref adjustment voltage	V_{ADJ}	1.225	1.25	1.275	V		
Sawtooth oscillator section	Maximum frequency	fmax	600	—	—	kHz		
	Minimum frequency	fmin	—	—	1	Hz		
	Frequency stability with input voltage	$\Delta f/f_{01}$	—	±1	±3	%	4.5 V ≤ V_{IN} ≤ 40 V (f_{01} = (fmax + fmin)/2)	
	Frequency stability with temperature	$\Delta f/f_{02}$	—	±5	—	%	–20°C ≤ Ta ≤ 85°C (f_{02} = (fmax + fmin)/2)	
	Oscillator frequency	f_{OSC}	90	100	110	kHz	R_T = 10 kΩ C_T = 1300 pF	
Dead-band adjustment section	Low level threshold voltage	V_{TL}	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	V_{TH}	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	ΔV_{TH}	0.5	0.6	0.7	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	
	Output source current	Isource	170	250	330	μA	DB pin: 0 V	
PWM comparator section	Low level threshold voltage	V_{TL}	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	V_{TH}	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	ΔV_{TH}	0.5	0.6	0.7	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	

Note: 1. Resistors connected to ON/$\overline{\text{OFF}}$ pin:



Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Error amplifier section	Input offset voltage	V_{IO}	—	2	10	mV		
	Input bias current	I_B	—	0.5	2.0	µA		
	Output sink current	I_{Osink}	28	40	52	µA	V_O = 2.5 V	
	Output source current	$I_{Osource}$	28	40	52	µA	V_O = 1.0 V	
	Common-mode input voltage range	V_{CM}	1.1	—	3.7	V		
	Voltage gain	A_V	40	50	—	dB	f = 10 kHz	
	Unity gain bandwidth	BW	—	4	—	MHz		
	High level output voltage	V_{OH}	3.5	4.0	—	V	I_O = 10 µA	
	Low level output voltage	V_{OL}	—	0.2	0.5	V	I_O = 10 µA	
Overcurrent detection section	Threshold voltage	V_{TH}	V_{IN}–0.22	V_{IN}–0.2	V_{IN}–0.18	V		
	CL(–) bias current	$I_{BCL(-)}$	140	200	260	µA	CL(–) = V_{IN}	
	Turn-off time	t_{OFF}	—	200	300	ns		1
			—	500	600	ns		2
UVL section	Vref high level threshold voltage	V_{TH}	1.7	2.0	2.3	V		
	Vref low level threshold voltage	V_{TL}	1.4	1.7	2.0	V		
	Threshold difference	Δ_{VTH}	0.1	0.3	0.5	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	
	VIN high level threshold voltage	V_{INH}	3.3	3.6	3.9	V		
	VIN low level threshold voltage	V_{INL}	3.0	3.3	3.6	V		

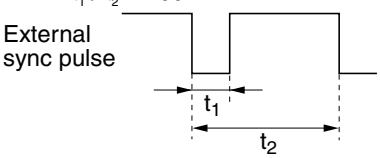
Notes: 1. HA16114 only.
2. HA16120 only.

Electrical Characteristics (cont.)

($Ta = 25°C$, $V_{IN} = 12$ V, $f_{OSC} = 100$ kHz)

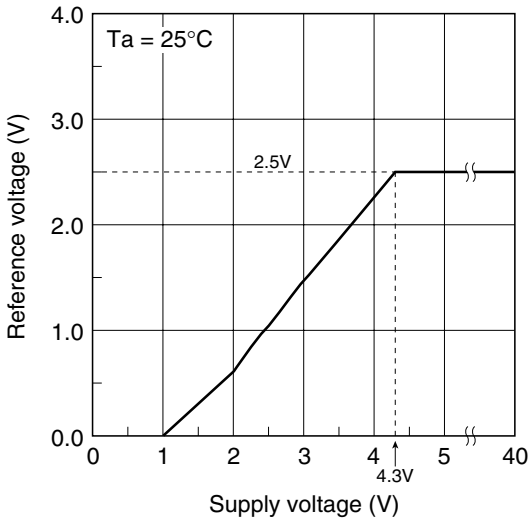
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Output stage	Output low voltage	V_{OL}	—	0.9	1.5	V	I_{Osink} = 10 mA	
	Output high voltage	V_{OH1}	V_{IN}–2.2	V_{IN}–1.6	—	V	$I_{Osource}$ = 10 mA	
	High voltage when off	V_{OH2}	V_{IN}–2.2	V_{IN}–1.6	—	V	$I_{Osource}$ = 1 mA ON/$\overline{OFF}$ pin: 0 V	1
	Low voltage when off	V_{OL2}	—	0.9	1.5	V	I_{Osink} = 1 mA ON/$\overline{OFF}$ pin: 0 V	2
	Rise time	t_r	—	50	200	ns	C_L = 1000 pF	
	Fall time	t_f	—	50	200	ns	C_L = 1000 pF	
External sync section	$\overline{SYNC}$ source current	$I_{\overline{SYNC}}$	120	180	240	µA	$\overline{SYNC}$ pin: 0 V	
	Sync input frequency range	$f_{\overline{SYNC}}$	f_{OSC}	—	$f_{OSC} \times 2$	kHz		
	External sync initiation voltage	$V_{\overline{SYNC}}$	Vref–1.0	—	Vref–0.5	V		
	Minimum pulse width of sync input	PWmin	300	—	—	ns		
	Input sync pulse duty cycle	PW	5	—	50	%		3
On/off section	ON/$\overline{OFF}$ sink current 1	$I_{ON/\overline{OFF}_1}$	60	90	120	µA	ON/$\overline{OFF}$ pin: 3 V	
	ON/$\overline{OFF}$ sink current 2	$I_{ON/\overline{OFF}_2}$	220	290	380	µA	ON/$\overline{OFF}$ pin: 5 V	
	IC on threshold	V_{ON}	1.1	1.4	1.7	V		
	IC off threshold	V_{OFF}	0.4	0.7	1.0	V		
	ON/$\overline{OFF}$ threshold difference	$\Delta V_{ON/\overline{OFF}}$	0.5	0.7	0.9	V		
Total device	Operating current	I_{IN}	6.0	8.5	11.0	mA	C_L = 1000 pF	
	Quiescent current	I_{OFF}	0	—	10	µA	ON/$\overline{OFF}$ pin: 0 V	1
			—	120	150	µA	ON/$\overline{OFF}$ pin: 0 V	2

Notes: 1. HA16114 only.
2. HA16120 only.
3. $PW = t_1 / t_2 \times 100$

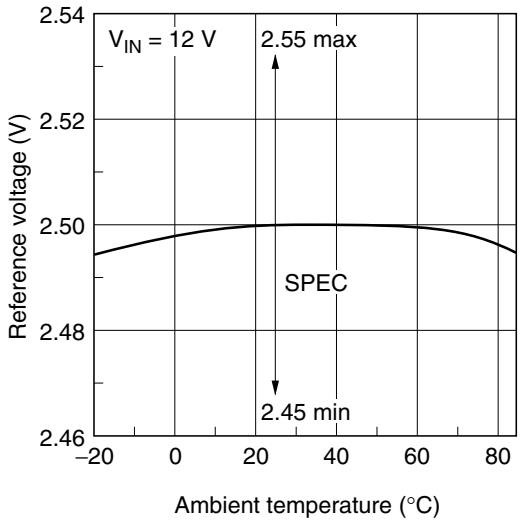


Characteristic Curves

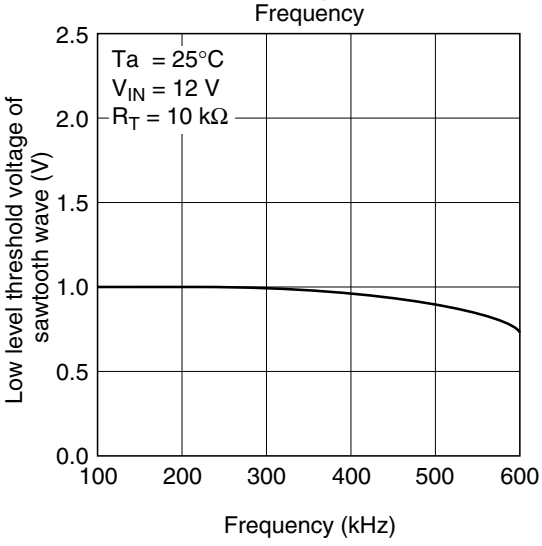
Reference Voltage vs. Supply Voltage



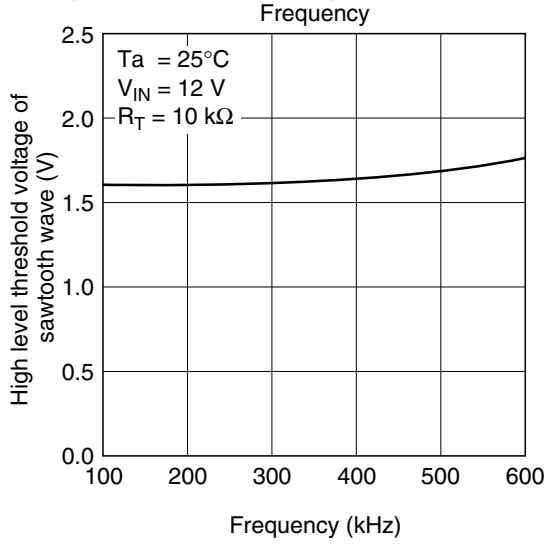
Reference Voltage vs. Ambient Temperature



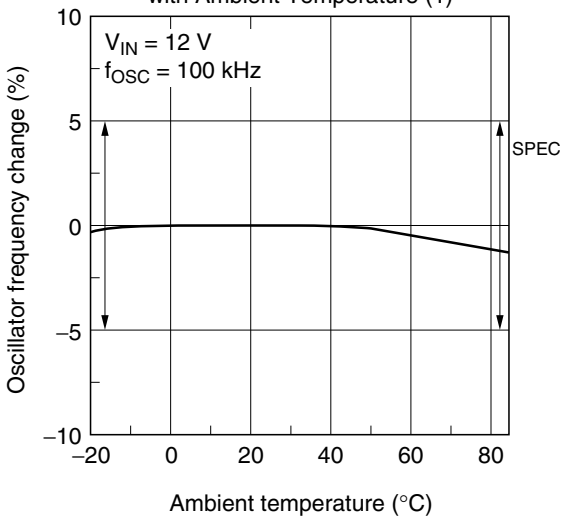
Low Level Threshold Voltage of Sawtooth Wave vs. Frequency



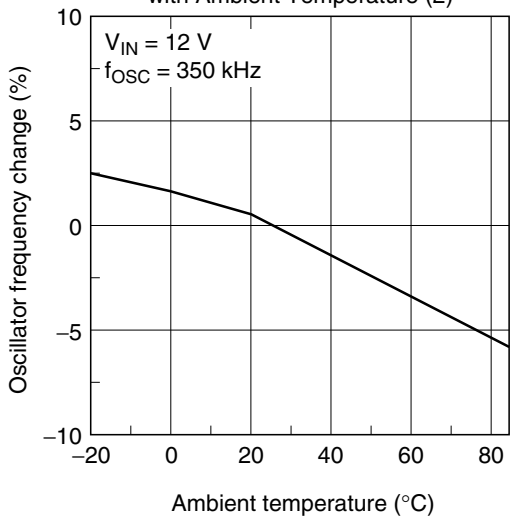
High Level Threshold Voltage of Sawtooth Wave vs. Frequency



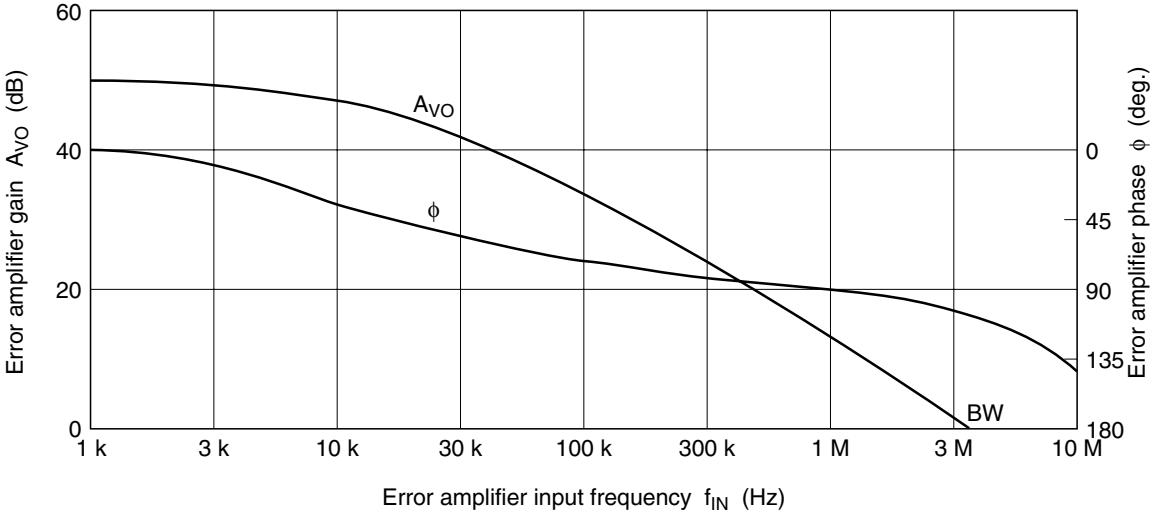
Oscillator Frequency Change with Ambient Temperature (1)



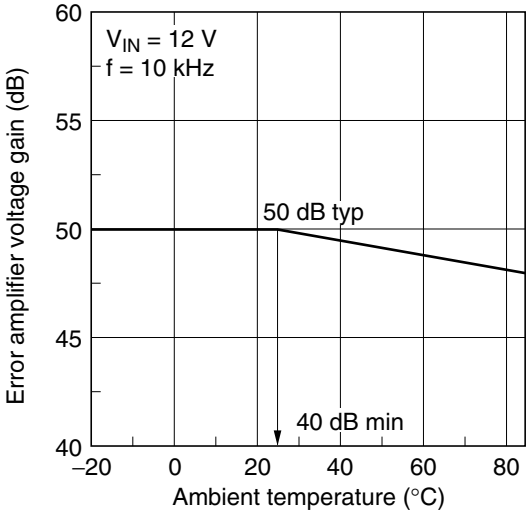
Oscillator Frequency Change with Ambient Temperature (2)



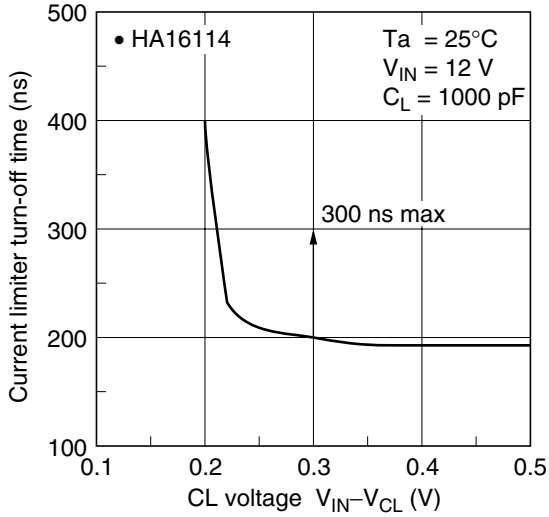
Error Amplifier Gain, Error Amplifier Phase vs. Error Amplifier Input Frequency



Error Amplifier Voltage Gain vs. Ambient Temperature

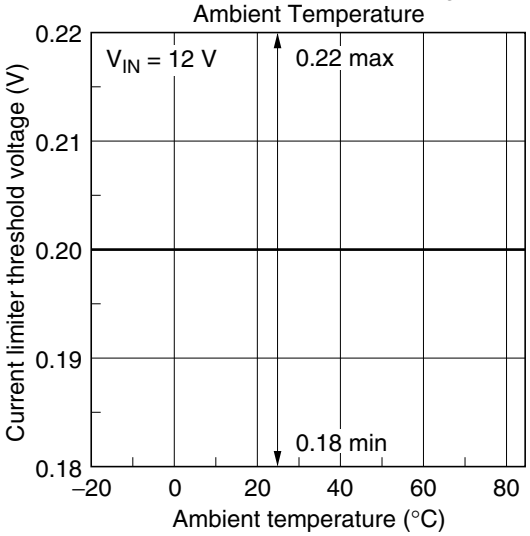


Current Limiter Turn-Off Time vs. Current Limiter Threshold Voltage Note

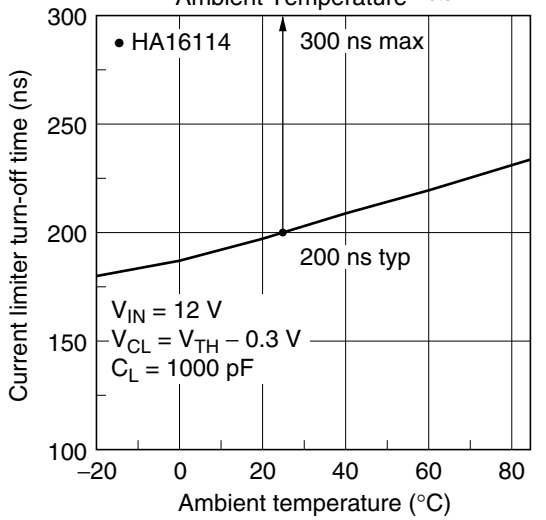


Note: Approximatery 300 ns greater than this in the case of the HA16120.

Current Limiter Threshold Voltage vs. Ambient Temperature

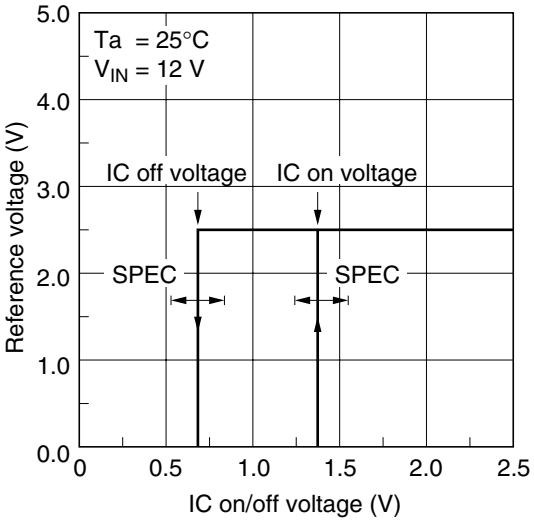


Current Limiter Turn-Off Time vs. Ambient Temperature Note

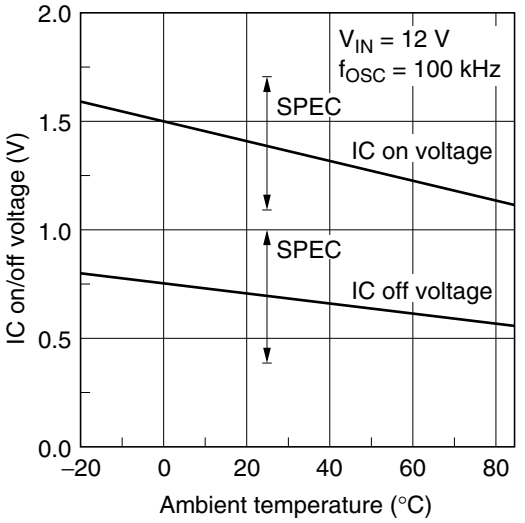


Note: Approximatery 300 ns greater than this in the case of the HA16120.

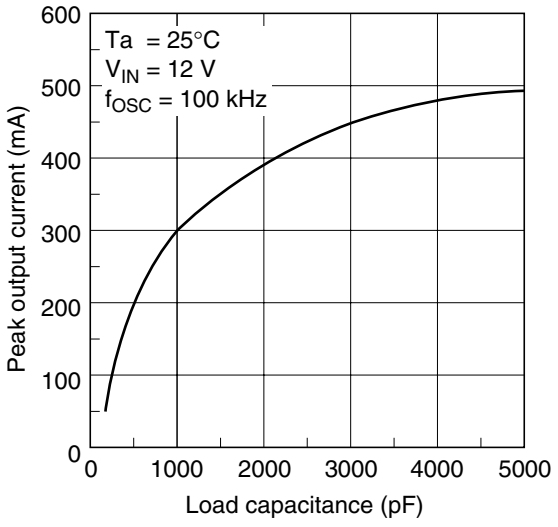
Reference Voltage vs. IC On/Off Voltages



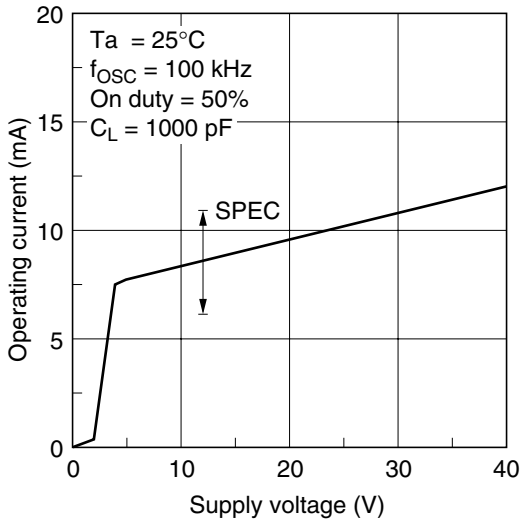
IC On/Off Voltages vs. Ambient Temperature



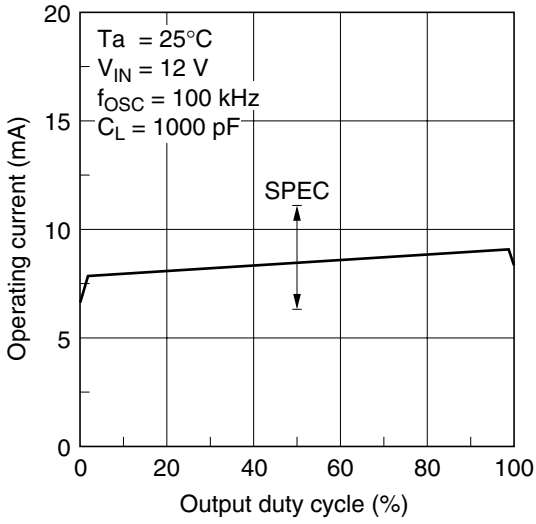
Peak Output Current vs. Load Capacitance



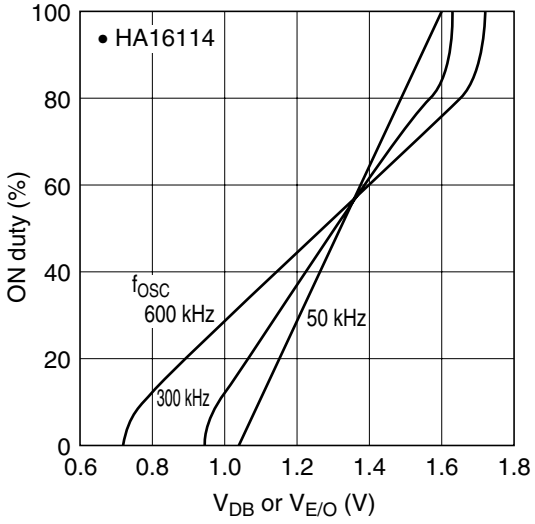
Operating Current vs. Supply Voltage



Operating Current vs. Output Duty Cycle

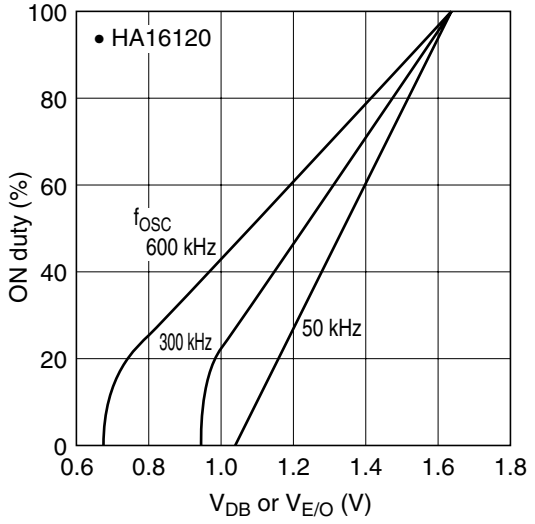


PWM Comparator Input vs. Output Duty Cycle (1)

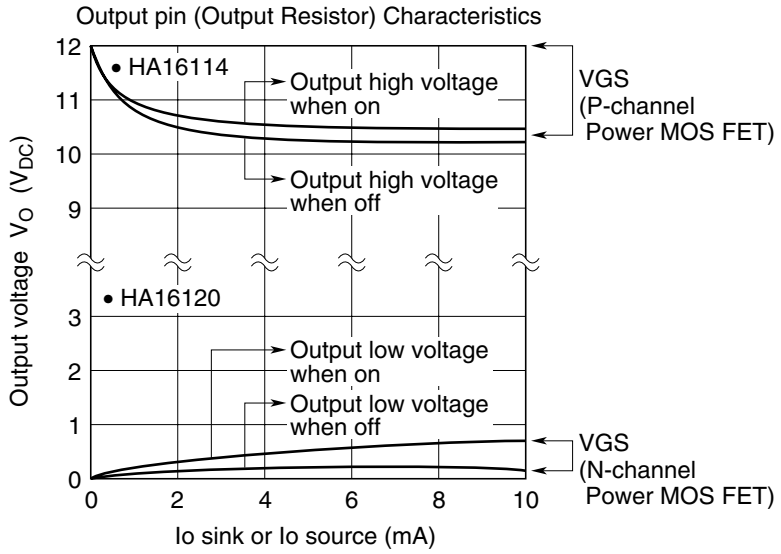


Note: The on-duty of the HA16114 is the proportion of one cycle during which output is low.

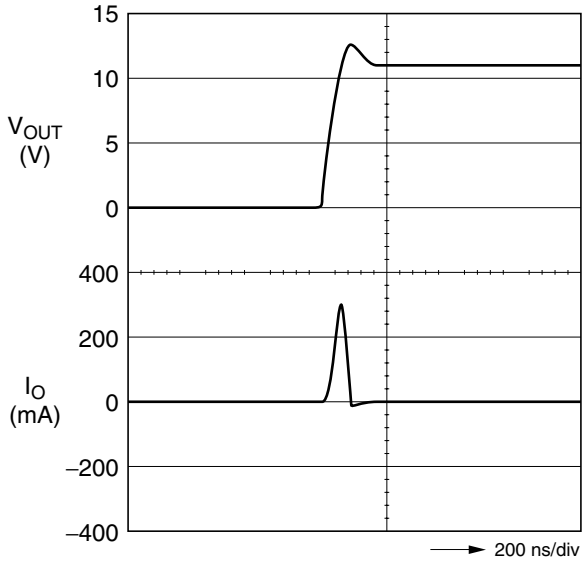
PWM Comparator Input vs. Output Duty Cycle (2)

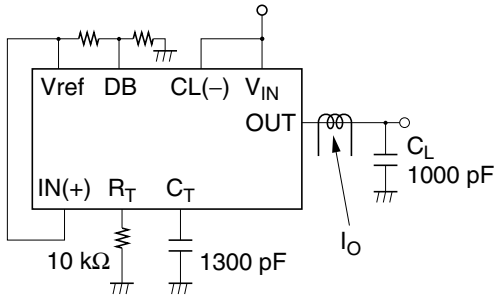


Note: The on-duty of the HA16120 is the proportion of one cycle during which output is high.


Output pin (Output Resistor) Characteristics
12
11
10
9
3
2
1
0
• HA16114
• HA16120
Output high voltage when on
Output high voltage when off
Output low voltage when on
Output low voltage when off
VGS (P-channel Power MOS FET)
VGS (N-channel Power MOS FET)
Output voltage V_O (V_{DC})
0
2
4
6
8
10
Io sink or Io source (mA)

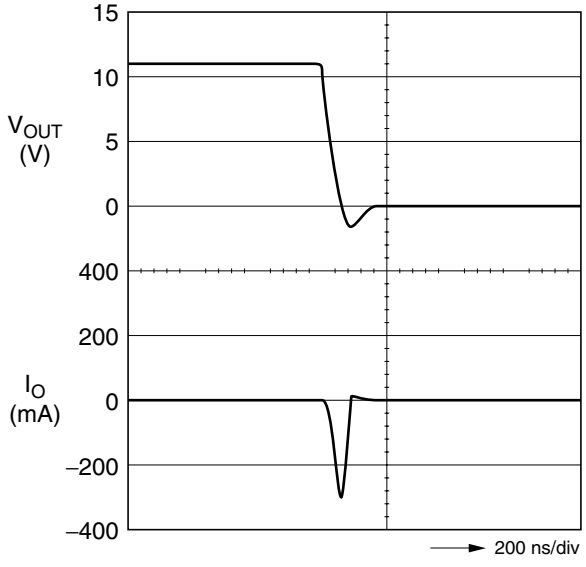
Output Waveforms: Rise of Output Voltage V_{OUT}

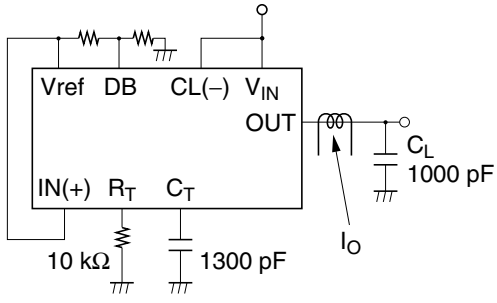




Test Circuit

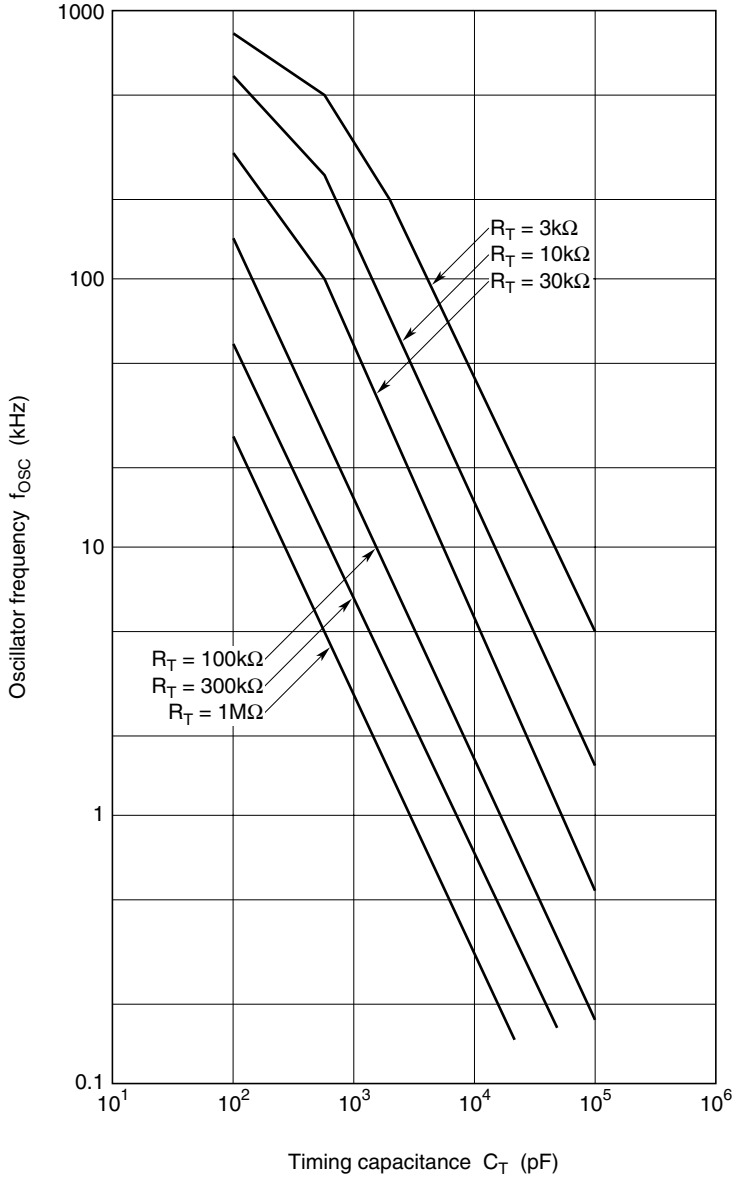
Output Waveforms: Fall of Output Voltage V_{OUT}



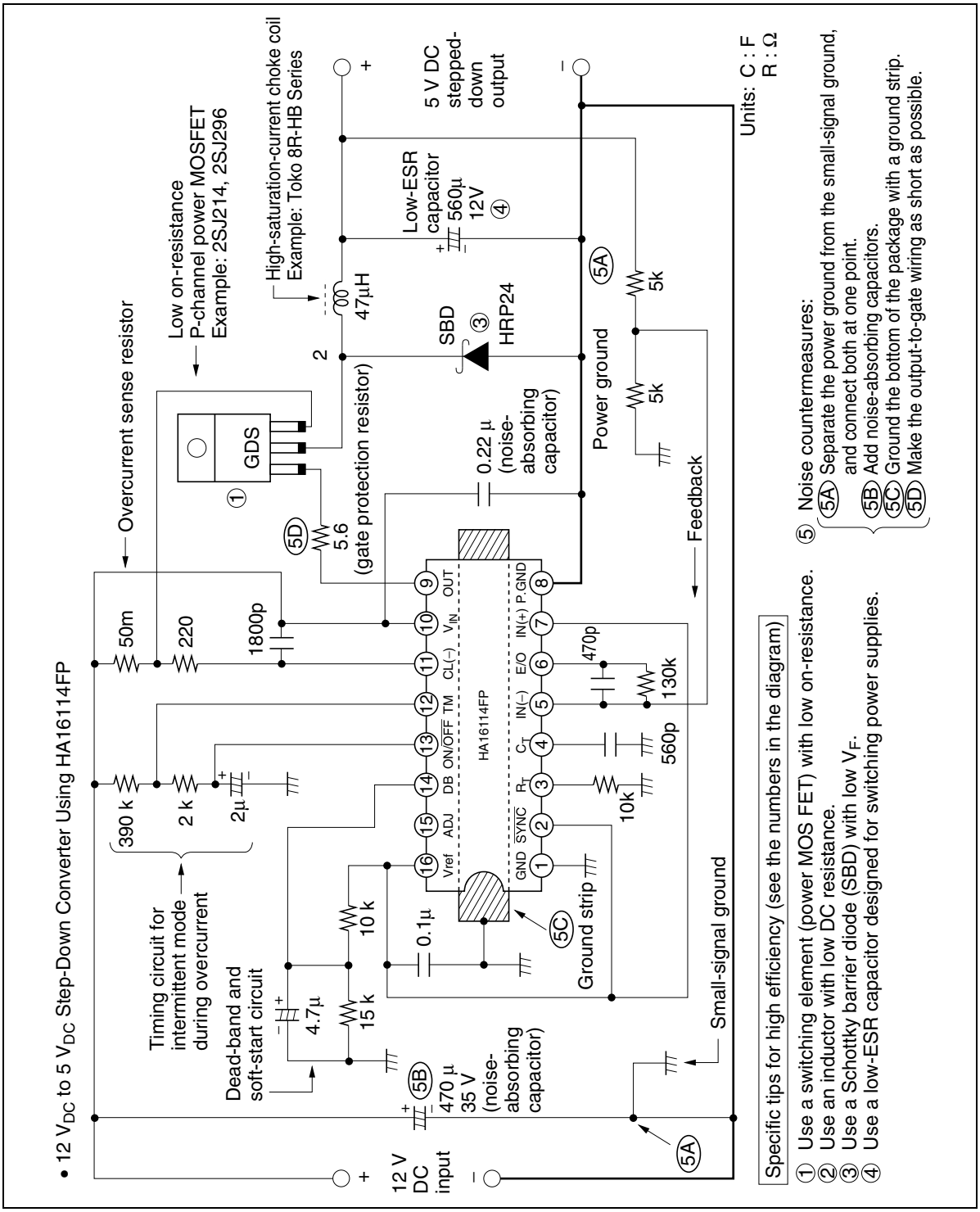


Test Circuit

Oscillator Frequency vs. Timing Capacitance



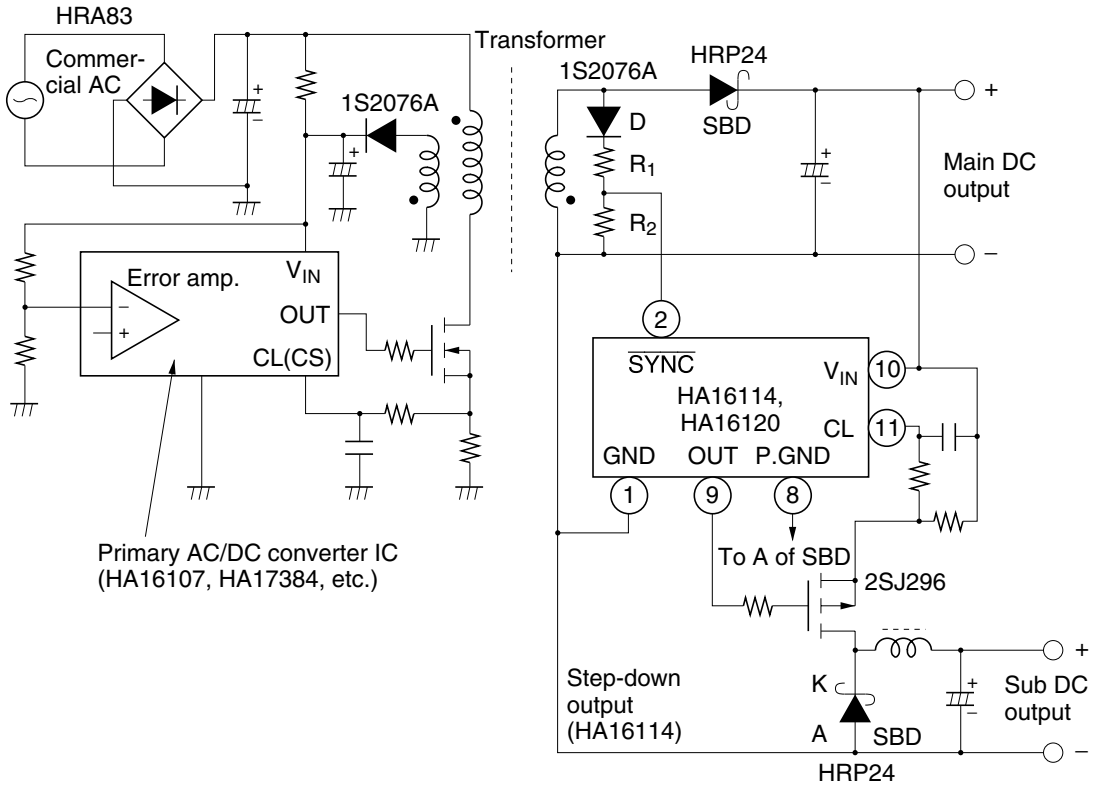
Application Examples (1)



Application Examples (2)

- External Synchronization with Primary-Control AC/DC Converter

  (1) Combination with a flyback AC/DC converter (simplified schematic)



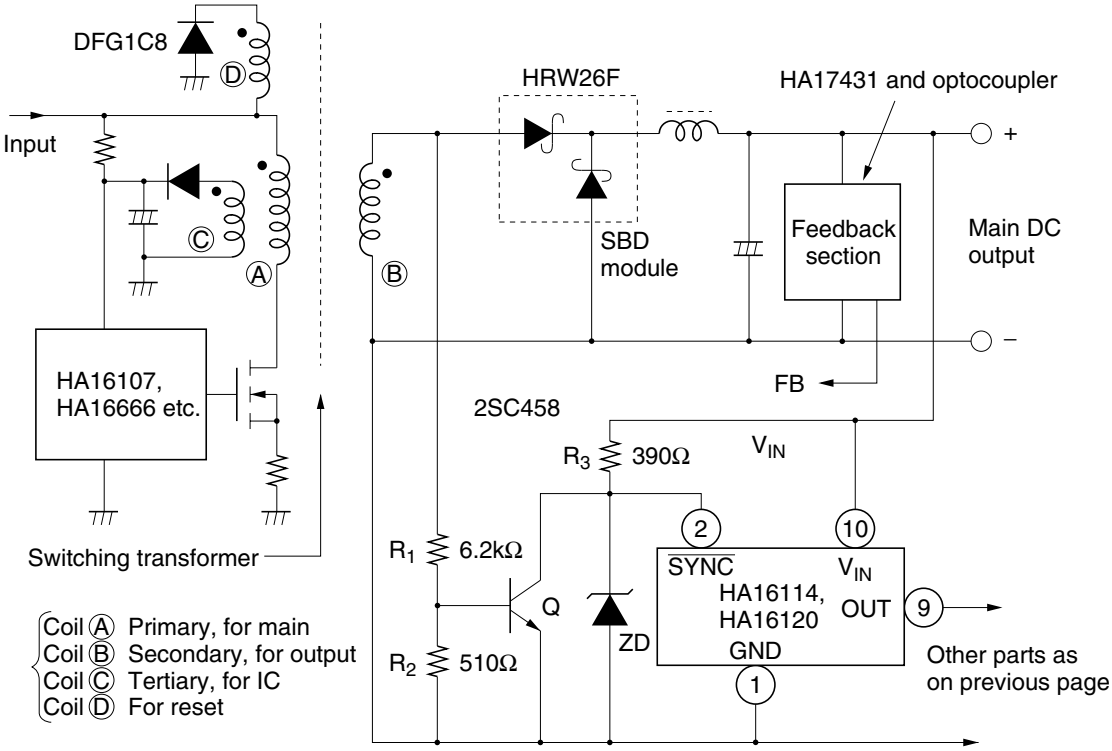
This is one example of a circuit that uses the features of the HA16114/120 by operating in synchronization with a flyback AC/DC converter. Note the following design points concerning the circuit from the secondary side of the transformer to the $\overline{\text{SYNC}}$ pin of the HA16114/120.

- Diode D prevents reverse current. Always insert a diode here. Use a general-purpose switching diode.
- Resistors R_1 and R_2 form a voltage divider to ensure that the input voltage swing at the $\overline{\text{SYNC}}$ pin does not exceed Vref (2.5 V). To maintain operating speed, $R_1 + R_2$ should not exceed 10 kΩ.

Application Examples (3)

• External Synchronization with Primary-Control AC/DC Converter (cont.)

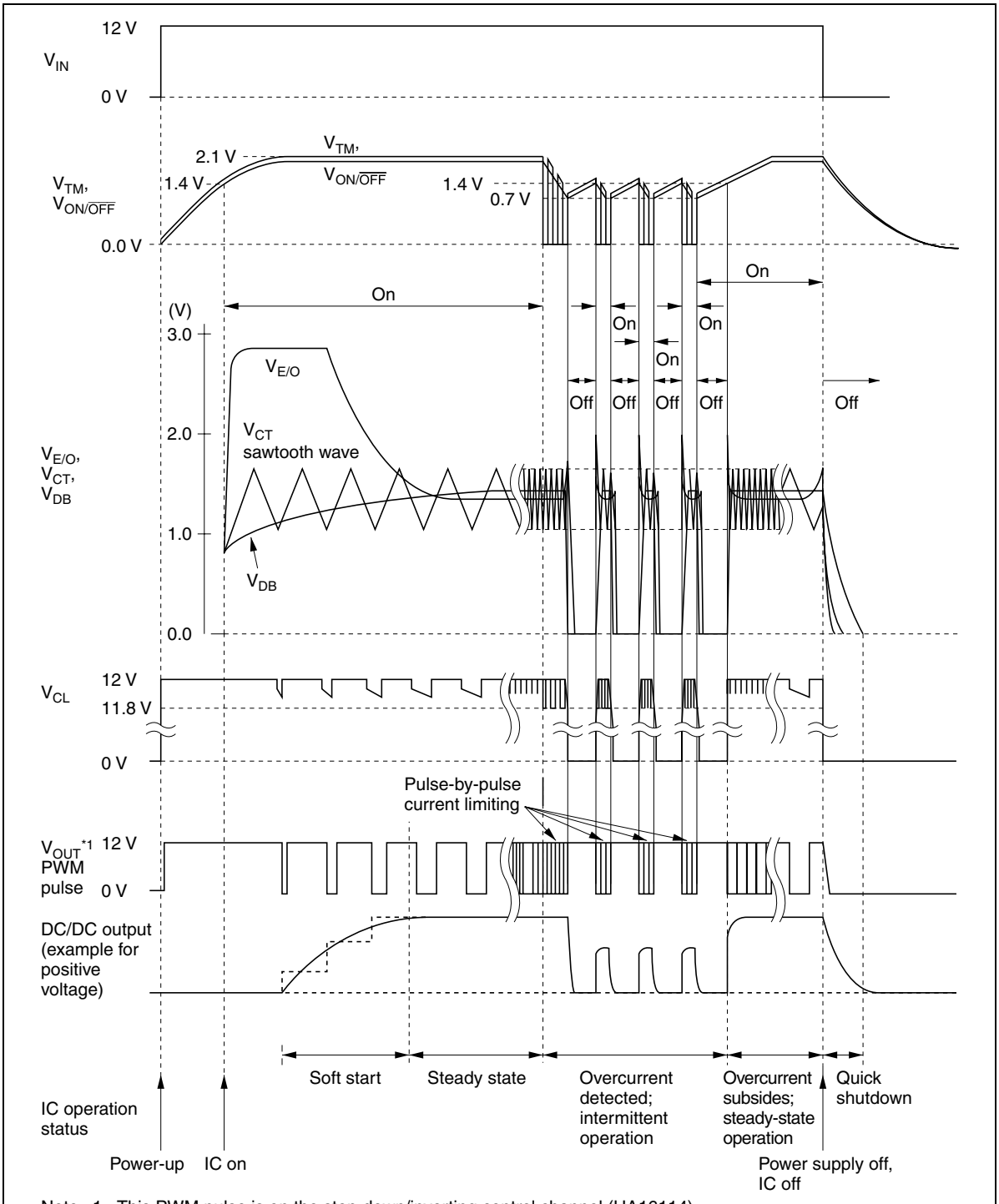
(2) Combination with a forward AC/DC converter (simplified schematic)



This circuit illustrates the combination of the HA16114/120 with a forward AC/DC converter. The HA16114/120 synchronizes with the falling edge of the external sync signal, so with a forward transformer, the sync pulses must be inverted. In the diagram, this is done by an external circuit consisting of the following components:

- Q: Transistor for inverting the pulses. Use a small-signal transistor.
- R_1 and R_2: These resistors form a voltage divider for driving the base of transistor Q. R_2 also provides a path for base discharge, so that the transistor can turn off quickly.
- R_3: Load resistor for transistor Q.
- ZD: Zener diode for protecting the $\overline{\text{SYNC}}$ pin.

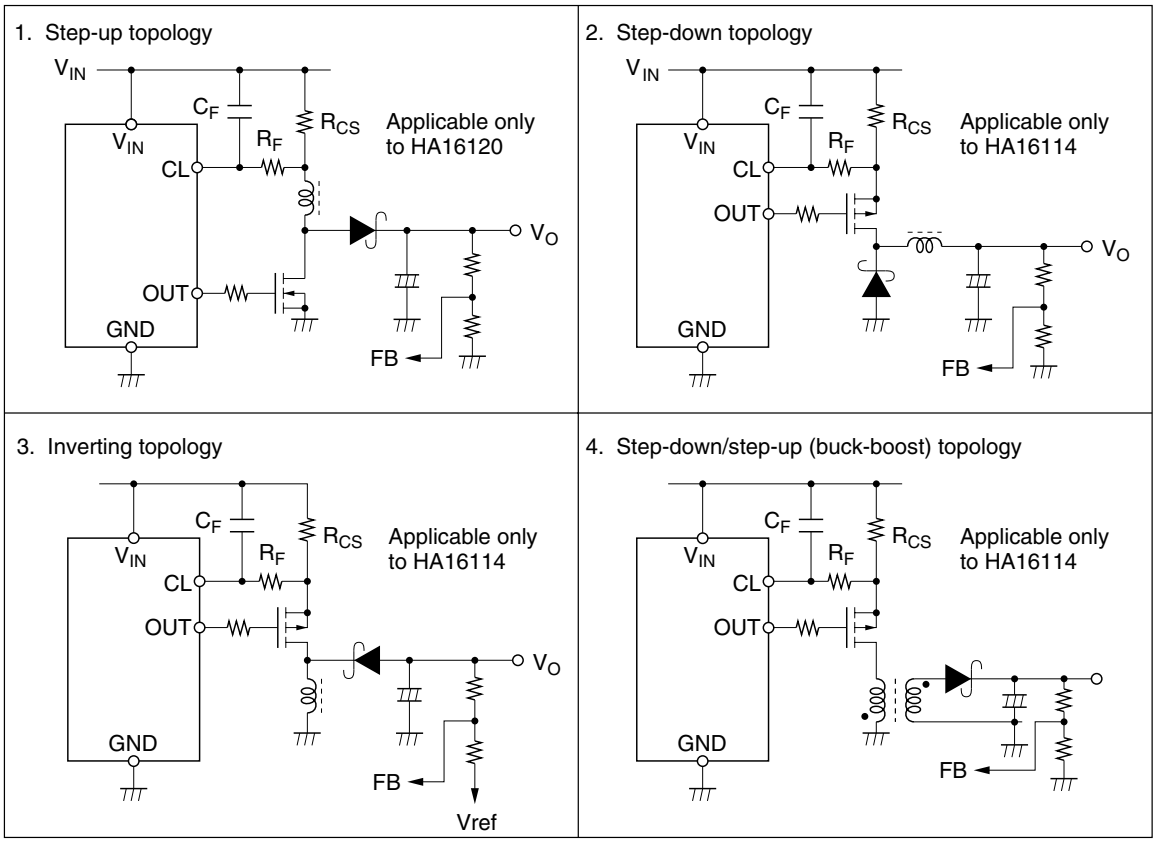
Overall Waveform Timing Diagram (for Application Example (1))



Note: 1. This PWM pulse is on the step-down/inverting control channel (HA16114).
The booster control channel (HA16120) output consists of alternating L and H of the IC on cycle.

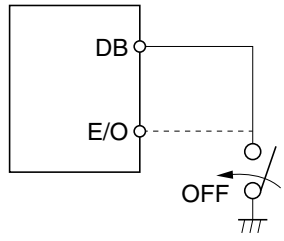
Application Examples (4) (Some Pointers on Use)

1. Inductor, Power MOS FET, and Diode Connections



2. Turning Output On and Off while the IC is On

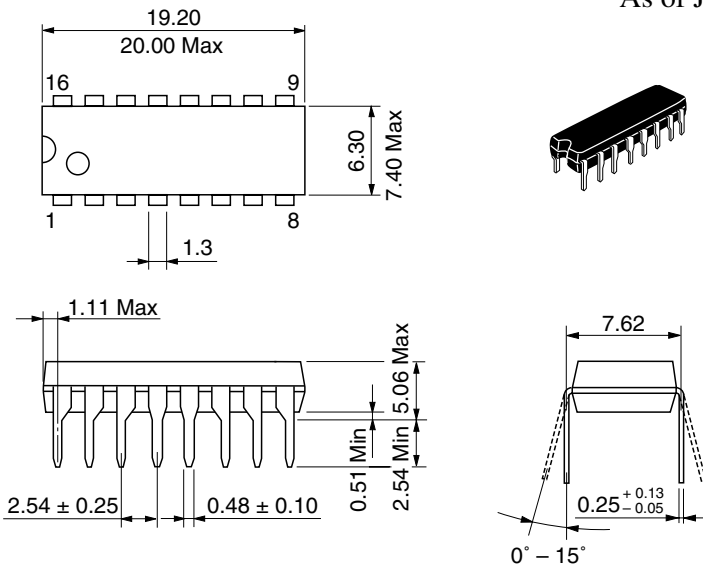
To turn only one channel off, ground the DB pin or the E/O pin.
In the case of E/O, however, there will be no soft start
when the output is turned back on.



Package Dimensions

As of January, 2002

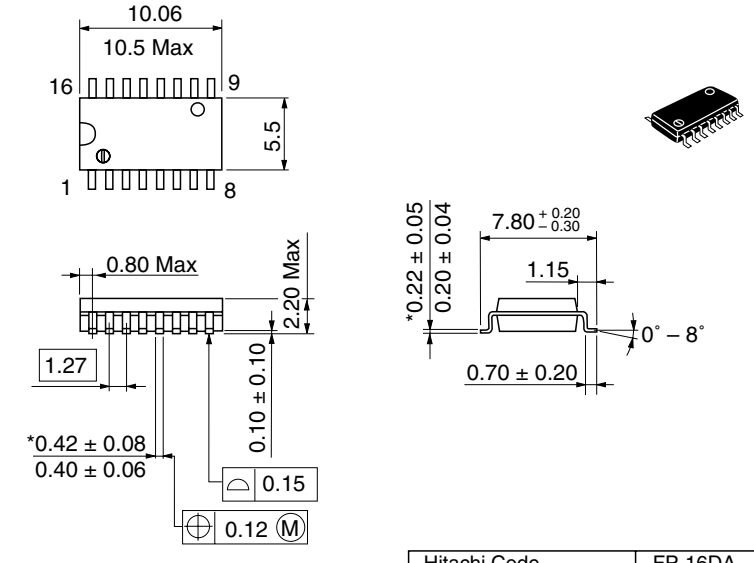
Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.07 g

As of January, 2002

Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Dimension including the plating thickness

Base material dimension

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