

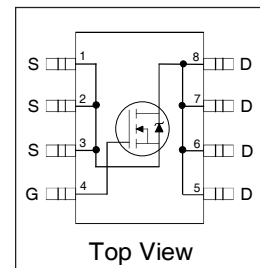
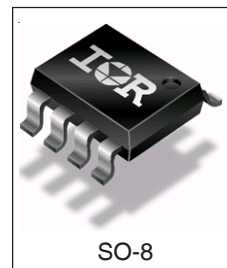
- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications
- 100% Tested for R_G

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRF7809AV has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and C_{dv}/dt -induced turn-on immunity. The IRF7809AV offers particularly low $R_{DS(on)}$ and high C_{dv}/dt immunity for synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.



DEVICE CHARACTERISTICS^⑤

	IRF7809AV
$R_{DS(on)}$	7.0m Ω
Q_G	41nC
Q_{sw}	14nC
Q_{oss}	30nC

Absolute Maximum Ratings

Parameter	Symbol	IRF7809A V	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain or Source Current ($V_{GS} \geq 4.5V$)	$T_A = 25^\circ C$	I_D	A
	$T_L = 90^\circ C$		
Pulsed Drain Current ^①	I_{DM}	100	
Power Dissipation	$T_A = 25^\circ C$	P_D	W
	$T_L = 90^\circ C$		
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$
Continuous Source Current (Body Diode)	I_S	2.5	A
Pulsed Source Current ^①	I_{SM}	50	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient ^③	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Lead	$R_{\theta JL}$	20	$^\circ C/W$

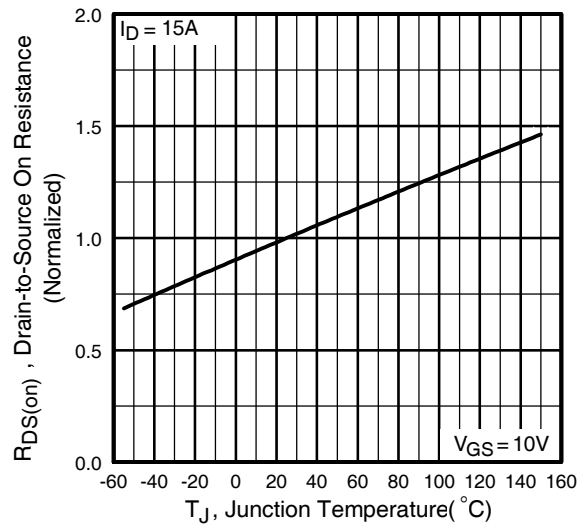
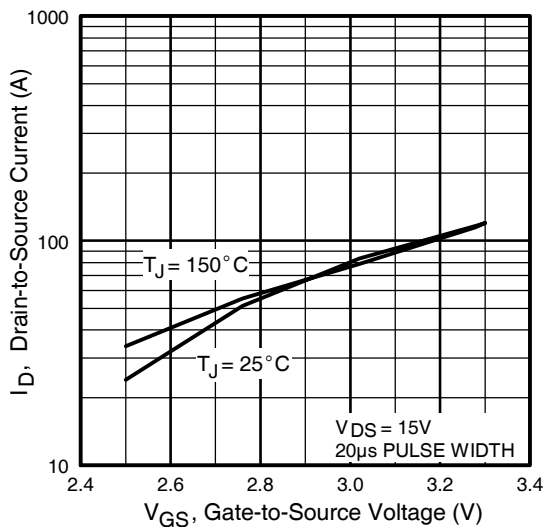
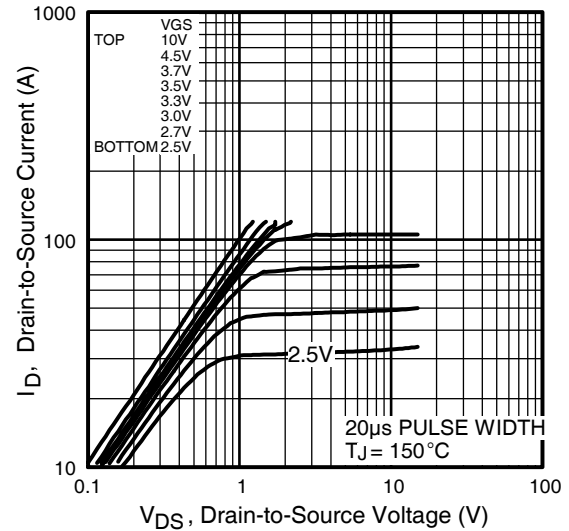
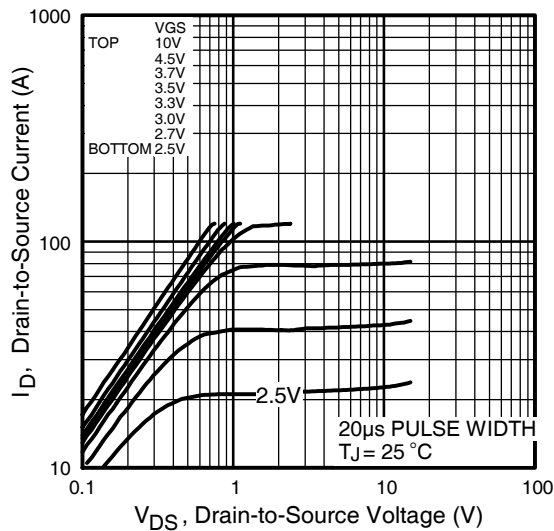
Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source on Resistance	$R_{DS(on)}$		7.0	9.0	m Ω	$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	I_{DSS}			30	μA	$V_{DS} = 24V, V_{GS} = 0$
				150		$V_{DS} = 24V, V_{GS} = 0,$ $T_J = 100^\circ C$
Gate-Source Leakage Current*	I_{GSS}			± 100	nA	$V_{GS} = \pm 12V$
Total Gate Chg Cont FET	Q_G		41	62	nC	$V_{GS}=5V, I_D=15A, V_{DS}=20V$
Total Gate Chg Sync FET	Q_G		36	54		$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}		7.0			$V_{DS} = 20V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}		2.3			
Gate to Drain Charge	Q_{GD}		12			$I_D=15A, V_{DS}=16V$
Switch Chg($Q_{GS2} + Q_{GD}$)	Q_{SW}		14	21		
Output Charge*	Q_{OSS}		30	45		$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	R_G		1.5	3.0	Ω	
Turn-on Delay Time	$t_{d(on)}$		14		ns	$V_{DD} = 16V, I_D = 15A$
Rise Time	t_r		36			$V_{GS} = 5V$
Turn-off Delay Time	$t_{d(off)}$		96			Clamped Inductive Load
Fall Time	t_f		10			
Input Capacitance	C_{iss}	—	3780	—	pF	$V_{DS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	—	1060	—		
Reverse Transfer Capacitance	C_{rss}	—	130	—		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.3	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge④	Q_{rr}		120		nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		150		nC	$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$

- Notes:**
- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
 - ③ When mounted on 1 inch square copper board, $t < 10$ sec.
 - ④ Typ = measured - Q_{OSS}
 - ⑤ Typical values measured at $V_{GS} = 4.5V, I_F = 15A$.



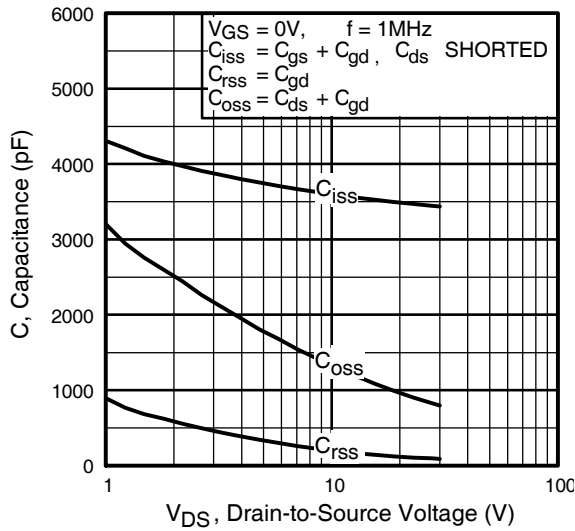


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

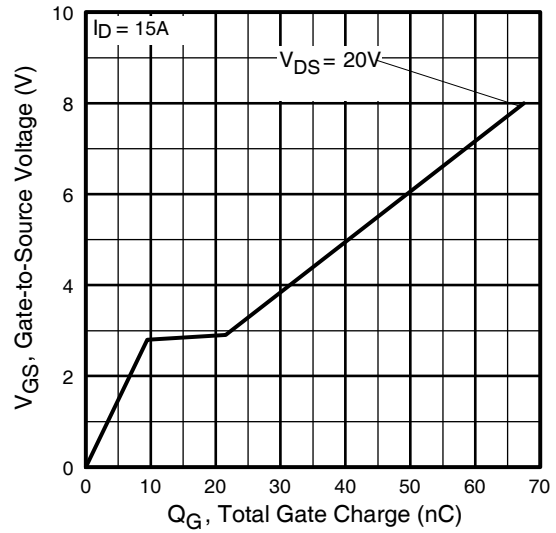


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

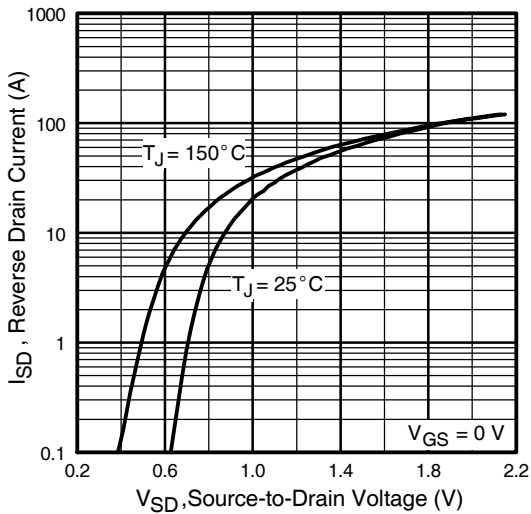


Fig 7. Typical Source-Drain Diode Forward Voltage

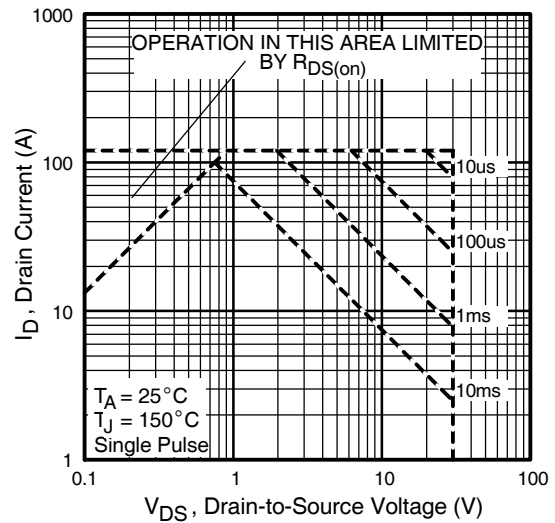


Fig 8. Maximum Safe Operating Area

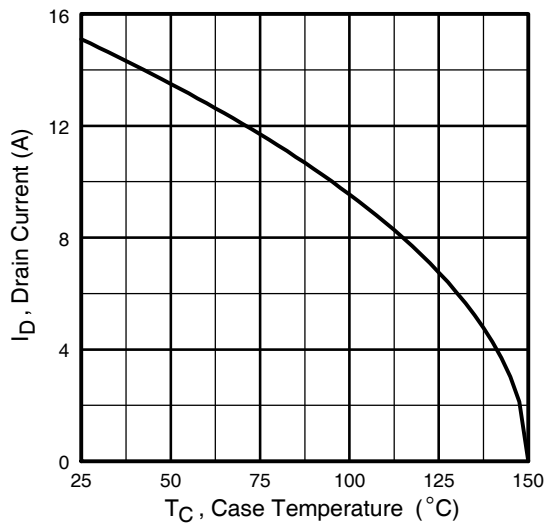


Fig 9. Maximum Drain Current Vs. Case Temperature

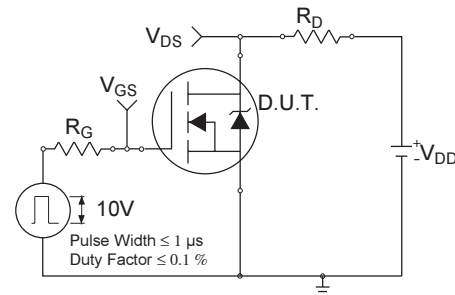


Fig 10a. Switching Time Test Circuit

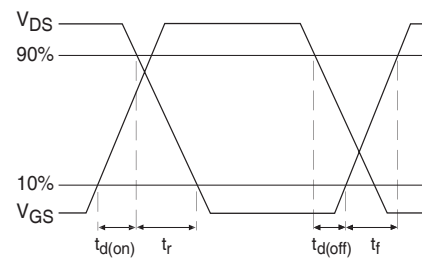


Fig 10b. Switching Time Waveforms

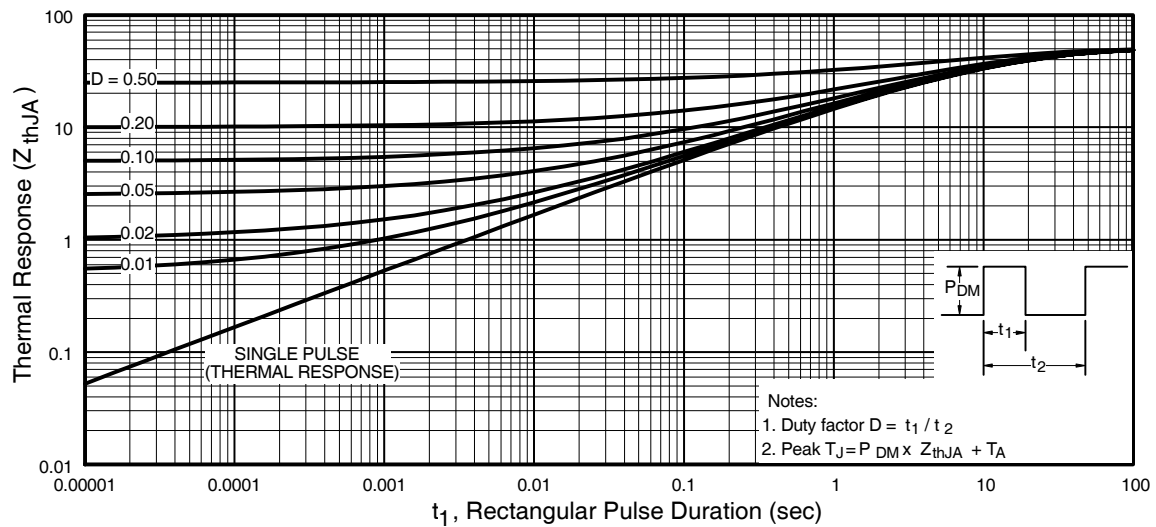


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

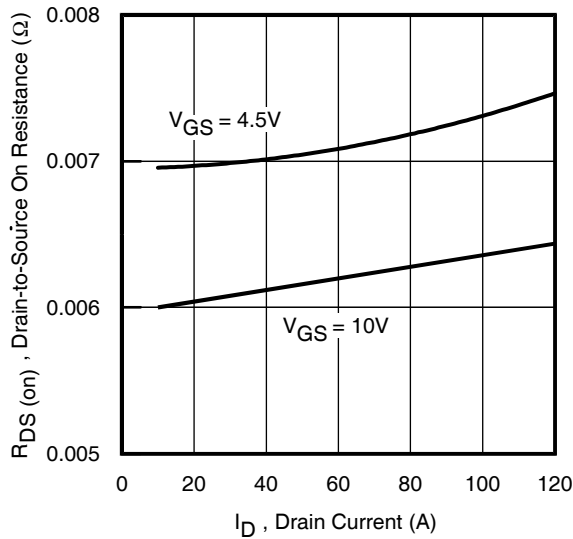


Fig 12. On-Resistance Vs. Drain Current

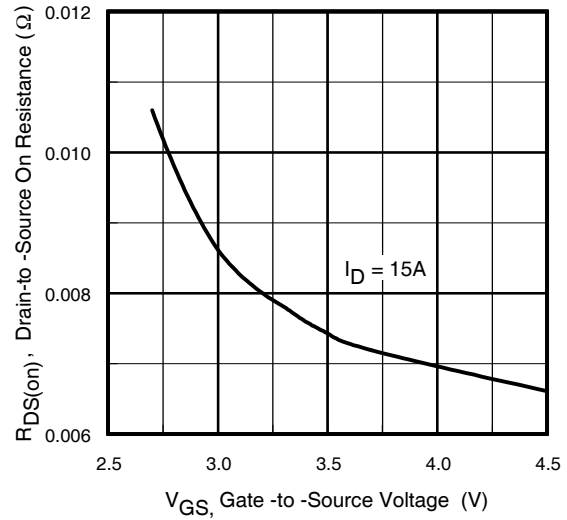


Fig 13. On-Resistance Vs. Gate Voltage

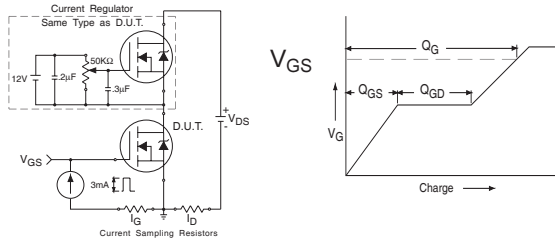


Fig 13a&b. Basic Gate Charge Test Circuit and Waveform

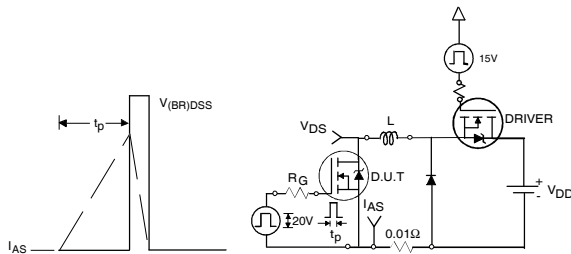


Fig 14a&b. Unclamped Inductive Test circuit and Waveforms

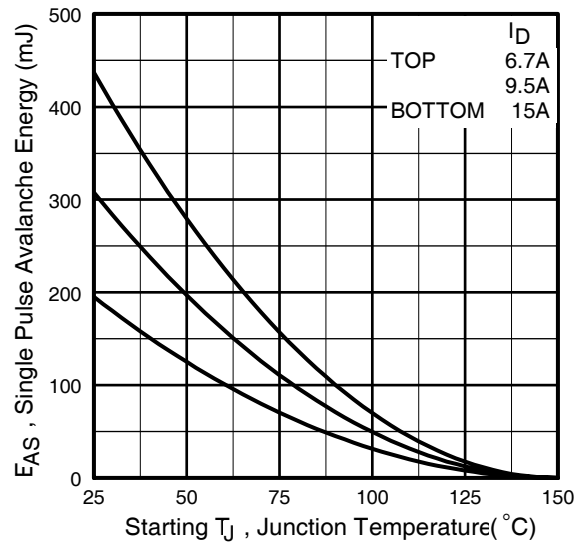
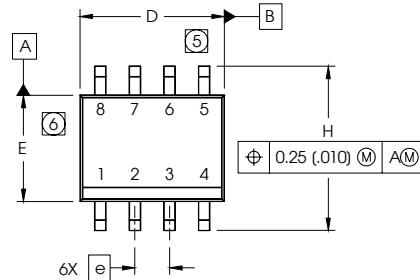
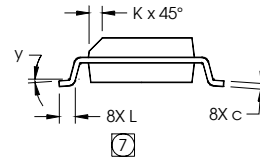
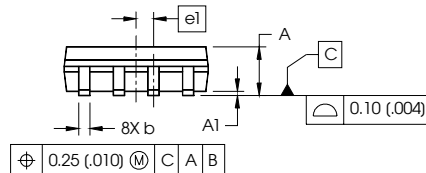


Fig 14c. Maximum Avalanche Energy Vs. Drain Current

SO-8 Package Details



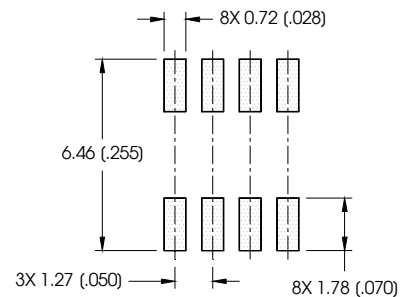
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

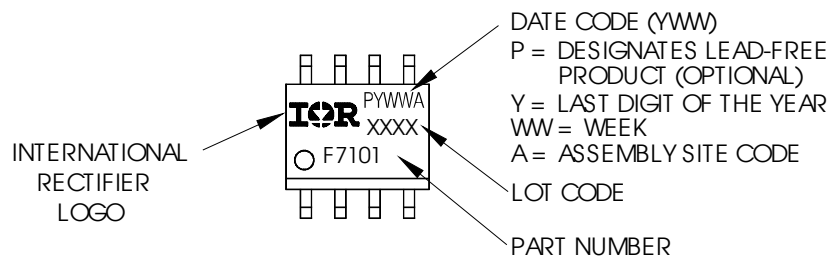
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

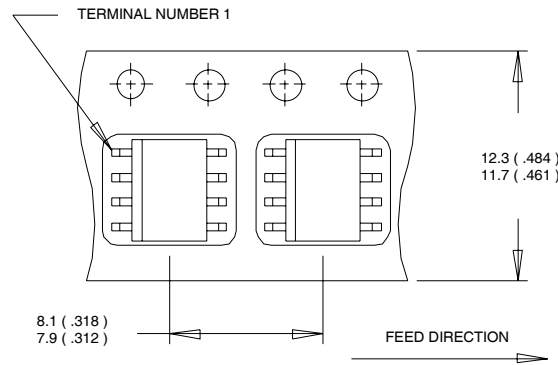
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



IRF7809AV

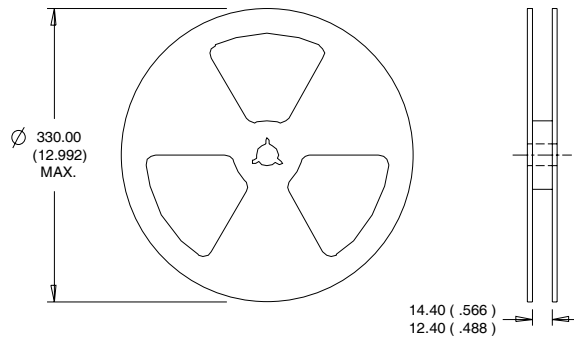
International
IOR Rectifier

SO-8 Tape and Reel



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
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