

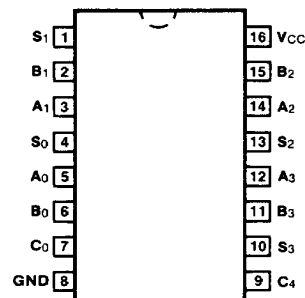
✓✓ 54/74283 010004  
 ✓ 54LS/74LS283 010006  
**4-BIT BINARY FULL ADDER**  
 (With Fast Carry)

**DESCRIPTION** — The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words ( $A_0$  —  $A_3$ ,  $B_0$  —  $B_3$ ) and a Carry input ( $C_0$ ). They generate the binary Sum outputs ( $S_0$  —  $S_3$ ) and the Carry output ( $C_4$ ) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74283PC, 74LS283PC		9B
Ceramic DIP (D)	A	74283DC, 74LS283DC	54283DM, 54LS283DM	6B
Flatpak (F)	A	74283FC, 74LS283FC	54283FM, 54LS283FM	4L

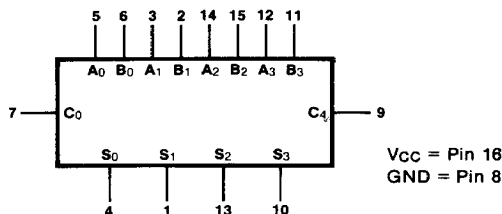
**CONNECTION DIAGRAM**  
PINOUT A



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0$ — $A_3$	A Operand Inputs	1.0/1.0	1.0/0.5
$B_0$ — $B_3$	B Operand Inputs	1.0/1.0	1.0/0.5
$C_0$	Carry Input	1.0/1.0	0.5/0.25
$S_0$ — $S_3$	Sum Outputs	20/10	10/5.0 (2.5)
$C_4$	Carry Output	10/5.0	10/5.0 (2.5)

**LOGIC SYMBOL**



**FUNCTIONAL DESCRIPTION** — The '283 adds two 4-bit binary words (A plus B) plus the incoming carry  $C_0$ . The binary sum appears on the Sum ( $S_0 - S_3$ ) and outgoing carry ( $C_4$ ) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus  $C_0$ ,  $A_0$ ,  $B_0$  can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if  $C_0$  is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	$C_0$	$A_0$	$A_1$	$A_2$	$A_3$	$B_0$	$B_1$	$B_2$	$B_3$	$S_0$	$S_1$	$S_2$	$S_3$	$C_4$
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH:  $0 + 10 + 9 = 3 + 16$

Active LOW:  $1 + 5 + 6 = 12 + 0$

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $S_3$  dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure b* shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $S_2$ ) is used merely as a means of getting a carry ( $C_{10}$ ) signal into the fourth stage (via  $A_2$  and  $B_2$ ) and bringing out the carry from the second stage on  $S_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, whether HIGH or LOW, they do not influence  $S_2$ . Similarly, when  $A_2$  and  $B_2$  are the same the carry into the third stage does not influence the carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1 - I_5$  that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1 - I_5$  are true, the output  $M_5$  is true.

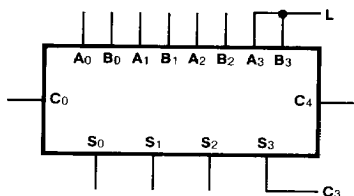


Fig. a 3-Bit Adder

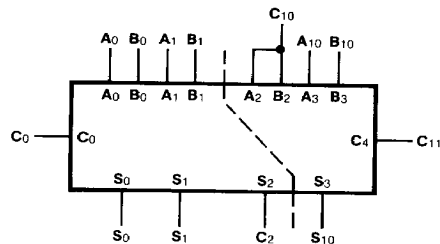


Fig. b 2-Bit and 1-Bit Adders

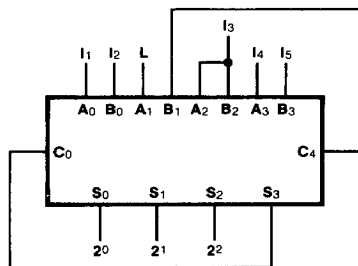


Fig. c 5-Input Encoder

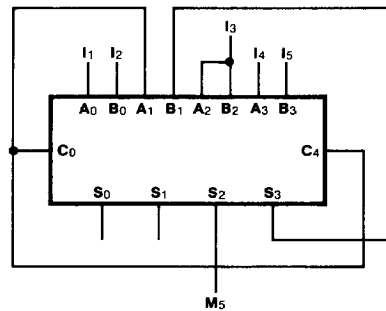
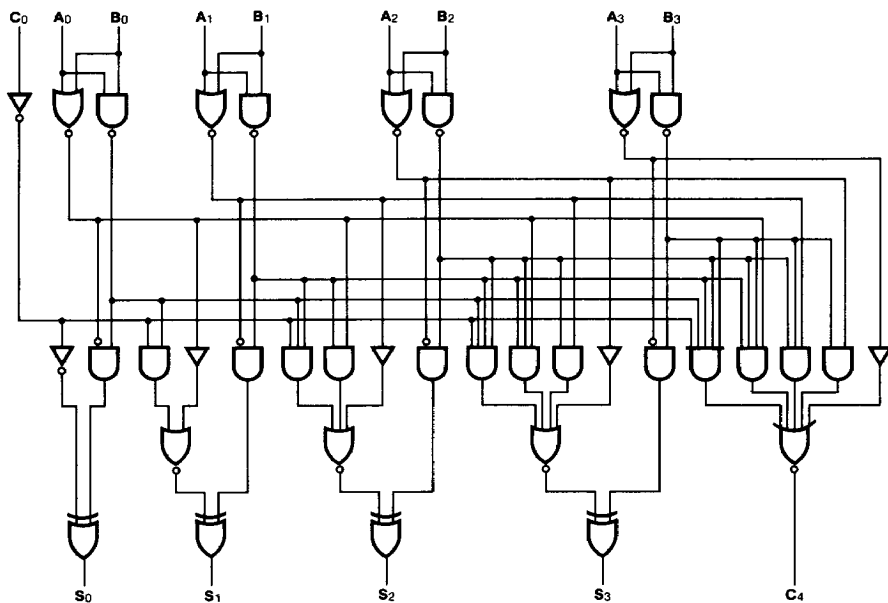


Fig. d 5-Input Majority Gate

## LOGIC DIAGRAM



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I <sub>OS</sub>	Output Short Circuit Current at S <sub>n</sub>	XM	-20	-55	-20	-100	mA	V <sub>CC</sub> = Max
		XC	-18	-55	-20	-100		
I <sub>OS</sub>	Output Short Circuit Current at C <sub>4</sub>	XM	-20	-70	-20	-100	mA	V <sub>CC</sub> = Max
		XC	-18	-70	-20	-100		
I <sub>CC</sub>	Power Supply Current	XM	99		39		mA	V <sub>CC</sub> = Max, Inputs = Gnd ('LS283) Inputs = 4.5 V ('283)
		XC	110		39			
		XM, XC			34		mA	V <sub>CC</sub> = Max Inputs = 4.5 V ('LS283)

**AC CHARACTERISTICS:** V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>0</sub> to S <sub>n</sub>	21 21		24 24		ns	Figs. 3-1, 3-20
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	24 24		24 24		ns	Figs. 3-1, 3-20
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>0</sub> to C <sub>4</sub>	14 16		17 17		ns	Figs. 3-1, 3-5 R <sub>L</sub> = 780 Ω ('283)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	14 16		17 17		ns	Figs. 3-1, 3-5 R <sub>L</sub> = 780Ω ('283)