

CTLSH1-40M832D
SURFACE MOUNT
DUAL, HIGH CURRENT, LOW V_F
SILICON SCHOTTKY DIODES



Top View



Bottom View

TLM832D CASE

MARKING CODE: CFA

CentralTM

Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLSH1-40M832D Dual, Isolated, Low V_F Schottky diodes are designed for applications where small size and operational efficiency are the prime requirements. With a maximum power dissipation of 1.65W, and a very small package footprint (approximately equal to the SOT-23), this leadless package design is capable of dissipating up to 4 times the power of similar devices in comparable sized surface mount packages.

FEATURES:

- Dual Chip Device
- High Current ($I_F=1.0A$)
- Low Forward Voltage Drop ($V_F=0.55V$ MAX @ 1.0A)
- High Thermal Efficiency
- Small TLM 3x2mm case

APPLICATIONS:

- DC/DC Converters
- Reverse Battery Protection
- Battery Powered Portable Equipment

MAXIMUM RATINGS: ($T_A=25^\circ C$)

Peak Repetitive Reverse Voltage
Continuous Forward Current
Peak Repetitive Forward Current, $t_p \leq 1ms$
Forward Surge Current, $t_p=8ms$
Power Dissipation
Operating and Storage
Junction Temperature
Thermal Resistance

SYMBOL

V_{RRM}	40
I_F	1.0
I_{FRM}	3.5
I_{FSM}	10
P_D	1.65
T_J, T_{stg}	-65 to +150
θ_{JA}	75.8

UNITS

V
A
A
A
W*
$^\circ C$
$^\circ C/W^*$

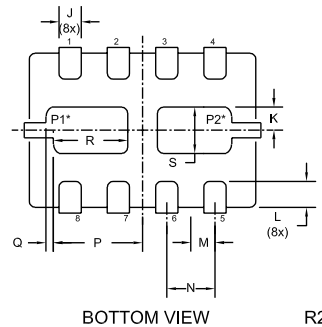
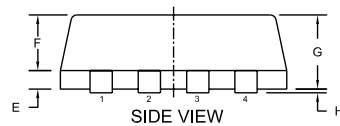
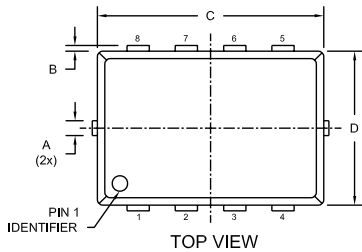
ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ C$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_R	$V_R=5V$			10	μA
I_R	$V_R=8V$			20	μA
I_R	$V_R=15V$			50	μA
BV_R	$I_R=100\mu A$	40			V
V_F	$I_F=10mA$			0.29	V
V_F	$I_F=100mA$			0.36	V
V_F	$I_F=500mA$			0.45	V
V_F	$I_F=1.0A$			0.55	V
C_J	$V_R=4.0V, f=1.0MHz$		50		pF

*FR-4 Epoxy PCB with copper mounting pad area of 54mm²

R2 (27-April 2006)

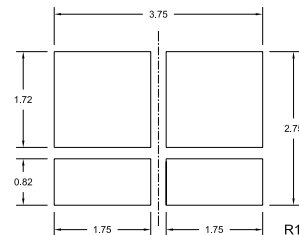
TLM832D CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

Suggested mounting pad layout
for maximum power dissipation
(Dimensions in mm)



For standard mounting refer
to TLM832D Package Details

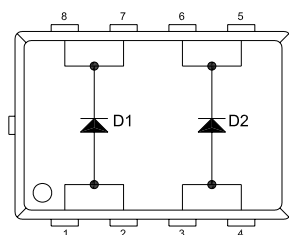
* Note:

- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6

LEAD CODE:

- 1) ANODE D1
- 2) ANODE D1
- 3) ANODE D2
- 4) ANODE D2
- 5) CATHODE D2
- 6) CATHODE D2
- 7) CATHODE D1
- 8) CATHODE D1

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