# WM9714L

## *AC'97 Audio Codec*

## DESCRIPTION

The WM9714L is a highly integrated input/output device designed for mobile computing and communications.

The chip is architected for dual CODEC operation, supporting hi-fi stereo CODEC functions via the AC link interface, and additionally supporting voice CODEC functions via a PCM type Synchronous Serial Port (SSP). A third, auxiliary DAC is provided which may be used to support generation of supervisory tones, or ring-tones at different sample rates to the main CODEC.

The device can connect directly to mono or stereo microphones, stereo headphones and a stereo speaker, reducing total component count in the system. Cap-less connections to the headphones, speakers, and earpiece may be used, saving cost and board area. Additionally, multiple analogue input and output pins are provided for seamless integration with analogue connected wireless communication devices.

All device functions are accessed and controlled through a single AC-Link interface compliant with the AC'97 standard. The 24.576 MHz master clock can be input directly or generated internally from a 13MHz (or other frequency) clock by an on-chip PLL. The PLL supports a wide range of input clock from 2.048MHz to 78.6MHz.

The WM9714L operates at supply voltages from 1.8V to 3.6V. Each section of the chip can be powered down under software control to save power. The device is available in a small leadless 7x7mm QFN package, ideal for use in hand-held portable systems.

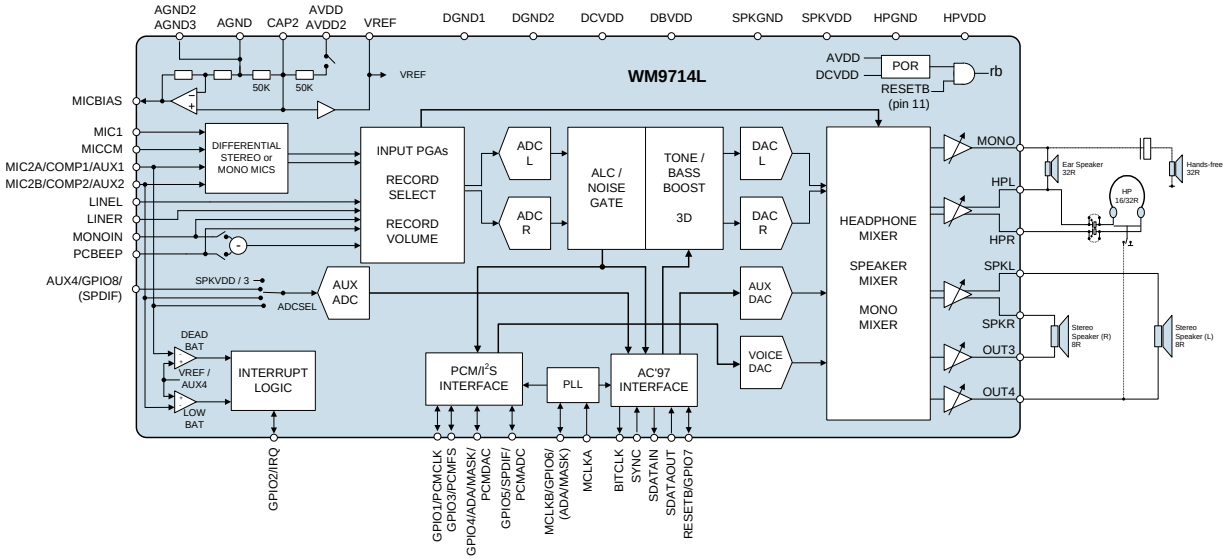
## FEATURES

- AC'97 Rev 2.2 compatible stereo CODEC
  - DAC SNR 94dB, THD –85dB
  - ADC SNR 87dB, THD –86dB
  - Variable Rate Audio, supports all WinCE sample rates
  - Tone Control, Bass Boost and 3D Enhancement
- On-chip 45mW headphone driver
- On-chip 400mW mono or stereo speaker drivers
- Stereo, mono or differential microphone input
  - Automatic Level Control (ALC)
  - Mic insert and mic button press detection
- Auxiliary mono DAC (ring tone or DC level generation)
- Seamless interface to wireless chipset
- Additional PCM/I$^2$S interface to support voice CODEC
- PLL derived audio clocks.
- Supports input clock ranging from 2.048MHz to 78.6MHz
- 1.8V to 3.6V supplies (digital down to 1.62V, speaker up to 4.2V)
- 7x7mm 48-lead QFN package

## APPLICATIONS

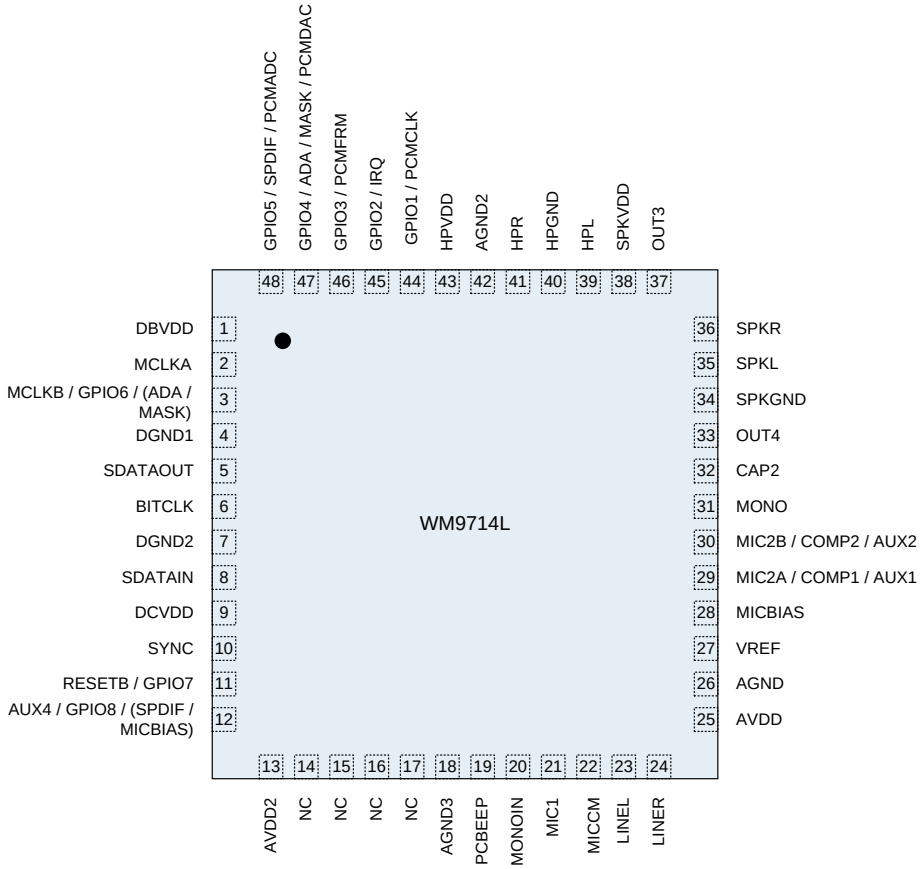
- Smartphones
- Personal Digital Assistants (PDA)
- Handheld and Tablet Computers

## BLOCK DIAGRAM



## TABLE OF CONTENTS

## PIN CONFIGURATION




## ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---|---|---|---|---|
| WM9714CLGEFL/V | -25 to +85°C | 48-lead QFN (Pb-free) | MSL3 | 260°C |
| WM9714CLGEFL/RV | -25 to +85°C | 48-lead QFN (Pb-free, tape and reel) | MSL3 | 260°C |

**Note:**

Reel quantity = 2,200

## PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | DBVDD | Supply | Digital I/O Buffer Supply |
| 2 | MCLKA | Digital Input | Master Clock A Input |
| 3 | MCLKB / GPIO6 / (ADA / MASK) | Digital In/Out | Master Clock B Input / GPIO6 / (ADA output / MASK input) |
| 4 | DGND1 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 5 | SDATAOUT | Digital Input | Serial Data Output from Controller / Input to WM9714L |
| 6 | BITCLK | Digital Output | Serial Interface Clock Output to Controller |

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 7 | DGND2 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 8 | SDATAIN | Digital Output | Serial Data Input to Controller / Output from WM9714L |
| 9 | DCVDD | Supply | Digital Core Supply |
| 10 | SYNC | Digital Input | Serial Interface Synchronisation Pulse from Controller |
| 11 | RESETB / GPIO7 | Digital In / Out | Reset (asynchronous, active Low, resets all registers to their default) / GPIO7 |
| 12 | AUX4 / GPIO8 / (S/PDIF) | Analogue In / Out | Auxiliary ADC input / GPIO8 / (S/PDIF digital audio output) |
| 13 | AVDD2 | Supply | Analogue Supply |
| 14 | NC | Analogue Input | Do not connect |
| 15 | NC | Analogue Input | Do not connect |
| 16 | NC | Analogue Input | Do not connect |
| 17 | NC | Analogue Input | Do not connect |
| 18 | AGND3 | Supply | Analogue Ground |
| 19 | PCBEEP | Analogue Input | Line Input to analogue audio mixers, typically used for beeps |
| 20 | MONOIN | Analogue Input | Mono Input (RX) |
| 21 | MIC1 | Analogue Input | Microphone preamp A input 1 |
| 22 | MICCM | Analogue Input | Microphone common mode input |
| 23 | LINEL | Analogue Input | Left Line Input |
| 24 | LINER | Analogue Input | Right Line Input |
| 25 | AVDD | Supply | Analogue Supply (audio DACs, ADCs, PGAs, mic amps, mixers) |
| 26 | AGND | Supply | Analogue Ground |
| 27 | VREF | Analogue Output | Internal Reference Voltage (buffered CAP2) |
| 28 | MICBIAS | Analogue Output | Bias Voltage for Microphones (buffered CAP2 × 1.8) |
| 29 | MIC2A / COMP1 / AUX1 | Analogue Input | Microphone preamp A input 2 / COMP1 input / Auxiliary ADC input |
| 30 | MIC2B / COMP2 / AUX2 | Analogue Input | Microphone preamp B input / COMP2 input / Auxiliary ADC input |
| 31 | MONO | Analogue output | Mono output driver (line or headphone) |
| 32 | CAP2 | Analogue In / Out | Internal Reference Voltage (normally AVDD/2, if not overdriven) |
| 33 | OUT4 | Analogue Output | Auxiliary output driver (speaker, line or headphone) |
| 34 | SPKGND | Supply | Speaker ground (feeds output buffers on pins 33, 35, 36 and 37) |
| 35 | SPKL | Analogue Output | Left speaker driver (speaker, line or headphone) |
| 36 | SPKR | Analogue Output | Right speaker driver (speaker, line or headphone) |
| 37 | OUT3 | Analogue Output | Auxiliary output driver (speaker, line or headphone) |
| 38 | SPKVDD | Supply | Speaker supply (feeds output buffers on pins 33, 35, 36 and 37) |
| 39 | HPL | Analogue Output | Headphone left driver (line or headphone) |
| 40 | HPGND | Supply | Headphone ground (feeds output buffers on pins 39 and 41) |
| 41 | HPR | Analogue Output | Headphone right driver (line or headphone) |
| 42 | AGND2 | Supply | Analogue ground, chip substrate |
| 43 | HPVDD | Supply | Headphone supply (feeds output buffers on pins 39 and 41) |
| 44 | GPIO1 / PCMCLK | Digital In / Out | GPIO Pin 1 / PCM interface clock |
| 45 | GPIO2 / IRQ | Digital In / Out | GPIO Pin 2 / IRQ (Interrupt Request) output |
| 46 | GPIO3 / PCMFS | Digital In / Out | GPIO Pin 3 / PCM frame signal |
| 47 | GPIO4 / ADA / MASK / PCMDAC | Digital In / Out | GPIO Pin 4 / ADA (ADC data available) output or Mask input / PCM input (DAC) data |
| 48 | GPIO5 / S/PDIF / PCMADC | Digital In / Out | GPIO Pin 5 / S/PDIF digital audio output / PCM output (ADC) data |
| 49 | GND_PADDLE | | Die Paddle (Note 1) |

**Notes:**

1. It is recommended that the GND_PADDLE is connected to analogue ground. Refer to “Recommended External Components” and “Package Dimensions” for further information.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|---|---|
| Digital supply voltages (DCVDD, DBVDD) | -0.3V | +3.63V |
| Analogue supply voltages (AVDD, AVDD2, HPVDD) | -0.3V | +3.63V |
| Speaker supply voltage (SPKVDD) | -0.3V | +4.2V |
| Voltage range digital inputs | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Operating temperature range, $T_A$ | -25ºC | +85ºC |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Digital input/output buffer supply range | DBVDD | | 1.71 | 3.3 | 3.6 | V |
| Digital core supply range | DCVDD | | 1.71 | 1.8 | 3.6 | V |
| Analogue supply range | AVDD, AVDD2, HPVDD | | 1.8 | 3.3 | 3.6 | V |
| Speaker supply range | SPKVDD | | 1.8 | 3.3 | 4.2 | V |
| Digital ground | DGND1, DGND2 | | | 0 | | V |
| Analogue ground | AGND, AGND3, HPGND, SPKGND | | | 0 | | V |
| Difference AGND to DGND | | Note 1 | -0.3 | 0 | +0.3 | V |

**Note:**

1. AGND is normally the same as DGND1/DGND2
2. DCVDD <= DBVDD and DCVDD <= AVDD
3. DCVDD should be >=2V when using the PLL

# ELECTRICAL CHARACTERISTICS

## AUDIO OUTPUTS

**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD=HPVDD=SPKVDD =3.3V, $T_A$ = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DAC to Line-Out (HPL/R, SPKL/R or MONO with 10kΩ / 50pF load)** | | | | | | |
| Full-scale output (0dBFS) | | AVDD = 3.3V, PGA gains set to 0dB | | 1 | | V rms |
| Signal to Noise Ratio (A-weighted) | SNR | | 85 | 94 | | dB |
| Total Harmonic Distortion | THD | -3dB output | | -85 | -74 | dB |
| Power Supply Rejection | PSRR | 100mV, 20Hz to 20kHz signal on AVDD | | 50 | | dB |
| **Speaker Output (SPKL/SPKR with 8Ω bridge tied load, INV=1)** | | | | | | |
| Output Power at 1% THD | $P_O$ | THD = 1% | | 400 | | mW (rms) |
| Abs. max output power | $P_O$max | | | 500 | | mW (rms) |
| Total Harmonic Distortion | THD | $P_O$ = 200mW | | -66<br>0.05 | | dB<br>% |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |
| **Stereo Speaker Output (SPKL/OUT4 and SPKR/OUT3 with 8Ω bridge tied load, INV=1)** | | | | | | |
| Output Power at 1% THD | $P_O$ | THD = 1% | | 400 | | mW (rms) |
| Abs. max output power | $P_O$max | | | 500 | | mW (rms) |
| Total Harmonic Distortion | THD | $P_O$ = 200mW | | -66<br>0.05 | | dB<br>% |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |
| **Headphone Output (HPL/R, OUT3/4 or SPKL/SPKR with 16Ω or 32Ω load)** | | | | | | |
| Output Power per channel | $P_O$ | Output power is very closely correlated with THD; see below. | | | | |
| Total Harmonic Distortion | THD | $P_O$=10mW, $R_L$=16Ω | | -80 | | dB |
| | | $P_O$=10mW, $R_L$=32Ω | | -80 | | |
| | | $P_O$=20mW, $R_L$=16Ω | | -78 | | |
| | | $P_O$=20mW, $R_L$=32Ω | | -79 | | |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |

**Note:**

1. All THD values are valid for the output power level quoted above – for example, at HPVDD=3.3V and $R_L$=16Ω, THD is –80dB when output power is 10mW. Higher output power is possible, but will result in deterioration in THD.

## AUDIO INPUTS

**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LINEL/R, MIC1/2A/2B, MONOIN and PCBEEP pins** | | | | | | |
| Full Scale Input Signal Level (0dBFS) | $V_{INFS}$ | AVDD = 3.3V | | 1.0 | | Vrms |
| | | AVDD = 1.8V | | 0.545 | | |
| | | differential input mode (MS = 01) AVDD = 3.3V | | 0.5 | | |
| | | differential input mode (MS = 01) AVDD = 1.8V | | 0.273 | | |
| Input Resistance | $R_{IN}$ | 0dB PGA gain | 25.6 | 32 | 38.4 | kΩ |
| | | 12dB PGA gain | 10.4 | 13 | 15.6 | |
| Input Capacitance | | | | 5 | | pF |
| **Line input to ADC (LINEL, LINER, MONOIN)** | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | | 80 | 87 | | dB |
| Total Harmonic Distortion | THD | -3dBFS input | | -86 | -80 | dB |
| Power Supply Rejection | PSRR | 20Hz to 20kHz | | 50 | | dB |
| **Microphone input to ADC (MIC1/2A/2B pins)** | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | 20dB boost enabled | | 80 | | dB |
| Total Harmonic Distortion | THD | 20dB boost enabled | | -80 | | dB |

## AUXILIARY MONO DAC (AUXDAC)

**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Resolution | | | | 12 | | bits |
| Full scale output voltage | | AVDD=3.3V | | 1 | | Vrms |
| Signal to Noise Ratio (A-weighted) | SNR | | | TBD | | dB |
| Total Harmonic Distortion | THD | | | TBD | | dB |

## PCM VOICE DAC (VXDAC)

**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Resolution | | | | 16 | | bits |
| Sample rates | | | | 8 | 16 | Ks/s |
| Full scale output voltage | | AVDD=3.3V | | 1 | | Vrms |
| Signal to Noise Ratio (A-weighted) | SNR | | | 80 | | dB |
| Total Harmonic Distortion | THD | | | 74 | | dB |

## AUXILIARY ADC

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Input Pins AUX4, COMP1/AUX1, COMP2/AUX2** | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | AUX pin not selected as AUX ADC input | | <10 | | nA |
| ADC Resolution | | | | 12 | | bits |
| Differential Non-Linearity Error | DNL | | | ±0.25 | ±1 | LSB |
| Integral Non-Linearity Error | INL | | | | ±2 | LSB |
| Offset Error | | | | | ±4 | LSB |
| Gain Error | | | | | ±6 | LSB |
| Power Supply Rejection | PSRR | | | 50 | | dB |
| Channel-to-channel isolation | | | | 80 | | dB |
| Throughput Rate | | DEL = 1111 (zero settling time) | | | 48 | kHz |
| Settling Time (programmable) | | MCLK = 24.576MHz | 0 | | 6 | ms |

## COMPARATORS

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **COMP1/AUX1 and COMP2/AUX2 (pins 29, 30 – when not used as mic inputs)** | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | pin not selected as AUX ADC input | | <10 | | nA |
| Comparator Input Offset (COMP1, COMP2 only) | | | -50 | | +50 | mV |
| COMP2 delay (COMP2 only) | | MCLK = 24.576MHz | 0 | | 10.9 | s |

## REFERENCE VOLTAGES

**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Audio ADCs, DACs, Mixers** | | | | | | |
| Reference Input/Output | CAP2 pin | | 1.63 | 1.65 | 1.66 | V |
| Buffered Reference Output | VREF pin | | 1.64 | 1.65 | 1.67 | V |
| **Microphone Bias** | | | | | | |
| Bias Voltage | $V_{MICBIAS}$ | | 2.92 | 2.97 | 3.00 | V |
| Bias Current Source | $I_{MICBIAS}$ | | | | 3 | mA |
| Output Noise Voltage | Vn | 1K to 20kHz | | 15 | | nV/√Hz |

## DIGITAL INTERFACE CHARACTERISTICS

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, $T_A$ = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Logic Levels (all digital input or output pins) – CMOS Levels** | | | | | | |
| Input HIGH level | $V_{IH}$ | | DBVDD×0.7 | | | V |
| Input LOW level | $V_{IL}$ | | | | DBVDD×0.3 | V |
| Output HIGH level | $V_{OH}$ | source current = 2mA | DBVDD×0.9 | | | |
| Output LOW level | $V_{OL}$ | sink current = 2mA | | | DBVDD×0.1 | |
| **Clock Frequency** | | | | | | |
| Master clock (MCLKA pin) | | | | 24.576 | | MHz |
| AC'97 bit clock (BIT_CLK pin) | | | | 12.288 | | MHz |
| AC'97 sync pulse (SYNC pin) | | | | 48 | | kHz |

**Note:**

1. All audio and non-audio sample rates and other timing scales proportionately with the master clock.
2. For signal timing on the AC-Link, please refer to the AC'97 specification (Revision 2.2)

## POWER CONSUMPTION

The power consumption of the WM9714L depends on the following factors:

- Supply voltages: Reducing the supply voltages also reduces digital supply currents, end therefore results in significant power savings especially in the digital sections of the WM9714L.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM9714L that are not used (e.g. audio ADC, DAC, AUXADC).
- Sample rates: Running at lower sample rates will reduce power consumption significantly. The figures below are for 48kHz (unless otherwise specified), but in many scenarios it is not necessary to run at this frequency, e.g. 8kHz PCM voice call scenario uses only 11.4mW (see below).

| MODE DESCRIPTION | AVDD Supply Current V / mA | | DCVDD Supply Current V / mA | | DBVDD Supply Current V / mA | | Total Power (mW) |
|---|---|---|---|---|---|---|---|
| Off (lowest possible power)<br>Clocks stopped. This is the default configuration after power-up. | 3.3 | 0.01 | 3.3 | 0 | 3.3 | 0.005 | 0.05 |
| LPS (Low Power Standby)<br>VREF maintained using 1MOhm string | 3.3 | 0.014 | 3.3 | 0 | 3.3 | 0.005 | 0.06 |
| PCM Voice call (fs=8kHz) | 2.8 | 2.37 | 2.8 | 1.7 | 2.8 | 0.006 | 11.4 |
| Record from mono microphone | 3.3 | 3.644 | 3.3 | 10.973 | 3.3 | 2.974 | 58.05 |
| Stereo DAC Playback (AC link to headphone) | 3.3 | 3.733 | 3.3 | 9.720 | 3.3 | 2.789 | 53.60 |
| Stereo DAC Playback (AC link to headphone)<br>PLL running with 13MHz input to MCLKB | 3.3 | 4.801 | 3.3 | 10.504 | 3.3 | 2.814 | 59.79 |
| Maximum Power - everything on | 3.3 | 13.656 | 3.3 | 15.472 | 3.3 | 2.938 | 105.82 |

**Table 1 Supply Current Consumption**

**Notes:**

1. Unless otherwise specified, all figures are at TA = +25C, audio sample rate fs = 48kHz, with zero signal (quiescent), and voltage references settled.
2. The power dissipated in headphones and speakers is not included in the above table.

## SIGNAL TIMING REQUIREMENTS

### AC97 INTERFACE TIMING

#### CLOCK SPECIFICATIONS

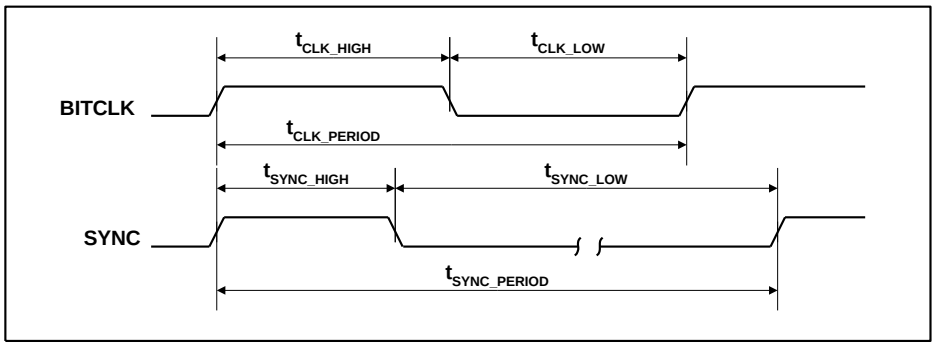



**Figure 1 Clock Specifications (50pF External Load)**

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, $T_A$ = -25°C to +85°C, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| BITCLK frequency | | | 12.288 | | MHz |
| BITCLK period | $t_{CLK\_PERIOD}$ | | 81.4 | | ns |
| BITCLK output jitter | | | | 750 | ps |
| BITCLK high pulse width (Note 1) | $t_{CLK\_HIGH}$ | 36 | 40.7 | 45 | ns |
| BITCLK low pulse width (Note 1) | $t_{CLK\_LOW}$ | 36 | 40.7 | 45 | ns |
| SYNC frequency | | | 48 | | kHz |
| SYNC period | $t_{SYNC\_PERIOD}$ | | 20.8 | | µs |
| SYNC high pulse width | $t_{SYNC\_HIGH}$ | | 1.3 | | µs |
| SYNC low pulse width | $t_{SYNC\_LOW}$ | | 19.5 | | µs |

**Note:**

1. Worst case duty cycle restricted to 45/55

## DATA SETUP AND HOLD

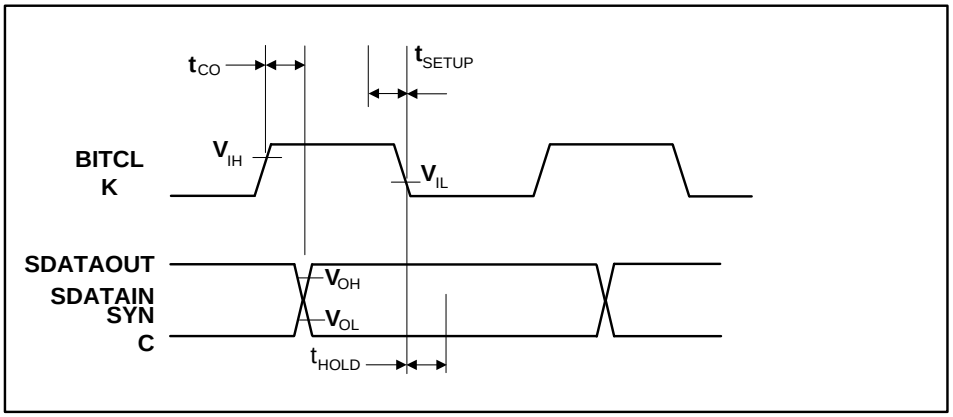



**Figure 2 Data Setup and Hold (50pF External Load)**

**Note:**

Setup and hold times for SDATAIN are with respect to the AC'97 controller, not the WM9713L.

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, $T_A$ = -25°C to +85°C, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Setup to falling edge of BITCLK | $t_{SETUP}$ | 10 | | | ns |
| Hold from falling edge of BITCLK | $t_{HOLD}$ | 10 | | | ns |
| Output valid delay from rising edge of BITCLK | $t_{CO}$ | | | 15 | ns |

## SIGNAL RISE AND FALL TIMES

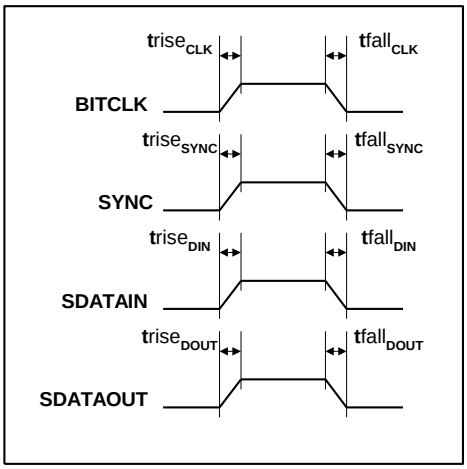



**Figure 3 Signal Rise and Fall Times (50pF External Load)**

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, $T_A$ = -25°C to +85°C, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| BITCLK rise time | $trise_{CLK}$ | 2 | | 6 | ns |
| BITCLK fall time | $tfall_{CLK}$ | 2 | | 6 | ns |
| SYNC rise time | $trise_{SYNC}$ | | | 6 | ns |
| SYNC fall time | $tfall_{SYNC}$ | | | 6 | ns |
| SDATAIN rise time | $trise_{DIN}$ | 2 | | 6 | ns |
| SDATAIN fall time | $tfall_{DIN}$ | 2 | | 6 | ns |
| SDATAOUT rise time | $trise_{DOUT}$ | | | 6 | ns |
| SDATAOUT fall time | $tfall_{DOUT}$ | | | 6 | ns |

## AC-LINK POWERDOWN

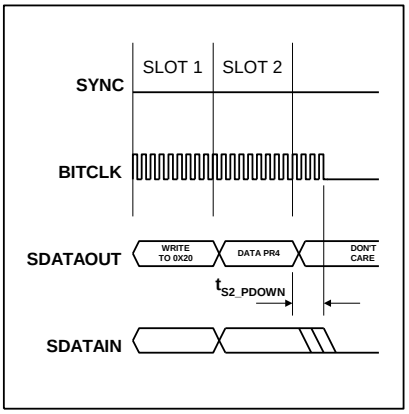



**Figure 4 AC-Link Powerdown Timing**

AC-Link powerdown occurs when PR4 (register 26h, bit 12) is set (see “Power Management”).

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| End of Slot 2 to BITCLK and SDATAIN low | $t_{S2\_PDOWN}$ | | | 1.0 | µs |

### COLD RESET (ASYNCHRONOUS – RESETS REGISTER SETTINGS)

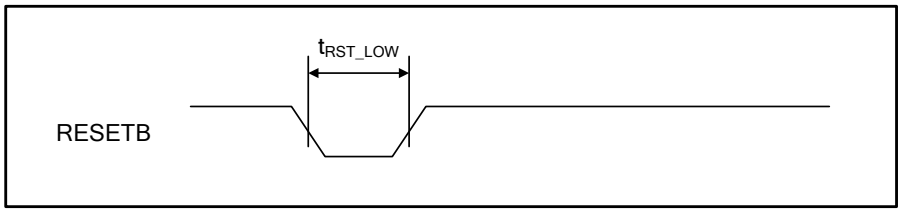



**Figure 5 Cold Reset Timing**

**Note:**

For correct operation SDATAOUT and SYNC must be held LOW for entire RESETB active low period otherwise the device may enter test mode. See AC'97 specification and Application Note WAN 0104 for further details.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| RESETB active low pulse width | $t_{RST\_LOW}$ | 1.0 | | | µs |

### WARM RESET (ASYNCHRONOUS – PRESERVES REGISTER SETTINGS)

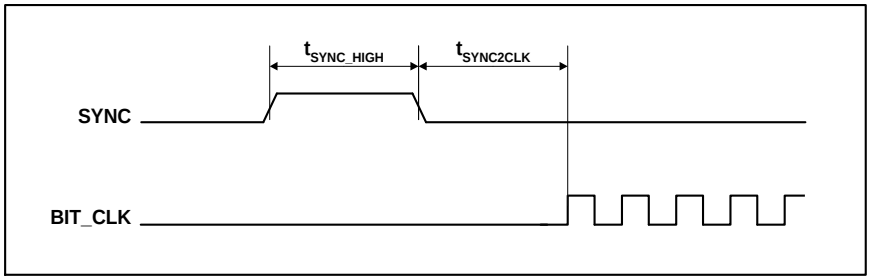



**Figure 6 Warm Reset Timing**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| SYNC active high pulse width | $t_{SYNC\_HIGH}$ | | 1.3 | | µs |
| SYNC inactive to BITCLK startup delay | $t_{RST2CLK}$ | 162.4 | | | ns |

## PCM AUDIO INTERFACE TIMING – SLAVE MODE

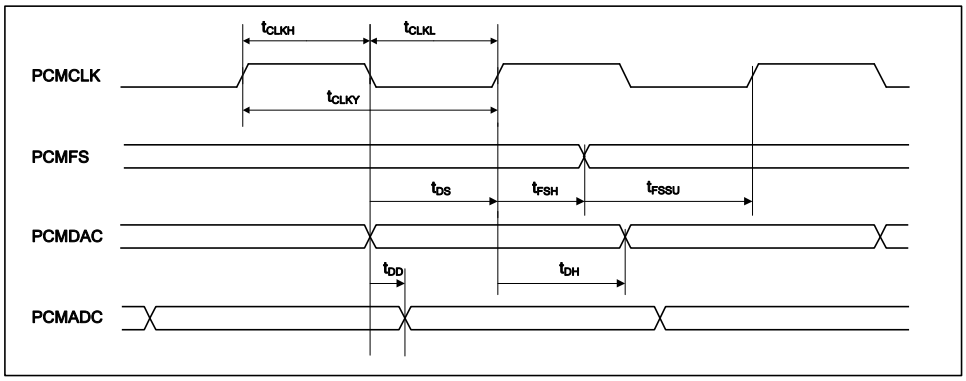



**Figure 7 Digital Audio Data Timing – Slave Mode**

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, $T_A$ = -25°C to +85°C, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Audio Data Input Timing Information** | | | | | |
| PCMCLK cycle time | $t_{PCMY}$ | 50 | | | ns |
| PCMCLK pulse width high | $t_{PCMH}$ | 20 | | | ns |
| PCMCLK pulse width low | $t_{PCML}$ | 20 | | | ns |
| PCMFS set-up time to PCMCLK rising edge | $t_{FSSU}$ | 10 | | | ns |
| PCMFS hold time from PCMCLK rising edge | $t_{FSH}$ | 10 | | | ns |
| PCMDAC set-up time from PCMCLK rising edge | $t_{DS}$ | 10 | | | ns |
| PCMDAC hold time from PCMCLK rising edge | $t_{DH}$ | 10 | | | ns |
| PCMADC propagation delay from PCMCLK falling edge | $t_{DD}$ | | | 10 | ns |

**Note:**

1. PCMCLK period should always be greater than or equal to Voice CLK period.

## PCM AUDIO INTERFACE TIMING – MASTER MODE

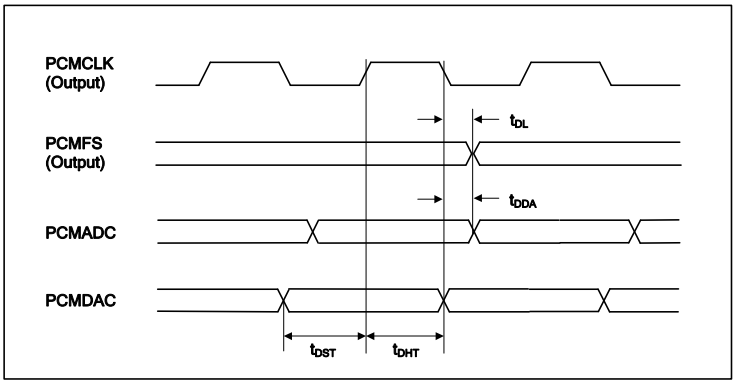



**Figure 8 Digital Audio Data Timing – Master Mode (see Control Interface)**

**Test Conditions**

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, $T_A$ = -25°C to +85°C, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Audio Data Input Timing Information** | | | | | |
| PCMFS propagation delay from PCMCLK falling edge | $t_{DL}$ | | | 10 | ns |
| PCMADC propagation delay from PCMCLK falling edge | $t_{DDA}$ | | | 10 | ns |
| PCMDAC setup time to PCMCLK rising edge | $t_{DST}$ | 10 | | | ns |
| PCMDAC hold time from PCMCLK rising edge | $t_{DHT}$ | 10 | | | ns |

# DEVICE DESCRIPTION

## INTRODUCTION

The WM9714L is a largely pin-compatible upgrade to WM9712, with a PCM voice CODEC added. This CODEC is interfaced via a PCM type audio interface which makes use of GPIO pins for connection.

It is designed to meet the mixed-signal requirements of portable and wireless smartphone systems. It includes audio recording and playback, battery monitoring, auxiliary ADC and GPIO functions, all controlled through a single 5-wire AC-Link interface. Additionally, PCM voice CODEC functions are supported through provision of an additional voice DAC and a PCM audio serial interface.

A PLL is included to allow unrelated reference clocks to be used for generation of the AC link system clock. Typically 13MHz or 2.048MHz clock sources might be used as a reference.

### SOFTWARE SUPPORT

The basic audio features of the WM9714L are software compatible with standard AC'97 device drivers. However, to better support additional functions, Cirrus Logic supplies custom device drivers for selected CPUs and operating systems. Please contact your local Cirrus Logic representative for more information.

### AC'97 COMPATIBILITY

The WM9714L uses an AC'97 interface to communicate with a microprocessor or controller. The audio and GPIO functions are largely compliant with AC'97 Revision 2.2. The following **differences** from the AC'97 standard are noted:

- Pinout: The function of some pins has been changed to support device specific features. The PHONE and PCBEEP pins have been moved to different locations on the device package.
- Package: The default package for the WM9714L is a 7×7mm leadless QFN package.
- Audio mixing: The WM9714L handles all the audio functions of a smartphone, including audio playback, voice recording, phone calls, phone call recording, ring tones, as well as simultaneous use of these features. The AC'97 mixer architecture does not fully support this. The WM9714L therefore uses a modified AC'97 mixer architecture with three separate mixers.
- Tone Control, Bass Boost and 3D Enhancement: These functions are implemented in the digital domain and therefore affect only signals being played through the audio DACs, not all output signals as stipulated in AC'97.

Some other functions are **additional** to AC'97:

- On-chip BTL loudspeaker driver for mono or stereo speakers
- On-chip BTL driver for ear speaker (phone receiver)
- Auxiliary mono DAC for ring tones, system alerts etc.
- Auxiliary ADC Inputs
- 2 Analogue Comparators for Battery Alarm
- Programmable Filter Characteristics for Tone Control and 3D Enhancement
- PCM interface to additional Voice DAC and existing audio ADCs
- PLL to create AC'97 system clock from unrelated reference clock input

### PCM CODEC

The PCM voice CODEC functions typically required by mobile telephony devices are provided by an extra voice DAC on the WM9714L, which is interfaced via a standard PCM type data interface, which is constructed through optional use of 4 of the GPIO pins on WM9714L. The audio output data from one or both of the audio ADCs can also be output over this PCM interface, allowing a full voice CODEC function to be implemented. This PCM interface supports sample rates from 8 to 48ks/s using the standard AC'97 master clock.

## AUDIO PATHS OVERVIEW

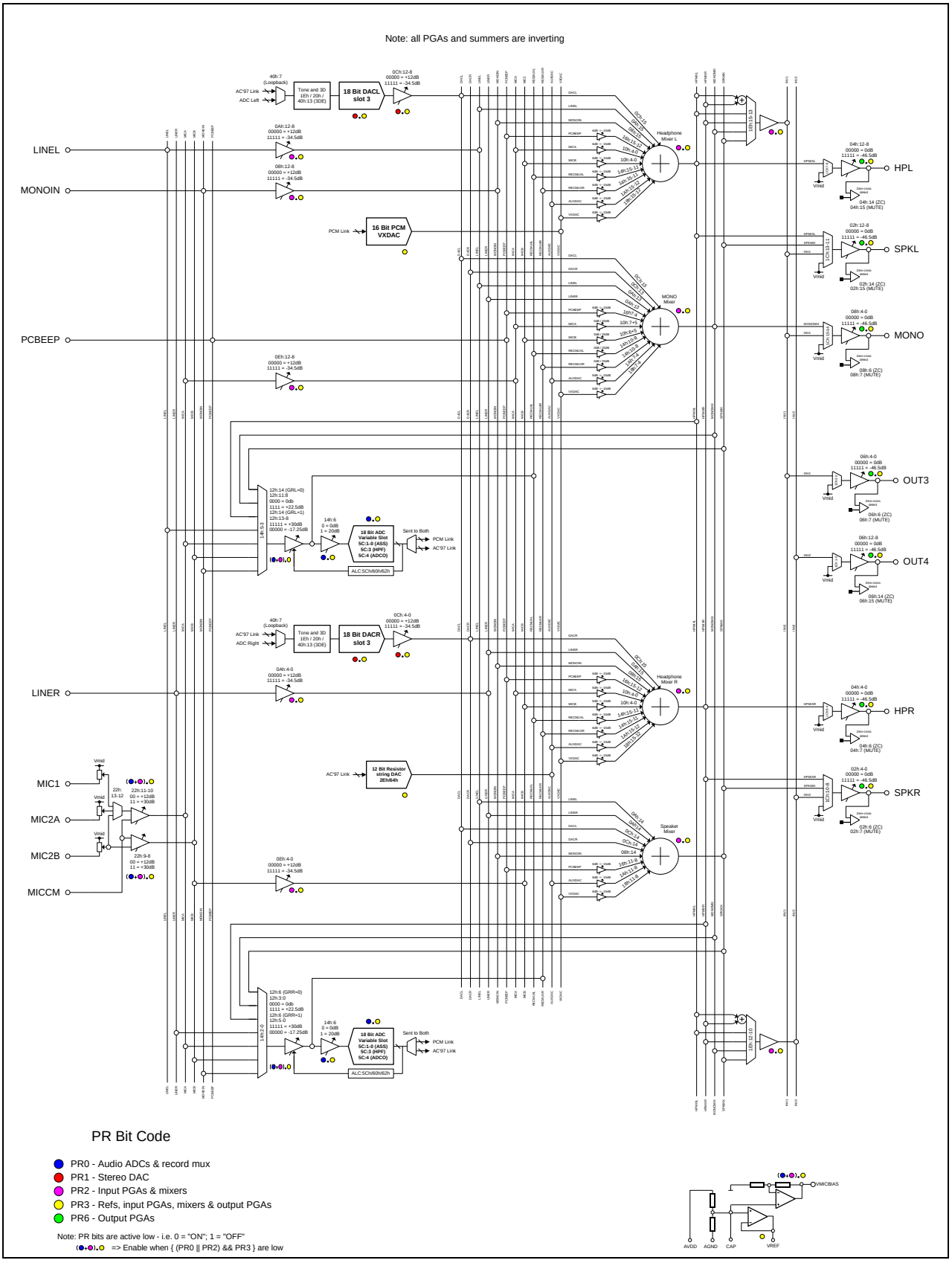



**Figure 9 Audio Paths Overview**

## CLOCK GENERATION

WM9714L supports clocking from 2 separate sources, which can be selected via the AC'97 interface:

- External clock input MCLKA
- External clock input MCLKB

The source clock is divided to appropriate frequencies in order to run the AC'97 interface, PCM interface, voice DAC and Hi-fi DSP by means of a programmable divider block. Clock rates may be changed during operation via the AC'97 link in order to support alternative modes, for example low power mode when voice data is being transmitted only. A PLL is present to add flexibility in selection of input clock frequencies, typical choices being 2.048MHz, 4.096MHz or 13MHz.

### INITIALISING THE AC'97 LINK

By default, the AC'97 link is disabled and therefore will not be running after power on or a COLD reset event. Before any register map configuration can begin, it is necessary to start the AC'97 link. This is achieved by sending a WARM reset to the CODEC as defined in Figure 6**.**

Default mode on power-up also assumes a clock will be present on MCLKA with the PLL powered down. After a WARM reset the CODEC will start the AC'97 link using MCLKA as a reference. This enables data to be clocked via the AC'97 link to define the desired clock divider mode and whether PLL needs to be activated.

**Note:** MCLKA can be any available frequency.

When muxing between MCLKA and MCLKB both clocks must be active for at least two clock cycles after the switching event.

## CLOCK DIVISION MODES

Figure 10 shows the clocking strategy for WM9714L. Clocking is controlled by CLK_MUX, CLK_SRC and S[6:0].

- CLKAX2, CLKBX2 – clock doublers on inputs MCLKA and MCLKB.
- CLK_MUX - selects between MCLKA and MCLKB.
- CLK_SRC – selects between external or PLL derived clock reference.
- S[3:0] – sets the voice DAC clock rate and PCM interface clock when in master mode (division ratio 1 to 16 available).
- S[6:4] - sets the hi-fi clocking rate (division ratio 1 to 8 available).

The registers used to set these switches can be accessed from register address 44h (see Table 3).

If a mode change requires switching from an external clock to a PLL generated clock then it is recommended to set the clock division ratios required for the PLL clock scheme prior to switching between clocks. This option is accommodated by means of two sets of registers. $S_{PLL}$[6:0] is used to set the divide ratio of the clock when in PLL mode and $S_{EXT}$[6:0] is used to divide the clock when it is derived from an external source. If the PLL is selected (CLK_SRC = 0), S[6:0] = $S_{PLL}$[6:0]. $S_{PLL}$[6:0] is defined in register 46h (see Table 4) and is written to using the page address mode. More details on page address mode for controlling the PLL are found on page 24. Register 46h also contains a number of separate control bits relating to the PLL's function. If an external clock is selected (CLK_SRC = 1) S[6:0] = $S_{EXT}$[6:0]. $S_{EXT}$[6:0] is defined in register address 44h. Writing to registers 44h and 46h enables pre-programming of the required clock mode before the PLL output is selected.

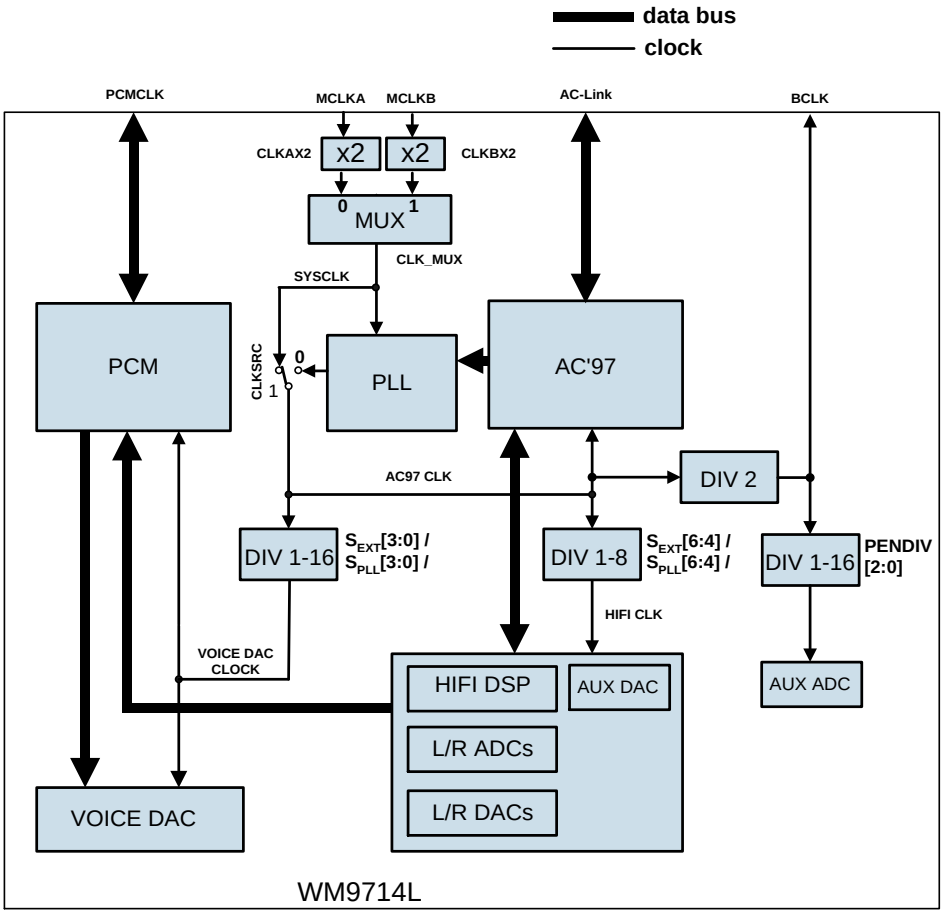



**Figure 10 Clocking Architecture for WM9714L**

## INTERNAL CLOCK FREQUENCIES

The internal clock frequencies are defined as follows (refer to Figure 10):

- AC97 CLK – nominally 24.576MHz, used to generate AC97 BITCLK at 12.288MHz.
- HIFI CLK – for hi-fi playback at 48ks/s HIFI CLK = 24.576MHz. See Table 2 for voice only playback.
- Voice DAC CLK – see Table 2 for sample rate vs clock frequency.

| SAMPLE RATE | VOICE DAC CLK FREQUENCY | HIFI CLK FREQUENCY |
|---|---|---|
| 8ks/s voice and hi-fi | 2.048MHz | 24.576MHz |
| 8ks/s voice only (power save) | 2.048MHz | 4.096MHz |
| 16ks/s voice and hi-fi | 4.096MHz | 24.576MHz |
| 16ks/s voice only (power save) | 4.096MHz | 8.192MHz |
| 32ks/s voice and hi-fi | 8.192MHz | 24.576MHz |
| 48ks/s voice and hi-fi | 12.288MHz | 24.576MHz |

**Table 2 Clock Division Mode Table**

### AUXADC

The clock for the AUXADC nominally runs at 768kHz and is derived from BITCLK. The divisor for the clock generator is set by PENDIV. This enables the AUXADC clock frequency to be set according to power consumption and conversion rate considerations.

Clock mode and division ratios are controlled by register 44h as shown in Table 3.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 44h | 14:12 | $S_{EXT}$[6:4] | 000 (div 1) | Defines clock division ratio for Hi-fi:<br>DSP, ADCs and DACs<br>000: f<br>001: f/2<br>...<br>111: f/8 |
| | 11:8 | $S_{EXT}$[3:0] | 0000 (div 1) | Defines clock division ratio for PCM interface and voice DAC in external clock mode only:<br>0000: f<br>0001: f/2<br>…<br>1111: f/16 |
| | 7 | CLKSRC | 1 (ext clk) | Selects between PLL clock and External clock<br>0: PLL clock<br>1: external clock |
| | 5:3 | PENDIV | 000 (div 16) | Sets AUXADC clock divisor<br>000: f/16<br>001: f/12<br>010: f/8<br>011: f/6<br>100: f/4<br>101: f/3<br>110: f/2<br>111: f |
| | 2 | CLKBX2 | 0 (Off) | Clock doubler for MCLKB |
| | 1 | CLKAX2 | 0 (Off) | Clock doubler for MCLKA |
| | 0 | CLKMUX | 0 (MCLKA) | Selects between MCLKA and MCLKB (N.B. On power-up clock must be present on MCLKA and must be active for 2 clock cycles after switching to MCLKB)<br>0: SYSCLK=MCLKA<br>1: SYSCLK=MCLKB |

**Table 3 Clock Muxing and Division Control**

## PLL MODE

The PLL operation is controlled by register 46h (see Table 4) and has two modes of operation:

- Integer N
- Fractional N

The PLL has been optimized for nominal input clock (PLL_IN) frequencies in the range 8.192MHz – 19.661MHz (LF=0) and 2.048MHz – 4.9152MHz (LF=1). Through use of a clock divider (div by 2 / 4) on the input to the PLL frequencies up to 78.6MHz can be accommodated. The input clock divider is enabled by DIVSEL (0=Off) and the division ratio is set by DIVCTL (0=div2, 1=div4).

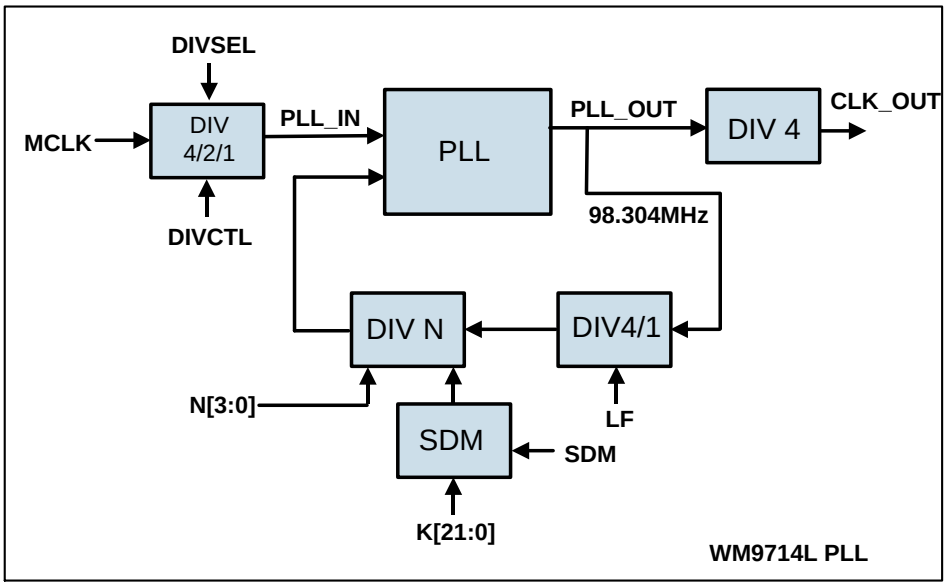



**Figure 11 PLL Architecture**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 46h | 15:12 | N[3:0] | 0000 | **PLL N Divide Control**<br>0000 = Divide by 1<br>0001 = Divide by 1<br>0010 = Divide by 2<br>…<br>1111 = Divide by 15<br>**Note:** must be set between 05h and 0Ch for integer N mode |
| | 11 | LF | 0 = off | **PLL Low Frequency Input Control**<br>1 = Low frequency mode (input clock < 8.192MHz)<br>0 = Normal mode |
| 46h | 10 | SDM | 0 = off | **PLL SDM Enable Control**<br>1 = Enable SDM (required for fractional N mode)<br>0 = Disable SDM |
| 46h | 9 | DIVSEL | 0 = off | **PLL Input Clock Division Control**<br>0 = Divide by 1<br>1 = Divide according to DIVCTL |
| | 8 | DIVCTL | 0 | **PLL Input Clock Division Value Control**<br>0 = Divide by 2<br>1 = Divide by 4 |
| 46h | 6:4 | PGADDR | 000 | **Pager Address**<br>Pager address bits to access programming of K[21:0] and $S_{PLL}$[6:0] |
| 46h | 3:0 | PGDATA | 0000 | **Pager Data**<br>Pager data bits |

**Table 4 PLL Clock Control**

### INTEGER N MODE

The nominal output frequency of the PLL (PLL_OUT) is 98.304MHz which is divided by 4 to achieve a nominal system clock of 24.576MHz.

The integer division ratio (N) is determined by: $F_{PLL\_out}$ / $F_{PLL\_IN}$ , and is set by N[3:0] and must be in the range 5 to 12 for integer N operation (0101 = div by 5, 1100 = div by 12). Note that setting LF=1 enables a further division by 4 required for input frequencies in the range 2.048MHz – 4.096MHz.

Integer N mode is selected by setting SDM=0.

### FRACTIONAL N MODE

Fractional N mode provides a divide resolution of $1/2^{22}$ and is set by K[21:0] (register 46h, see section). The relationship between the required division X, the fractional division K[21:0] and the integer division N[3:0] is:

$$K = 2^{22}(X - N)$$

where 0 < (X – N) < 1 and K is rounded to the nearest whole number.

For example, if the PLL_IN clock is 13MHz and the desired PLL_OUT clock is 98.304MHz then the desired division, X, is 7.5618. So N[3:0] will be 7h and K[21:0] will be 23F488h to produce the desired 98.304MHz clock (see Table 5).

| INPUT CLOCK (PLL_IN) | DESIRED PLL OUTPUT (PLL_OUT) | DIVISION REQUIRED (X) | FRACTIONAL DIVISION (K) | INTEGER DIVISION (N) |
|---|---|---|---|---|
| 2.048MHz | 98.304MHz | 48 | 0 | 12x4* |
| 4.096MHz | 98.304MHz | 24 | 0 | 6x4* |
| 12.288MHz | 98.304MHz | 8 | 0 | 8 |
| 13MHz | 98.304MHz | 7.5618 | 0.5618 | 7 |
| 27MHz (13.5MHz)** | 98.304MHz | 7.2818 | 0.2818 | 7 |
| *Divide by 4 enabled in PLL feedback path for low frequency inputs. (LF = 1)<br>**Divide by 2 enabled at PLL input for frequencies > 14.4MHz > 38MHz (DIVSEL = 1, DIVCTL = 0) | | | | |

**Table 5 PLL Modes of Operation**

### PLL REGISTER PAGE ADDRESS MAPPING

The clock division control bits $S_{PLL}$[6:0] and the PLL fractional N division bits are accessed through register 46h using a sub-page address system. The 3-bit pager address allows 8 blocks of 4-bit data words to be accessed whilst the register address is set to 46h. This means that when register address 46h is selected a further 7 cycles of programming are required to set all of the page data bits. Control bit allocation for these page addresses is described in Table 6.

| PAGE ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 111 | 31:28 | $S_{PLL}$[6:4] | 0h | Clock division control bus SPLL[6:0]. Clock divider reads this control word if PLL is enabled. Bits [6:4] and [3:0] have the same functionality as 44h [14:12] and [11:8] respectively |
| 110 | 27:24 | $S_{PLL}$[3:0] | 0h | |
| 101 | 23:22 | Reserved | 0h | Reserved bits |
| | 21:20 | K[21:0] | 0h | Sigma Delta Modulator control word for fractional N division. Division resolution is $1/22^2$ |
| 100 | 19:16 | | 0h | |
| 011 | 15:12 | | 0h | |
| 010 | 11:8 | | 0h | |
| 001 | 7:4 | | 0h | |
| 000 | 3:0 | $S_{PLL}$[3:0] | 0h | |

**Table 6 Pager Control Bit Allocation**

Powerdown for the PLL and internal clocks is via registers 26h and 3Ch (see Table 7).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 26h | 13 | PR5 | 1 (Off) | **Internal Clock Disable Control**<br>1 = Disabled<br>0 = Enabled |
| 3Ch | 9 | PLL | 1 (Off) | **PLL Disable Control**<br>1 = Disabled<br>0 = Enabled |
| N.B. both PR5 and PLL must be asserted low before PLL is enabled | | | | |

**Table 7 PLL Powerdown Control**

## DIGITAL INTERFACES

The WM9714L has two interfaces, a data and control AC'97 interface and a data only PCM interface. The AC'97 interface is available through dedicated pins (SDATAOUT, SDATAIN, SYNC, BITCLK and RESETB) and is the sole control interface with access to all data streams on the device except for the Voice DAC. The PCM interface is available through the GPIO pins (PCMCLK, PCMFS, PCMDAC and PCMADC) and provides access to the Voice DAC. It can also transmit the data from the Stereo ADC. This can be useful, for example, to allow both sides of a phone conversation to be recorded by mixing the transmit and receive paths on one of the ADC channels and transmitting it over the PCM interface.

## AC97 INTERFACE

### INTERFACE PROTOCOL

The WM9714L uses an AC'97 interface for both data transfer and control. The AC-Link has 5 wires:

- SDATAIN (pin 8) carries data from the WM9714L to the controller
- SDATAOUT (pin 5) carries data from the controller to the WM9714L
- BITCLK (pin 6) is a clock, derived from either MCLKA or MCLKB inputs and supplied to the controller.
- SYNC is a synchronization signal generated by the controller and passed to the WM9714L
- RESETB resets the WM9714L to its default state

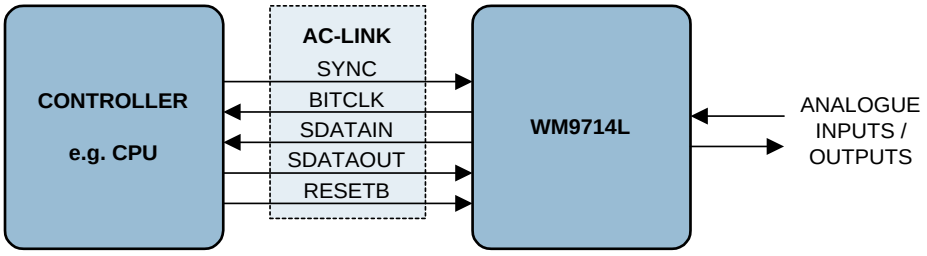



**Figure 12 AC-Link Interface (typical case with BITCLK generated by the AC97 CODEC)**

The SDATAIN and SDATAOUT signals each carry 13 time-division multiplexed data streams (slots 0 to 12). A complete sequence of slots 0 to 12 is referred to as an AC-Link frame, and contains a total of 256 bits. The frame rate is 48kHz. This makes it possible to simultaneously transmit and receive multiple data streams (e.g. audio, AUXADC, control) at sample rates up to 48kHz.

Detailed information can be found in the AC'97 (Revision 2.2) specification, which can be obtained at www.intel.com/design/chipsets/audio/

**Note:**

SDATAOUT and SYNC must be held low when RESETB is applied. These signals must be held low for the entire duration of the RESETB pulse and especially during the low-to-high transition of RESETB. If SDATAOUT or SYNC is high during reset, the WM9714L may enter test modes. Information relating to this operation is available in the AC'97 specification and in Application Note WAN 0104.

## PCM INTERFACE

### OPERATION

WM9714L can implement a PCM voice CODEC function using the dedicated VXDAC and either one or both of the existing hi-fi ADC's. In PCM CODEC mode, VXDAC input and ADC output are interfaced via a PCM style port via GPIO pins.

This interface can support one ADC channel, or stereo/dual ADC channels if required, (two channels of data are sent per PCM frame as back to back words).

In voice-only mode, the AC link is used only for control information, not audio data. Therefore it will generally be shut down (PR4=1), except when control data must be sent.

The PCM interface makes use of 4 of the GPIO interface pins, for clock, frame, and data in/out. If the PCM CODEC function is not enabled then the GPIO pins may be used for other functions.

## INTERFACE PROTOCOL

The WM9714L PCM audio interface is used for the input of data to the Voice DAC and the output of data from the Stereo ADC. When enabled, the PCM audio interface uses four GPIO pins:

- GPIO1/PCMCLK: Bit clock
- GPIO3/PCMFS: Frame Sync
- GPIO4/PCMDAC: Voice DAC data input
- GPIO5/PCMADC: Stereo ADC data output

Depending on the mode of operation (see “PCM Interface Modes”), at least one of these four pins must be set up as an output by writing to register 4Ch (see Table 57). When not enabled the GPIOs may be used for other functions on the WM9714L.

## PCM INTERFACE MODES

The WM9714L PCM audio interface may be configured in one of four modes:

- Disabled Mode: The WM9714L disables and tri-states all PCM interface pins. Any clock input is ignored and ADC/DAC data is not transferred.
- Slave Mode: The WM9714L accepts PCMCLK and PCMFS as inputs from an external source.
- Master Mode: The WM9714L generates PCMCLK and PCMFS as outputs.
- Partial Master Mode: The WM9714L generates PCMCLK as an output, and accepts PCMFS as an external input.

## PCM AUDIO DATA FORMATS

Four different audio data formats are supported:

- DSP mode
- Left justified
- Right justified
- $I^2S$

All four of these modes are MSB first. They are described below. Refer to “Signal Timing Requirements” for timing information.

**Note:**
PCMCLK and PCMFS must be synchronized with the BITCLK from the AC’97 interface.

The PCM Interface may be configured for Mono mode, where only one channel of ADC data is output. In this mode the interface should be configured for DSP mode. A short or long frame sync is supported and the MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of VXCLK.

Note that when operating in stereo mode the mono Voice DAC always uses the left channel data as its input.

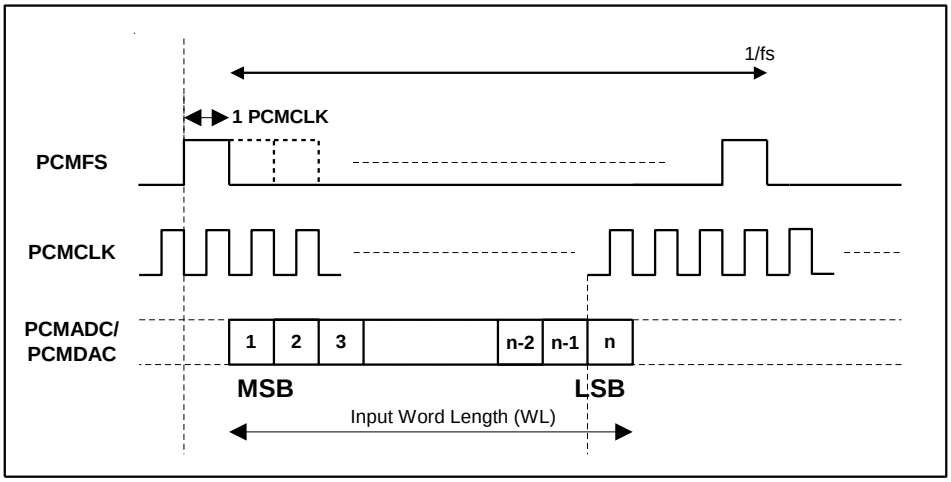



**Figure 13 PCM Interface Mono Mode (mode A, FSP=0)**

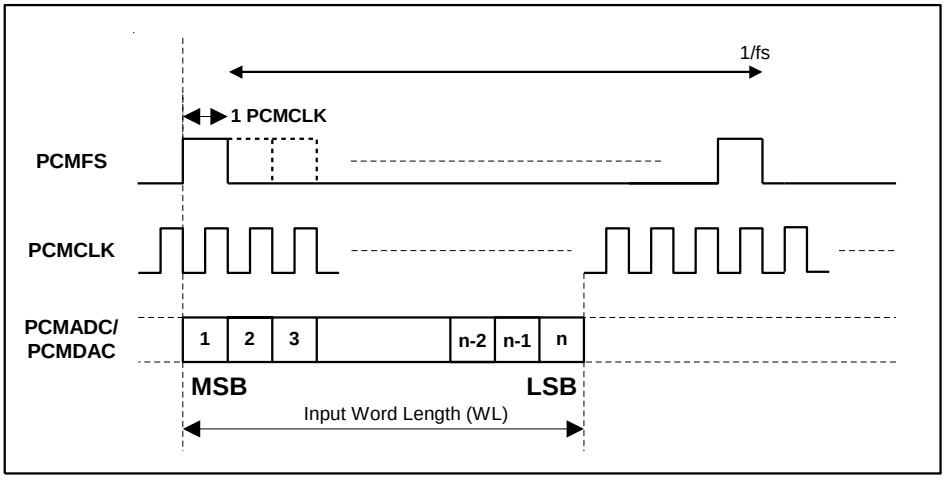



**Figure 14 PCM Interface Mono Mode (mode B, FSP=1)**

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of PCMCLK (selectable by FSP) following a rising edge of PCMFS. Right channel data immediately follows left channel data. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles between the LSB of the right channel data and the next sample.

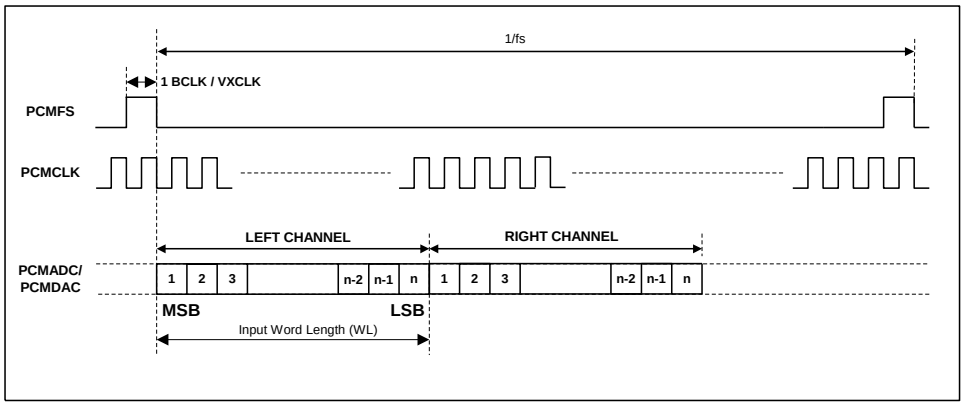



**Figure 7 DSP Mode Audio Interface (mode A, FSP=0)**

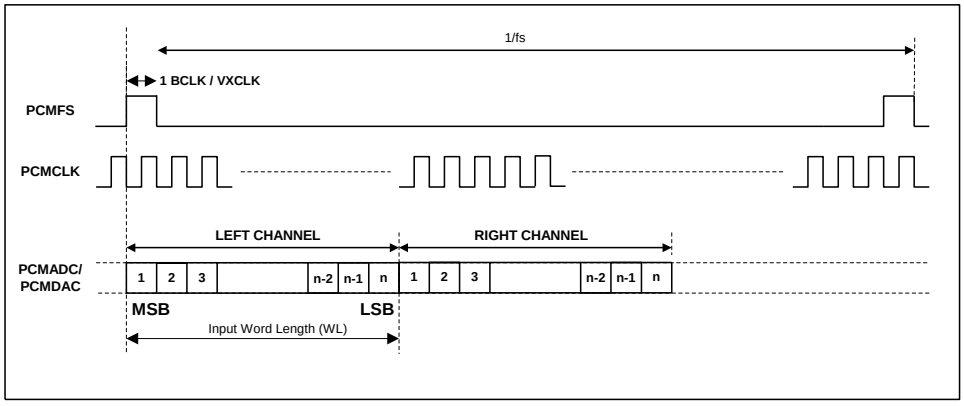



**Figure 15 DSP Mode Audio Interface (mode B, FSP=1)**

In Left Justified mode, the MSB is available on the first rising edge of PCMCLK following a PCMFS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles before each PCMFS transition.

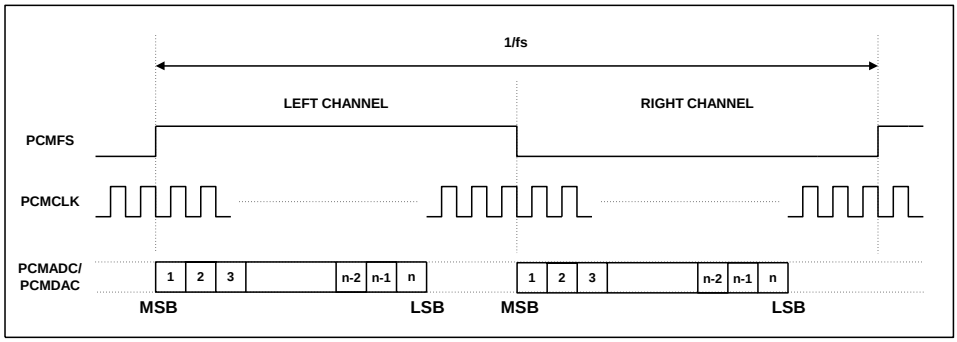



**Figure 16 Left Justified Audio Interface (assuming n-bit word length)**

In Right Justified mode, the LSB is available on the last rising edge of PCMCLK before a PCMFS transition. All other bits are transmitted before (MSB first). Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles after each PCMFS transition.

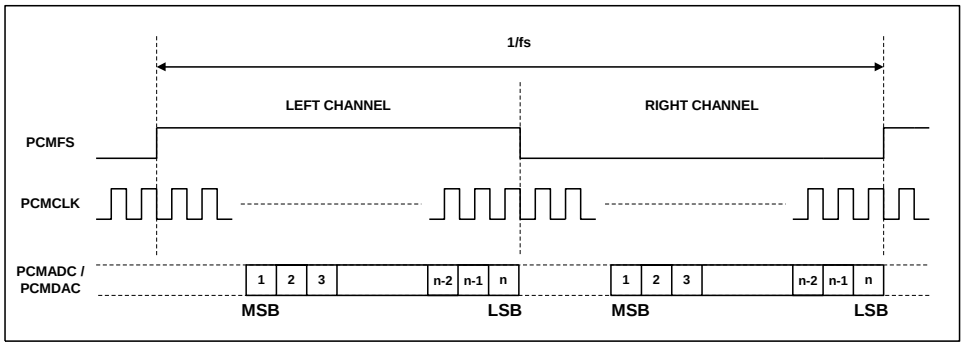



**Figure 17 Right Justified Audio Interface (assuming n-bit word length)**

In I²S mode, the MSB is available on the second rising edge of PCMCLK following a PCMFS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles between the LSB of one sample and the MSB of the next.

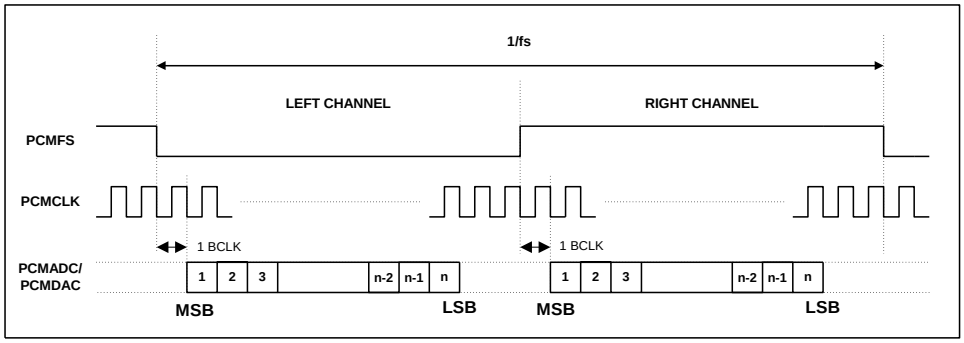



**Figure 18 I²S Justified Audio Interface (assuming n-bit word length)**

## CONTROL

The register bits controlling PCM audio format, word length and operating modes are summarised below. CTRL must be set to override the normal use of the PCM interface pins as GPIOs, MODE must be set to specify master/slave modes.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| 36h<br>PCM Control | 15 | CTRL | 0 | **GPIO Pin Configuration Control**<br>0 = GPIO pins as GPIOs<br>1 = GPIO pins configured as PCM interface and controlled by this register | |
| | 14:13 | MODE | 10 | **PCM Interface Mode Control**<br>00 = PCM interface disabled [PCMCLK tri-stated, PCMFS tri-stated]<br>01 = PCM interface in slave mode [PCMCLK as input, PCMFS as input]<br>10 = PCM interface in master mode [PCMCLK as output, PCMFS as output]<br>11 = PCM interface in partial master mode [PCMCLK as output, PCMFS as input] | |
| | 11:9 | DIV | 010 | **PCMCLK Rate Control**<br>000 = Voice DAC clock<br>001 = Voice DAC clock / 2<br>010 = Voice DAC clock / 4<br>011 = Voice DAC clock / 8<br>100 = Voice DAC clock / 16<br>All other values are reserved | |
| | 8 | VDACOSR | 1 | **Voice DAC Oversampling Rate Control**<br>0: 128 x fs<br>1: 64 x fs | |
| | 7 | CP | 0 | **PCMCLK Polarity Control**<br>0 = Normal<br>1 = Inverted | |
| | 6 | FSP | 0 | FMT = 00, 01 or 10 | FMT = 11 |
| | | | | **PCMFS Polarity Control**<br>0 = Normal<br>1 = Inverted | **DSP Mode Control**<br>0 = DSP Mode A<br>1 = DSP Mode B |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| | 5:4 | SEL | 10 | **PCM ADC Output Channel Control**<br>00 = Normal stereo<br>01 = Reverse stereo<br>10 = Output left ADC data only<br>11 = Output right ADC data only |
| | 3:2 | WL | 00 | **PCM Data Word Length Control**<br>00 = 16-bit<br>01 = 20-bit<br>10 = 24-bit<br>11 = 32-bit (not supported when FMT=00) |
| | 1:0 | FMT | 11 | **PCM Data Format Control**<br>00 = Right justified<br>01 = Left justified<br>10 = $I^2S$<br>11 = DSP mode |

**Table 8 PCM CODEC Control**

**Note:** Right justified does not support 32-bit data.

# AUDIO ADCS

## STEREO ADC

The WM9714L has a stereo sigma-delta ADC to digitize audio signals. The ADC achieves high quality audio recording at low power consumption. The ADC sample rate can be controlled by writing to a control register (see “Variable Rate Audio / Sample Rate Conversion”). It is independent of the DAC sample rate.

To save power, the left and right ADCs can be separately switched off using the Powerdown bits ADCL and ADCR (register 3Ch, bits 5:4), whereas PR0 disables both ADCs (see “Power Management”). If only one ADC is running, the same ADC data appears on both the left and right AC-Link slots.

The output from the ADC can be sent over either the AC link as usual, or output via the PCM interface which may be configured on the GPIO pins.

### HIGH PASS FILTER

The WM9714L audio ADC incorporates a digital high pass filter that eliminates any DC bias from the ADC output data. The filter is enabled by default. For DC measurements, it can be disabled by writing a ‘1’ to the HPF bit (register 5Ch, bit 3).

This high pass filter corner frequency can be selected to have different values in WM9714L, to suit applications such as voice where a higher cutoff frequency is required.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 5Ch | 3 | HPF | 0 | **ADC HPF Disable Control**<br>0 = HPF enabled (for audio)<br>1 = HPF disabled (for DC measurements) |
| 5Ah | 5:4 | HPMODE | 00 | **HPF Cut-Off Control**<br>00 = 7Hz @ fs=48kHz<br>01 = 82Hz @ fs=16kHz<br>10 = 82Hz @ fs=8kHz<br>11 = 170Hz @ fs=8kHz |
| **Note**: the filter corner frequency is proportional to the sample rate. | | | | |

**Table 9 Controlling the ADC High-pass Filter**

### ADC SLOT MAPPING

By default, the output of the left audio ADC appears on slot 3 of the SDATAIN signal (pin 8), and the right ADC data appears on slot 4. However, the ADC output data can also be sent to other slots, by setting the ASS (ADC slot select) control bits as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | |
|---|---|---|---|---|---|---|
| 5Ch Additional Functions (2) | 1:0 | ASS | 00 | **ADC Data Slot Mapping Control** | | |
| | | | | | **Left Data** | **Right Data** |
| | | | | 00 = | Slot 3 | Slot 4 |
| | | | | 01 = | Slot 7 | Slot 8 |
| | | | | 10 = | Slot 6 | Slot 9 |
| | | | | 11 = | Slot 10 | Slot 11 |

**Table 10 ADC Slot Mapping**

## RECORD SELECTOR

The record selector determines which input signals are routed into the audio ADC. The left and right channels can be selected independently. This is useful for recording a phone call: one channel can be used for the RX signal and the other for the TX signal, so that both sides of the conversation are digitized.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 14h<br>Record Routing / Mux Select | 6 | RECBST | 0 | **ADC Record Boost Control**<br>1 = +20dB<br>0 = 0dB<br>**Note:** RECBST gain is in addition to the microphone pre-amps (MPABST and MPBBST bits) and record gain (GRL and GRR / GRL bits). |
| | 5:3 | RECSL | 000 | **Left Record Mux Source Control**<br>000 = MICA (pre-PGA)<br>001 = MICB (pre-PGA)<br>010 = LINEL (pre-PGA)<br>011 = MONOIN (pre-PGA)<br>100 = HPMIXL<br>101 = SPKMIC<br>110 = MONOMIX<br>111 = Reserved |
| | 2:0 | RECSR | 000 | **Right Record Mux Source Control**<br>000 = MICA (pre-PGA)<br>001 = MICB (pre-PGA)<br>010 = LINEL (pre-PGA)<br>011 = MONOIN (pre-PGA)<br>100 = HPMIXL<br>101 = SPKMIC<br>110 = MONOMIX<br>111 = Reserved |

**Table 11 Audio Record Selector**

## RECORD GAIN

The amplitude of the signal that enters the audio ADC is controlled by the Record PGA (Programmable Gain Amplifier). The PGA gain can be programmed either by writing to the Record Gain register, or by the Automatic Level Control (ALC) circuit (see page 34). If the ALC is enabled, any writes to the Record Gain register have no effect.

Two different gain ranges can be implemented: the standard gain range defined in the AC'97 standard, or an extended gain range with smaller gain steps. The ALC circuit always uses the extended gain range, as this has been found to result in better sound quality.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| 12h<br>Record Gain | 15 | RMU | 1 | **Audio ADC Input Mute Control**<br>1 = Mute<br>0 = No mute<br>**Note:** This control applies to both channels | |
| | 14 | GRL | 0 | **Left ADC PGA Gain Range Control**<br>1 = Extended<br>0 = Standard | |
| | 13:8 | RECVOLL | 000000 | **Left ADC Recording Volume Control** | |
| | | | | Standard (GRL=0) | Extended (GRL=1) |
| | | | | XX0000: 0dB<br>XX0001: +1.5dB<br>… (1.5dB steps)<br>XX1111: +22.5dB | 000000: -17.25dB<br>000001: -16.5dB<br>… (0.75dB steps)<br>111111: +30dB |
| | 7 | ZC | 0 | **ADC PGA Zero Cross Control**<br>1 = Zero cross enabled (volume changes when signal is zero or after time-out)<br>0 = Zero cross disabled (volume changes immediately) | |
| | 6 | GRR | 0 | **Right ADC PGA Gain Range Control**<br>1 = Extended<br>0 = Standard | |
| | 5:0 | RECVOLR | 000000 | **Right ADC Recording Volume Control** | |
| | | | | Standard (GRR=0) | Extended (GRR=1) |
| | | | | XX0000: 0dB<br>XX0001: +1.5dB<br>… (1.5dB steps)<br>XX1111: +22.5dB | 000000: -17.25dB<br>000001: -16.5dB<br>… (0.75dB steps)<br>111111: +30dB |

**Table 12 Record Gain Register**

The output of the Record PGA can also be mixed into the phone and/or headphone outputs (see "Audio Mixers"). This makes it possible to use the ALC function for the microphone signal in a smartphone application.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 14h<br>Record Routing | 15:14 | R2H | 11 (mute) | **Record Mux to Headphone Mixer Path Control**<br>00 = stereo<br>01 = left ADC only<br>10 = right ADC only<br>11=mute left and right |
| | 13:11 | R2HVOL | 010 (0dB) | **Record Mux to Headphone Mixer Path Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 10:9 | R2M | 11 (mute) | **Record Mux to Mono Mixer Path Control**<br>00 = stereo<br>01 = left record mux only<br>10 = right record mux only<br>11 = mute left and right |
| | 8 | R2MBST | 0 (OFF) | **Record Mux to Headphone Mixer Boost Control**<br>1 = +20dB<br>0 = 0dB |

**Table 13 Record PGA Routing Control**

## AUTOMATIC LEVEL CONTROL

The WM9714L has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

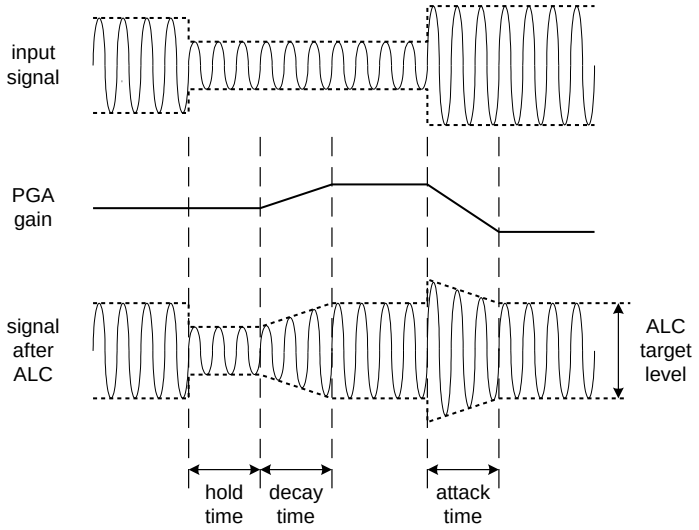



**Figure 19 ALC Operation**

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively.

### HOLD TIME

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two ($2^n$) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

### DECAY (GAIN RAMP-UP) TIME

Decay time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two ($2^n$) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

### ATTACK (GAIN RAMP-DOWN) TIME

Attack time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to –15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two ($2^n$) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 62h<br>ALC / Noise Gate Control | 15:14 | ALCSEL | 00<br>(OFF) | ALC function select<br>00 = ALC off (PGA gain set by register)<br>01 = Right channel only<br>10 = Left channel only<br>11 = Stereo (PGA registers unused) |
| | 13:11 | MAXGAIN | 111<br>(+30dB) | PGA gain limit for ALC<br>111 = +30dB<br>110 = +24dB<br>….(6dB steps)<br>001 = -6dB<br>000 = -12dB |
| | 10:9 | ZCTIMEOUT | 11 | Programmable zero cross timeout (delay for 12.288MHz BITCLK):<br>11: 2^17 * tbitclk (10.67 ms)<br>10: 2^16 * tbitclk (5.33 ms)<br>01: 2^15 * tbitclk (2.67 ms)<br>00: 2^14 * tbitclk (1.33 ms) |
| 60h<br>ALC Control | 15:12 | ALCL | 1011<br>(-12dB) | ALC target – sets signal level at ADC input<br>0000 = -28.5dB FS<br>0001 = -27.0dB FS<br>… (1.5dB steps)<br>1110 = -7.5dB FS<br>1111 = -6dB FS |
| | 11:8 | HLD | 0000<br>(0ms) | ALC hold time before gain is increased.<br>0000 = 0ms<br>0001 = 2.67ms<br>0010 = 5.33ms<br>… (time doubles with every step)<br>1111 = 43.691s |
| | 7:4 | DCY | 0011<br>(192ms) | ALC decay (gain ramp-up) time<br>0000 = 24ms<br>0001 = 48ms<br>0010 = 96ms<br>… (time doubles with every step)<br>1010 or higher = 24.58s |
| | 3:0 | ATK | 0010<br>(24ms) | ALC attack (gain ramp-down) time<br>0000 = 6ms<br>0001 = 12ms<br>0010 = 24ms<br>… (time doubles with every step)<br>1010 or higher = 6.14s |

**Table 14 ALC Control**

### MAXIMUM GAIN

The MAXGAIN register sets the maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

### PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

(Note: If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used).

### NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM9714L has a noise gate function that prevents noise pumping by comparing the signal level at the input pins (i.e. before the record PGA) against a noise gate threshold, NGTH. Provided that the noise gate function is enabled (NGAT = 1), the noise gate cuts in when:

Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dB] < NGTH [dB]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet). If the NGG bit is set, the ADC output is also muted when the noise gate cuts in.

Table 15 summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 62h<br>ALC / Noise Gate Control | 7 | NGAT | 0 | Noise gate function enable<br>1 = enable<br>0 = disable |
| | 5 | NGG | 0 | Noise gate type<br>0 = PGA gain held constant<br>1 = mute ADC output |
| | 4:0 | NGTH(4:0) | 00000 | Noise gate threshold<br>00000: -76.5dBFS<br>00001: -75dBFS<br>… 1.5 dB steps<br>11110: -31.5dBFS<br>11111: -30dBFS |

**Table 15 Noise Gate Control**

# AUDIO DACS

## STEREO DAC

The WM9714L has a stereo sigma-delta DAC that achieves high quality audio playback at low power consumption. Digital tone control, adaptive bass boost and 3-D enhancement functions operate on the digital audio data before it is passed to the stereo DAC. (Contrary to the AC'97 specification, they have no effect on analogue input signals or signals played through the auxiliary DAC. Nevertheless, the ID2 and ID5 bits in the reset register, 00h, are set to '1' to indicate that the WM9714L supports tone control and bass boost.)

The DAC output has a PGA for volume control. The DAC sample rate can be controlled by writing to a control register (see "Variable Rate Audio / Sample Rate Conversion"). It is independent of the ADC sample rate.

When not in use the DACs can be separately powered down using the Powerdown register bits DACL and DACR (register 3Ch, bits [7:6]).

### STEREO DAC VOLUME

The volume of the DAC output signal is controlled by a PGA (Programmable Gain Amplifier). Each DAC can be mixed into the headphone, speaker and mono mixer paths (see "Audio Mixers") controlled by register 0Ch.

Each DAC-to-mixer path has an independent mute bit. When all DAC-to-mixer paths are muted the DAC PGA is muted automatically.

When not in use the DAC PGAs can be powered down using the Powerdown register bits DACL and DACR (register 3Ch, bits [7:6]).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0Ch<br>DAC Volume | 15 | D2H | 1 | **DAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | D2S | 1 | **DAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 13 | D2M | 1 | **DAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 12:8 | DACL VOL | 01000 (0dB) | **Left DAC to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |
| | 4:0 | DACR VOL | 01000 (0dB) | **Right DAC to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |
| 5Ch<br>Additional Functions (2) | 15 | AMUTE | 0 | **DAC Automute Status (Read-Only)**<br>0 = DAC not muted<br>1 = DAC auto-muted |
| | 7 | AMEN | 0 | **DAC Automute Control**<br>0 = Disabled<br>1 = Enabled (DAC automatically muted when digital input is zero) |

**Table 16 Stereo DAC Volume Control**

## TONE CONTROL / BASS BOOST

The WM9714L provides separate controls for bass and treble with programmable gains and filter characteristics. This function operates on digital audio data before it is passed to the audio DACs.

Bass control can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function.

Treble, linear bass and 3D enhancement can all produce signals that exceed full-scale. In order to avoid limiting under these conditions, it is recommended to set the DAT bit to attenuate the digital input signal by 6dB. The gain at the outputs should be increased by 6dB to compensate for the attenuation. Cut-only tone adjustment (i.e. bass and treble gains ≤ 0) and adaptive bass boost cannot produce signals above full-scale and therefore do not require the DAT bit to be set.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| 20h<br>DAC Tone Control | 15 | BB | 0 | **Bass Mode Control**<br>0 = Linear bass control<br>1 = Adaptive bass boost | |
| | 12 | BC | 0 | **Bass Cut-off Frequency Control**<br>0 = Low (130Hz at 48kHz sampling)<br>1 = High (200Hz at 48kHz sampling) | |
| | 11:8 | BASS | 1111 (off) | **Bass Intensity Control** | |
| | | | | BB=0 | BB=0 |
| | | | | 0000 = +9dB<br>0001 = +9dB<br>… (1.5dB steps)<br>0111 = 0dB<br>… (1.5dB steps)<br>1011-1110 = -6dB<br>1111 = Bypass (off) | 0000 = +9dB<br>0001 = +9dB<br>… (1.5dB steps)<br>0111 = 0dB<br>… (1.5dB steps)<br>1011-1110 = -6dB<br>1111 = Bypass (off) |
| | 6 | DAT | 0 | **Pre-DAC Attenuation Control**<br>0 = 0dB<br>1 = -6dB | |
| | 4 | TC | 0 | **Treble Cut-off Frequency Control**<br>0 = High (8kHz at 48kHz sampling)<br>1 = Low (4kHz at 48kHz sampling) | |
| | 3:0 | TRBL | 1111 (off) | **Treble Intensity Control**<br>0000 = +9dB<br>0001 = +9dB<br>… (1.5dB steps)<br>0111 = 0dB<br>… (1.5dB steps)<br>1011-1110 = -6dB<br>1111 = Bypass (off) | |

**Table 17 DAC Tone Control**

**Note:**

1. All cut-off frequencies change proportionally with the DAC sample rate.

### 3D STEREO ENHANCEMENT

The 3D stereo enhancement function artificially increases the separation between the left and right channels by amplifying the (L-R) difference signal in the frequency range where the human ear is sensitive to directionality. The programmable 3D depth setting controls the degree of stereo expansion introduced by the function. Additionally, the upper and lower limits of the frequency range used for 3D enhancement can be selected using the 3DFILT control bits.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 40h<br>General Purpose | 13 | 3DE | 0<br>(disabled) | **3D Enhancement Control**<br>1 = Enabled<br>0 = Disabled |
| 1Eh<br>DAC 3D Control | 5 | 3DLC | 0 | **3D Lower Cut-off Frequency Control**<br>1 = High (500Hz at 48kHz sampling)<br>0 = Low (200Hz at 48kHz sampling) |
| | 4 | 3DUC | 0 | **3D Upper Cut-off Frequency Control**<br>1 = Low (1.5kHz at 48kHz sampling)<br>0 = High (2.2kHz at 48kHz sampling) |
| | 3:0 | 3DDEPTH | 0000 | **3D Depth Control**<br>0000 = 0%<br>… (6.67% steps)<br>1111 = 100% |

**Table 18 Stereo Enhancement Control**

**Note:**

1. All cut-off frequencies change proportionally with the DAC sample rate.

## VOICE DAC

VXDAC is a 16-bit mono DAC intended for playback of Rx voice signals input via the PCM interface. Performance has been optimised for operating at 8ks/s or 16ks/s. The VXDAC will function at other sample rates up to 48ks/s, but this is not recommended.

The analogue output of VXDAC is routed directly into the output mixers. The signal gain into each mixer can be adjusted at the mixer inputs using control register 18h.

When not in use the VXDAC can be powered down using the Powerdown register bit VXDAC (register 3Ch, bit 12).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3Ch<br>Powerdown (1) | 12 | VXDAC | 1 | **VXDAC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| 18h<br>VXDAC Output Control | 15 | V2H | 1 | **VXDAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14:12 | V2HVOL | 010<br>(0dB) | **VXDAC to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 11 | V2S | 1 | **VXDAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 10:8 | V2SVOL | 010<br>(0dB) | **VXDAC to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 7 | V2M | 1 | **VXDAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6:4 | V2MVOL | 010<br>(0dB) | **VXDAC to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |

**Table 19 VXDAC Control**

## AUXILIARY DAC

AUXDAC is a simple 12-bit mono DAC. It can be used to generate DC signals (with the numeric input written into a control register), or AC signals such as telephone-quality ring tones or system beeps (with the input signal supplied through an AC-Link slot). In AC mode (XSLE = 1), the input data is binary offset coded; in DC mode (XSLE = 0), there is no offset.

The analogue output of AUXDAC is routed directly into the output mixers. The signal gain into each mixer can be adjusted at the mixer inputs using control register 12h. In slot mode (XSLE = 1), the AUXDAC also supports variable sample rates (See “Variable Rate Audio / Sample Rate Conversion”).

When not in use the auxiliary DAC can be powered down using the Powerdown register bit AUXDAC (register 3Ch, bit 11).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3Ch<br>Powerdown (1) | 11 | AUXDAC | 0 | **AUXDAC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| 64h<br>AUXDAC Input Control | 15 | XSLE | 0 | **AUXDAC Input Select Control**<br>0 = From AUXDACVAL[11:0] (for DC signals)<br>1 = From AC-Link (for AC signals) |
| | 14:12 | AUXDAC SLT | 000 | **AUXDAC Input Control (XSLE=1)**<br>000 = Slot 5, bits 8-19<br>001 = Slot 6, bits 8-19<br>010 = Slot 7, bits 8-19<br>011 = Slot 8, bits 8-19<br>100 = Slot 9, bits 8-19<br>101 = Slot 10, bits 8-19<br>110 = Slot 11, bits 8-19<br>111 = Reserved |
| | 11:0 | AUXDAC VAL | 000h | **AUXDAC Input Control (XSLE=0)**<br>000h = Minimum<br>FFFh = Full scale |
| 1Ah<br>AUXDAC Output Control | 15 | A2H | 1 | **AUXDAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14:12 | A2HVOL | 010<br>(0dB) | **AUXDAC to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 11 | A2S | 1 | **AUXDAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 10:8 | A2SVOL | 010<br>(0dB) | **AUXDAC to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 7 | A2M | 1 | **AUXDAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6:4 | A2MVOL | 010<br>(0dB) | **AUXDAC to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |

**Table 20 AUXDAC Control**

## VARIABLE RATE AUDIO / SAMPLE RATE CONVERSION

By using an AC'97 Rev2.2 compliant audio interface, the WM9714L can record and playback at all commonly used audio sample rates, and offer full split-rate support (i.e. the DAC, ADC and AUXDAC sample rates are completely independent of each other – any combination is possible).

The default sample rate is 48kHz. If the VRA bit in register 2Ah is set, then other sample rates can be selected by writing to registers 2Ch, 32h and 2Eh. The AC-Link continues to run at 48k frames per second irrespective of the sample rate selected. However, if the sample rate is less than 48kHz, then some frames do not carry an audio sample.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 2Ah<br>Extended Audio Stat/Ctrl | 0 | VRA | 0 (OFF) | **Variable Rate Audio Control**<br>1 = Enable VRA<br>0 = Disable VRA (ADC and DAC run at 48kHz)<br>**Note:** When VRA=1, sample rates are controlled by 2Ch, 2Eh and 32h |
| 2Ch<br>Audio DAC Sample Rate | 15:0 | DACSR | BB80h<br>(48kHz) | **Stereo DAC Sample Rate Control**<br>1F40h = 8kHz<br>2B11h = 11.025kHz<br>2EE0h = 12kHz<br>3E80h = 16kHz<br>5622h = 22.05kHz<br>5DC0h = 24kHz<br>7D00h = 32kHz<br>AC44h = 44.1kHz<br>BB80h = 48kHz<br>Any other value defaults to the nearest supported sample rate |
| 32h<br>Audio ADC Sample Rate | 15:0 | ADCSR | BB80h<br>(48kHz) | **Stereo ADC Sample Rate Control**<br>Values as DACSR |
| 2Eh<br>AUXDAC Sample Rate | 15:0 | AUXDACSR | BB80h<br>(48kHz) | **AUXDAC Sample Rate Control**<br>Values as DACSR |

**Table 21 Audio Sample Rate Control**

**Note:**

Changing the ADC and / or DAC sample rate will only be effective if the ADCs and DACs are enabled and powered up before the sample rate is changed. This is done by setting the relevant bits in registers 26h and 3Ch, as well as the VRA bit in register 2Ah.

The process is as follows:

1. Enable and power up ADCs and or DACs in registers 26h and 3Ch.
2. Enable VRA bit in 2Ah, bit 0.
3. Change the sample rate in the respective register.

## AUDIO INPUTS

The following sections give an overview of the analogue audio input pins and their function. See "Applications Information" for more information on recommended external components.

## LINE INPUT

The LINEL and LINER inputs are designed to record line level signals, and/or to mix into one of the analogue outputs.

Both pins are directly connected to the record selector. The record PGA adjusts the recording volume, controlled by register 12h or by the ALC function.

For analogue mixing, the line input signals pass through a separate PGA, controlled by register 0Ah. The signals can be mixed into the headphone, speaker and mono mixer paths (see "Audio Mixers").

Each LINE-to-mixer path has an independent mute bit. When all LINE-to-mixer paths are muted the line PGA is muted automatically. When the line inputs are not used, the line PGA can be switched off to save power (see "Power Management").

LINEL and LINER are biased internally to the reference voltage VREF. Whenever the inputs are muted or the device placed into standby mode, the inputs remain biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0Ah | 15 | L2H | 1 | **LINE to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | L2S | 1 | **LINE to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 13 | L2M | 1 | **LINE to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 12:8 | LINEL VOL | 01000 (0dB) | **LINEL to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |
| | 4:0 | LINER VOL | 01000 (0dB) | **LINER to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |

**Table 22 Line Input Control**

Additionally, line inputs can be used as single-ended microphone inputs through the record mux to provide a click-less ALC function by bypassing offset introduced through the microphone pre-amps. Note that the line inputs to the mixers should all be deselected if this is input configuration is used.

## MICROPHONE INPUT

### MICROPHONE PRE-AMPS

There are two microphone pre-amplifiers, MPA and MPB, which can be configured in a variety of ways to accommodate up to 3 selectable differential microphone inputs or 2 differential microphone inputs operating simultaneously for stereo or noise cancellation. The microphone input circuit is shown in Figure 20.

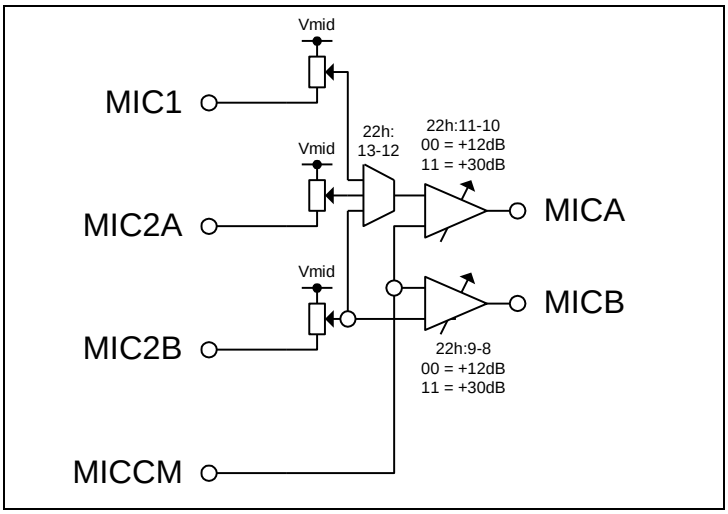



**Figure 20 Microphone Input Circuit**

The input pins used for the microphones are MIC1, MICCM, MIC2A and MIC2B. Note that input pins MIC2A and MIC2B are multi-function inputs and must be configured for use as microphone inputs when required. This is achieved using MICCMPSEL[1:0] in register 22h (see Table 23). The input to microphone pre-amp A can be selected from any of the three microphone inputs MIC1, MIC2A and MIC2B using MPASEL[1:0]. Each pre-amp has independent boost control from +12dB to +30dB in four steps. This is controlled by MPABST[1:0] and MPBBST[1:0].

When not in use each microphone pre-amp can be powered down using the Powerdown register bits MPA and MPB (register 3Eh, bits [1:0]). If disabled, the inputs are tied to Vmid (for MIC2A and MIC2B, this only applies if they are selected as microphone inputs – otherwise, they are left floating).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 22h | 15:14 | MICCMPSEL | 00 | **MIC2A/MIC2B Pin Function Control**<br>00 = MIC2A and MIC2B are mic inputs<br>01 = MIC2A mic input only<br>10 = MIC2B mic input only<br>11 = MIC2A and MIC2B are not mic inputs |
| | 13:12 | MPASEL | 00 | **MPA Pre-Amp Source Control**<br>00 = MIC1<br>01 = MIC2A<br>10 = MIC2B<br>11 = Reserved |
| | 11:10 | MPABST | 00 | **MPA Pre-Amp Volume Control**<br>00 = +12dB<br>01 = +18dB<br>10 = +24dB<br>11 = +30dB |
| | 9:8 | MPBBST | 00 | **MPB Pre-Amp Volume Control**<br>As MPABST |

**Table 23 Microphone Pre-amp Control**

## SINGLE MIC OPERATION

Up to three microphones can be connected in a single-ended configuration. Any one of the three MICs can be selected as the input to MPA using MPASEL[1:0] (Register 22h, bits 13:12). Only the microphone on MIC2B can be selected to MPB. Note that MPABST always sets the gain for the selected MPA input microphone. If MIC2B is the selected input for MPA it is recommended that MPB is disabled.

## DUAL MIC OPERATION

Up to two microphones can be connected in a dual differential configuration. This is suitable for stereo microphone or noise cancellation applications. Mic1 is connected between the MIC2A and MICCM inputs and mic2 is connected between the MIC2B and MICCM inputs as shown in Figure 21. Additionally, another microphone can be supported on MIC1 selected through the MPA input mux. Note that the microphones can be connected in a single-ended configuration.

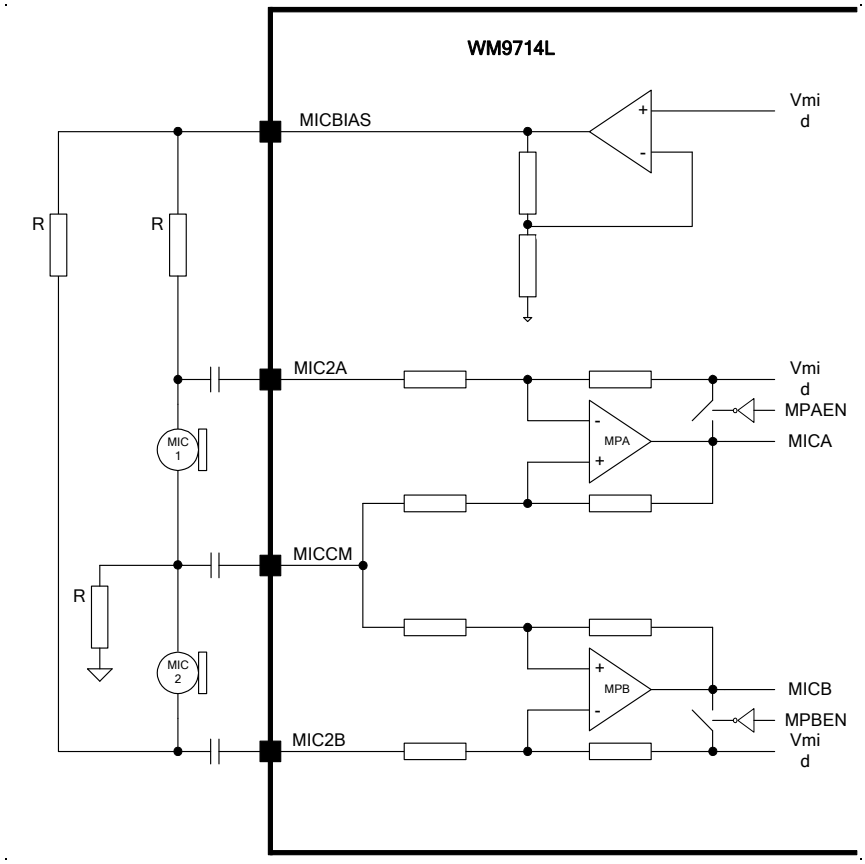



**Figure 21 Dual Microphone Configuration**

## MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to “Applications Information” for recommended external components. The MICBIAS voltage can be altered via MBVOL in register 22h. When MBVOL=0, MICBIAS=0.9*AVDD and when MBVOL=1, MICBIAS=0.75*AVDD.

The microphone bias is driven to a dedicated MICBIAS pin 28 and is enabled by MPOP1EN in register 22h. It can also be configured to drive out on GPIO8 pin 12 enabled by MPOP2EN in register 22h.

When not in use the microphone bias can be powered down using the Powerdown register bit MICBIAS (register 3Eh, bit 14).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 22h | 7 | MBOP2EN | 0 (Off) | **MICBIAS Output 2 Enable Control**<br>1 = Enable MICBIAS output on GPIO8 (pin 12)<br>0 = Disable MICBIAS output on GPIO8 (pin 12) |
| | 6 | MBOP1EN | 1 (On) | **MICBIAS Output 1 Enable Control**<br>1 = Enable MICBIAS output on MICBIAS (pin 28)<br>0 = Disable MICBIAS output on MICBIAS (pin 28) |
| | 5 | MBVOL | 0 | **MICBIAS Output Voltage Control**<br>1 = 0.75 x AVDD<br>0 = 0.9 x AVDD |

**Table 24 Microphone Bias Voltage Control**

The internal MICBIAS circuitry is shown in Figure 22. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

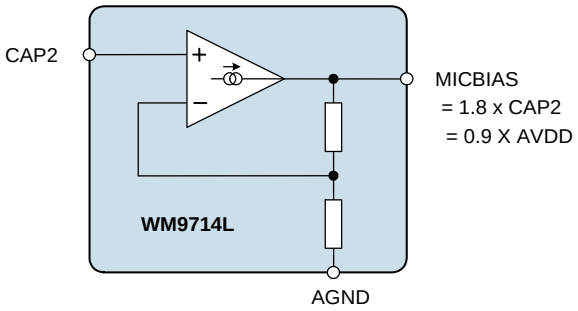



**Figure 22 Microphone Bias Schematic**

## MICBIAS CURRENT DETECT

The WM9714L includes a microphone bias current detect circuit with programmable thresholds for the microphone bias current, above which an interrupt will be triggered. There are two separate interrupt bits, MICDET to e.g. distinguish between one or two microphones connected to the WM9714L, and MICSHT to detect a shorted microphone (mic button press). The microphone current detect threshold is set by MCDTHR[2:0], for MICDET, and MCDSCTHR[1:0] for MICSHT. Thresholds for each code are shown in Table 25

When not in use the microphone bias current detect circuit can be powered down using the Powerdown register bit MCD (register 3Eh, bit 15).

See the GPIO and Interrupt Controller sections for details on the interrupt and status readback for these MICBIAS current detection features.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 22h | 4:2 | MCDTHR | 000 | **Mic Detect Threshold Control**<br>000 = 100µA<br>… (100µA steps)<br>111 = 800µA<br>**Note:** These values are for 3.3V supply and scale with supply voltage (AVDD). |
| | 1:0 | MCDSCTR | 00 | **Mic Detect Short Circuit Threshold Control**<br>00 = 600µA<br>01 = 1200uA<br>10 = 1800uA<br>11 = 2400µA<br>**Note:** These values are for 3.3V supply and scale with supply voltage (AVDD). |

**Table 25 Microphone Current Detect Control**

## MICROPHONE PGAS

The microphone pre-amps MPA and MPB drive into two microphone PGAs whose gain is controlled by register 0Eh. The PGA signals can be routed into the headphone mixers and the mono mixer, but not the speaker mixer (to prevent forming a feedback loop) controlled by register 10h. If the PGA signals are not selected as an input to any of the mixers, the outputs of the PGAs are muted automatically.

When not in use the microphone PGAs can be powered down using the Powerdown register bits MA and MB (register 3Eh, bits [3:2]).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0Eh<br>Mic PGA Volume | 12:8 | MICAVOL | 01000<br>(0dB) | **MICA PGA Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |
| | 4:0 | MICBVOL | 01000<br>(0dB) | **MICB PGA Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |

**Table 26 Microphone PGA Volume Control**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 10h<br>MIC Routing | 7 | MA2M | 1 | **MICA to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6 | MB2M | 1 | **MICB to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 5 | MIC2MBST | 0 | **MIC to Mono Mixer Boost Control**<br>1 = +20dB<br>0 = 0dB |
| | 4:3 | MIC2H | 11 | **MIC to Headphone Mixer Path Control**<br>00 = stereo<br>01 = MICA only<br>10 = MICB only<br>11 = mute MICA and MICB |
| | 2:0 | MIC2HVOL | 010<br>(0dB) | **MIC to Headphone Mixer Path Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |

**Table 27 Microphone PGA Routing Control**

## MONOIN INPUT

Pin 20 (MONOIN) is a mono input designed to connect to the receive path of a telephony device. The pin connects directly to the record selector for phone call recording (Note: to record both sides of a phone call, one ADC channel should record the MONOIN signal while the other channel records the MIC signal). The record PGA adjusts the recording volume, and is controlled by register 12h or by the ALC function (see “Record Gain” and “Automatic Level Control”).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 14h<br>Record Routing | 15:14 | R2H | 11 (mute) | **Record Mux to Headphone Mixer Path Control**<br>00 = stereo<br>01 = left record mux only<br>10 = right rec mux only<br>11=mute left and right |
| | 13:11 | R2HVOL | 010 (0dB) | **Record Mux to Headphone Mixer Path Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 10:9 | R2M | 11 (mute) | **Record Mux to Mono Mixer Path Control**<br>00 = stereo<br>01 = left record mux only<br>10 = right record mux only<br>11 = mute left and right |
| | 8 | R2MBST | 0 (0dB) | **Record Mux to Headphone Mixer Boost Control**<br>1 = +20dB<br>0 = 0dB |

**Table 28 Record PGA Routing Control**

To listen to the MONOIN signal, the signal passes through a separate PGA, controlled by register 08h. The signal can be routed into the headphone mixer (for normal phone call operation) and/or the speaker mixer (for speakerphone operation), but not into the mono mixer (to prevent forming a feedback loop). When the signal is not selected as an input to any of the mixers the output of the PGA is muted automatically.

When not in use, the MONOIN PGA can be powered down using the Powerdown register bit MOIN (register 3Eh, bit 4).

MONOIN is biased internally to the reference voltage VREF. Whenever the input is muted or the device placed into standby mode, the input remains biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 08h<br>MONOIN PGA Vol / Routing | 15 | M2H | 1 | **MONOIN to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | M2S | 1 | **MONOIN to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 12:8 | MONOIN VOL | 01000 (0dB) | **MONOIN to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB |

**Table 29 Mono PGA Control**

## PCBEEP INPUT

Pin 19 (PCBEEP) is a mono, line level input intended for externally generated signal or warning tones. It is routed directly to the record selector and all three output mixers, without an input amplifier. The signal gain into each mixer can be independently controlled, with a separate mute bit for each signal path.

PCBEEP is biased internally to the reference voltage VREF. When the signal is not selected as an input to any of the mixers the input remains biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 16h<br>PCBEEP input | 15 | B2H | 1 | **PCBEEP to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14:12 | B2HVOL | 010<br>(0dB) | **PCBEEP to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 11 | B2S | 1 | **PCBEEP to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 10:8 | B2SVOL | 010<br>(0dB) | **PCBEEP to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |
| | 7 | B2M | 1 | **PCBEEP to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6:4 | B2MVOL | 010<br>(0dB) | **PCBEEP to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB |

**Table 30 PCBEEP Control**

## DIFFERENTIAL MONO INPUT

PCBEEP and MONOIN inputs can be configured to provide a differential mono input. This is achieved by mixing the two inputs together using the headphone mixers or the speaker mixer. Note that the gain of the MONOIN PGA must match the gain of the PCBEEP mixer input to achieve a balanced differential mono input.

# AUDIO MIXERS

## MIXER OVERVIEW

The WM9714L has four separate low-power audio mixers to cover all audio functions required by smartphones, PDAs and handheld computers. These mixers are used to drive the audio outputs HPL, HPR, MONO, SPKL, SPKR, OUT3 and OUT4. There are also two inverters used to provide differential output signals (e.g. for driving BTL loads)

## HEADPHONE MIXERS

There are two headphone mixers, headphone mixer left and headphone mixer right (HPMIXL and HPMIXR). These mixers are the stereo output driver source. They are used to drive the stereo outputs HPL and HPR. They can also be used to drive SPKL and SPKR outputs and, when used in conjunction with OUT3 and OUT4, they can be configured to drive complementary signals through the two output inverters to support bridge-tied load (BTL) stereo loudspeaker outputs. The following signals can be mixed into the headphone path:

- MONOIN (controlled by register 08h, see “Audio Inputs”)
- LINEL/R (controlled by register 0Ah, see “Audio Inputs”)
- the output of the Record PGA (controlled by register 14h, see “Audio ADCs”, “Record Gain”)
- the stereo DAC signal (controlled by register 0Ch, see “Audio DACs”)
- the MIC signal (controlled by register 10h, see “Audio Inputs”)
- PC_BEEP (controlled by register 16h, see “Audio Inputs”)
- the VXDAC signal (controlled by register 18h, see “Audio DACs”)
- the AUXDAC signal (controlled by register 1Ah, see “Auxiliary DAC”)

In a typical smartphone application, the headphone signal is a mix of MONOIN / VXDAC and sidetone (for phone calls) and the stereo DAC signal (for music playback).

If not in use, the headphone mixers can be powered down using the Powerdown register bits HPLX and HPRX (register 3Ch, bits [3:2]).

## SPEAKER MIXER

The speaker mixer (SPKMIX) is a mono source. It is typically used to drive a mono loudspeaker in BTL configuration. The following signals can be mixed into the speaker path:

- MONOIN (controlled by register 08h, see “Audio Inputs”)
- LINEL/R (controlled by register 0Ah, see “Audio Inputs”)
- the stereo DAC signal (controlled by register 0Ch, see “Audio DACs”)
- PC_BEEP (controlled by register 16h, see “Audio Inputs”)
- the VXDAC signal (controlled by register 18h, see “Audio DACs”)
- the AUXDAC signal (controlled by register 1Ah, see “Auxiliary DAC”)

In a typical smartphone application, the speaker signal is a mix of AUXDAC (for system alerts or ring tone playback), MONOIN / VXDAC (for speakerphone function), and PC_BEEP (for externally generated ring tones).

Note that when selected the stereo input pairs LINEL/R and DACL/R are summed and attenuated by -6dB so that 0dBFS signals on each channel sum to give a 0dBFS mono signal.

If not in use, the speaker mixer can be powered down using the Powerdown register bit SPKX (register 3Ch, bit 1).

## MONO MIXER

The mono mixer drives the MONO pin. The following signals can be mixed into MONO:

- LINEL/R (controlled by register 0Ah, see “Audio Inputs”)
- the output of the Record PGA (controlled by register 14h, see “Audio ADCs”, “Record Gain”)
- the stereo DAC signal (controlled by register 0Ch, see “Audio DACs”)
- the MIC signal (controlled by register 10h, see “Audio Inputs”)
- PC_BEEP (controlled by register 16h, see “Audio Inputs”)
- the VXDAC signal (controlled by register 18h, see “Audio DACs”)
- the AUXDAC signal (controlled by register 12h, see “Auxiliary DAC”)

In a typical smartphone application, the MONO signal is a mix of the amplified microphone signal (possibly with Automatic Gain Control) and (if enabled) an audio playback signal from the stereo DAC or the auxiliary DAC.

Note that when selected the stereo input pairs LINEL/R and DACL/R are summed and attenuated by -6dB so that 0dBFS signals on each channel sum to give a 0dBFS mono signal.

If not in use, the mono mixer can be powered down using the Powerdown register bit MX (register 3Ch, bit 0).

## MIXER OUTPUT INVERTERS

There are two general purpose mixer output inverters, INV1 and INV2. Each inverter can be selected to drive HPMIXL, HPMIXR, SPKMIX, MONOMIX or { ( HPMIXL + HPMIXR ) / 2 }. The outputs of the inverters can be used to generate complimentary signals (to drive BTL configured loads) and to provide greater flexibility in output driver configurations. INV1 can be selected as the source for SPKL, MONO and OUT3 and INV2 as the source for SPKR and OUT4.

The input source for each inverter is selected using INV1[2:0] and INV2[2:0] in register 1Eh (see Table 31). If no input is selected, the inverter is powered down.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1Eh | 15:13 | INV1 | 000 (OFF) | **INV1 Source Select**<br>000 = No input (tri-stated)<br>001 = MONOMIX<br>010 = SPKMIX<br>011 = HPMIXL<br>100 = HPMIXR<br>101 = HPMIXMONO<br>110 = Reserved<br>111 = VMID |
| | 12:10 | INV2 | 000 (OFF) | **INV2 Source Select**<br>000 = No input (tri-stated)<br>001 = MONOMIX<br>010 = SPKMIX<br>011 = HPMIXL<br>100 = HPMIXR<br>101 = HPMIXMONO<br>110 = Reserved<br>111 = VMID |

**Table 31 Mixer Inverter Source Select**

## ANALOGUE AUDIO OUTPUTS

The following sections give an overview of the analogue audio output pins. The WM9714L has three outputs capable of driving loads down to 16Ω (headphone / line drivers) – HPL, HPR and MONO - and four outputs capable of driving loads down to 8Ω (loudspeaker / line drivers) – SPKL, SPKR, OUT3 and OUT4. The combination of output drivers, mixers and mixer inverters means that many output configurations can be supported.

For examples of typical output and mixer configurations, see "Typical Output Configurations". For more information on recommended external components, see "Applications Information".

Each output is driven by a PGA with a gain range of 0dB to -46.5dB in -1.5dB steps. Each PGA has an input source mux, mute and zero-cross detect circuit (delaying gain changes until a zero-cross is detected, or after time-out).

## HEADPHONE OUTPUTS – HPL AND HPR

The HPL and HPR outputs (pins 39 and 41) are designed to drive a 16Ω or 32Ω headphone load. They can also be used as line outputs. They can be used in and AC coupled or DC coupled (capless) configuration. The available input sources are HPMIXL/R and Vmid (see Table 32).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1Ch<br>Output PGA<br>Mux Select | 7:6 | HPL | 00 (Vmid) | **HPL Source Control**<br>00 = VMID<br>01 = No input (tri-stated if HPL is disabled in 3Eh)<br>10 = HPMIXL<br>11 = Reserved |
| | 5:4 | HPR | 00 (Vmid) | **HPR Source Control**<br>00 = VMID<br>01 = No input (tri-stated if HPR is disabled in 3Eh)<br>10 = HPMIXR<br>11 = Reserved |

**Table 32 HPL / HPR PGA Input Source**

The signal volume on HPL and HPR can be independently adjusted under software control by writing to register 04h.

When not in use HPL and HPR can be powered down using the Powerdown register bits HPL and HPR (register 3Eh, bits [10:9]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 04h<br>Headphone Volume | 15 | MUL | 1 (Mute) | **HPL Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | ZCL | 0 | **HPL Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 13:8 | HPLVOL | 000000 (0dB) | **HPL Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |
| | 7 | MUR | 1 (Mute) | **HPR Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6 | ZCR | 0 | **HPR Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 5:0 | HPRVOL | 000000 (0dB) | **HPR Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |

**Table 33 HPL / HPR PGA Control**

## MONO OUTPUT

The MONO output (pin 31) is designed to drive a 16Ω headphone load and can also be used as a line output. The available input sources are MONOMIX, INV1 and Vmid (see Table 34)

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1Ch<br>Output PGA Mux Select | 15:14 | MONO | 00 (Vmid) | **MONO Source Control**<br>00 = VMID<br>01 = No input (tri-stated if MONO is disabled in 3Eh)<br>10 = MONOMIX<br>11 = INV1 |

**Table 34 MONO PGA Input Source**

The signal volume on MONO can be independently adjusted under software control by writing to register 08h.

When not in use MONO can be powered down using the Powerdown register bit MONO (register 3Eh, bit 13). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 08h<br>MONO Vol | 7 | MU | 1 (Mute) | **MONO Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6 | ZC | 0 | **MONO Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 5:0 | MONOVOL | 000000<br>(0dB) | **MONO Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |

**Table 35 Mono PGA Control**

## SPEAKER OUTPUTS – SPKL AND SPKR

The SPKL and SPKR (pins 35 and 36) are designed to drive a loudspeaker load down to 8Ω and can also be used as line outputs and headphone outputs. They are designed to drive an 8Ω load AC coupled or in a BTL (capless) configuration. The available input sources are HPMIXL/R, SPKMIXL/R, INV1/2 and Vmid (see Table 36).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1Ch<br>Output PGA<br>Mux Select | 13:11 | SPKL | 000<br>(Vmid) | **SPKL Source Control**<br>000 = VMID<br>001 = No input (tri-stated if SPKL is disabled in 3Eh)<br>010 = HPMIXL<br>011 = SPKMIX<br>100 = INV1<br>All other values are reserved |
| | 10:8 | SPKR | 000<br>(Vmid) | **SPKR Source Control**<br>000 = VMID<br>001 = No input (tri-stated if SPKR is disabled in 3Eh)<br>010 = HPMIXR<br>011 = SPKMIX<br>100 = INV2<br>All other values are reserved |

**Table 36 SPKL / SPKR PGA Input Source**

The signal volume on SPKL and SPKR can be independently adjusted under software control by writing to register 02h.

When not in use SPKL and SPKR can be powered down using the Powerdown register bits SPKL and SPKR (register 3Eh, bits [8:7]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 02h Speaker Volume | 15 | MUL | 1 (Mute) | **SPKL Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | ZCL | 0 | **SPKL Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 13:8 | SPKLVOL | 000000 (0dB) | **SPKL Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |
| | 7 | MUR | 1 (Mute) | **SPKR Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6 | ZCR | 0 | **SPKR Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 5:0 | SPKRVOL | 000000 (0dB) | **SPKR Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |

**Table 37 SPKL / SPKR PGA Control**

**Note:**

1. For BTL speaker drive, it is recommended that both PGAs have the same gain setting.

## AUXILIARY OUTPUTS – OUT3 AND OUT4

The OUT3 and OUT4 outputs (pins 37 and 33) are designed to drive a loudspeaker load down to 8Ω and can also be used as line outputs and headphone outputs. They are designed to drive an 8Ω load AC coupled or in a BTL (cap-less) configuration and can be used as a mid-rail buffer to drive the headphone outputs in a cap-less DC configuration. The available input sources are INV1/2 and Vmid (see Table 38).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1Ch Output PGA Mux Select | 3:2 | OUT3 | 00 (Vmid) | **OUT3 Source Control**<br>00 = VMID<br>01 = No input (tri-stated if OUT3 is disabled in 3Eh)<br>10 = INV1<br>11 = Reserved |
| | 1:0 | OUT4 | 00 (Vmid) | **OUT4 Source Control**<br>00 = VMID<br>01 = No input (tri-stated if OUT4 is disabled in 3Eh)<br>10 = INV2<br>11 = Reserved |

**Table 38 OUT3 / OUT4 PGA Input Source**

The signal volume on OUT3 and OUT4 can be independently adjusted under software control by writing to register 06h.

When not in use OUT3 and OUT4 can be powered down using the Powerdown register bits OUT3 and OUT4 (register 3Eh, bits [11:12]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 06h<br>Speaker<br>Volume | 15 | MU4 | 1 (Mute) | **OUT4 Mute Control**<br>1 = Mute<br>0 = No mute |
| | 14 | ZC4 | 0 | **OUT4 Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 13:8 | OUT4VOL | 000000<br>(0dB) | **OUT4 Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |
| | 7 | MU3 | 1 (Mute) | **OUT3 Mute Control**<br>1 = Mute<br>0 = No mute |
| | 6 | ZC3 | 0 | **OUT3 Zero Cross Control**<br>1 = Zero cross enabled (change volume only on zero crossings, or after time-out)<br>0 = Zero cross disabled (change volume immediately) |
| | 5:0 | OUT3VOL | 000000<br>(0dB) | **OUT3 Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB |

**Table 39 OUT3 / OUT4 PGA Control**

## THERMAL SENSOR

The speaker and headphone outputs can drive very large currents. To protect the WM9714L from becoming too hot, a thermal sensor has been built in. If the chip temperature reaches approximately 150°C, and the TSHUT bit is cleared, and the GP11 bit is set, the WM9714L de-asserts TI, a virtual GPIO that can be set up to generate an interrupt to the CPU (see "GPIO and Interrupt Control").

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| 3Ch | 13 | TSHUT | 1 (disabled) | **Thermal Sensor Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| 4Eh | 11 | GP11 | 1 | **Thermal Sensor Polarity Control**<br>1 = Active Low<br>0 = Active High | |
| 54h | 11 | TI | 0 | **Thermal Sensor Status Bit (Virtual GPIO)**<br>See also "GPIO and Interrupt Control" section. | |
| | | | | GP11 = 1 (default) | GP11 = 0 |
| | | | | 1 = Temp < 150°C<br>0 = Temp > 150°C | 1 = Temp > 150°C<br>0 = Temp < 150°C |

**Table 40 Thermal Shutdown Control**

## JACK INSERTION AND AUTO-SWITCHING

In a phone application, a BTL ear speaker may be connected across MONO and HPL, a stereo headphone on HPL and HPR and stereo speakers on SPKL, SPKR, OUT3 and OUT4 (see Figure 23). Typically, only one of these three output devices is used at any given time: when no headphone is plugged in, the BTL ear speaker or stereo speakers are active, otherwise the headphone is used.

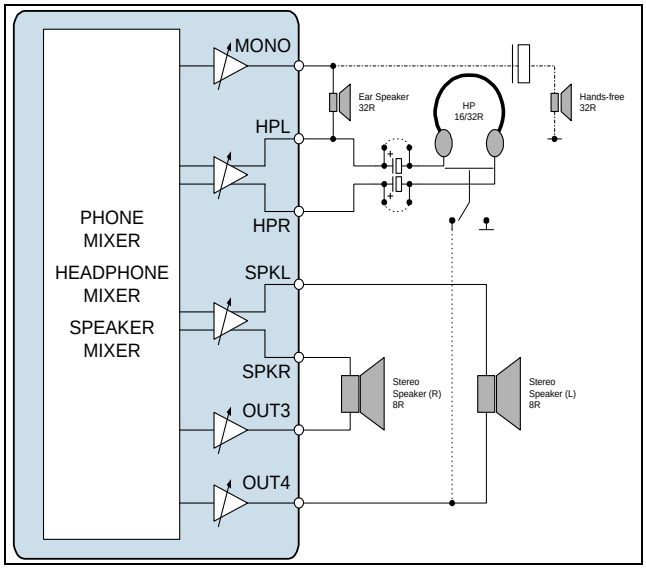



**Figure 23 Typical Output Configuration**

The presence of a headphone can be detected using one of GPIO1/6/7/8 (pins 44, 3, 11 & 12) and an external pull-up resistor (see Figure 35, page 114 for a circuit diagram). When the jack is inserted, the GPIO is pulled low by a switch on the socket. When the jack is removed the GPIO is pulled high by a resistor. If the JIEN bit is set, the WM9714L automatically switches between headphone and any other output configuration, typically ear speaker or stereo speaker that has been set up in the Powerdown and Output PGA Mux Select registers.

**Note:** Please refer to Application Note WAN 0182 for further information on jack detect configuration.

In addition to the typical configuration explained above, the WM9714L can also support automatic switching between the following three configurations set as BTL ear speaker and headphone.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 24h<br>Output Volume Mapping (Jack Insert) | 1:0 | EARSPKSEL | 00 | **Ear Speaker Source Control**<br>00 = Default, no ear speaker configuration selected.<br>01 = MONO and HPL driver selected as BTL ear speaker.<br>10 = OUT3 and HPL driver selected as BTL ear speaker.<br>11 = OUT4 and HPL driver selected as BTL ear speaker. |

**Table 41 Ear Speaker Configuration**

For example, if OUT4 and HPL is selected as the BTL ear speaker, the user should select EARSPKSEL = 3h, then OUT4 is tri-stated on jack insert to prevent sound across the ear speaker during headphone operation and HPL volume is set to OUT4 volume on jack out to ensure correct ear speaker operation. It should be noted that all other outputs except HPL, HPR and selected ear speaker driver are disabled and internally connected to VREF on jack insert. This maintains VREF at those outputs and helps prevent pops when the outputs are enabled.

Finally if the user wishes to DC couple the headphone outputs the user needs to select between OUT3 and OUT4 as the mid-rail output buffer driver. The selected mid-rail output buffer is enabled on jack insert. On jack out it defaults to whatever configuration has been set up in the Powerdown and Output PGA Mux Select registers.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 24h<br>Output Volume Mapping (Jack Insert) | 3:2 | DCDRVSEL | 00 | **Jack Insert Headphone DC Reference Control**<br>00 = AC coupled headphones, no DC source<br>01 = OUT3 is mid-rail output buffer<br>10 = Reserved<br>11 = OUT4 is mid-rail output buffer |

**Table 42 DC Coupled Headphone Configuration**

In summary:

JIEN not set: Outputs work as normal as selected in the Powerdown and Output PGA Mux Select registers.

JIEN set: On jack insertion, GPIO1/6/7/8 is pulled low, HPL and HPR are enabled, DCDRVSEL decides if the headphones are DC or AC coupled and configures OUT3 or OUT4 to suit, EARSPKSEL decides if MONO, OUT3 or OUT4 need to be tri-stated to ensure no sound out on the ear-speaker and finally all other outputs are disabled as explained above to prevent pops on re-enabling.

On jack removal, GPIO1/6/7/8 is pulled high, the outputs work as normal as selected in the Powerdown and Output PGA Mux Select registers except that HPL Volume is controlled by EARSPKSEL to ensure correct ear speaker operation.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 24h Output Volume Mapping (Jack Insert) | 4 | JIEN | 0 (OFF) | **Jack Insert Control**<br>0 = Disable jack insert circuitry<br>1 = Enable jack insert circuitry |
| 5Ah Additional Functions (1) | 7:6 | JSEL | 00 (GPIO1) | **Jack Detect Pin Input Control**<br>00 = GPIO1<br>01 = GPIO6<br>10 = GPIO7<br>11 = GPIO8 |

**Table 43 Jack Insertion / Auto-Switching (1)**

| JIEN | EARSPKSEL | DCDRVSEL | GPIO1 | MODE DESCRIPTION | HPL STATE | HPL VOLUME | HPR STATE | HPR VOLUME | MONO STATE | OUT3 STATE | OUT4 STATE | SPKL STATE | SPKR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | XX | XX | X | Jack Insert Detection Disabled. | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |
| 1 | 00 | 00 | 0 | Jack Insert Detection Enabled.<br>Headphone plugged in.<br>No Ear Speaker Selected.<br>AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | HZ | HZ | HZ | HZ |
| 1 | 01 | 00 | 0 | Jack Insert Detection Enabled.<br>Headphone plugged in.<br>MONO Ear Speaker Selected.<br>AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | Tri-Stated | HZ | HZ | HZ | HZ |
| 1 | 10 | 00 | 0 | Jack Insert Detection Enabled.<br>Headphone plugged in.<br>OUT3 Ear Speaker Selected.<br>AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | Tri-Stated | HZ | HZ | HZ |
| 1 | 11 | 00 | 0 | Jack Insert Detection Enabled.<br>Headphone plugged in.<br>OUT4 Ear Speaker Selected.<br>AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | HZ | Tri-Stated | HZ | HZ |
| 1 | 11 | 01 | 0 | Jack Insert Detection Enabled.<br>Headphone plugged in.<br>OUT4 Ear Speaker Selected.<br>OUT3 DC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | VMID | Tri-Stated | HZ | HZ |
| 1 | 00 | XX | 1 | Jack Insert Detection Enabled.<br>Headphone plugged out.<br>No Ear Speaker Selected. | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |
| 1 | 11 | XX | 1 | Jack Insert Detection Enabled. Headphone plugged out.<br>OUT4 Ear Speaker Selected. | User Controlled | OUT4 Volume | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |

**Table 44 Jack Insertion / Auto-Switching (2)**

## DIGITAL AUDIO (S/PDIF) OUTPUT

The WM9714L supports the S/PDIF standard. Pins 48 & 12 can be used to output the S/PDIF data. Note that pins 48 & 12 can also be used as GPIO pins. The GE5 & GE8 bits (register 56h, bit 5 & bit 8) select between GPIO and S/PDIF functionality for pins 48 & 12 respectively (see "GPIO and Interrupt Control").

Register 3Ah is a read/write register that controls S/PDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With the exception of V, this register should only be written to when the S/PDIF transmitter is disabled (S/PDIF bit in register 2Ah is '0'). Once the desired values have been written to this register, the contents should be read back to ensure that the sample rate in particular is supported, then S/PDIF validity bit SPCV in register 2Ah should be read to ensure the desired configuration is valid. Only then should the S/PDIF enable bit in register 2Ah be set. This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 2Ah<br>Extended Audio | 10 | SPCV | 0 | **S/PDIF Validity Bit (Read Only)**<br>1 = Valid<br>0 = Not valid |
| | 5:4 | SPSA | 01 | **S/PDIF Slot Assignment Control**<br>00 = Slots 3 and 4<br>01 = Slots 6 and 9<br>10 = Slots 7 and 8<br>11 = Slots 10 and 11<br>**Note:** This control is only valid when ADCO=0 in 5Ch |
| | 2 | SEN | 0 | **S/PDIF Output Enable Control**<br>1 = Enabled<br>0 = Disabled |
| 3Ah<br>S/PDIF Control Register | 15 | V | 0 | **S/PDIF Validity Bit**<br>1 = Valid<br>0 = Not valid |
| | 14 | DRS | 0 | Indicates that the WM9713L does not support double rate S/PDIF output (read-only) |
| | 13:12 | SPSR | 10 | Indicates that the WM9713L only supports 48kHz sampling on the S/PDIF output (read-only) |
| | 11 | L | 0 | **S/PDIF L-bit Control**<br>Programmed as required by user |
| | 10:4 | CC | 0000000 | **S/PDIF Category Code Control**<br>Category code; programmed as required by user |
| | 3 | PRE | 0 | **S/PDIF Pre-emphasis Indication Control**<br>0 = no pre-emphasis<br>1 = 50/15µs pre-emphasis |
| | 2 | COPY | 0 | **S/PDIF Copyright Indication Control**<br>0 = Copyright not asserted<br>1 = Copyright asserted |
| | 1 | AUDIB | 0 | **S/PDIF Non-audio Indication Control**<br>0 = PCM data<br>1 = Non-PCM data (e.g. DD or DTS) |
| | 0 | PRO | 0 | **S/PDIF Professional Indication Control**<br>0 = Consumer mode<br>1 = Professional mode |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 5Ch<br>Additional Function Control | 4 | ADCO | 0 | **S/PDIF Data Source Control**<br>0 = From SDATAOUT (pin 5)<br>1 = Output from audio ADC<br>**Note:** Slot selected by SPSA in 2Ah |

**Table 45 S/PDIF Output Control**

## AUXILIARY ADC

The WM9714L includes a very low power, 12-bit successive approximation type ADC which can be used for battery and auxiliary measurements. Three pins that can be used as auxiliary ADC inputs:

- MIC2A / COMP1 / AUX1 (pin 29)
- MIC2B / COMP2 / AUX2 (pin 30)
- AUX4 (pin 12)

Pins 29 and 30 are also used as comparator inputs (see “Battery Alarm and Analogue Comparators”), but auxiliary measurements can still be taken on these pins at any time.

Additionally, the speaker supply (SPKVDD) can be used as an auxiliary ADC input through an on-chip potential divider giving an input to the auxiliary ADC of SPKVDD/3. This input is referred to as the AUX3 input.

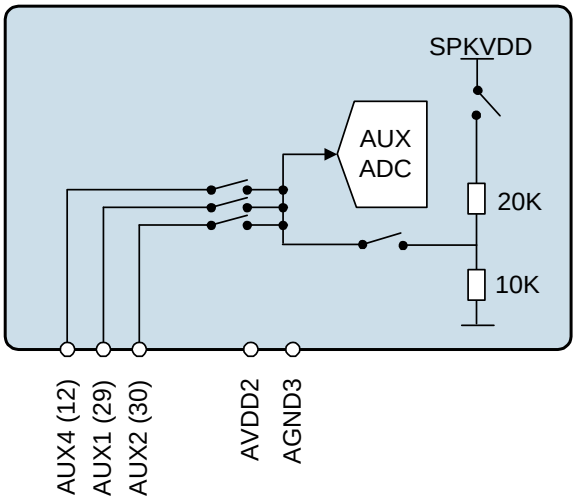



**Figure 24 Auxiliary ADC Inputs**

The AUX ADC is accessed and controlled through the AC-Link interface.

## AUXADC POWER MANAGEMENT

To save power, the AUXADC can be independently disabled when not used.

The AUXADC is powered-down using PADCPD, register 3Ch bit 15.

The state of the ADC is controlled using the bits described in Table 46.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3Ch | 15 | PADCPD | 1 = off | **AUXADC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| 78h | 15:14 | PRP | 00 | **Additional Enable for AUXADC**<br>00 = Disabled<br>01 = Reserved<br>10 = Reserved<br>11 = Enabled |

**Table 46 AUXADC Power Management**

## INITIATION OF MEASUREMENTS

The WM9714L AUXADC interface supports both polling routines and DMA (direct memory access) to control the flow of data from the AUX ADC to the host CPU.

In a polling routine, the CPU starts each measurement individually by writing to the POLL bit (register 74h, bit 9). This bit automatically resets itself when the measurement is completed.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 74h | 9 | POLL | 0 | **Poll Measurement Control**<br>Writing "1" initiates a measurement (when CTC=0) |
| | 8 | CTC | 0 | **AUXADC Measurement Mode**<br>0 = Polling mode<br>1 = Continuous mode (for DMA) |
| 76h | 9:8 | CR | 00 | **Continuous Mode Conversion Rate**<br>Continuous mode rate (DEL ≠ 1111)<br>00: 93.75 Hz (every 512 AC-Link frames)<br>01: 120 Hz (every 400 AC-Link frames)<br>10: 153.75 Hz (every 312 AC-Link frames)<br>11: 187.5Hz (every 256 AC-Link frames)<br><br>Continuous mode "fast rate" (DEL = 1111)<br>00: 8 kHz (every six AC-Link frames)<br>01: 12 kHz (every four AC-Link frames)<br>10: 24 kHz (every other AC-Link frame)<br>11: 48 kHz (every AC-Link frame) |

**Table 47 AUX ADC Control (Initiation of Measurements)**

In continuous mode (CTC = 1), the WM9714L autonomously initiates measurements (or sets of measurements) at the rate set by CR, and supplies the measured data to the CPU on one of the unused AC'97 time slots. DMA-enabled CPUs can write the data directly into a FIFO without any intervention by the CPU core. This reduces CPU loading and speeds up the execution of user programs in handheld systems.

Note that the measurement frequency in continuous mode is also affected by the DEL bits (see "Register Bits by Address", Register 76h). The faster rates achieved when DEL = 1111 may be useful when the ADC is used for multiple measurements.

### MEASUREMENT TYPES

The ADCSEL control bits determine which type of measurement is performed (see below).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 74h | 7 | ADCSEL_AUX4 | 0 | **AUX4 Measurement Enable Control**<br>0 = Disable AUX4 measurement (pin 12)<br>1 = Enable AUX4 measurement (pin 12) |
| | 6 | ADCSEL_AUX3 | 0 | **AUX3 Measurement Enable Control**<br>0 = Disable AUX3 measurement (SPKVDD/3)<br>1 = Enable AUX3 measurement (SPKVDD/3) |
| | 5 | ADCSEL_AUX2 | 0 | **AUX2 Measurement Enable Control**<br>0 = Disable AUX2 measurement (pin 30)<br>1 = Enable AUX2 measurement (pin 30) |
| | 4 | ADCSEL_AUX1 | 0 | **AUX1 Measurement Enable Control**<br>0 = Disable AUX1 measurement (pin 29)<br>1 = Enable AUX1 measurement (pin 29) |
| **Note:** Only one bit in 74h[7:4] should be set at any one time | | | | |

**Table 48 AUX ADC Control (Measurement Types)**

The WM9714L performs a single measurement – either in polling mode or continuously, as indicated by the CTC bit. The type of measurement is specified by the ADCSEL[7:4] bits. Only one of the ADCSEL[7:4] bits should be set.

### CONVERSION RATE

The AUXADC conversion rate is specified by the CR bits (reg 76h).

CR may be set to 93.75Hz (every 512 AC-Link Frames), 120Hz (every 400 AC-Link Frames), 153.75Hz (every 312 AC-Link frames) or 187.5Hz (every 256 AC-Link frames).

If only one ADRSEL[7:1] bit is set, each individual conversion occurs at the rate specified by CR.

If multiple ADRSEL[7:1] bits are set, the complete set of conversions requested is completed at the rate specified by CR.

### DATA READBACK

AUXADC measured data is stored in register 7Ah, and can be retrieved by reading the register in the usual manner (see “AC97 Interface”). Additionally, the data can also be passed to the controller on one of the AC-Link time slots not used for audio functions.

The output data word of the AUX ADC interface consists of three parts:

- 1 Unused bit (Ignore).
- Output data from the AUX ADC (12 bits)
- ADCSRC: 3 additional bits that indicate the source of the ADC data.

If the data is being read back using the polling method, there are several ways to determine when a measurement has finished:

- Reading back the POLL bit. If it has been reset to '0', then the measurement has finished.
- Monitoring the ADA signal (see "GPIO and Interrupt Control"). ADA goes high after every single conversion.
- Reading back 7Ah until the new data appears

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7Ah<br>or<br>AC-Link slot selected by SLT | 14:12 | ADCSRC | 000 | **AUXADC Source**<br>000 = No measurement<br>001 = Reserved<br>010 = Reserved<br>011 = Reserved<br>100 = COMP1/AUX1 measurement (pin 29)<br>101 = COMP2/AUX2 measurement (pin 30)<br>110 = AUX3 measurements (SPKVDD/3)<br>111 = AUX4 measurement (pin 12) |
| | 11:0 | ADCD | 000h | **AUXADC Data (Read-only)**<br>Bit 0 = LSB<br>Bit 11 = MSB |
| 78h | 9 | WAIT | 0 | **AUXADC Data Control**<br>0 = Overwrite existing data in 7Ah with new data<br>1 = Retain existing data in 7Ah until it is read |

**Table 49 AUX ADC Data**

To avoid losing data that has not yet been read, the WM9714L can delay overwriting register 7Ah with new conversions until the old data has been read. This function is enabled using the WAIT bit. If the SLEN bit is set to '1', then the ADC data appears on the AC-Link slot selected by the SLT control bits, as shown below. The Slot 0 'tag' bit corresponding to the selected time slot is asserted whenever there is new data on that slot.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 76h | 3 | SLEN | 0 | **Slot Readback Enable Control**<br>0 = Disabled (readback through register map only)<br>1 = Enabled (readback slot selected by SLT) |
| | 2:0 | SLT | 110 | **AC'97 Slot for AUXADC Data Control**<br>000 = Slot 5<br>001 = Slot 6<br>010 = Slot 7<br>011 = Slot 8<br>100 = Slot 9<br>101 = Slot 10<br>110 = Slot 11<br>111 = Reserved |

**Table 50 Returning AUX ADC Data Through an AC-Link Time Slot**

### MASK INPUT CONTROL

Sources of glitch noise, such as the signals driving an LCD display, may feed through to the AUX ADC inputs and affect measurement accuracy. In order to minimise this effect, a signal may be applied to MASK (pin 47 / pin 3) to delay or synchronise the sampling of any input to the ADC. The effect of the MASK signal depends on the MSK bits of register 78h, as described in Table 51.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 78h | 7:6 | MSK | 00 | **Mask Input Control**<br>see Table 52 for details |

**Table 51 MASK Input Control**

| MSK[1-0] | EFFECT OF SIGNAL ON MASK PIN |
|---|---|
| 00 | Mask has no effect on conversions GPIO input disabled (default) |
| 01 | Static; 'hi' on MASK pin stops conversions, 'lo' has no effect. |
| 10 | Edge triggered; rising or falling edge on MASK pin delays conversions<br>by an amount set in the DEL[3-0] register. Conversions are asynchronous to the MASK signal. |
| 11 | Synchronous mode; conversions wait until rising or falling edge on MASK initiates cycle; screen starts to be driven when the edge arrives, the conversion sample being taken a period set by DEL[3-0] after the edge. |

**Table 52 Controlling the MASK Feature**

Note that pin 47 / pin 3 can also be used as a GPIO (see "GPIO and Interrupt Control"), or to output the ADA signal (see below).

### ADA (ADC DATA AVAILABLE) SIGNAL

Whenever data becomes available from the AUXADC, the internal ADA (ADC Data Available) signal goes high and remains high until the data has been read from register 7Ah (if SLEN = 0) or until it has been sent out on an AC-Link slot (if SLEN = 1).

ADA goes high after every AUXADC conversion (in normal mode, COO=0)

ADA can be used to generate an interrupt, if the AW bit (register 52h, bit 12) is set (see "GPIO and Interrupt Control").

It is also possible to output the ADA signal on pin 47 / pin 3, if this pin is not used as a GPIO. The GE4/6 bit must be set to '0' to achieve this (see "GPIO and Interrupt Control").

Alternatively, ADA can be read from bit 12 in register 54h.

## ADDITIONAL FEATURES

### BATTERY ALARM AND ANALOGUE COMPARATORS

The battery alarm function differs from battery measurement in that it does not actually measure the battery voltage. Battery alarm only indicates “OK”, “Low” or “Dead”. The advantage of the battery alarm function is that it does not require a clock and can therefore be used in low-power sleep or standby modes.

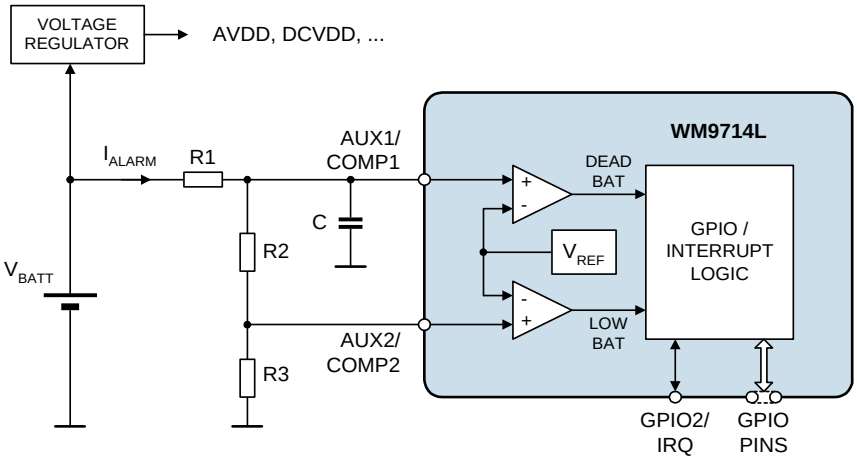



**Figure 25 Battery Alarm Example Schematic**

The typical schematic for a dual threshold battery alarm is shown above. This alarm has two thresholds, “dead battery” (COMP1) and “low battery” (COMP2). R1, R2 and R3 set the threshold voltages. Their values can be up to about 1MΩ in order to keep the battery current [$I_{ALARM} = V_{BATT} / (R1+R2+R3)$] to a minimum (higher resistor values may affect the accuracy of the system as leakage currents into the input pins become significant).

Dead battery alarm: COMP1 triggers when $V_{BATT} < VREF \times (R1+R2+R3) / (R2+R3)$

A dead battery alarm is the highest priority of interrupt in the system. It should immediately save all unsaved data and shut down the system. The GP15, GS15 and GW15 bits must be set to generate this interrupt.

Low battery alarm: COMP2 triggers when $V_{BATT} < VREF \times (R1+R2+R3) / R3$

A low battery alarm has a lower priority than a dead battery alarm. Since the threshold voltage is higher than for a dead battery alarm, there is enough power left in the battery to give the user a warning and/or shut down “gracefully”. When $V_{BATT}$ gets close to the low battery threshold, spurious alarms are filtered out by the COMP2 delay function.

The purpose of the capacitor C is to remove from the comparator inputs any high frequency noise or glitches that may be present on the battery (for example, noise generated by a charge pump). It forms a low pass filter with R1, R2 and R3.

$$\text{Low pass cutoff } f_c \text{ [Hz]} = 1/ (2\pi\, C \times (R1 \parallel (R2+R3)))$$

Provided that the cutoff frequency is several orders of magnitude lower than the noise frequency $f_n$, this simple circuit can achieve excellent noise rejection.

$$\text{Noise rejection [dB]} = 20 \log (f_n / f_c)$$

The circuit shown above also allows for measuring the battery voltage $V_{BATT}$. This is achieved simply by setting the AUXADC input to be either COMP1 (ADCSEL = 100) or COMP2 (ADCSEL = 101) (see also Auxiliary ADC Inputs).

The WM9714L has two on-chip comparators that can be used to implement a battery alarm function, or other functions such as a window comparator. Each comparator has one of its inputs tied to COMP1 (pin 29) or COMP2 (pin 30), and the other tied to a voltage reference. The voltage reference can be either internally generated (VREF = AVDD/2) or externally connected on AUX4 (pin 12).

The comparator output signals are passed to the GPIO logic block (see "GPIO and Interrupt Control" section), where they can be used to send an interrupt to the CPU via the AC-Link or via the IRQ pin, and / or to wake up the WM9714L from sleep mode. COMP1/AUX1 (pin 29) corresponds to GPIO bit 15 and COMP2/AUX2 (pin30) to bit 14.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 4Eh | 15 | CP1 | 1 | **COMP1 Polarity Control**<br>0: Alarm when COMP1 voltage is below VREF<br>1: Alarm when COMP1 voltage is above VREF<br>**Note:** see also "GPIO and Interrupt Control" |
| | 14 | CP2 | 1 | **COMP2 Polarity Control**<br>0: Alarm when COMP2 voltage is below VREF<br>1: Alarm when COMP2 voltage is above VREF<br>**Note:** see also "GPIO and Interrupt Control" |
| 5Ah | 15:13 | COMP2 DEL | 000 | **Low Battery Alarm Delay Control**<br>000 = No delay<br>001 = $2^{13}$ AC-link frames (0.17s)<br>010 = $2^{14}$ AC-link frames (0.34s)<br>011 = $2^{15}$ AC-link frames (0.68s)<br>100 = $2^{16}$ AC-link frames (1.4s)<br>101 = $2^{17}$ AC-link frames (2.7s)<br>110 = $2^{18}$ AC-link frames (5.5s)<br>111 = $2^{19}$ AC-link frames (10.9s) |

**Table 53 Comparator Control**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 5Ch<br>Additional Analogue Functions | 14 | C1REF | 0 | **Comparator 1 Reference Voltage Select**<br>0 = AVDD/2<br>1 = AUX4 (pin 12) |
| | 13:12 | C1SRC | 00 | **Comparator 1 Signal Source**<br>00 = AVDD/2 when C1REF=1, else COMP1 powered down<br>01 = COMP1/AUX1 (pin 29)<br>10 = COMP2/AUX2 (pin 30)<br>11 = Reserved |
| | 11 | C2REF | 0 | **Comparator 2 Reference Voltage Select**<br>0 = AVDD/2<br>1 = AUX4 (pin 12) |
| | 10:9 | C2SRC | 00 | **Comparator 2 Signal Source**<br>00 = AVDD/2 when C2REF=1, else COMP2 powered down<br>01 = COMP1/AUX1 (pin 29)<br>10 = COMP2/AUX2 (pin 30)<br>11 = Reserved |

**Table 54 Comparator Reference and Source Control**

### COMP2 DELAY FUNCTION

COMP2 has an optional delay function for use when the input signal is noisy. When COMP2 triggers and the delay is enabled (i.e. COMP2DEL is non-zero), then GPIO bit 14 does not change state immediately, and no interrupt is generated. Instead, the WM9714L starts a delay timer and checks COMP2 again after the delay time has passed. If COMP2 is still active, then the GPIO bit is set and an interrupt may be generated (depending on the state of the GW14 bit). If COMP2 is no longer active, the GPIO bit is not set, i.e. all register bits are as if COMP2 had never triggered.

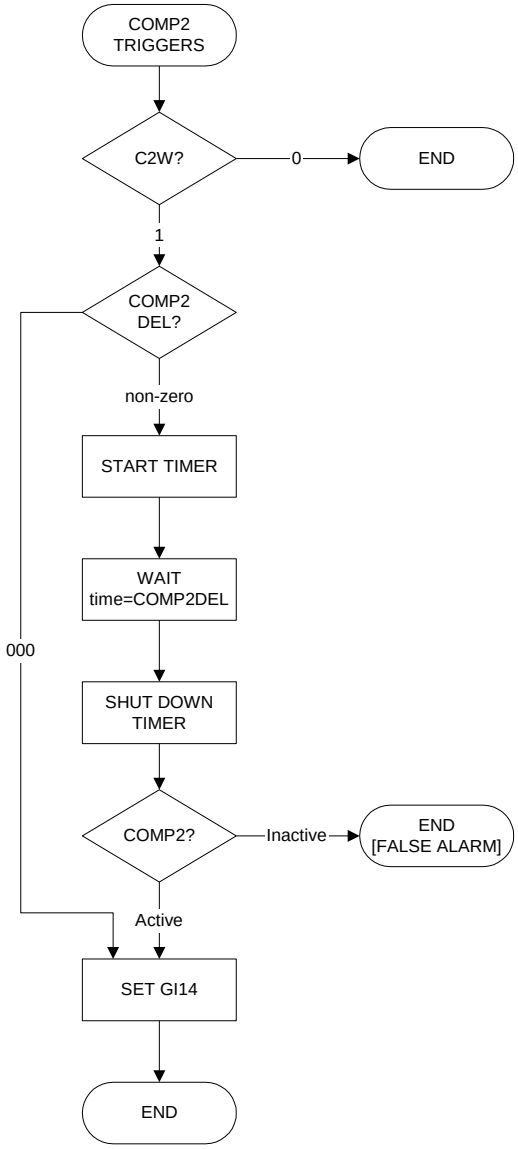



**Figure 26 COMP2 Delay Flow Chart**

## GPIO AND INTERRUPT CONTROL

The WM9714L has eight GPIO pins that operate as defined in the AC'97 Revision 2.2 specification. Each GPIO pin can be set up as an input or as an output, and has corresponding bits in register 54h and in slot 12. The state of a GPIO output is determined by sending data through slot 12 of outgoing frames (SDATAOUT). Data can be returned from a GPIO input by reading the register bit, or examining slot 12 of incoming frames (SDATAIN). GPIO inputs can be made sticky, and can be programmed to generate an interrupt, transmitted either through the AC-Link or through a dedicated, level-mode interrupt pin (GPIO2/IRQ, pin 45).

In addition, the GPIO pins 1, 3, 4 and 5 can be used for the PCM interface by setting bit 15 of register 36h (see "PCM Audio Data Formats" section). Setting this bit disables any GPIO functions selected on these pins.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 36h<br>PCM CODEC Control | 15 | CTRL | 0 | **GPIO Pin Configuration Control**<br>0 = GPIO pins used as GPIOs<br>1 = GPIO pins used as PCM interface<br>**Note:** For PCM interface, one or more of these pins (depending on master/slave/partial master mode) must be set up as an output by writing to register 4Ch (see Table 57) |
| 56h<br>GPIO Pin Sharing | 8:2 | GE# | 1 (GPIO) | **Toggle GPIO pin function**<br>0: secondary function enabled<br>1: GPIO enabled |

**Table 55 GPIO Additional Function Control**

GPIO pins 2 to 8 are multi-purpose pins that can also be used for other (non-GPIO / -PCM) purposes, e.g. as a S/PDIF output. This is controlled by register 56h (see Table 58).

Note that GPIO6/7/8 each have an additional function independent of the GPIO / auxiliary functions discussed above. If these pins are to be used as GPIO then the independent function needs to be disabled using its own control registers, e.g. to use pin 11 as a GPIO then the RESETB function needs to be disabled (RSTDIS, register 5Ah, bit 8).

Independently of the GPIO pins, the WM9714L also has seven virtual GPIOs. These are signals from inside the WM9714L, which are treated as if they were GPIO input signals. From a software perspective, virtual GPIOs are the same as GPIO pins, but they cannot be set up as outputs, and are not tied to an actual pin. This allows for simple, uniform processing of different types of signals that may generate interrupts (e.g. battery warnings, jack insertion, high-temperature warning, or GPIO signals).

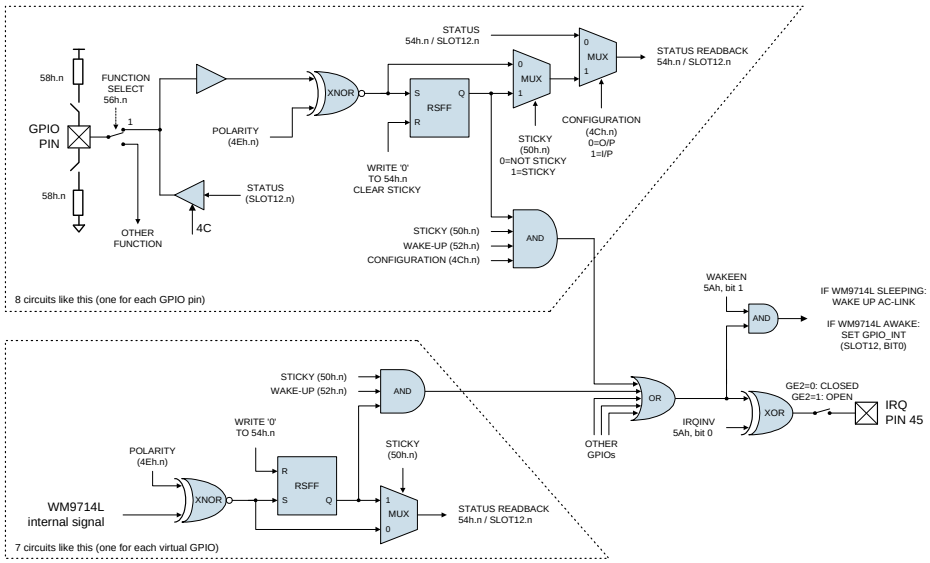



**Figure 27 GPIO Logic**

| GPIO BIT | SLOT 12 BIT | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|---|
| 1 | 5 | GPIO Pin | 44 | GPIO1 |
| 2 | 6 | GPIO Pin | 45 | GPIO2 / IRQ<br>enabled only when pin not used as IRQ |
| 3 | 7 | GPIO Pin | 46 | GPIO3 |
| 4 | 8 | GPIO Pin | 47 | GPIO4 / ADA / MASK<br>enabled only when pin not used as ADA |
| 5 | 9 | GPIO Pin | 48 | GPIO5 / S/PDIF_OUT<br>enabled only when pin not used as S/PDIF_OUT |
| 6 | 10 | GPIO Pin | 3 | GPIO6 / ADA / MASK<br>Enabled only when pin not used as ADA |
| 7 | 11 | GPIO Pin | 11 | GPIO7 |
| 8 | 12 | GPIO Pin | 12 | GPIO8 / S/PDIF_OUT<br>enabled only when pin not used as S/PDIF_OUT |
| 9 | 13 | Virtual GPIO | - [MICDET] | Internal microphone bias current detect, generates an interrupt above a threshold (see MICBIAS Current Detect) |
| 10 | 14 | Virtual GPIO | - [MICSHT] | Internal shorted microphone detect, generates an interrupt above a threshold (see MICBIAS Current Detect) |
| 11 | 15 | Virtual GPIO | - [Thermal Cutout] | Internal thermal cutout signal, indicates when internal temperature reaches approximately 150°C (see “Thermal Sensor”) |
| 12 | 16 | Virtual GPIO | - [ADA] | Internal ADA (ADC Data Available) Signal<br>enabled only when AUXADC is active |
| 14 | 18 | Virtual GPIO | - [COMP2] | Internal COMP2 output (Low Battery Alarm)<br>enabled only when COMP2 is on |
| 15 | 19 | Virtual GPIO | - [COMP1] | Internal COMP1 output (Dead Battery Alarm)<br>enabled only when COMP1 is on |

**Table 56 GPIO Bits and Pins**

**Note:** GPIO7 (Pin 11) has an independent RESETB function. This must be disabled using RSTDIS (Register 5Ah, bit 8) before using Pin 11 as a GPIO.

The properties of the GPIOs are controlled through registers 4Ch to 52h, as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| 4Ch | n | GCn | 1 | **GPIO Pin Configuration Control**<br>0 = Output<br>1 = Input (GC9-15 are always inputs) | |
| 4Eh | n | GPn | 1 | **GPIO Pin Polarity / Type** (Note 1) | |
| | | | | Input (GCn = 1) | Input (GCn = 1) |
| | | | | 0 = Active low<br>1 = Acitve high | 0 = Active low<br>1 = Acitve high |
| 50h | n | GSn | 0 | **GPIO Pin Sticky Control**<br>0 = Not sticky<br>1 = Sticky | |
| 52h | n | GWn | 0 | **GPIO Pin Wake-up Control**<br>0 = No wake-up (no interrupts generated by GPIO)<br>1 = Wake-up (generate interrupts from GPIO) | |
| 54h | n | GIn | N/A | **GPIO Pin Status**<br>Read = Returns status of GPIO<br>Write = Writing 0 clears sticky bits | |

**Table 57 GPIO Control**

**Note 1:** Excludes GP11. For Thermal Sensor Polarity Control (GP11) see Table 40 on page 59.

The following procedure is recommended for handling interrupts:

When the controller receives an interrupt, check register 54h. For each GPIO bit in descending order of priority, check if the bit is '1'. If yes, execute corresponding interrupt routine, then write '0' to corresponding bit in 54h. If no, continue to next lower priority GPIO. After all GPIOs have been checked, check if interrupt still present or no. If yes, repeat procedure. If no, then jump back to process that ran before the interrupt.

If the system CPU cannot execute such an interrupt routine, it may be preferable to switch internal signals directly onto the GPIO pins. However, in this case the interrupt signals cannot be made sticky, and more GPIO pins are tied up both on the WM9714L and on the CPU.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 56h<br>GPIO pins function select | 2 | GE2 | 1 | **GPIO2 (Pin 45) Function Control**<br>0 = Pin 45 is not controlled by GPIO logic<br>1 = Pin 45 is controlled by GPIO logic<br>**Note:** When GE2=0,<br>set GC2=0 in 4Ch to output IRQ |
| | 4 | GE4 | 1 | **GPIO4 (Pin 47) Function Control**<br>0 = Pin 47 is not controlled by GPIO logic<br>1 = Pin 47 is controlled by GPIO logic<br>**Note:** When GE4=0,<br>set GC4=0 in 4Ch to output ADA<br>set GC4=1 in 4Ch to input MASK |
| | 5 | GE5 | 1 | **GPIO5 (Pin 48) Function Control**<br>0 = Pin 48 is not controlled by GPIO logic<br>1 = Pin 48 is controlled by GPIO logic<br>**Note:** When GE5=0,<br>set GC5=0 in 4Ch to output S/PDIF |
| | 6 | GE6 | 1 | **GPIO6 (Pin 3) Function Control**<br>0 = Pin 3 is not controlled by GPIO logic<br>1 = Pin 3 is controlled by GPIO logic<br>**Note:** When GE6=0,<br>set GC6=0 in 4Ch to output ADA signal<br>set GC6=1 in 4Ch to input MASK signal |
| | 8 | GE8 | 1 | **GPIO8 (Pin 12) Function Control**<br>0 = Pin 12 is not controlled by GPIO logic<br>1 = Pin 12 is controlled by GPIO logic<br>**Note:** When GE8=0,<br>set GC8=0 in 4Ch to output S/PDIF |

**Table 58 Using GPIO Pins for Non-GPIO Functions**

# POWER MANAGEMENT

## INTRODUCTION

The WM9714L includes the standard power down control register defined by the AC'97 specification (register 26h). Additionally, it also allows more specific control over the individual blocks of the device through register Powerdown registers 3Ch and 3Eh. Each particular circuit block is active when both the relevant bit in register 26h AND the relevant bit in the Powerdown registers 3Ch and 3Eh are set to '0'.

Note that the default power-up condition is all OFF.

## AC97 CONTROL REGISTER

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 26h<br>Powerdown/ Status register | 14 | PR6 | 1 (disabled) | **Output PGAs Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 13 | PR5 | 1 (disabled) | **Internal Clock Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 12 | PR4 | 1 (disabled) | **AC-Link Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 11 | PR3 | 1 (disabled) | **Analogue Disable Control**<br>1 = Disabled<br>0 = Enabled<br>**Note:** This control disables VREF, input PGAs, DACs, ADCs, mixers and outputs |
| | 10 | PR2 | 1 (disabled) | **Input PGAs and Mixers Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 9 | PR1 | 1 (disabled) | **Stereo DAC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 8 | PR0 | 1 (disabled) | **Stereo ADC and Record Mux Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 3 | REF | 0 | **VREF Ready (Read Only)**<br>1 = VREF ready<br>0 = VREF not ready |
| | 2 | ANL | 0 | **Analogue Mixers Ready (Read Only)**<br>1 = Analogue mixers ready<br>0 = Analogue mixers not ready |
| | 1 | DAC | 0 | **Stereo DAC Ready (Read Only)**<br>1 = DAC ready<br>0 = DAC not ready |
| | 0 | ADC | 0 | **Stereo ADC Ready (Read Only)**<br>1 = ADC ready<br>0 = ADC not ready |

**Table 59 Powerdown and Status Register (Conforms to AC'97 Rev 2.2)**

## EXTENDED POWERDOWN REGISTERS

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3Ch Powerdown (1) | 15 | PADCPD | 1 (disabled) | **AUXADC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 14 | VMID1M | 1 (disabled) | **1Meg VMID String Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 13 | TSHUT | 1 (disabled) | **Thermal Shutdown Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 12 | VXDAC | 1 (disabled) | **Voice DAC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 11 | AUXDAC | 1 (disabled) | **AUXDAC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 10 | VREF | 1 (disabled) | **VREF Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 9 | PLL | 1 (disabled) | **PLL Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 7 | DACL | 1 (disabled) | **Left DAC Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 6 | DACR | 1 (disabled) | **Right DAC Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 5 | ADCL | 1 (disabled) | **Left ADC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 4 | ADCR | 1 (disabled) | **Right ADC Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 3 | HPLX | 1 (disabled) | **Left Headphone Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 2 | HPRX | 1 (disabled) | **Right Headphone Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 1 | SPKX | 1 (disabled) | **Speaker Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 0 | MX | 1 (disabled) | **Mono Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled |
| **Note:** When analogue inputs or outputs are disabled, they are internally connected to VREF through a large resistor (VREF=AVDD/2 except when VREF and VMID1M are both OFF). This maintains the potential at that node and helps to eliminate pops when the pins are re-enabled. | | | | |

**Table 60 Extended Power Down Register (1) (Additional to AC'97 Rev 2.2)**

**Note:** When disabling a PGA, always ensure that it is muted first.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3Eh Powerdown (2) | 15 | MCD | 1 (disabled) | **Microphone Current Detect Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 14 | MICBIAS | 1 (disabled) | **Microphone Bias Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 13 | MONO | 1 (disabled) | **MONO PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 12 | OUT4 | 1 (disabled) | **OUT4 PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 11 | OUT3 | 1 (disabled) | **OUT3 PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 10 | HPL | 1 (disabled) | **HPL PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 9 | HPR | 1 (disabled) | **HPR PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 8 | SPKL | 1 (disabled) | **SPKL PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 7 | SPKR | 1 (disabled) | **SPKR PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 6 | LL | 1 (disabled) | **LINEL PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 5 | LR | 1 (disabled | **LINER PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 4 | MOIN | 1 (disabled) | **MONOIN PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 3 | MA | 1 (disabled) | **MICA PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 2 | MB | 1 (disabled) | **MICB PGA Disable Control** (see Note 1)<br>1 = Disabled<br>0 = Enabled |
| | 1 | MPA | 1 (disabled) | **Mic Pre-amp MPA Disable Control**<br>1 = Disabled<br>0 = Enabled |
| | 0 | MPB | 1 (disabled) | **Mic Pre-amp MPB Disable Control**<br>1 = Disabled<br>0 = Enabled |
| **Note:** When analogue inputs or outputs are disabled, they are internally connected to VREF through a large resistor (VREF=AVDD/2 except when VREF and VMID1M are both OFF). This maintains the potential at that node and helps to eliminate pops when the pins are re-enabled. | | | | |

**Table 61 Extended Power Down Register (2) (Additional to AC'97 Rev 2.2)**

**Note:** When disabling a PGA, always ensure that it is muted first.

## ADDITIONAL POWER MANAGEMENT

Mixer output inverters: see “Mixer Output Inverters” section. Inverters are disabled by default.

### SLEEP MODE

Whenever the PR4 bit (reg. 26h) is set, the AC-Link interface is disabled, and the WM9714L is in sleep mode. There is in fact a very large number of different sleep modes, depending on the other control bits. For example, the low-power standby mode described below is a sleep mode. It is desirable to use sleep modes whenever possible, as this will save power. The following functions do not require a clock and can therefore operate in sleep mode:

- Analogue-to-analogue audio (DACs and ADCs unused), e.g. phone call mode
- GPIO and interrupts
- Battery alarm / analogue comparators

The WM9714L can awake from sleep mode as a result of

- A warm reset on the AC-Link (according to the AC’97 specification)
- A signal on a GPIO pin (if the pin is configured as an input, with wake-up enabled – see “GPIO and Interrupt Control” section)
- A virtual GPIO event such as battery alarm, etc. (see “GPIO and Interrupt Control” section)

### LOW-POWER STANDBY MODE

If all the bits in registers 26h, 3Ch and 3Eh are set except VMID1M (register 3Ch, bit 14), then the WM9714L is in low-power standby mode and consumes very little current. A 1MΩ resistor string remains connected across AVDD to generate VREF. This is necessary if the on-chip analogue comparators are used (see “Battery Alarm and Analogue Comparators” section), and helps shorten the delay between wake-up and playback readiness. If VREF is not required, the 1MΩ resistor string can be disabled by setting the VMID1M bit, reducing current consumption further.

### SAVING POWER AT LOW SUPPLY VOLTAGES

The analogue supplies to the WM9714L can run from 1.8V to 3.6V. By default, all analogue circuitry on the IC is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. However, at lower voltages, it is possible to save power by reducing the internal bias currents used in the analogue circuitry. This is controlled as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 5Ch | 6:5 | VBIAS | 00 | **Analogue Bias Optimization Control**<br>0X = Default bias current, optimized for 3.3V<br>10 = Low bias current, optimized for 2.5V<br>11 = Lowest bias current, optimized for 1.8V |

**Table 62 Analogue Bias Selection**

## POWER-ON RESET (POR)

The WM9714L has an internal power on reset (PORB) which ensures that a reset is applied to all registers until a supply threshold has been exceeded. The POR circuitry monitors the voltage for both AVDD and DCVDD and will release the internal reset signal once these supplies are both nominally greater than 1.36V. The internal reset signal is an AND of the PORB and RESETB input signal.

It is recommended that for operation of the WM9714L, all device power rails should be stable before configuring the device for operation.

## REGISTER MAP

| Reg | Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | Reset | 0 | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 6174h |
| 02h | Speaker Volume | MUL | ZCL | SPKLVOL | | | | | | MUR | ZCR | SPKRVOL | | | | | | 8080h |
| 04h | Headphone Volume | MUL | ZCL | HPLVOL | | | | | | MUR | ZCR | HPRVOL | | | | | | 8080h |
| 06h | OUT3/4 Volume | MU4 | ZC4 | OUT4VOL | | | | | | MU3 | ZC3 | OUT3VOL | | | | | | 8080h |
| 08h | MONO Vol & MONOIN PGA Vol / Routing | M2H | M2S | 0 | MONOINVOL | | | | | MU | ZC | MONOVOL | | | | | | C880h |
| 0Ah | LINEIN PGA Volume / Routing | L2H | L2S | L2M | LINELVOL | | | | | 0 | 0 | 0 | LINERVOL | | | | | E808h |
| 0Ch | DAC PGA Volume / Routing | D2H | D2S | D2M | DACLVOL | | | | | 0 | 0 | 0 | DACRVOL | | | | | E808h |
| 0Eh | MIC PGA Volume | 0 | 0 | 0 | MICAVOL | | | | | 0 | 0 | 0 | MICBVOL | | | | | 0808h |
| 10h | MIC Routing | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MA2M | MB2M | MIC2MBST | MIC2H | MIC2HVOL | | | | 00DAh |
| 12h | Record PGA Volume | RMU | GRL | (Extended) | RECVOLL | | | | | ZC | GRR | (Extended) | RECVOLR | | | | | 8000h |
| 14h | Record Routing / Mux Select | R2H | | R2HVOL | | R2M | | R2MBST | | 0 | RECBST | RECSL | | RECSR | | | | D600h |
| 16h | PCBEEP Volume / Routing | B2H | B2HVOL | | B2S | B2SVOL | | | | B2M | B2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 18h | VxDAC Volume / Routing | V2H | V2HVOL | | V2S | V2SVOL | | | | V2M | V2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 1Ah | AUXDAC Volume / Routing | A2H | A2HVOL | | A2S | A2SVOL | | | | A2M | A2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 1Ch | Output PGA Mux Select | MONO | | SPKL | | SPKR | | | | HPL | | HPR | | OUT3 | | OUT4 | | 0000h |
| 1Eh | DAC 3D Control & INV Mux Select | INVA | | | INVB | | | 0 | 0 | 0 | 0 | 3DLC | 3DUC | 3DDEPTH | | | | 0000h |
| 20h | DAC Tone Control | BB | 0 | 0 | BC | BASS | | | | 0 | DAT | 0 | TC | TRBL | | | | 0F0Fh |
| 22h | MIC Input Select & Bias / Detect Ctrl | MICCMPSEL | | MPASEL | | MPABST | | MPBBST | | MBOP2EN | MBOP1EN | MBVOL | MCDTHR | | | MCDSCTHR | | 0040h |
| 24h | Output Volume Mapping (Jack Insert) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | JIEN | DCDRVSEL | | EARSPKSEL | | 0000h |
| 26h | Powerdown Ctrl/Stat | 0 | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | 0 | 0 | 0 | 0 | REF | ANL | DAC | ADC | 7F00h |
| 28h | Extended Audio ID | ID1 | ID0 | 0 | 0 | REV1 | REV0 | AMAP | LDAC | SDAC | CDAC | 0 | 0 | VRM | SPDIF | DRA | VRA | 0405h |
| 2Ah | Ext'd Audio Stat/Ctrl | 0 | 0 | 0 | 0 | 0 | SPCV | 0 | 0 | 0 | 0 | SPSA | | 0 | SEN | 0 | VRA | 0410h |
| 2Ch | Audio DACs Sample Rate | DACSR (Audio DACs Sample Rate) | | | | | | | | | | | | | | | | BB80h |
| 2Eh | AUXDAC Sample Rate | AUXDACSR (Auxiliary DAC Sample Rate) | | | | | | | | | | | | | | | | BB80h |
| 32h | Audio ADCs Sample Rate | ADCSR (Audio ADCs Sample Rate) | | | | | | | | | | | | | | | | BB80h |
| 36h | PCM codec control | CTRL | MODE | | 0 | DIV | | | VDACOSR | CP | FSP | SEL | | WL | | FMT | | 4523h |
| 3Ah | SPDIF control | V | DRS | SPSR | | L | CC (Category Code) | | | | | | | PRE | COPY | AUDIB | PRO | 2000h |
| 3Ch | Powerdown (1) | PADCPD | VMID 1M | TSHUT | VXDAC | AUXDAC | VREF | PLL | 1 | DACL | DACR | ADCL | ADCR | HPLX | HPRX | SPKX | MX | FDFFh |
| 3Eh | Powerdown (2) | MCD | MIC BIAS | MONO | OUT4 | OUT3 | HPL | HPR | SPKL | SPKR | LL | LR | MOIN | MA | MB | MPA | MPB | FFFFh |
| 40h | General Purpose | 0 | 0 | 3DE | 0 | 0 | 0 | 0 | 0 | LB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000h |
| 42h | Fast Power-Up Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MONO | SPKL | SPKR | HPL | HPR | OUT3 | OUT4 | 0000h |
| 44h | MCLK / PLL Control | 0 | SEXT[6:4] | | | SEXT[3:0] | | | | CLKSRC | 0 | PENDIV | | | CLKBX2 | CLKAX2 | CLKMUX | 0080h |
| 46h | MCLK / PLL Control | N[3:0] | | | | LF | SDM | DIVSEL | DIVCTL | 0 | PGADDR | | | PGDATA | | | | 0000h |
| 4Ch | GPIO Pin Configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | GC8 | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | 0 | FFFEh |
| 4Eh | GPIO Pin Polarity / Type | C1P | C2P | PP | AP | TP | SP | MP | GP8 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | 1 | FFFFh |
| 50h | GPIO Pin Sticky | C1S | C2S | PS | AS | TS | SS | MS | GS8 | GS7 | GS6 | GS5 | GS4 | GS3 | GS2 | GS1 | 0 | 0000h |
| 52h | GPIO Pin Wake-Up | C1W | C2W | PW | AW | TW | SW | MW | GW8 | GW7 | GW6 | GW5 | GW4 | GW3 | GW2 | GW1 | 0 | 0000h |
| 54h | GPIO Pin Status | C1I | C2I | PI | AI | TI | SI | MI | GI8 | GI7 | GI6 | GI5 | GI4 | GI3 | GI2 | GI1 | 0 | GPIO pins |
| 56h | GPIO Pin Sharing | 1 | 1 | 1 | 1 | 1 | 1 | 1 | GE8 | 0 | GE6 | GE5 | GE4 | 0 | GE2 | 1 | 0 | FFFEh |
| 58h | GPIO Pull UP/DOWN Ctrl | PU8 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | 4000h |
| 5Ah | Additional Functions (1) | COMP2DEL | | | 0 | 0 | 0 | 0 | RSTDIS | JSEL | | HPMODE | | Die Revision | | WAKEEN | IRQ INV | 0000h |
| 5Ch | Additional Functions (2) | AMUTE | C1 REF | C1SRC | | C2 REF | C2SRC | | 0 | AMEN | VBIAS | | ADCO | HPF | 0 | ASS | | 0000h |
| 60h | ALC Control | ALCL (target level) | | | | HLD (hold time) | | | | DCY (decay time) | | | | ATK (attack time) | | | | B032h |
| 62h | ALC / Noise Gate Control | ALCSEL | MAXGAIN | | | ZCTIMEOUT | | | 0 | NGAT | 0 | NGG | NGTH (threshold) | | | | | 3E00h |
| 64h | AUXDAC input control | XSLE | AUXDACSLT | | | AUXDAC VAL | | | | | | | | | | | | 0000h |
| 74h | Digitiser Reg 1 | 0 | 0 | 0 | 0 | 0 | 0 | POLL | CTC | ADCSEL | | | | | | | 0 | 0000h |
| 76h | Digitiser Reg 2 | 0 | 0 | 0 | 0 | 0 | 0 | CR | | DEL | | | | SLEN | SLT | | | 0006h |
| 78h | Digitiser Reg 3 | PRP | | 0 | 0 | 0 | 0 | WAIT | 0 | MSK | | 0 | 0 | 0 | 0 | 0 | 1 | 0001h |
| 7Ah | Digitiser Read Back | 0 | ADCSRC | | | ADCD (AUXADC DATA) | | | | | | | | | | | | 0000h |
| 7Ch | Vendor ID1 | ASCII character "W" | | | | | | | | ASCII character "M" | | | | | | | | 574Dh |
| 7Eh | Vendor ID2 | ASCII character "L" | | | | | | | | Device Identifier | | | | | | | | 4C13h |

**Table 63 WM9714L Register Map**

**Note:** Register 46h provides access to a sub-page address system to set the $S_{PLL}$[6:0] and K[21:0] register bits (see Table 6).

## REGISTER BITS BY ADDRESS

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 00h<br>read-only | 14:10 | SE [4:0] | 11000 | Indicates a CODEC from Cirrus Logic | Intel's AC'97 Component Specification, Revision 2.2, page 50 |
| | 9:6 | ID9:6 | 0101 | Indicates 18 bits resolution for ADCs and DACs | |
| | 5 | ID5 | 1 | Indicates that the WM9714L supports bass boost | |
| | 4 | ID4 | 1 | Indicates that the WM9714L has a headphone output | |
| | 3 | ID3 | 0 | Indicates that the WM9714L does not support simulated stereo | |
| | 2 | ID2 | 1 | Indicates that the WM9714L supports bass and treble control | |
| | 1 | ID1 | 0 | Indicates that the WM9714L does not support modem functions | |
| | 0 | ID0 | 0 | Indicates that the WM9714L does not have a dedicated microphone ADC | |

**Register 00h** is a read-only register. Writing any value to this register resets all registers to their default, but does not change the contents of reg. 00h. Reading the register reveals information about the CODEC to the driver, as required by the AC'97 Specification, Revision 2.2

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 02h | 15 | MUL | 1 (mute) | **SPKL Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Audio Outputs |
| | 14 | ZCL | 0 (disabled) | **SPKL Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 13:8 | SPKLVOL | 000000 (0dB) | **SPKL Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |
| | 7 | MUR | 1 (mute) | **SPKR Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6 | ZCR | 0 (disabled) | **SPKR Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 5:0 | SPKRVOL | 000000 (0dB) | **SPKR Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |

**Register 02h** controls the output pins SPKL and SPKR.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 04h | 15 | MUL | 1 (mute) | **HPL Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Audio Outputs |
| | 14 | ZCL | 0 (disabled) | **HPL Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 13:8 | HPL VOL | 000000 (0dB) | **HPL Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |
| | 7 | MUR | 1 (mute) | **HPR Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6 | ZCR | 0 (disabled) | **HPR Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 5:0 | HPR VOL | 000000 (0dB) | **HPR Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |

**Register 04h** controls the headphone output pins, HPL and HPR.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 06h | 15 | MU4 | 1 (mute) | **OUT4 Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Audio Outputs |
| | 14 | ZC4 | 0 (disabled) | **OUT4 Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 13:8 | OUT4VOL | 000000 (0dB) | **OUT4 Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |
| | 7 | MU3 | 1 (mute) | **OUT3 Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6 | ZC3 | 0 (disabled) | **OUT3 Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 5:0 | OUT3VOL | 000000 (0dB) | **OUT3 Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |

**Register 06h** controls the analogue output pins OUT3 and OUT4.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 08h | 15 | M2H | 1 (mute) | **MONOIN to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Inputs; Analogue Audio Outputs |
| | 14 | M2S | 1 (mute) | **MONOIN to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 12:8 | MONOINVOL | 01000 (0dB) | **MONOIN to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |
| | 7 | MU | 1 (mute) | **MONO Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6 | ZC | 0 (disabled) | **MONO Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | |
| | 5:0 | MONOVOL | 000000 (0dB) | **MONO Volume Control**<br>000000 = 0dB (maximum)<br>… (1.5dB steps)<br>011111 = -46.5dB<br>1xxxxx = -46.5dB | |

**Register 08h** controls the analogue output pin MONO and the analogue input pin MONOIN.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 0Ah | 15 | L2H | 1 (mute) | **LINE to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Inputs, Line Input |
| | 14 | L2S | 1 (mute) | **LINE to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 13 | L2M | 1 (mute) | **LINE to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 12:8 | LINELVOL | 01000 (0dB) | **LINEL to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |
| | 4:0 | LINERVOL | 01000 (0dB) | **LINER to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |

**Register 0Ah** controls the analogue input pins LINEL and LINER.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 0Ch | 15 | D2H | 1 (mute) | **DAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Audio DACs |
| | 14 | D2S | 1 (mute) | **DAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 13 | D2M | 1 (mute) | **DAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 12:8 | DACLVOL | 01000 (0dB) | **Left DAC to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |
| | 4:0 | DACRVOL | 01000 (0dB) | **Right DAC to Mixers Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |

**Register 0Ch** controls the audio DACs (but not AUXDAC).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 0Eh | 12:8 | MICAVOL | 01000 (0dB) | **MICA PGA Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | Analogue Inputs, Microphone Input |
| | 4:0 | MICBVOL | 01000 (0dB) | **MICB PGA Volume Control**<br>00000 = +12dB<br>… (1.5dB steps)<br>11111 = -34.5dB | |

**Register 0Eh** controls the microphone PGA volume (MICA and MICB).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 10h | 7 | MA2M | 1 (mute) | **MICA to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Inputs, Microphone Input |
| | 6 | MB2M | 1 (mute) | **MICB to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 5 | MIC2MBST | 0 (0dB) | **MIC to Mono Mixer Boost Control**<br>1 = +20dB<br>0 = 0dB | |
| | 4:3 | MIC2H | 11 (mute) | **MIC to Headphone Mixer Path Control**<br>00 = stereo<br>01 = MICA only<br>10 = MICB only<br>11 = mute MICA and MICB | |
| | 2:0 | MIC2HVOL | 010 (0dB) | **MIC to Headphone Mixer Path Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |

**Register 10h** controls the microphone routing (MICA and MICB).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | REFER TO |
|---|---|---|---|---|---|---|
| 12h | 15 | RMU | 1 (mute) | **Audio ADC Input Mute Control**<br>1 = Mute<br>0 = No mute | | Audio ADC, Record Gain |
| | 14 | GRL | 0 (standard) | **Left ADC PGA Gain Range Control**<br>1 = Extended<br>0 = Standard | | |
| | 13:8 | RECVOLL | 000000 (0dB) | **Left ADC Recording Volume Control** | | |
| | | | | Standard (GRL=0) | Extended (GRL=1) | |
| | | | | XX0000: 0dB<br>XX0001: +1.5dB<br>… (1.5dB steps)<br>XX1111: +22.5dB | 000000: -17.25dB<br>000001: -16.5dB<br>… (0.75dB steps)<br>111111: +30dB | |
| | 7 | ZC | 0 (disabled) | **ADC PGA Zero Cross Control**<br>1 = Zero cross enabled<br>0 = Zero cross disabled | | |
| | 6 | GRR | 0 (standard) | **Right ADC PGA Gain Range Control**<br>1 = Extended<br>0 = Standard | | |
| | 5:0 | RECVOLR | 000000 (0dB) | **Right ADC Recording Volume Control** | | |
| | | | | Standard (GRR=0) | Extended (GRR=1) | |
| | | | | XX0000: 0dB<br>XX0001: +1.5dB<br>… (1.5dB steps)<br>XX1111: +22.5dB | 000000: -17.25dB<br>000001: -16.5dB<br>… (0.75dB steps)<br>111111: +30dB | |

**Register 12h** controls the record volume.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 14h | 15:14 | R2H | 11 (mute) | **Record Mux to Headphone Mixer Path Control**<br>00 = stereo<br>01 = left record mux only<br>10 = right rec mux only<br>11=mute left and right | Audio ADC, Record Selector |
| | 13:11 | R2HVOL | 010 (0dB) | **Record Mux to Headphone Mixer Path Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 10:9 | R2M | 11 (mute) | **Record Mux to Mono Mixer Path Control**<br>00 = stereo<br>01 = left record mux only<br>10 = right record mux only<br>11 = mute left and right | |
| | 8 | R2MBST | 0 (0dB) | **Record Mux to Headphone Mixer Boost Control**<br>1 = +20dB<br>0 = 0dB | |
| | 6 | RECBST | 0 (0dB) | **ADC Record Boost Control**<br>1 = +20dB<br>0 = 0dB | |
| | 5:3 | RECSL | 000 (mic) | **Left Record Mux Source Control**<br>000 = MICA (pre-PGA)<br>001 = MICB (pre-PGA)<br>010 = LINEL (pre-PGA)<br>011 = MONOIN (pre-PGA)<br>100 = HPMIXL<br>101 = SPKMIC<br>110 = MONOMIX<br>111 = Reserved | |
| | 2:0 | RECSR | 000 (mic) | **Right Record Mux Source Control**<br>000 = MICA (pre-PGA)<br>001 = MICB (pre-PGA)<br>010 = LINEL (pre-PGA)<br>011 = MONOIN (pre-PGA)<br>100 = HPMIXL<br>101 = SPKMIC<br>110 = MONOMIX<br>111 = Reserved | |

**Register 14h** controls the.record selector and the ADC to mono mixer path.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 16h | 15 | B2H | 1 (mute) | **PCBEEP to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Analogue Inputs, PCBEEP Input |
| | 14:12 | B2HVOL | 010 (0dB) | **PCBEEP to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 11 | B2S | 1 (mute) | **PCBEEP to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 10:8 | B2SVOL | 010 (0dB) | **PCBEEP to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 7 | B2M | 1 (mute) | **PCBEEP to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6:4 | B2MVOL | 010 (0dB) | **PCBEEP to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |

**Register 16h** controls the analogue input pin PCBEEP.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 18h | 15 | V2H | 1 (mute) | **VXDAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Audio Mixers, Side Tone Control |
| | 14:12 | V2HVOL | 010 (0dB) | **VXDAC to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 11 | V2S | 1 (mute) | **VXDAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 10:8 | V2SVOL | 010 (0dB) | **VXDAC to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 7 | V2M | 1 (mute) | **VXDAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6:4 | V2MVOL | 010 (0dB) | **VXDAC to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |

**Register 18h** controls the output signal of the Voice DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 1Ah | 15 | A2H | 1 (mute) | **AUXDAC to Headphone Mixer Mute Control**<br>1 = Mute<br>0 = No mute | Auxiliary DAC |
| | 14:12 | A2HVOL | 010 (0dB) | **AUXDAC to Headphone Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 11 | A2S | 1 (mute) | **AUXDAC to Speaker Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 10:8 | A2SVOL | 010 (0dB) | **AUXDAC to Speaker Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |
| | 7 | A2M | 1 (mute) | **AUXDAC to Mono Mixer Mute Control**<br>1 = Mute<br>0 = No mute | |
| | 6:4 | A2MVOL | 010 (0dB) | **AUXDAC to Mono Mixer Volume Control**<br>000 = +6dB<br>… (+3dB steps)<br>111 = -15dB | |

**Register 1Ah** controls the output signal of the auxiliary DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 1Ch | 15:14 | MONO | 00 (VMID) | **MONO Source Control**<br>00 = VMID<br>01 = No input (tri-stated if MONO is disabled)<br>10 = MONOMIX<br>11 = INV1 | Analogue Audio Outputs |
| | 13:11 | SPKL | 000 (VMID) | **SPKL Source Control**<br>000 = VMID<br>001 = No input (tri-stated if SPKL is disabled)<br>010 = HPMIXL<br>011 = SPKMIX<br>100 = INV1<br>All other values are reserved | |
| | 10:8 | SPKR | 000 (VMID) | **SPKR Source Control**<br>000 = VMID<br>001 = No input (tri-stated if SPKR is disabled)<br>010 = HPMIXR<br>011 = SPKMIX<br>100 = INV2<br>All other values are reserved | |
| | 7:6 | HPL | 00 (VMID) | **HPL Source Control**<br>00 = VMID<br>01 = No input (tri-stated if HPL is disabled)<br>10 = HPMIXL<br>11 = Reserved | |
| | 5:4 | HPR | 00 (VMID) | **HPR Source Control**<br>00 = VMID<br>01 = No input (tri-stated if HPR is disabled)<br>10 = HPMIXR<br>11 = Reserved | |
| | 3:2 | OUT3 | 00 (VMID) | **OUT3 Source Control**<br>00 = VMID<br>01 = No input (tri-stated if OUT3 is disabled)<br>10 = INV1<br>11 = Reserved | |
| | 1:0 | OUT4 | 00 (VMID) | **OUT4 Source Control**<br>00 = VMID<br>01 = No input (tri-stated if OUT4 is disabled)<br>10 = INV2<br>11 = Reserved | |

**Register 1Ch** controls the inputs to the output PGAs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 1Eh | 15:13 | INV1 | 000 ($Z_H$) | **INV1 Source Select**<br>000 = No input (tri-stated)<br>001 = MONOMIX<br>010 = SPKMIX<br>011 = HPMIXL<br>100 = HPMIXR<br>101 = HPMIXMONO<br>110 = Reserved<br>111 = VMID | Audio DACs, 3D Stereo Enhancement; Analogue Audio Outputs |
| | 12:10 | INV2 | 000 ($Z_H$) | **INV2 Source Select**<br>000 = No input (tri-stated)<br>001 = MONOMIX<br>010 = SPKMIX<br>011 = HPMIXL<br>100 = HPMIXR<br>101 = HPMIXMONO<br>110 = Reserved<br>111 = VMID | |
| | 5 | 3DLC | 0 (low) | **3D Lower Cut-off Frequency Control**<br>1 = High (500Hz at 48kHz sampling)<br>0 = Low (200Hz at 48kHz sampling) | |
| | 4 | 3DUC | 0 (high) | **3D Upper Cut-off Frequency Control**<br>1 = Low (1.5kHz at 48kHz sampling)<br>0 = High (2.2kHz at 48kHz sampling) | |
| | 3:0 | 3DDEPTH | 0000 (0%) | **3D Depth Control**<br>0000 = 0%<br>… (6.67% steps)<br>1111 = 100% | |

**Register 1Eh** controls 3D stereo enhancement for the audio DACs and input muxes to the output inverters INV1 and INV2.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | REFER TO |
|---|---|---|---|---|---|---|
| 20h | 15 | BB | 0 (linear) | **Bass Mode Control**<br>0 = Linear bass control<br>1 = Adaptive bass boost | | Audio DACs, Tone Control / Bass Boost |
| | 12 | BC | 0 (low) | **Bass Cut-off Frequency Control**<br>0 = Low (130Hz at 48kHz sampling)<br>1 = High (200Hz at 48kHz sampling) | | |
| | 11:8 | BASS | 1111 (off0) | **Bass Intensity Control** | | |
| | | | | BB=0 | BB=1 | |
| | | | | 0000 = +9dB<br>0001 = +9dB<br>… (1.5dB steps)<br>0111 = 0dB<br>… (1.5dB steps)<br>1011-1110 = -6dB<br>1111 = Bypass (off) | 0000 = 15dB<br>… (1dB steps)<br>1110 = 1dB<br>1111 = Bypass (off) | |
| | 6 | DAT | 0 (0dB) | **Pre-DAC Attenuation Control**<br>0 = 0dB<br>1 = -6dB | | |
| | 4 | TC | 0 (high) | **Treble Cut-off Frequency Control**<br>0 = High (8kHz at 48kHz sampling)<br>1 = Low (4kHz at 48kHz sampling) | | |
| | 3:0 | TRBL | 1111 (off) | **Treble Intensity Control**<br>0000 = +9dB<br>0001 = +9dB<br>… (1.5dB steps)<br>0111 = 0dB<br>… (1.5dB steps)<br>1011-1110 = -6dB<br>1111 = Bypass (off) | | |

**Register 20h** controls the bass and treble response of the left and right audio DAC (but not AUXDAC).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 22h | 15:14 | MICCMP SEL | 00 (mics) | **MIC2A/MIC2B Pin Function Control**<br>00 = MIC2A and MIC2B are microphone inputs<br>01 = MIC2A microphone input only<br>10 = MIC2B microphone input only<br>11 = MIC2A and MIC2B are not microphone inputs | Analogue Inputs, Microphone Input |
| | 13:12 | MPASEL | 00 (MIC1) | **MPA Pre-Amp Source Control**<br>00 = MIC1<br>01 = MIC2A<br>10 = MIC2B<br>11 = Reserved | |
| | 11:10 | MPABST | 00 (12dB) | **MPA Pre-Amp Volume Control**<br>00 = +12dB<br>01 = +18dB<br>10 = +24dB<br>11 = +30dB | |
| | 9:8 | MPBBST | 00 (12dB) | **MPB Pre-Amp Volume Control**<br>00 = +12dB<br>01 = +18dB<br>10 = +24dB<br>11 = +30dB | |
| | 7 | MBOP2EN | 0 (Off) | **MICBIAS Output 2 Enable Control**<br>1 = Enable MICBIAS output on GPIO8 (pin 12)<br>0 = Disable MICBIAS output on GPIO8 (pin 12) | |
| | 6 | MBOP1EN | 1 (On) | **MICBIAS Output 1 Enable Control**<br>1 = Enable MICBIAS output on MICBIAS (pin 28)<br>0 = Disable MICBIAS output on MICBIAS (pin 28) | |
| | 5 | MBVOL | 0 (0.9xAVDD) | **MICBIAS Output Voltage Control**<br>1 = 0.75 x AVDD<br>0 = 0.9 x AVDD | |
| | 4:2 | MCDTHR | 000 (100uA) | **Mic Detect Threshold Control**<br>000 = 100µA<br>… (100µA steps)<br>111 = 800µA | |
| | 1:0 | MCDSCTHR | 00 (600uA) | **Mic Detect Short Circuit Threshold Control**<br>00 = 600µA<br>01 = 1200uA<br>10 = 1800uA<br>11 = 2400µA | |

**Register 22h** controls the microphone input configuration and microphone bias and detect configuration.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 24h | 4 | JIEN | 0 (disabled) | **Jack Insert Control**<br>0 = Disable jack insert circuitry<br>1 = Enable jack insert circuitry | Analogue Audio Outputs |
| | 3:2 | DCDRVSEL | 00 (AC) | **Jack Insert Headphone DC Reference Control**<br>00 = AC coupled headphones, no DC source<br>01 = OUT3 is mid-rail output buffer<br>10 = Reserved<br>11 = OUT4 is mid-rail output buffer | |
| | 1:0 | EARSPK SEL | 00 (none) | **Ear Speaker Source Control**<br>00 = No ear speaker<br>01 = MONO and HPL<br>10 = OUT3 and HPL<br>11 = OUT4 and HPL | |

**Register 24h** controls the output volume mapping on headphone jack insertion.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 26h | 14 | PR6 | 1 (OFF) | **Output PGAs Disable Control**<br>1 = Disabled<br>0 = Enabled | Power Management |
| | 13 | PR5 | 1 (OFF) | **Internal Clock Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 12 | PR4 | 1 (OFF) | **AC-Link Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 11 | PR3 | 1 (OFF) | **Analogue Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 10 | PR2 | 1 (OFF) | **Input PGAs and Mixers Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 9 | PR1 | 1 (OFF) | **Stereo DAC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 8 | PR0 | 1 (OFF) | **Stereo ADC and Record Mux Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 3 | REF | 0 | **VREF Ready (Read Only)**<br>1 = VREF ready<br>0 = VREF not ready | |
| | 2 | ANL | 0 | **Analogue Mixers Ready (Read Only)**<br>1 = Analogue mixers ready<br>0 = Analogue mixers not ready | |
| | 1 | DAC | 0 | **Stereo DAC Ready (Read Only)**<br>1 = DAC ready<br>0 = DAC not ready | |
| | 0 | ADC | 0 | **Stereo ADC Ready (Read Only)**<br>1 = ADC ready<br>0 = ADC not ready | |

**Register 26h** is for power management according to the AC'97 specification. Note that the actual state of many circuit blocks depends on both register 26h AND registers 3Ch and 3Eh.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 28h | 15:14 | ID | 00 | Indicates that the WM9714L is configured as the primary CODEC in the system. | Intel's AC'97 Component Specification, Revision 2.2, page 59 |
| | 11:10 | REV | 01 | Indicates that the WM9714L conforms to AC'97 Rev2.2 | |
| | 9 | AMAP | 0 | Indicates that the WM9714L does not support slot mapping | |
| | 8 | LDAC | 0 | Indicates that the WM9714L does not have an LFE DAC | |
| | 7 | SDAC | 0 | Indicates that the WM9714L does not have Surround DACs | |
| | 6 | CDAC | 0 | Indicates that the WM9714L does not have a Centre DAC | |
| | 3 | VRM | 0 | Indicates that the WM9714L does not have a dedicated, variable rate microphone ADC | |
| | 2 | SPDIF | 1 | Indicates that the WM9714L supports S/PDIF output | |
| | 1 | DRA | 0 | Indicates that the WM9714L does not support double rate audio | |
| | 0 | VRA | 1 | Indicates that the WM9714L supports variable rate audio | |

**Register 28h** is a read-only register that indicates to the driver which advanced AC'97 features the WM9714L supports.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 2Ah | 10 | SPCV | 1 (valid) | **S/PDIF Validity Bit (Read Only)**<br>1 = Valid<br>0 = Not valid | Digital Audio (S/PDIF) Output |
| | 5:4 | SPSA | 01 (slots 6, 9) | **S/PDIF Slot Assignment Control**<br>00 = Slots 3 and 4<br>01 = Slots 6 and 9<br>10 = Slots 7 and 8<br>11 = Slots 10 and 11 | |
| | 2 | SEN | 0 (OFF) | **S/PDIF Output Enable Control**<br>1 = Enabled<br>0 = Disabled | |
| | 0 | VRA | 0 (OFF) | **Variable Rate Audio Control**<br>1 = Enable VRA<br>0 = Disable VRA (ADC and DAC run at 48kHz) | |

**Register 2Ah** controls the S/PDIF output and variable rate audio.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 2Ch | all | DACSR | BB80h | **Stereo DAC Sample Rate Control**<br>1F40h = 8kHz<br>2B11h = 11.025kHz<br>2EE0h = 12kHz<br>3E80h = 16kHz<br>5622h = 22.05kHz<br>5DC0h = 24kHz<br>7D00h = 32kHz<br>AC44h = 44.1kHz<br>BB80h = 48kHz<br>Any other value defaults to the nearest supported sample rate | Variable Rate Audio / Sample Rate Conversion |
| 2Eh | all | AUXDACSR | BB80h | **AUXDAC Sample Rate Control**<br>1F40h = 8kHz<br>2B11h = 11.025kHz<br>2EE0h = 12kHz<br>3E80h = 16kHz<br>5622h = 22.05kHz<br>5DC0h = 24kHz<br>7D00h = 32kHz<br>AC44h = 44.1kHz<br>BB80h = 48kHz<br>Any other value defaults to the nearest supported sample rate | |
| 32h | all | ADCSR | BB80h | **Stereo ADC Sample Rate Control**<br>1F40h = 8kHz<br>2B11h = 11.025kHz<br>2EE0h = 12kHz<br>3E80h = 16kHz<br>5622h = 22.05kHz<br>5DC0h = 24kHz<br>7D00h = 32kHz<br>AC44h = 44.1kHz<br>BB80h = 48kHz<br>Any other value defaults to the nearest supported sample rate | |
| Note: The VRA bit in register 2Ah must be set first to obtain sample rates other than 48kHz | | | | | |

**Registers 2Ch, 2Eh 32h and** control the sample rates for the stereo DAC, auxiliary DAC and audio ADC, respectively.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 36h | 15 | CTRL | 0 (GPIO reg) | **GPIO Pin Configuration Control**<br>0 = GPIO pins used as GPIOs<br>1 = GPIO pins used as PCM interface | PCM CODEC |
| | 14:13 | MODE | 10 (master mode) | **PCM Interface Mode Control**<br>00 = PCM interface disabled<br>01 = Slave mode<br>10 = Master mode<br>11 = Partial master mode | |
| | 11:9 | DIV | 010 (1/4) | **PCMCLK Rate Control**<br>000 = Voice DAC clock<br>001 = Voice DAC clock / 2<br>010 = Voice DAC clock / 4<br>011 = Voice DAC clock / 8<br>100 = Voice DAC clock / 16<br>All other values are reserved | |
| | 8 | VDACOSR | 0 (64x) | **Voice DAC Oversampling Rate Control**<br>0 = 64 x fs<br>1 = 128 x fs | |
| | 7 | CP | 0 (normal) | **PCMCLK Polarity Control**<br>0 = Normal<br>1 = Inverted | |
| | 6 | FSP | 0 | FMT = 00, 01 or 10 / FMT = 11<br>**PCMFS Polarity Control**<br>0 = Normal<br>1 = Inverted / **DSP Mode Control**<br>0 = DSP Mode A<br>1 = DSP Mode B | |
| | 5:4 | SEL | 00 (LandR data) | **PCM ADC Output Channel Control**<br>00 = Normal stereo<br>01 = Reverse stereo<br>10 = Output left ADC data only<br>11 = Output right ADC data only | |
| | 3:2 | WL | 10 (24 bits) | **PCM Data Word Length Control**<br>00 = 16-bit<br>01 = 20-bit<br>10 = 24-bit<br>11 = 32-bit (not supported when FMT=00) | |
| | 1:0 | FMT | 10 ($I^2S$) | **PCM Data Format Control**<br>00 = Right justified<br>01 = Left justified<br>10 = $I^2S$<br>11 = DSP mode | |

**Register 36h** controls the PCM CODEC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 3Ah | 15 | V | 0 | **S/PDIF Validity Bit**<br>1 = Valid<br>0 = Not valid | Digital Audio (S/PDIF) Output |
| | 14 | DRS | 0 | Indicates that the WM9713L does not support double rate S/PDIF output (read-only) | |
| | 13:12 | SPSR | 10 | Indicates that the WM9713L only supports 48kHz sampling on the S/PDIF output (read-only) | |
| | 11 | L | 0 | **S/PDIF L-bit Control**<br>Programmed as required by user | |
| | 10:4 | CC | 0000000 | **S/PDIF Category Code Control**<br>Category code; programmed as required by user | |
| | 3 | PRE | 0 | **S/PDIF Pre-emphasis Indication Control**<br>0 = no pre-emphasis<br>1 = 50/15µs pre-emphasis | |
| | 2 | COPY | 0 | **S/PDIF Copyright Indication Control**<br>0 = Copyright not asserted<br>1 = Copyright asserted | |
| | 1 | AUDIB | 0 | **S/PDIF Non-audio Indication Control**<br>0 = PCM data<br>1 = Non-PCM data | |
| | 0 | PRO | 0 | **S/PDIF Professional Indication Control**<br>0 = Consumer mode<br>1 = Professional mode | |

**Register 3Ah** Read/Write. Controls the S/PDIF output.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 3Ch | 15 | PD15 | 1 (disabled) | **AUXADC Disable Control**<br>1 = Disabled<br>0 = Enabled | Power Management |
| | 14 | VMID1M | 1 (disabled) | **1Meg VMID String Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 13 | TSHUT | 1 (disabled) | **Thermal Shutdown Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 12 | VXDAC | 1 (disabled) | **Voice DAC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 11 | AUXDAC | 1 (disabled) | **AUXDAC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 10 | VREF | 1 (disabled) | **VREF Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 9 | PLL | 1 (disabled) | **PLL Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 7 | DACL | 1 (disabled) | **Left DAC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 6 | DACR | 1 (disabled) | **Right DAC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 5 | ADCL | 1 (disabled) | **Left ADC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 4 | ADCR | 1 (disabled) | **Right ADC Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 3 | HPLX | 1 (disabled) | **Left Headphone Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 2 | HPRX | 1 (disabled) | **Right Headphone Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 1 | SPKX | 1 (disabled) | **Speaker Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 0 | MX | 1 (disabled) | **Mono Mixer Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| * "0" corresponds to "ON", if and only if the corresponding bit in register 26h is also 0. | | | | | |

**Register 3Ch** is for power management additional to the AC'97 specification. Note that the actual state of each circuit block depends on both register 3Ch AND register 26h.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 3Eh | 15 | MCD | 1 (disabled) | **Microphone Current Detect Disable Control**<br>1 = Disabled<br>0 = Enabled | Power Management |
| | 14 | MICBIAS | 1 (disabled) | **Microphone Bias Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 13 | MONO | 1 (disabled) | **MONO PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 12 | OUT4 | 1 (disabled) | **OUT4 PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 11 | OUT3 | 1 (disabled) | **OUT3 PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 10 | HPL | 1 (disabled) | **HPL PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 9 | HPR | 1 (disabled) | **HPR PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 8 | SPKL | 1 (disabled) | **SPKL PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 7 | SPKR | 1 (disabled) | **SPKR PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 6 | LL | 1 (disabled) | **LINEL PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 5 | LR | 1 (disabled) | **LINER PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 4 | MOIN | 1 (disabled) | **MONOIN PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 3 | MA | 1 (disabled) | **MICA PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 2 | MB | 1 (disabled) | **MICB PGA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 1 | MPA | 1 (disabled) | **Mic Pre-amp MPA Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| | 0 | MPB | 1 (disabled) | **Mic Pre-amp MPB Disable Control**<br>1 = Disabled<br>0 = Enabled | |
| * "0" corresponds to "ON", if and only if the corresponding bit in register 26h is also 0. | | | | | |

**Register 3Eh** is for power management additional to the AC'97 specification. Note that the actual state of each circuit block depends on both register 3Eh AND register 26h.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 40h | 13 | 3DE | 0 (disabled) | **3D Enhancement Control**<br>1 = Enabled<br>0 = Disabled | Audio DACs, 3D Stereo Enhancement |
| | 7 | LB | 0 (disabled) | **Digital Loopback Control**<br>1 = Enabled<br>0 = Disabled | Intel's AC'97 Component Specification, Revision 2.2, page 55 |

**Register 40h** is a "general purpose" register as defined by the AC'97 specification. Only two bits are implemented in the WM9714L.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 42h | 6 | MONO | 0 (normal) | **MONO Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | Analogue Audio Outputs, Power-Up |
| | 5 | SPKL | 0 (normal) | **SPKL Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |
| | 4 | SPKR | 0 (normal) | **SPKR Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |
| | 3 | HPL | 0 (normal) | **HPL Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |
| | 2 | HPR | 0 (normal) | **HPR Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |
| | 1 | OUT3 | 0 (normal) | **OUT3 Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |
| | 0 | OUT4 | 0 (normal) | **OUT4 Fast Power Up Control**<br>1 = Fast power up<br>0 = Normal power up | |

**Register 42h** controls power-up conditions for output PGAs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 44h | 14:12 | $S_{EXT}$[6:4] | 000 (div 1) | **Hi-fi Block Clock Division Control**<br>000 = f<br>001 = f/2<br>…<br>111 = f/8 | Clock Generation |
| | 11:8 | $S_{EXT}$[3:0] | 0000 (div 1) | **Voice DAC Clock Division Control**<br>0000 = f<br>0001 = f/2<br>…<br>1111 = f/16 | |
| | 7 | CLKSRC | 1 (ext clk) | **AC97 CLK Source Control**<br>1 = External clock<br>0 = PLL clock | |
| | 5:3 | PENDIV | 000 (div 16) | **AUXADC Clock Division Control**<br>000 = f/16<br>001 = f/12<br>010 = f/8<br>011 = f/6<br>100 = f/4<br>101 = f/3<br>110 = f/2<br>111 = f | |
| | 2 | CLKBX2 | 0 (Off) | **MCLKB Multiplier Control**<br>0 = Normal<br>1 = Multiply by 2 | |
| | 1 | CLKAX2 | 0 (Off) | **MCLKA Multiplier Control**<br>0 = Normal<br>1 = Multiply by 2 | |
| | 0 | CLKMUX | 0 (MCLKA) | **External Clock Source Control**<br>0 = Use MCLKA<br>1 = Use MCLKB | |

**Register 44h** controls clock division and muxing.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 46h | 15:12 | N[3:0] | 0000 (div by 1) | **PLL N Divide Control**<br>0000 = Divide by 1<br>0001 = Divide by 1<br>0010 = Divide by 2<br>…<br>1111 = Divide by 15 | Analogue Audio Outputs, Power-Up |
| | 11 | LF | 0 (normal) | **PLL Low Frequency Input Control**<br>1 = Low frequency mode (input clock < 8.192MHz)<br>0 = Normal mode | |
| | 10 | SDM | 0 (disabled) | **PLL SDM Enable Control**<br>1 = Enable SDM (required for fractional N mode)<br>0 = Disable SDM | |
| | 9 | DIVSEL | 0 (div by 1) | **PLL Input Clock Division Control**<br>0 = Divide by 1<br>1 = Divide according to DIVCTL | |
| | 8 | DIVCTL | 0 | **PLL Input Clock Division Value Control**<br>0 = Divide by 2<br>1 = Divide by 4 | |
| | 6:4 | PGADDR | 000 | **Pager Address**<br>Pager address bits to access programming of K[21:0] and $S_{PLL}$[6:0] | |
| | 3:0 | PGDATA | 0000 | **Pager Data**<br>Pager data bits | |

**Register 46h** controls PLL clock generation.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | REFER TO |
|---|---|---|---|---|---|---|
| 4Ch | *n* | GC*n* | 1 (input) | **GPIO Pin Configuration Control**<br>0 = Output<br>1 = Input (GC9-15 are always inputs) | | GPIO and Interrupt Control |
| 4Eh | *n* | GP*n* | 1 (active high) | **GPIO Pin Polarity / Type** | | |
| | | | | Input (GCn = 1) | Output (GCn = 0) | |
| | | | | 0 = Active low<br>1 = Acitve high | 0 = CMOS output<br>1 = Open drain | |
| 50h | *n* | GS*n* | 0 (not sticky) | **GPIO Pin Sticky Control**<br>0 = Not sticky<br>1 = Sticky | | |
| 52h | *n* | GW*n* | 0 (no wake-up) | **GPIO Pin Wake-up Control**<br>0 = No wake-up (no interrupts generated by GPIO)<br>1 = Wake-up (generate interrupts from GPIO) | | |
| 54h | *n* | GI*n* | N/A | **GPIO Pin Status**<br>Read = Returns status of GPIO<br>Write = Writing 0 clears sticky bits | | |
| Bit definitions for registers 4Ch to 54h | 15 | | | Controls Comparator 1 signal (virtual GPIO) | | |
| | 14 | | | Controls Comparator 2 signal (virtual GPIO) | | |
| | 12 | | | Controls ADA signal (virtual GPIO) | | |
| | 11 | | | Controls Thermal sensor signal (virtual GPIO) | | |
| | 10 | | | Controls Microphone short detect (virtual GPIO) | | |
| | 9 | | | Controls Microphone insert detect (virtual GPIO) | | |
| | 8 | | | Controls GPIO8 (pin 3) | | |
| | 7 | | | Controls GPIO7 (pin 11) | | |
| | 6 | | | Controls GPIO6 (pin 12) | | |
| | 5 | | | Controls GPIO5 (pin 48) | | |
| | 4 | | | Controls GPIO4 (pin 47) | | |
| | 3 | | | Controls GPIO3 (pin 46) | | |
| | 2 | | | Controls GPIO2 (pin 45) | | |
| | 1 | | | Controls GPIO1 (pin 44) | | |

**Register 4Ch to 54h** control the GPIO pins and virtual GPIO signals.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 56h | 8 | GE8 | 1 (GPIO) | **GPIO8 (Pin 12) Function Control**<br>0 = Pin 12 is not controlled by GPIO logic<br>1 = Pin 12 is controlled by GPIO logic | GPIO and Interrupt Control |
| | 6 | GE6 | 1 (GPIO) | **GPIO6 (Pin 3) Function Control**<br>0 = Pin 3 is not controlled by GPIO logic<br>1 = Pin 3 is controlled by GPIO logic | |
| | 5 | GE5 | 1 (GPIO) | **GPIO5 (Pin 48) Function Control**<br>0 = Pin 48 is not controlled by GPIO logic<br>1 = Pin 48 is controlled by GPIO logic | |
| | 4 | GE4 | 1 (GPIO) | **GPIO4 (Pin 47) Function Control**<br>0 = Pin 47 is not controlled by GPIO logic<br>1 = Pin 47 is controlled by GPIO logic | |
| | 2 | GE2 | 1 (GPIO) | **GPIO2 (Pin 45) Function Control**<br>0 = Pin 45 is not controlled by GPIO logic<br>1 = Pin 45 is controlled by GPIO logic | |

**Register 56h** controls the use of GPIO pins for non-GPIO functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 58h | 15:8 | PU | 01000000 | **GPIO Pin Pull-Up Control**<br>1 = Enables weak pull-up on GPIO pins<br>0 = No pull-up on GPIO pins | GPIO and Interrupt Control |
| | 7:0 | PD | 00000000 | **GPIO Pin Pull-Down Control**<br>1 = Enables weak pull-down on GPIO pins<br>0 = No pull-down on GPIO pins | |

**Register 56h** controls GPIO pull-up/down.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 5Ah | 15:13 | COMP2DEL | 000 (no delay) | **Low Battery Alarm Delay Control**<br>000 = No delay<br>001 = $2^{13}$ AC-link frames<br>010 = $2^{14}$ AC-link frames<br>011 = $2^{15}$ AC-link frames<br>100 = $2^{16}$ AC-link frames<br>101 = $2^{17}$ AC-link frames<br>110 = $2^{18}$ AC-link frames<br>111 = $2^{19}$ AC-link frames | Battery Alarm |
| | 8 | RSTDIS | 0 (RESETB enabled) | **RESETB Pin Disable Control**<br>0 = Pin 11 is RESETB<br>1 = Pin 11 is GPIO (RESETB function disabled) | GPIO Interrupt and Control |
| | 7:6 | JSEL | 00 (GPIO1) | **Jack Detect Pin Input Control**<br>00 = GPIO1<br>01 = GPIO6<br>10 = GPIO7<br>11 = GPIO8 | Jack Insertion & Auto-Switching |
| | 5:4 | HPMODE | 00 (7Hz) | **HPF Cut-Off Control**<br>00 = 7Hz @ fs=48kHz<br>01 = 82Hz @ fs=16kHz<br>10 = 82Hz @ fs=8kHz<br>11 = 170Hz @ fs=8kHz | Audio ADCs |
| | 3:2 | DIE REV | N/A | **Device Revision (Read-Only)**<br>00 = Rev.A<br>01 = Rev.B<br>10 = Rev.C | N/A |
| | 1 | WAKEEN | 0 (disabled) | **GPIO Wake Up Control**<br>0 = Disable wake-up<br>1 = Enable wake up | GPIO and Interrupt Control |
| | 0 | IRQ INV | 0 (normal) | **IRQ Polarity Control**<br>0 = Normal<br>1 = Inverted | |

**Register 5Ah** controls several additional functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 5Ch | 15 | AMUTE | 0 | **DAC Automute Status (Read-Only)**<br>0 = DAC not muted<br>1 = DAC auto-muted | Audio DACs, Stereo DACs |
| | 14 | C1REF | 0 (AVDD/2) | **Comparator 1 Reference Voltage Select**<br>0 = AVDD/2<br>1 = WIPER/AUX4 (pin 12) | Battery Alarm |
| | 13:12 | C1SRC | 00 (power down) | **Comparator 1 Signal Source**<br>00 = AVDD/2 when C1REF=1, else powered down<br>01 = COMP1/AUX1 (pin 29)<br>10 = COMP2/AUX2 (pin 30)<br>11 = Reserved | |
| | 11 | C2REF | 0 (AVDD/2) | **Comparator 2 Reference Voltage Select**<br>0 = AVDD/2<br>1 = WIPER/AUX4 (pin 12) | |
| | 10:9 | C2SRC | 00 (OFF) | **Comparator 2 Signal Source**<br>00 = AVDD/2 when C2REF=1, else powered down<br>01 = COMP1/AUX1 (pin 29)<br>10 = COMP2/AUX2 (pin 30)<br>11 = Reserved | |
| | 7 | AMEN | 0 (OFF) | **DAC Automute Control**<br>0 = Disabled<br>1 = Enabled | |
| | 6:5 | VBIAS | 00 (3.3V) | **Analogue Bias Optimization Control**<br>0X = Optimized for 3.3V<br>10 = Optimized for 2.5V<br>11 = Optimized for 1.8V | Power Management |
| | 4 | ADCO | 0 (SDATAOUT) | **S/PDIF Data Source Control**<br>0 = From SDATAOUT<br>1 = Output from audio ADC | Digital Audio (S/PDIF) Output |
| | 3 | HPF | 0 (enabled) | **ADC HPF Disable Control**<br>0 = HPF enabled<br>1 = HPF disabled | Audio ADC |
| | 1:0 | ASS | 00 (slots 3, 4) | **ADC Data Slot Mapping Control**<br>**Left Data** / **Right Data**<br>00 = Slot 3 / Slot 4<br>01 = Slot 7 / Slot 8<br>10 = Slot 6 / Slot 9<br>11 = Slot 10 / Slot 11 | Audio ADC, ADC Slot Mapping |

**Register 5Ch** controls several additional functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 60h | 15:12 | ALCL | 1011 (-12dB) | **ALC Target Level Control**<br>0000 = -28.5dBFS<br>… (1.5dB steps)<br>1111 = -6dBFS | Audio ADC, Automatic Level Control |
| | 11:8 | HLD | 0000 (0 ms) | **ALC Hold Time Control**<br>0000 = 0ms<br>0001 = 2.67ms<br>… (time doubles with every step)<br>1111 = 43.691s | |
| | 7:4 | DCY | 0011 (192 ms) | **ALC Decay Time Control**<br>0000 = 24ms<br>… (time doubles with every step)<br>1010 to 1111 = 24.58s | |
| | 3:0 | ATK | 0010 (24 ms) | **ALC Attack Time Control**<br>0000 = 6ms<br>… (time doubles with every step)<br>1010 to 1111 = 6.14s | |
| 62h | 15:14 | ALCSEL | 00 (OFF) | **ALC Function Channel Control**<br>00 = ALC disabled<br>01 = ALC on right channel only<br>10 = ALC or left channel only<br>11 = ALC on both left and right channels | |
| | 13:11 | MAXGAIN | 111 (+30dB) | **ALC PGA Gain Limit Control**<br>000 = -12dB<br>… (6dB steps)<br>111 = +30dB | |
| | 10:9 | ZC TIMEOUT | 11 (slowest) | **ALC Zero Cross Timeout Delay Control**<br>00 = $2^{14}$ x $t_{BITCLK}$ (1.33ms)<br>01 = $2^{15}$ x $t_{BITCLK}$ (2.67ms)<br>10 = $2^{16}$ x $t_{BITCLK}$ (5.33ms)<br>11 = $2^{17}$ x $t_{BITCLK}$ (10.67ms) | |
| | 7 | NGAT | 0 (OFF) | **Noise Gate Enable Control**<br>0 = Disabled<br>1 = Enabled | |
| | 5 | NGG | 0 (hold gain) | **Noise Gate Function Control**<br>0 = Hold PGA gain at last value<br>1 = Mute ADC output | |
| | 4:0 | NGTH | 00000 (-76.5dB) | **Noise Gate Threshold Control**<br>00000 = -76.5dBFS<br>… (1.5dB steps)<br>11111 = -30dBFS | |

**Registers 60h and 62h** control the ALC and Noise Gate functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 64h | 15 | XSLE | 0 | **AUXDAC Input Select Control**<br>0 = From AUXDACVAL[11:0] (for DC signals)<br>1 = From AC-Link (for AC signals) | Auxiliary DAC |
| | 14:12 | AUXDACSLT | 000 (Slot 5) | **AUXDAC Input Control (XSLE=1)**<br>000 = Slot 5, bits 8-19<br>001 = Slot 6, bits 8-19<br>010 = Slot 7, bits 8-19<br>011 = Slot 8, bits 8-19<br>100 = Slot 9, bits 8-19<br>101 = Slot 10, bits 8-19<br>110 = Slot 11, bits 8-19<br>111 = Reserved | |
| | 11:0 | AUXDACVAL | 000000000 | **AUXDAC Input Control (XSLE=0)**<br>000h = Minimum<br>FFFh = Full scale | |

**Register 64h** controls the input signal of the auxiliary DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 74h | 9 | POLL | 0 | **Poll Measurement Control**<br>Writing "1" initiates a measurement (when CTC is not set) | AUXADC |
| | 8 | CTC | 0 | **AUXADC Measurement Mode**<br>0 = Polling mode<br>1 = Continuous mode (for DMA) | |
| | 7 | ADCSEL_AUX4 | 0 | **AUX4 Measurement Enable Control**<br>0 = Disable AUX4 measurement (pin 12)<br>1 = Enable AUX4 measurement (pin 12) | |
| | 6 | ADCSEL_AUX3 | 0 | **AUX3 Measurement Enable Control**<br>0 = Disable AUX3 measurement (SPKVDD/3)<br>1 = Enable AUX3 measurement (SPKVDD/3) | |
| | 5 | ADCSEL_AUX2 | 0 | **AUX2 Measurement Enable Control**<br>0 = Disable AUX2 measurement (pin 30)<br>1 = Enable AUX2 measurement (pin 30) | |
| | 4 | ADCSEL_AUX1 | 0 | **AUX1 Measurement Enable Control**<br>0 = Disable AUX1 measurement (pin 29)<br>1 = Enable AUX1 measurement (pin 29) | |

**Registers 74h** controls the measurements for the AUXADC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | REFER TO |
|---|---|---|---|---|---|---|
| 76h | 9:8 | CR | 00 (93.75Hz) | **Continuous Mode Conversion Rate** | | AUXADC |
| | | | | **DEL < 1111** | **DEL = 1111** | |
| | | | | 00 = 93.75Hz | 00 = 8kHz | |
| | | | | 01 = 120Hz | 01 = 12kHz | |
| | | | | 10 = 153.75kHz | 10 = 24kHz | |
| | | | | 11 = 187.5Hz | 11 = 48kHz | |
| | 7:4 | DEL | 0000 (20.8µs) | **AUXADC Settling Time Control**<br>0000 = 1 AC-link frame (20.8µs)<br>0001 = 2 AC-link frames (41.7µs)<br>0010 = 4 AC-link frames (83.3µs)<br>0011 = 8 AC-link frames (167µs)<br>0100 = 16 AC-link frames (333µs)<br>0101 = 32 AC-link frames (667µs)<br>0110 = 48 AC-link frames (1ms)<br>0111 = 64 AC-link frames (1.33ms)<br>1000 = 96 AC-link frame (2ms)<br>1001 = 128 AC-link frames (2.67ms)<br>1010 = 160 AC-link frames (3.33ms)<br>1011 = 192 AC-link frames (4ms)<br>1100 = 224 AC-link frames (4.67ms)<br>1101 = 256 AC-link frames (5.33ms)<br>1110 = 288 AC-link frames (6ms)<br>1111 = No delay, switch matrix always on | | |
| | 3 | SLEN | 1 | **Slot Readback Enable Control**<br>0 = Disabled (readback through register map only)<br>1 = Enabled (readback slot selected by SLT) | | |
| | 2:0 | SLT | 110 (slot 11) | **AC'97 Slot for AUXADC Data Control**<br>000 = Slot 5<br>001 = Slot 6<br>010 = Slot 7<br>011 = Slot 8<br>100 = Slot 9<br>101 = Slot 10<br>110 = Slot 11<br>111 = Reserved | | |

**Registers 76h** controls the AUXADC measurement timing.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 78h | 15:14 | PRP | 00 | **Additional Enable for AUXADC**<br>00 = Disabled<br>01 = Reserved<br>10 = Reserved<br>11 = Enabled | AUXADC |
| | 9 | WAIT | 0 | **AUXADC Data Control**<br>0 = Overwrite existing data in 7Ah with new data<br>1 = Retain existing data in 7Ah until it is read | |
| | 7:6 | MSK | 00 (disabled) | **Mask Input Control**<br>00 = Disabled<br>01 = Static<br>10 = Edge-triggered<br>11 = Synchronous | |

**Register 78h** control the physical properties of the AUXADC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 7Ah<br>read-only | 14:12 | ADCSRC | 000 (none) | **AUXADC Source**<br>000 = No measurement<br>001 = Reserved<br>010 = Reserved<br>011 = Reserved<br>100 = COMP1/AUX1 measurement (pin 29)<br>101 = COMP2/AUX2 measurement (pin 30)<br>110 = AUX3 measurement (SPKVDD/3)<br>111 = AUX4 measurement (pin 12) | AUXADC |
| | 11:0 | ADCD | 000h | **AUXADC Data (Read-only)**<br>Bit 0 = LSB<br>Bit 11 = MSB | |

**Registers 7Ah** is a read-only register which reports the AUXADC measurement results

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|---|---|---|---|---|---|
| 7Ch | 15:8 | F7:0 | 57h | ASCII character “W” for Wolfson | Intel’s AC’97 Component Specification, Revision 2.2, page 50 |
| | 7:0 | S7:0 | 4Dh | ASCII character “M” | |
| 7Eh | 15:8 | T7:0 | 4Ch | ASCII character “L” | |
| | 7:0 | REV7:0 | 13h | Device identifier | |

**Register 7Ch and 7Eh** are read-only registers that indicate to the driver that the CODEC is a WM9714L.

## APPLICATIONS INFORMATION

### RECOMMENDED EXTERNAL COMPONENTS

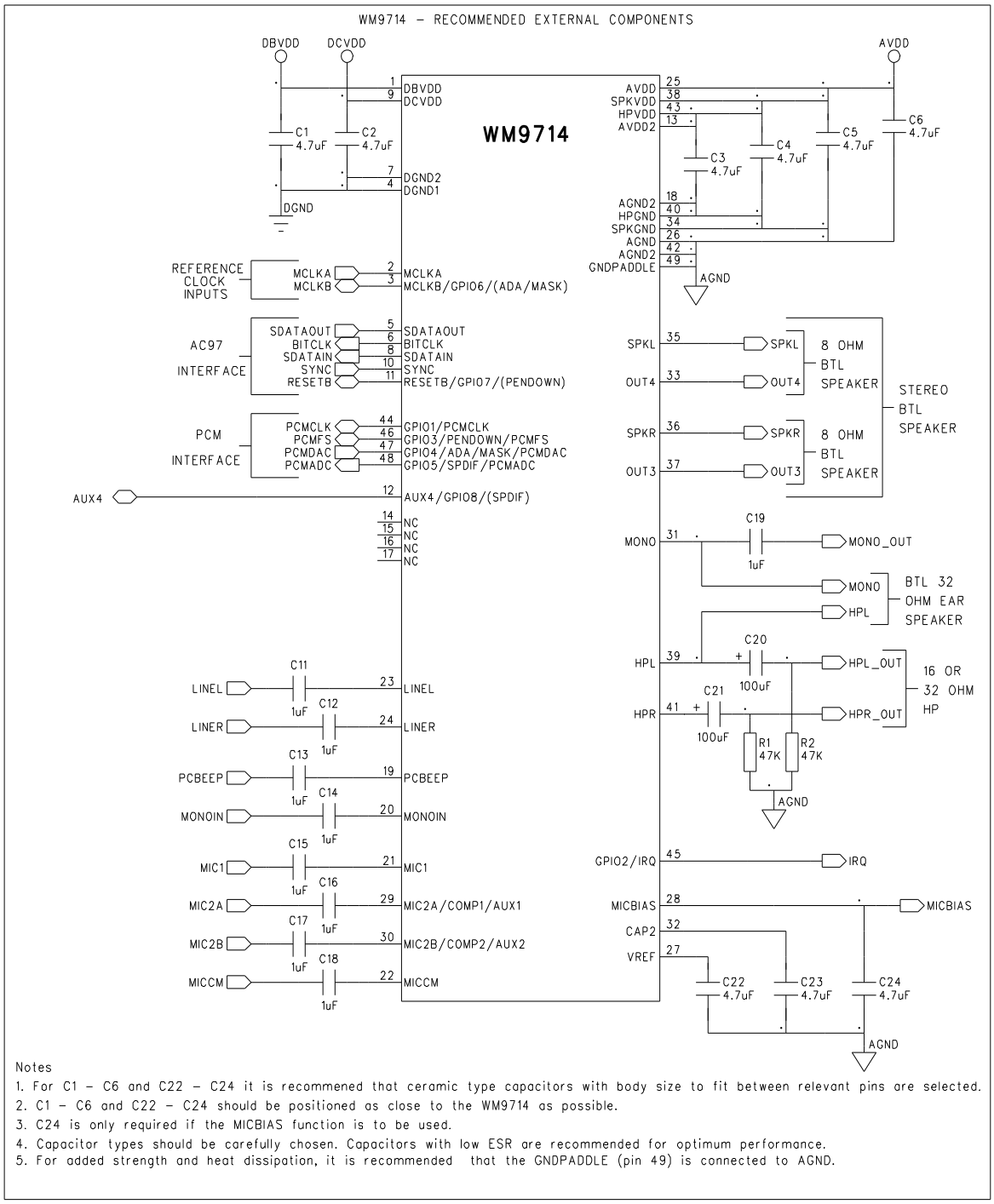



**Figure 28 Recommended External Component Diagram**

## LINE OUTPUT

The headphone outputs, HPL and HPR, can be used as stereo line outputs. The speaker outputs, SPKL and SPKR, can also be used as line outputs. Recommended external components are shown below.

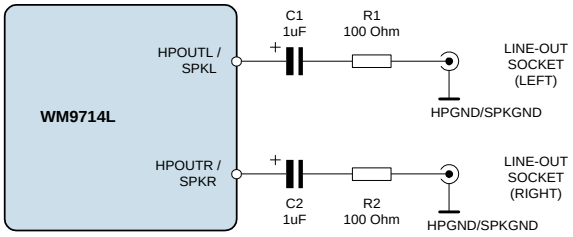



**Figure 29 Recommended Circuit for Line Output**

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, fc. Assuming a 10 kΩ load and C1, C2 = 10μF:

$$fc = 1 / 2\pi (R_L+R_1) C_1 = 1 / (2\pi \times 10.1k\Omega \times 1\mu F) = 16 Hz$$

Increasing the capacitance lowers fc, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

## AC-COUPLED HEADPHONE OUTPUT

The circuit diagram below shows how to connect a stereo headphone to the WM9714L.

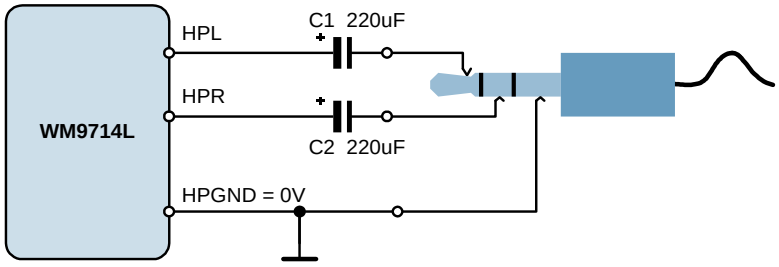



**Figure 30 Simple Headphone Output Circuit Diagram**

The DC blocking capacitors C1 and C2 together with the load resistance determine the lower cut-off frequency, fc. Increasing the capacitance lowers fc, improving the bass response. Smaller capacitance values will diminish the bass response. For example, with a 16Ω load and C1 = 220μF:

$$fc = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45 Hz$$

## DC-COUPLED (CAPLESS) HEADPHONE OUTPUT

In the interest of saving board space and cost, it may be desirable to eliminate the 220µF DC blocking capacitors. This can be achieved by using OUT3 as a headphone pseudo-ground, as shown below.

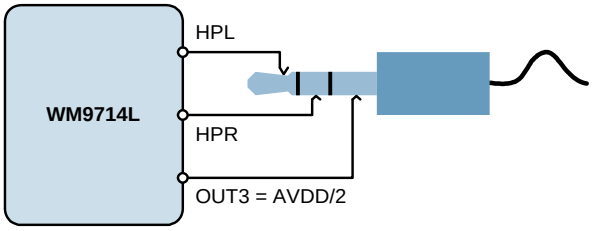



**Figure 31 Capless Headphone Output Circuit Diagram**

As the OUT3 pin produces a DC voltage of AVDD/2, there is no DC offset between HPL/HPR and OUT3, and therefore no DC blocking capacitors are required. However, this configuration has some drawbacks:

- The power consumption of the WM9714L is increased, due to the additional power consumed in the OUT3 output buffer.
- If the DC coupled output is connected to the line-in of a grounded piece of equipment, then OUT3 becomes short-circuited. Although the built-in short circuit protection will prevent any damage to the WM9714L, the audio signal will not be transmitted properly.
- OUT3 cannot be used for another purpose

## BTL LOUDSPEAKER OUTPUT

SPKL and SPKR can differentially drive a mono 8Ω loudspeaker as shown below.

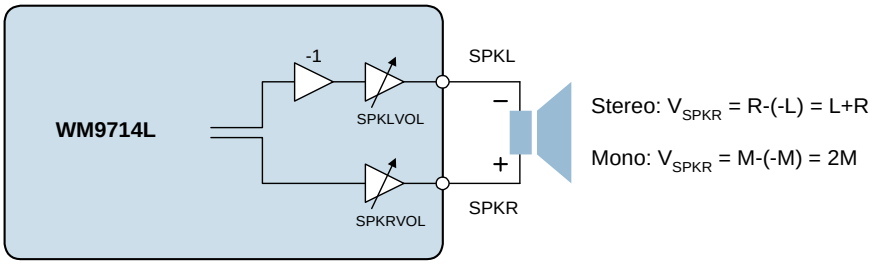



**Figure 32 Speaker Output Connection (INV = 1)**

To drive out differentially one of the speaker outputs must be inverted using INV1 or INV2.

## COMBINED HEADSET / BTL EAR SPEAKER

In smartphone applications with a loudspeaker and separate ear speaker (receiver), a BTL ear speaker can be connected at the OUT3 pin, as shown below.

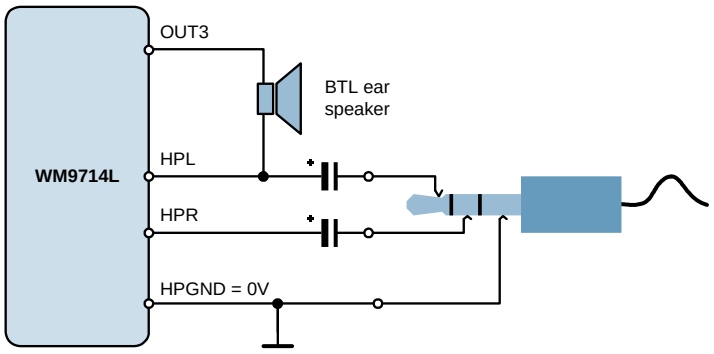



**Figure 33 Combined Headset / BTL Ear Speaker**

The ear speaker and the headset play the same signal. Whenever the headset is plugged in, the headphone outputs are enabled and OUT3 disabled. When the headset is not plugged in, OUT3 is enabled (see “Jack Insertion and Auto-Switching”).

## COMBINED HEADSET / SINGLE-ENDED EAR SPEAKER

Instead of a BTL ear speaker, a single-ended ear speaker can also be used, as shown below.

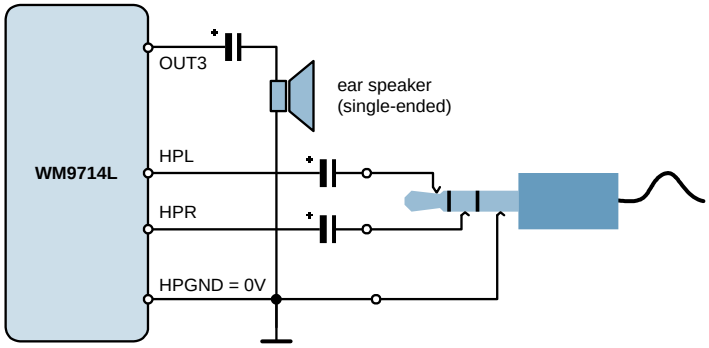



**Figure 34 Combined Headset / Single-ended Ear Speaker**

## JACK INSERT DETECTION

The circuit diagram below shows how to detect when a headphone or headset has been plugged into the headphone socket. It generates an interrupt, instructing the controller to enable HPL and HPR and disable OUT3.

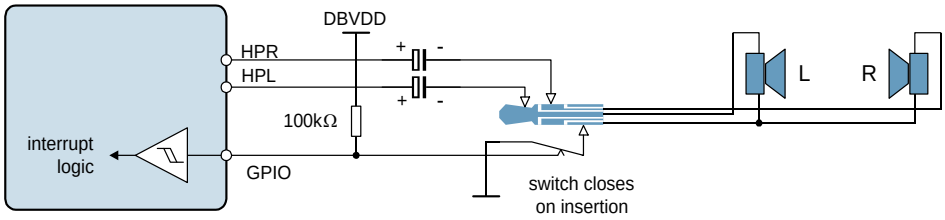



**Figure 35 Jack Insert Detection Circuit**

The circuit requires a headphone socket with a switch that closes on insertion (for using sockets with a switch that opens on insertion, please refer to Application Note WAN0182). It detects both headphones and phone headsets. Any GPIO pin can be used, provided that it is configured as an input.

## HOOKSWITCH DETECTION

Alternatively a headphone socket with a switch that opens on insertion can be used. For this mode of operation the GPIO input must be inverted.

The circuit diagram below shows how to detect when the "hookswitch" of a phone headset is pressed (pressing the hookswitch is equivalent to lifting the receiver in a stationary telephone).

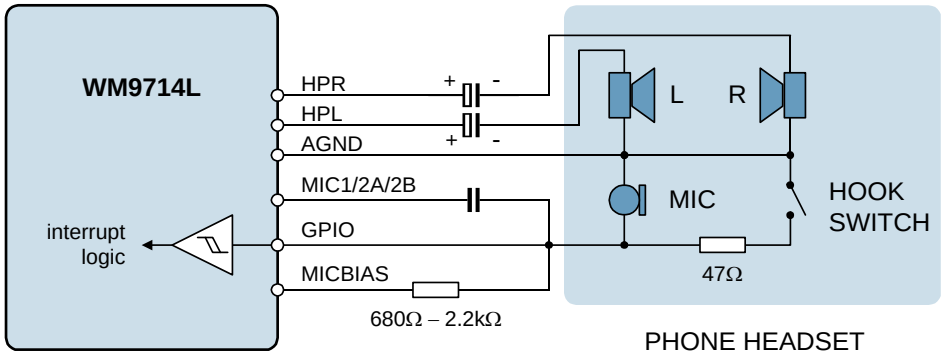



**Figure 36 Hookswitch Detection Circuit**

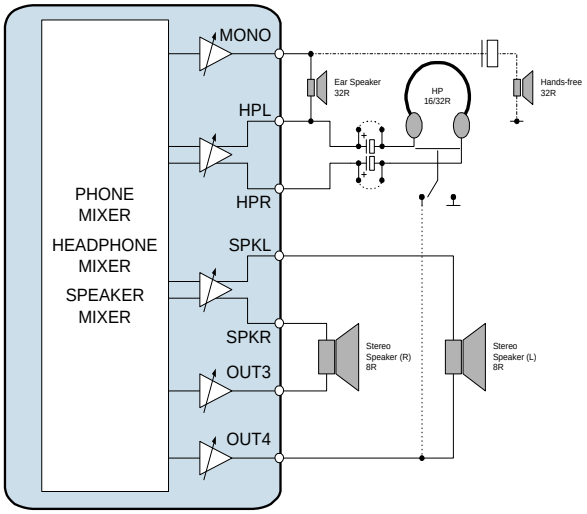
The circuit uses a GPIO pin as a sense input. The impedance of the microphone and the resistor in the MICBIAS path must be such that the potential at the GPIO pin is above 0.7×DBVDD when the hookswitch is open, and below 0.3×DBVDD when it is closed.

## TYPICAL OUTPUT CONFIGURATIONS

The WM9714L has three outputs capable of driving loads down to 16Ω (headphone / line drivers) – HPL, HPR and MONO - and four outputs capable of driving loads down to 8Ω (loudspeaker / line drivers) – SPKL, SPKR, OUT3 and OUT4. The combination of output drivers, mixers and mixer inverters means that many output configurations can be supported. Below are some examples of typical output configurations for smartphone applications.

### STEREO SPEAKER

Figure 37 shows a typical output configuration for stereo speakers with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).

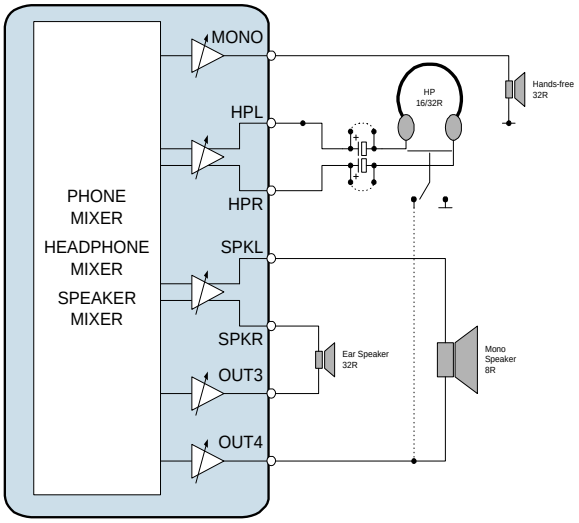



| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Stereo Speaker | Headphone |
|---|---|---|---|---|---|---|---|---|
| **mono** | mmix | spkmix | mmix | -hpmixR | mmix | -hpmixR | - | $Z_H$ |
| **spkl** | - | - | - | - | hpmixL | hpmixL | hpmixL | ($Z_H$) |
| **spkr** | - | - | - | - | hpmixR | hpmixR | hpmixR | - |
| **hpl** | $Z_H$ | $Z_H$ | $V_{mid}$ | hpmixL | $V_{mid}$ | hpmixL | - | hpmixL |
| **hpr** | - | - | - | - | - | - | - | hpmixR |
| **out3** | - | - | - | - | -hpmixR | -hpmixR | -hpmixR | - |
| **out4** | - | - | - | - | -hpmixL | -hpmixL | -hpmixL | ($V_{mid}$) |

**Figure 37 Stereo Speaker Output Configuration**

## MONO SPEAKER

Figure 38 shows a typical output configuration for mono speaker with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).



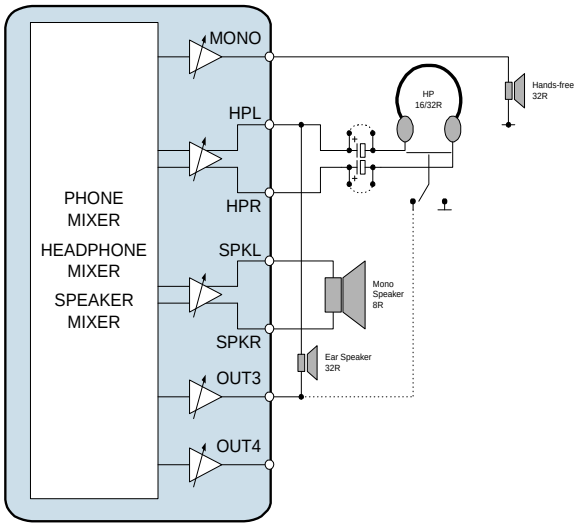

| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Mono Speaker | Headphone |
|---|---|---|---|---|---|---|---|---|
| **mono** | mmix | spkmix | - | - | - | - | | - |
| **spkl** | - | - | - | - | hpmixL | hpmixL | spkmix | ($Z_H$) |
| **spkr** | - | - | mmix | hpmixR | mmix | hpmixR | | - |
| **hpl** | - | - | - | - | - | - | | hpmixL |
| **hpr** | - | - | - | - | - | - | | hpmixR |
| **out3** | - | - | -mmix | -hpmixL | -mmix | -hpmixL | | - |
| **out4** | - | - | - | - | -hpmixR | -hpmixR | -spkmix | ($V_{mid}$) |

**Figure 38 Mono Speaker Output Configuration**

### WM9714L MONO SPEAKER

Figure 39 shows a typical output configuration compatible with the WM9712 for mono speaker with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).

When using this configuration note that AVDD, HPVDD and SPKVDD must all be at the same voltage to achieve the best performance.

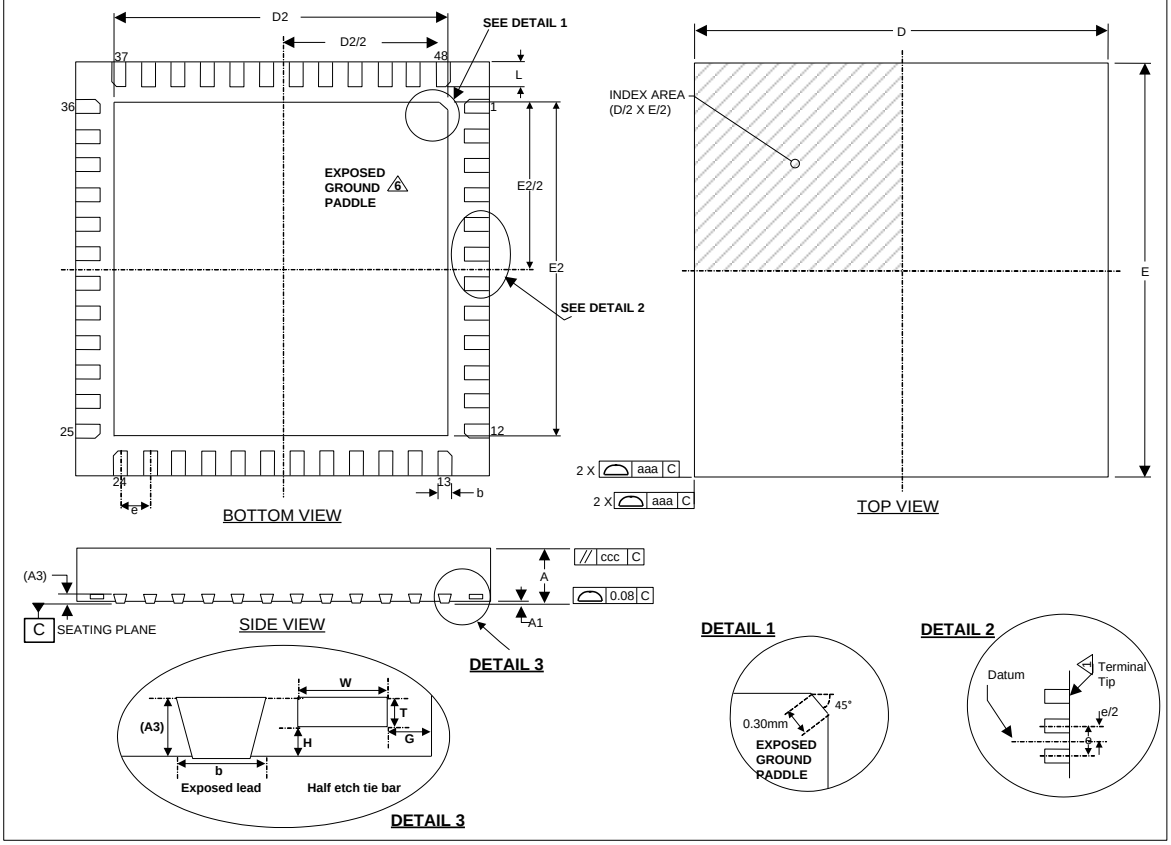



| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Mono Speaker | Headphone |
|---|---|---|---|---|---|---|---|---|
| **mono** | mmix | spkmix | - | - | - | - | | - |
| **spkl** | - | - | - | - | hpmixL | hpmixL | spkmix | - |
| **spkr** | - | - | | | -hpmixR | hpmixR | -spkmix | - |
| **hpl** | - | - | $V_{mid}$ | hpmixL | mmix | hpmixL | | hpmixL |
| **hpr** | - | - | - | - | - | - | | hpmixR |
| **out3** | - | - | mmix | -hpmixR | -mmix | -hpmixR | | ($Z_H$) |
| **out4** | - | - | - | - | - | - | | - |

**Figure 39 WM9714L Mono Speaker Configuration**

## PACKAGE DIMENSIONS

**FL: 48 PIN QFN PLASTIC PACKAGE 7 x 7 x 0.9 mm BODY, 0.50 mm LEAD PITCH** **DM103.A**




| Symbols | Dimensions (mm) | | | |
|---|---|---|---|---|
| | MIN | NOM | MAX | NOTE |
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0 | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 | 1 |
| D | | 7.00 BSC | | |
| D2 | 5.55 | 5.65 | 5.75 | |
| E | | 7.00 BSC | | |
| E2 | 5.55 | 5.65 | 5.75 | |
| e | | 0.5 BSC | | |
| G | | 0.20 | | |
| H | | 0.10 | | |
| L | 0.30 | 0.4 | 0.50 | |
| T | | 0.103 | | |
| W | | 0.15 | | |
| Tolerances of Form and Position | | | | |
| aaa | | 0.15 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| REF | JEDEC, MO-220, VARIATION VKKD-4 | | | |

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

## IMPORTANT NOTICE

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## REVISION HISTORY

| DATE | REV | ORIGINATOR | CHANGES |
|---|---|---|---|
| 30/08/10 | 3.3 | SS | Made changes to 'Thermal Sensor' section and Table 40 to correct and clarify.<br>Added note in Table 57 'GPIO Control' to exclude Thermal Sensor from polarity description and refer to Table 40 'Thermal Shutdown Control'. |
| 10/10/11 | 3.3 | JMacD | Order codes changed from WM9714LGEFL/V and WM9714LGEFL/RV to WM9714**C**LGELF/V and WM9714**C**LGEFL/RV to reflect change to copper wire bonding. |
| 10/10/11 | 3.3 | JMacD | Package Diagram changed to DM103.A |
| 09/03/12 | 3.4 | JMacD | Pin Diagram updated to show Pin 29 and Pin 30 labelling correctly. |
| 19/12/16 | 4.0 | PH | Updated to Cirrus Logic template |