

TLF4277

Low Drop Out Linear Voltage Regulator
Integrated Current Monitor TLF4277EL

Data Sheet

Rev. 1.02, 2011-07-05

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Low Drop Out Linear Voltage Regulator Integrated Current Monitor

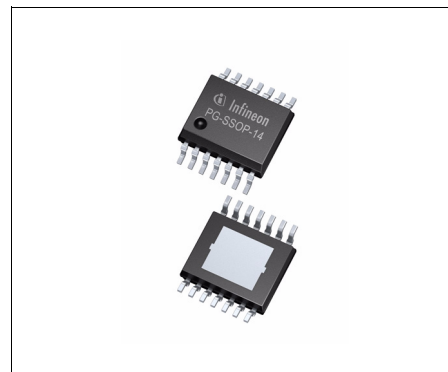
TLF4277EL



1 Overview

Features

- Integrated Current Monitor
- Adjustable Current Limitation
- Adjustable Output Voltage
- Overvoltage Detection
- Output Current up to 200 mA
- Very Low Current Consumption
- Very Low Dropout Voltage
- Wide Input Voltage Range up to 40 V
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range $-40\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$
- Green Product (RoHS and WEEE compliant)
- AEC Qualified



PG-SSOP14 EP

Description

The TLF4277 is the ideal companion IC to supply active antennas for car infotainment applications. The adjustable output voltage makes the TLF4277 capable of supplying the majority of standard active antennas such as:

- FM/AM
- DAB
- XM
- SIRIUS

The TLF4277 is a monolithic integrated low drop out voltage regulator capable of supplying loads up to 200 mA. For an input voltage up to 40 V the TLF4277 provides an adjustable output voltage in a range from 5 V up to 12 V. The integrated current monitor function is a unique feature that provides diagnosis and system protection functionality. Fault conditions such as overtemperature and output overvoltage are monitored and indicated at the current sense output. The maximum output current limit of the device is adjustable to provide additional protection to the connected load.

Via the enable function the IC can be disabled to lower the power consumption. The PG-SSOP14 EP package provides an enhanced thermal performance within a SO8 body size.

Type	Package	Marking
TLF4277EL	PG-SSOP14 EP	TLF4277

2 Block Diagram

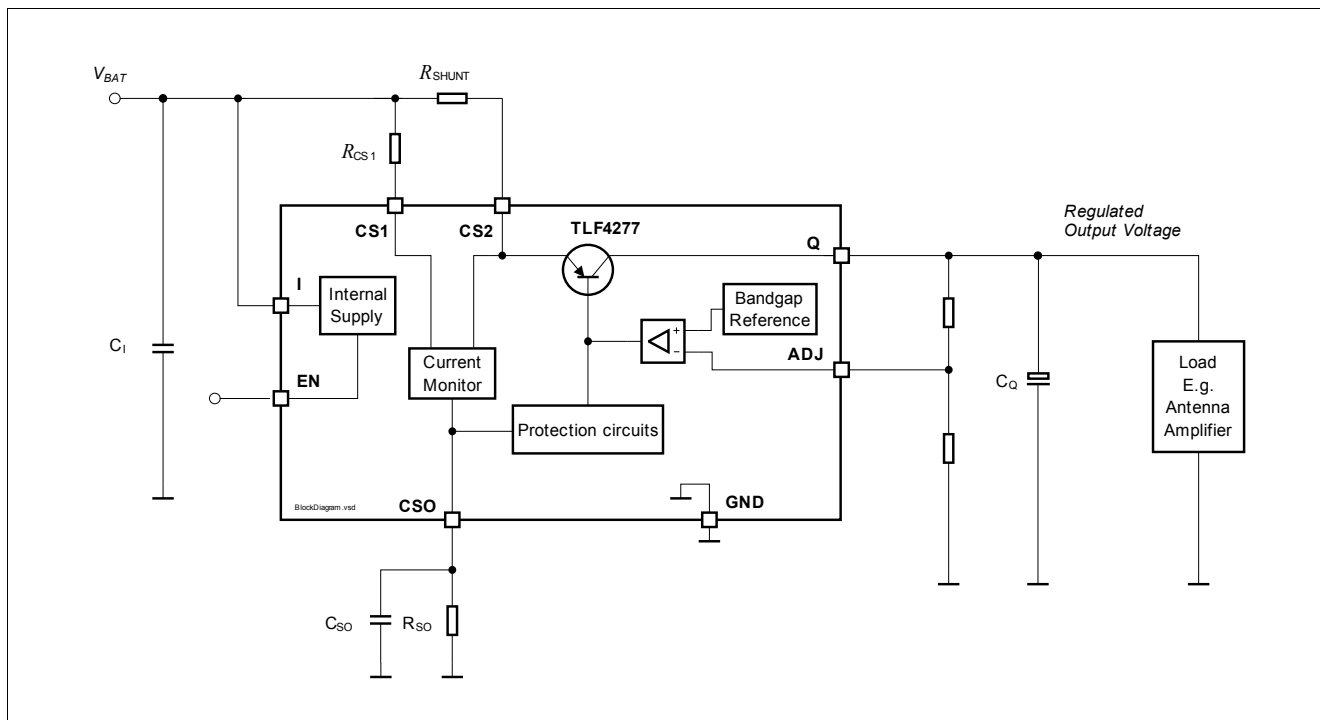


Figure 1 Block and simplified application diagram TLF4277 (Package PG-SSOP14 EP)

3 Pin Configuration

3.1 Pin Assignment

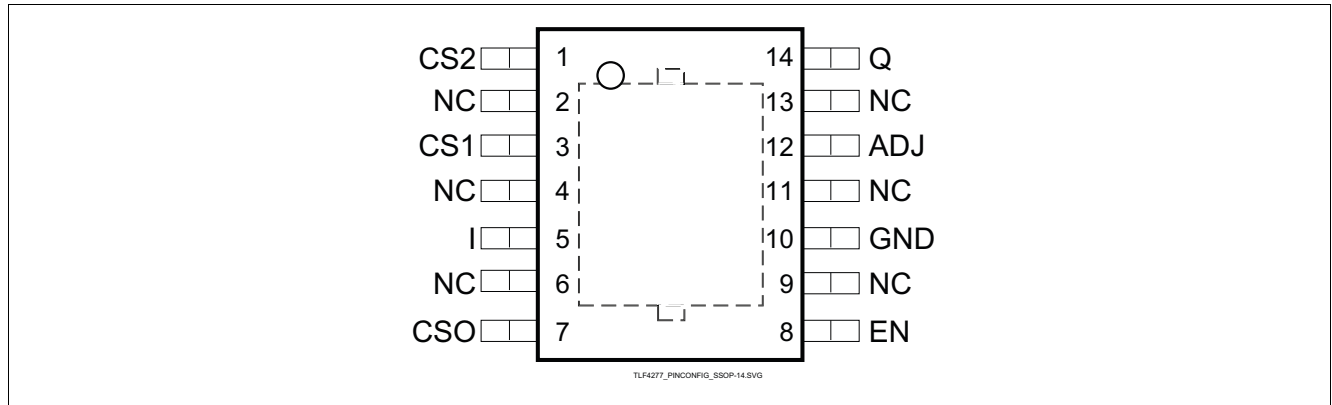


Figure 2 Pin Configuration (top view)

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	CS2	Current Sense In 2 current monitor and power stage input
3	CS1	Current Sense In 1 current monitor input
5	I	IC Supply Place a capacitor from I (Pin 5) to GND close to the IC for compensating line influences.
7	CSO	Current Sense Out current monitor and status output
8	EN	Enable high signal enables the regulator; low signal disables the regulator; connect to I, if the Enable function is not needed
10	GND	Ground connect pin to PCB and heat sink area
12	ADJ	Voltage Adjust connect an external voltage divider to configure the output voltage
14	Q	Regulator Output connect a capacitor between Q (Pin 8) and GND close to the IC pins, respecting the values given for its capacitance C_Q and ESR in the table Chapter 4.2
	PAD	Heat sink connect to PCB heat sink area and GND
2,4,6	NC	Not Connected Internally not connected; Connect to PCB GND
9,11,13	NC	Not Connected Internally not connected; Connect to PCB GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings ¹⁾

$T_j = -40\text{ °C}$ to $+150\text{ °C}$; all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		

Voltage Ratings

4.1.1	IC Supply I	V_I	-42	45	V	–
4.1.2	Enable Input EN	V_{EN}	-42	45	V	–
4.1.3	Voltage Adjust Input ADJ	V_{ADJ}	-0.3	10	V	–
4.1.4	Regulator Output Q	V_Q	-1	40	V	–
4.1.5	Current Monitor Input CS1	V_{CS1}	-42	45	V	–
4.1.6	Current Monitor Input CS2	V_{CS2}	-42	45	V	–
4.1.7	Current Monitor Out CSO	V_{CSO}	-0.3	5	V	–

Temperatures

4.1.8	Junction Temperature	T_j	-40	150	°C	–
4.1.9	Storage Temperature	T_{stg}	-55	150	°C	–

ESD Susceptibility

4.1.10	ESD Resistivity to GND	V_{ESD}	-2	2	kV	HBM ²⁾
4.1.11	ESD Resistivity	V_{ESD}	-1	1	kV	CDM ³⁾

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to AEC-Q-100-002-JESD22-A114

3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage	V_I	5	40	V	–
4.2.2	Input Voltage Power Stage	V_{CS2}	$V_Q + 0.5$	40	V	$V_Q = V_{CS2} - V_{dr}$
4.2.3	Differential Input Voltage	V_{SHUNT}	0	0.5	V	$V_{SHUNT} = V_{BAT} - V_{CS2}$
4.2.4	Output Voltage Range	V_Q	5	12	V	–
4.2.5	Reference Resistor	R_{CS1}	100	1000	Ω	–
4.2.6	Current Sense Output Resistor	R_{CSO}	1k	5k	Ω	–
4.2.7	Current Sense Output Capacitor	C_{CSO}	1	4.7	μF	–
4.2.8	Junction Temperature	T_j	-40	150	$^{\circ}C$	–
4.2.9	Output Capacitor Requirements	C_Q	10	–	μF	– ¹⁾
4.2.10		ESR_{CQ}	–	3	Ω	– ²⁾

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) Relevant ESR value at $f = 10$ kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case... ¹⁾	R_{thJC}	–	–	10	K/W	measured to the exposed pad
4.3.2	Junction to Ambient ¹⁾	R_{thJA}	–	150	–	K/W	Footprint only ²⁾
4.3.3			–	64	–	K/W	300 mm ² PCB heat sink area ²⁾
4.3.4			–	55	–	K/W	600 mm ² PCB heat sink area ²⁾
4.3.5			–	50	–	K/W	2s2p PCB ³⁾

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μ m Cu).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μ m Cu, 2 × 35 μ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled by comparing the feedback voltage (V_{ADJ}) to an internal reference voltage and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q , the output capacitor ESR, the load current and the chip temperature. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the [Table 4.2 "Functional Range" on Page 7](#) have to be maintained. For stability details please refer to the typical performance graph "Output Capacitor Series Resistivity ESR_{CQ} " on [Page 11](#). In addition the output capacitor may need to be sized larger to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general a buffered supply voltage is recommended for the device. For details see [Chapter 9](#).

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. The integrated safeguards consist of output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, an integrated safe operation monitor lowers the maximum output current input voltages above $V_{BAT} = 22\text{ V}$.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLF4277 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This reverse current has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

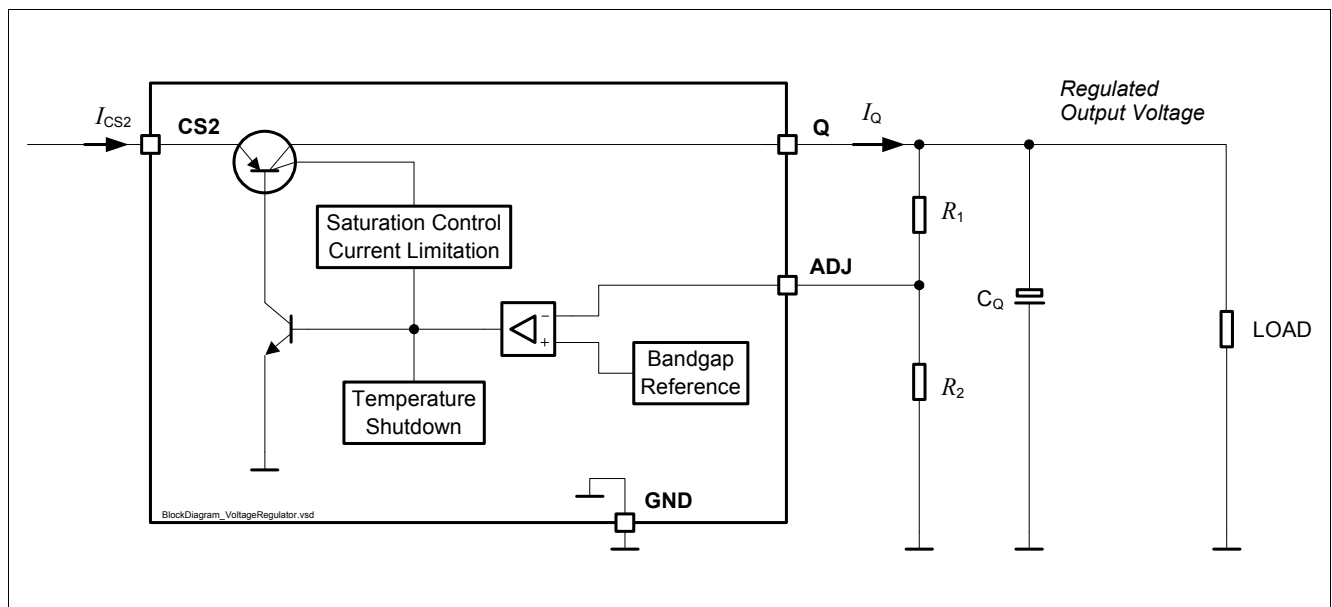


Figure 3 Block Diagram Voltage Regulator Circuit

5.2 Electrical Characteristics Voltage Regulator

Electrical Characteristics: Voltage Regulator

$V_{BAT} = 13.5 \text{ V}$, $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, all voltages with respect to ground, direction of currents as shown in **Figure 7 “Measuring Circuit” on Page 19** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Reference Voltage	$V_{REF,int}$	–	1.22	–	V	¹⁾ –
5.2.2	Output Voltage Tolerance ²⁾	V_Q	-2	–	2	%	$1 \text{ mA} \leq I_Q \leq 200 \text{ mA}$; $9 \text{ V} \leq V_{BAT} \leq 16 \text{ V}$
5.2.3			-2	–	2	%	$1 \text{ mA} \leq I_Q \leq 150 \text{ mA}$; $6 \text{ V} \leq V_{BAT} \leq 16 \text{ V}$
5.2.4			-2	–	2	%	$1 \text{ mA} \leq I_Q \leq 100 \text{ mA}$; $16 \text{ V} \leq V_{BAT} \leq 32 \text{ V}^{3)}$
5.2.5			-2	–	2	%	$1 \text{ mA} \leq I_Q \leq 10 \text{ mA}$; $32 \text{ V} \leq V_{BAT} \leq 45 \text{ V}^{3)}$
5.2.6	Load Regulation steady-state	$dV_{Q,load}$	-30	-5	–	mV	$I_Q = 1 \text{ mA}$ to 150 mA ; $V_{BAT} = 6 \text{ V}$ $V_Q = 5 \text{ V}$
5.2.7	Line Regulation steady-state	$dV_{Q,line}$	–	5	20	mV	$V_{BAT} = 6 \text{ V}$ to 32 V ; $I_Q = 5 \text{ mA}$ $V_Q = 5 \text{ V}$
5.2.8	Power Supply Ripple Rejection ¹⁾	$PSRR$	60	65	–	dB	$f_{ripple} = 100 \text{ Hz}$; $V_{ripple} = 1 \text{ Vpp}$
5.2.9	Dropout Voltage	V_{dr}	–	120	250	mV	$I_Q = 50 \text{ mA}^{4)}$
5.2.10	$V_{dr} = V_{CS2} - V_Q$		–	250	500	mV	$I_Q = 150 \text{ mA}^{4)}$
5.2.11	Output Current Limitation	$I_{Q,max}$	300	–	600	mA	$0 \text{ V} \leq V_Q \leq 0.95 \cdot V_{Q,nom}$; CSO pin connected to GND
5.2.12	Reverse Current	I_Q	-2	-1	–	mA	$V_{BAT} = V_{CS2} = 0 \text{ V}$; $V_Q = 5 \text{ V}$
5.2.13	Reverse Current at Negative Input Voltage	I_{BAT}	-10	-6	–	mA	$V_{BAT} = -16 \text{ V}$; $V_Q = 0 \text{ V}$
5.2.14	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	$^{\circ}\text{C}$	T_j increasing ¹⁾
5.2.15	Overtemperature Shutdown Threshold Hysteresis	$T_{j,hy}$	–	25	–	K	T_j decreasing ¹⁾

1) Parameter not subject to production test; specified by design.

2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.

3) See typical performance graph for details.

4) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

5.3 Application Information for the setting the variable output voltage

The output voltage of the TLF4277 can be adjusted between 5 V and 12 V by an external output voltage divider, closing the control loop to the voltage adjust pin ADJ.

The voltage at pin ADJ is compared to the internal reference of typical 1.22 V in an error amplifier. It controls the output voltage.

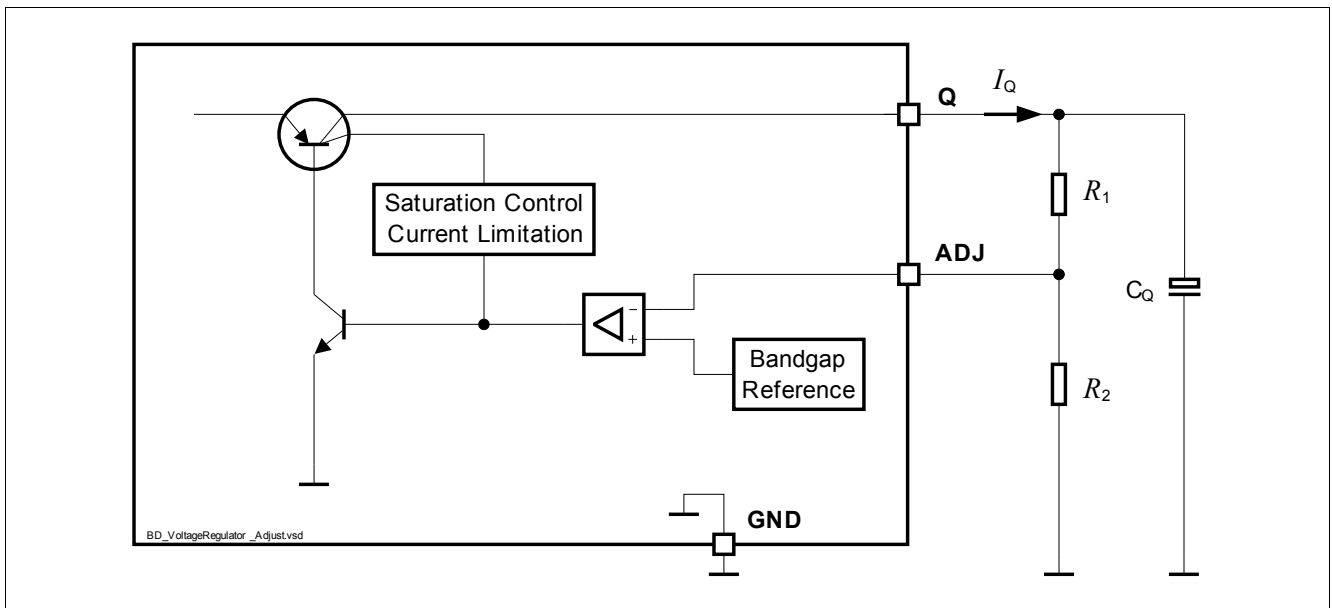


Figure 4 Application Detail External Components at Output for Variable Voltage Regulator

The output voltage is calculated according to [Equation \(1\)](#):

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (1)$$

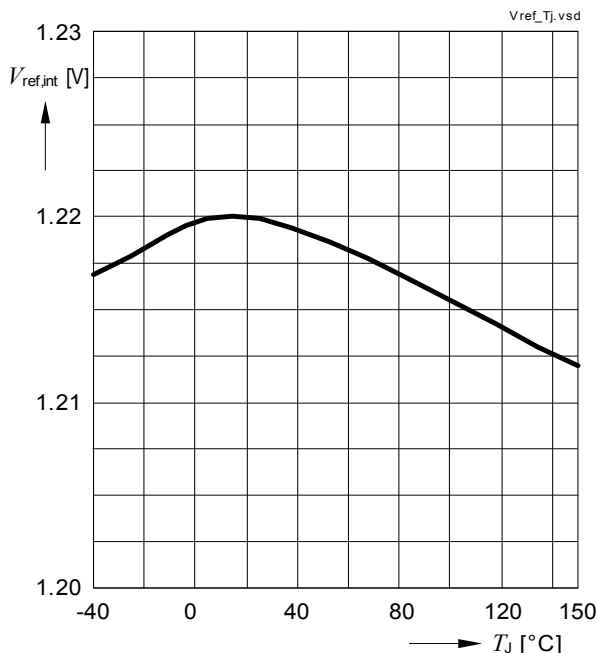
$V_{REF,int}$ is typically 1.22 V.

To avoid errors caused by leakage current I_{ADJ} , we recommend to choose the resistor value for $R_2 < 27 \text{ k}\Omega$.

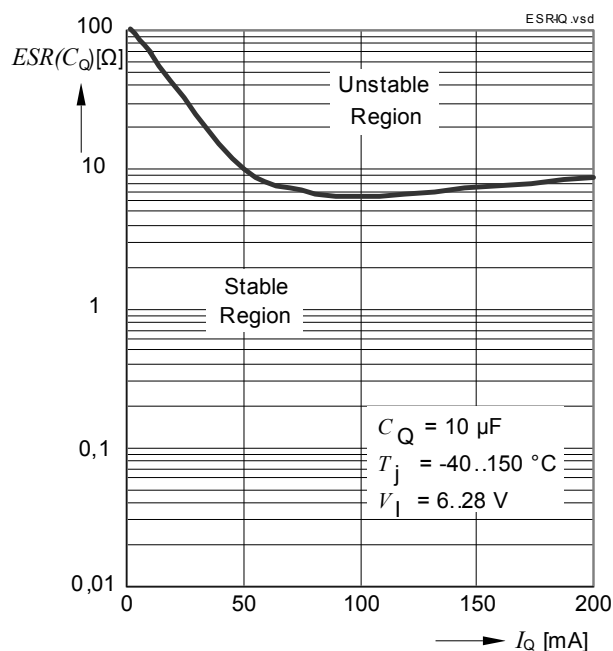
The accuracy of the resistors for the external voltage divider can lead to a higher tolerance of the output voltage. To achieve a reasonable accuracy resistors with a tolerance of 1% or lower are recommended for the feedback divider.

5.4 Typical Performance Characteristics Voltage Regulator

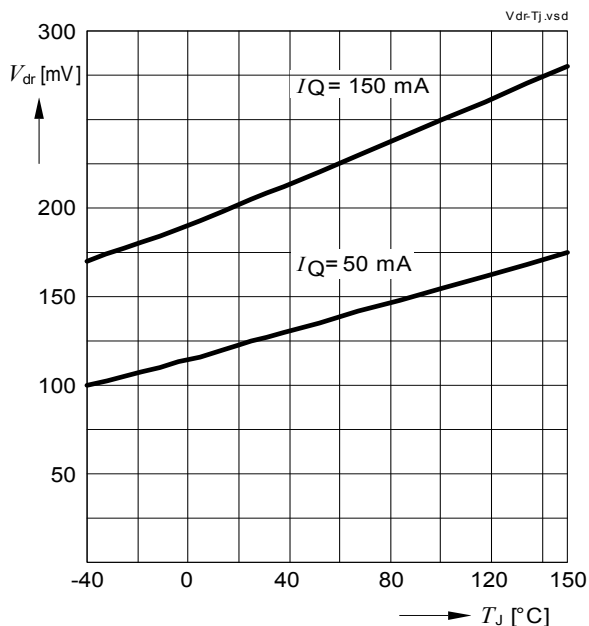
Reference Voltage $V_{REF,int}$ vs.
Junction Temperature T_j



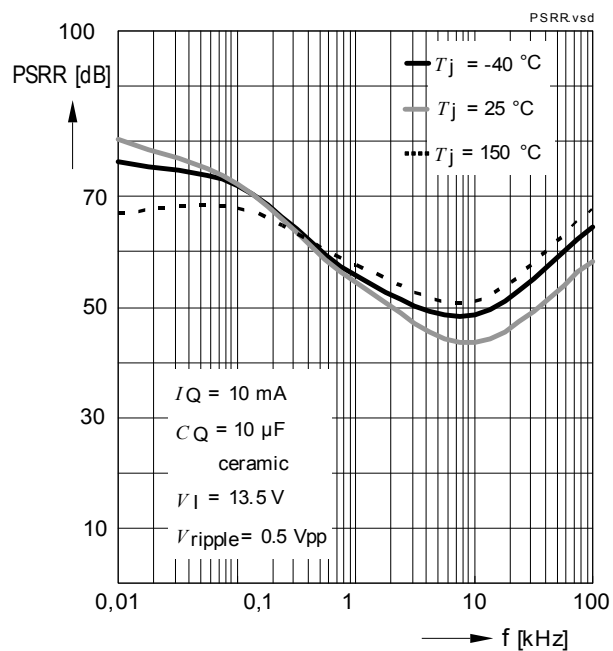
Output Capacitor Series Resistivity ESR_{C_Q}
vs. Output Current I_Q



Dropout Voltage V_{dr} vs.
Output Current I_Q



Power Supply Ripple Rejection $PSRR$



6 Current Consumption

6.1 Electrical Characteristics Current Consumption

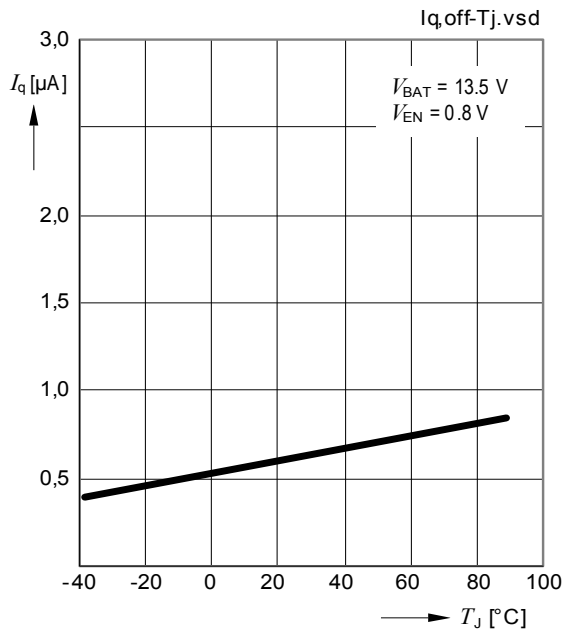
Electrical Characteristics: Current Consumption

$V_{BAT} = 13.5 \text{ V}$, $T_j = -40 \text{ °C}$ to $+150 \text{ °C}$, all voltages with respect to ground; direction of currents as shown in [Figure 7 "Measuring Circuit" on Page 19](#) (unless otherwise specified)

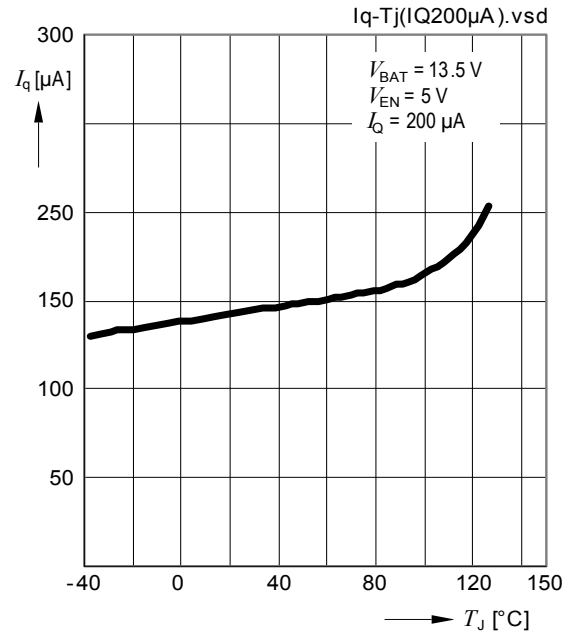
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Current Consumption	$I_{q,on}$	–	150	200	μA	$I_Q \leq 200 \mu\text{A}$; $T_j \leq 25 \text{ °C}$; $V_{EN} = 5 \text{ V}$; $I_q = I_l + I_{CS2} - I_Q$
6.1.2			–	175	250	μA	$I_Q \leq 200 \mu\text{A}$; $T_j \leq 85 \text{ °C}$; $V_{EN} = 5 \text{ V}$; $I_q = I_l + I_{CS2} - I_Q$
6.1.3			–	1.2	2.6	mA	$I_Q = 50 \text{ mA}$ $V_{EN} = 5 \text{ V}$; $I_q = I_l + I_{CS2} - I_Q$
6.1.4			–	3.5	6	mA	$I_Q = 100 \text{ mA}$ $V_{EN} = 5 \text{ V}$; $I_q = I_l + I_{CS2} - I_Q$
6.1.5			–	5	10	mA	$I_Q = 150 \text{ mA}$ $V_{EN} = 5 \text{ V}$; $I_q = I_l + I_{CS2} - I_Q$
6.1.6	Current Consumption	$I_{q,off}$	–	–	3	μA	$T_j \leq 25 \text{ °C}$ $V_{EN} = 0.8 \text{ V}$ $I_q = I_l + I_{CS2} - I_Q$
6.1.7			–	–	5	μA	$T_j \leq 85 \text{ °C}$; $V_{EN} = 0.8 \text{ V}$ $I_q = I_l + I_{CS2} - I_Q$

6.2 Typical Performance Graphs Current Consumption

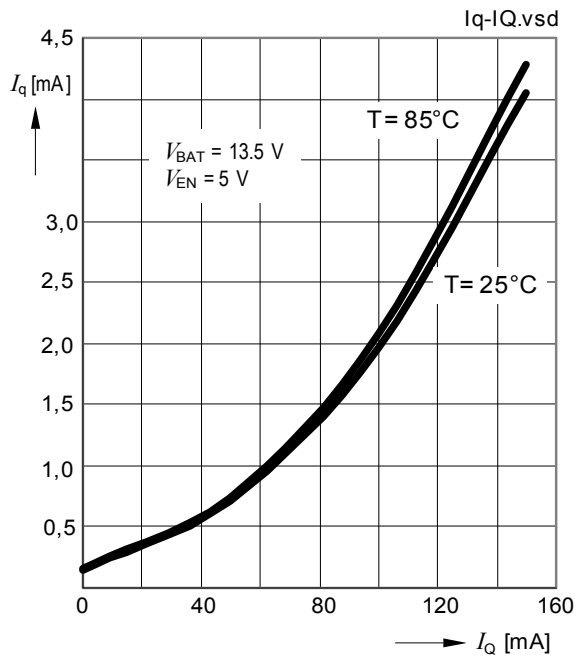
Current Consumption $I_{q,off}$ vs.
Junction Temperature T_j



Current Consumption $I_{q,on}$ vs.
Junction Temperature T_j



Current Consumption $I_{q,on}$ vs.
Output Current I_Q



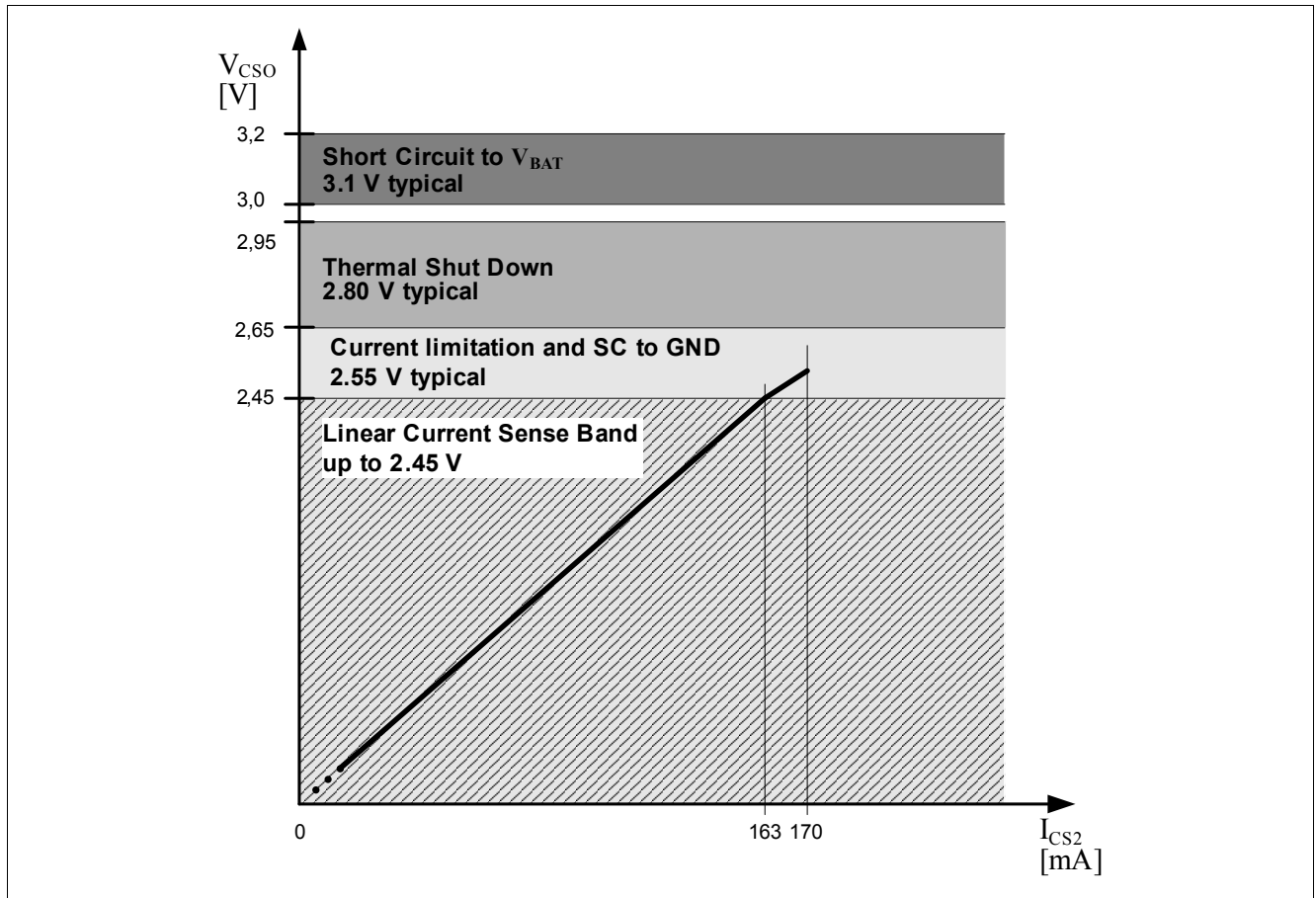


Figure 6 Output levels and functionality of the CSO output¹⁾

7.1.1 Linear Current Monitor

Inside the linear current monitor area the current driven out of the CSO pin is proportional to the voltage which is measured between pin CS1 and CS2.

The level of the current I_{CSO} can be adjusted according to [Equation \(2\)](#):

$$I_{CSO} = \frac{V_{BAT} - V_{CS2}}{R_{CS1}} = I_{CS2} \times \frac{R_{SHUNT}}{R_{CS1}}$$

Adjustment I_{CSO} (2)

$$V_{CSO} = \frac{(V_{BAT} - V_{CS2}) \times R_{CSO}}{R_{CS1}} = V_{SHUNT} \times \frac{R_{CSO}}{R_{CS1}}$$

Adjustment of the voltage level for V_{CSO} (3)

1) The graph is just an example and only valid for an certain configuration of the external components

7.1.2 Adjustable Output Current Limitation

The TLF4277 has an adjustable current limitation for the current flowing into the power stage (pin CS2). If the level of the voltage drop across the sense resistor R_{SHUNT} is higher than the desired linear monitor range the output current of the TLF4277 will be limited.

$$I_{CS2,lim} = \frac{2.55V \times R_{CS1}}{R_{SHUNT} \times R_{CSO}}$$

Setting of the adjustable current limitation

(4)

A voltage level as defined in [Table 7.2.6 "" on Page 17](#) will be applied at the CSO pin.

To achieve a current limitation of 170mA the following configuration can be used:

$$I_{CS2,lim} = \frac{2.55V \times 100\Omega}{1\Omega \times 1.5k\Omega} = 170mA$$

$$R_{SHUNT} = 1\Omega$$

$$R_{CS1} = 100\Omega$$

$$R_{CSO} = 1.5k\Omega$$

7.1.3 Overvoltage Detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277 has an overvoltage detection implemented. An overvoltage will be detected, if the voltage level at the ADJ pin is 20% higher than the internal reference voltage $V_{REF,int}$ defined in [Table 5.2.1 "" on Page 9](#).

Under this condition the CSO pin will be driven through an internal voltage buffer with a voltage level as defined in [Table 7.2.7 "" on Page 17](#).

7.1.4 Thermal Shutdown Detection

If the junction temperature will exceed the limits defined in the [Table 5.2.14 "" on Page 9](#) the TLF4277 will disable the output voltage. In this case a voltage level as defined in [Table 7.2.8 "" on Page 17](#) will be applied at the CSO pin.

7.2 Electrical Characteristics Current and Protection Monitor

Electrical Characteristics: Current Monitor Function

$V_{BAT} = 13.5 \text{ V}$, $T_j = -40 \text{ °C}$ to $+150 \text{ °C}$, all voltages with respect to ground, direction of currents as shown in [Figure 7 “Measuring Circuit” on Page 19](#) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Linear Current Monitor							
7.2.1	Current Sense Output Current I_{CSO} ($V_{SHUNT} = 10 \text{ mV}$)	I_{CSO}	0.08	0.1	0.12	mA	$T_j = 25^\circ\text{C}$ $R_{SHUNT} = 1\Omega$ $R_{CS1} = 100\Omega$ $R_{CSO} = 1.5 \text{ k}\Omega^{1)}$
7.2.2	($V_{SHUNT} = 50 \text{ mV}$)		0.47	0.5	0.53	mA	
7.2.3	($V_{SHUNT} = 100 \text{ mV}$)		0.97	1	1.03	mA	
7.2.4	($V_{SHUNT} = 150 \text{ mV}$)		1.45	1.5	1.55	mA	
Adjustable Current Limitation							
7.2.5	Adjustable Current Limit	$I_{CS2,lim}$	162	170	187	mA	$R_{SHUNT} = 1\Omega$ $R_{CS1} = 100\Omega$ $R_{CSO} = 1.5 \text{ k}\Omega$ $V_Q < 0,95 * V_{Q,nom}^{1)}$
7.2.6	CSO Voltage Level Current limitation	V_{CSO,cur_lim}	2.45	2.55	2.65	V	
Output Level Overvoltage Detected							
7.2.7	CSO Voltage Level Overvoltage detected	$V_{CSO,OV}$	3.0	3.1	3.2	V	$V_{ADJ} > 1.2 * V_{REF,nom}^{1)}$
Output Level Overtemperature Detected							
7.2.8	CSO Voltage Level Overtemperature Detected ²⁾	$V_{CSO,TSD}$	2.65	2.8	2.95	V	$150^\circ\text{C} < T_j < 180^\circ\text{C}$

1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation

2) Specified by design; not subject to production test

8 Enable Function

8.1 Description Enable Function

The TLF4277 can be turned on or turned off via the EN Input. With voltage levels higher than $V_{EN,high}$ applied to the EN Input the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The Enable Input has an build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input.

8.2 Electrical Characteristics Enable Function

Electrical Characteristics: Enable Function

$V_{BAT} = 13.5 \text{ V}$, $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, all voltages with respect to ground, direction of currents as shown in [Figure 7 “Measuring Circuit” on Page 19](#) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.1	Enable Low Signal Valid	$V_{EN,low}$	–	–	0.8	V	–
8.2.2	Enable High Signal Valid	$V_{EN,high}$	2	–	–	V	V_Q settled
8.2.3	Enable Threshold Hysteresis	$V_{EN,hyst}$	50	–	–	mV	–
8.2.4	Enable Input current	I_{EN}	–	–	2	μA	$V_{EN} = 5 \text{ V}$
8.2.5	Enable internal pull-down resistor	R_{EN}	3	4.5	6	$\text{M}\Omega$	–

11 Revision History

Revision	Date	Changes
1.02	2011-07-04	Updated Cover Page Fixed Linear Current Monitor formulas (2,3) on Page 15
1.01	2011-05-07	Template Update
1.0	2009-05-07	Data Sheet

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Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

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