

# MN3672RE (Preliminary)

Color CCD Linear Image Sensor  
with 5000 Bits each for R, G, and B Colors

## Overview

The MN3672RE is a high speed high responsivity CCD color linear image sensor with 5000 pixels for each of the colors R, G, and B. This device consists of a photodetector region having low dark output floating photodiodes and a CCD analog shift register in the read out region.

It is possible to read out an A3 size color document with a high quality and a high resolution of 400dpi.

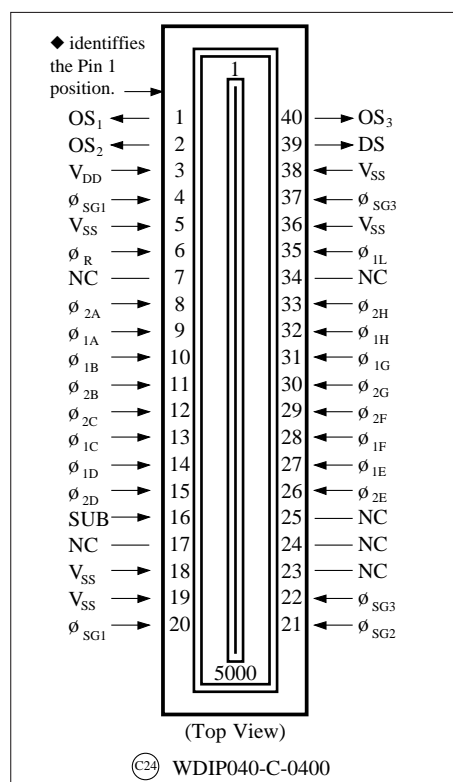
## Features

- 5000 floating photodiodes for each color R, G, and B, and an n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Since the photodiode lines for each color are neighboring (with a line spacing of 14μm), it is possible to greatly reduce the memory for compensation between lines.
- The configuration of the signal processing circuits such as the preamplifier, sample and hold circuit, etc., becomes simpler since the separate signal output pins are provided for the pixels of each of the colors R, G, and B.
- RGB primary colors type on chip color filters are used for color separation.
- The dark signal output voltage has been suppressed to a very low level due to the use of photodiodes with a new structure. (0.2mV (typ.) at accumulation time of 10ms.)
- Large signal output of typically 1.0V at saturation can be obtained.
- Operation with a single +12V positive power supply.

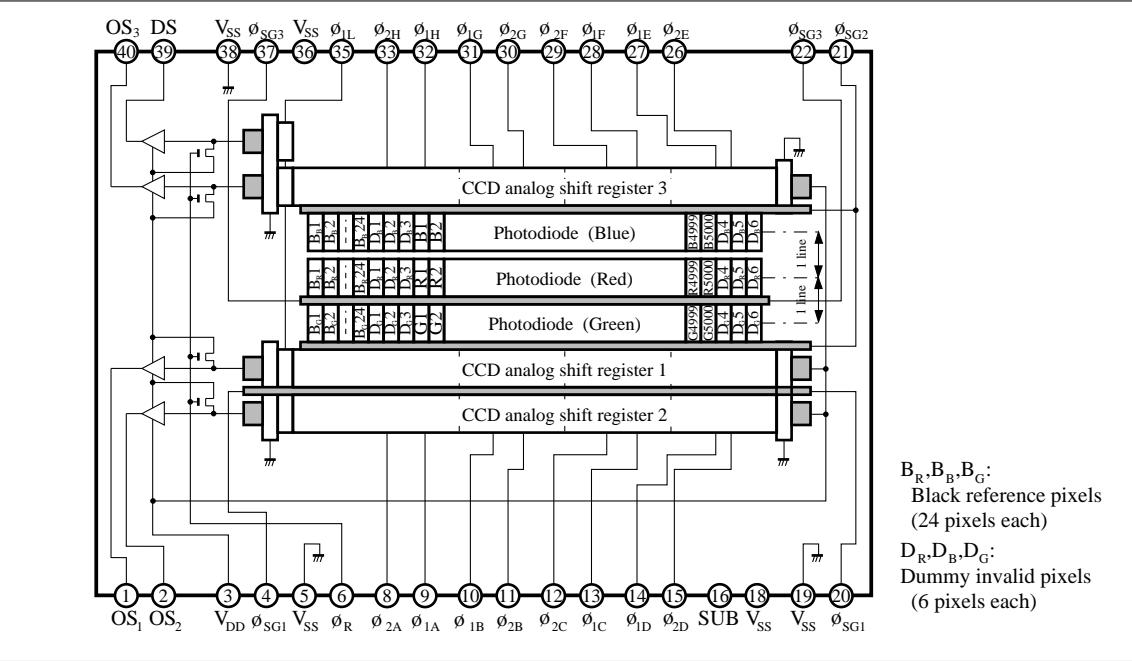
## Application

- Color graphic read out in color copying machines, color scanners, and color fax machines.

## Pin Assignments



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C, VSS=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V <sub>DD</sub>	− 0.3 to +17	V
Input pin voltage	V <sub>I</sub>	− 0.3 to +17	V
Output pin voltage	V <sub>O</sub>	− 0.3 to +17	V
Operating temperature range	T <sub>opr</sub>	0 to + 60	°C
Storage temperature range	T <sub>stg</sub>	−25 to + 85	°C

■ Operating Conditions

• Voltage conditions (Ta=0 to + 60°C, VSS=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V <sub>DD</sub>		11.0	12.0	13.0	V
CCD shift register clock High level	V <sub>φH</sub>	( $\phi_{1A} \sim \phi_{1L}$ , $\phi_{2A} \sim \phi_{2H}$ )	—	10.0	11.0	V
CCD shift register clock Low level	V <sub>φL</sub>	( $\phi_{1A} \sim \phi_{1L}$ , $\phi_{2A} \sim \phi_{2H}$ )	0	0.5	0.8	V
Shift gate clock High level	V <sub>S1H</sub>	( $\phi_{SG1}$ )	—	V <sub>φH</sub> +2	—	V
	V <sub>S2H</sub>	( $\phi_{SG2}$ )	9.0	10.0	11.0	V
	V <sub>S3H</sub>	( $\phi_{SG3}$ )	—	4.0	—	V
Shift gate clock Low level	V <sub>SL</sub>	( $\phi_{SG1} \sim \phi_{SG3}$ )	0	0.5	0.8	V
Reset gate clock High level	V <sub>RH</sub>	( $\phi_R$ )	V <sub>DD</sub> −1	V <sub>DD</sub>	V <sub>DD</sub>	V
Reset gate clock Low level	V <sub>RL</sub>	( $\phi_R$ )	0	0.5	0.8	V

• Timing conditions (Ta=0 to + 60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	$f_C$	See drive timing diagram (2) $f_C=1/2T$	0.1	1.0	5.0	MHz
Reset clock frequency (=data rate)	$f_R$	See drive timing diagram (2) $f_R=1/2T$	0.1	1.0	5.0	MHz
Shift register clock rise time	$t_{Cr}$	See drive timing diagram (2) $f_R=1/2T$	0	10	20	ns
Shift register clock fall time	$t_{Cf}$		0	10	20	ns
Shift clock 1 rise time	$t_{SG1r}$		0	20	50	ns
Shift clock 1 fall time	$t_{SG1f}$		0	20	50	ns
Shift clock 1 set up time	$t_{SG1s}$		See drive timing diagram (1)			μs
Shift clock 1 pulse width	$t_{SG1w}$					μs
Shift clock 2 rise time	$t_{SG2r}$		0	15	50	ns
Shift clock 2 fall time	$t_{SG2f}$		0	15	50	ns
Shift clock 2 pulse width	$t_{SG2w}$	See drive timing diagram (1)				μs
Shift clock 3 rise time	$t_{SG3r}$		0	20	50	ns
Shift clock 3 fall time	$t_{SG3f}$		0	20	50	ns
Shift clock 3 set up time	$t_{SG3s}$		See drive timing diagram (1)			μs
Shift clock 3 pulse width	$t_{SG3w}$					μs
Shift clock 3 hold time	$t_{SG3h}$					μs
Reset clock rise time	$t_{Rr}$	See drive timing diagram (2)	0	5	10	ns
Reset clock fall time	$t_{Rf}$		0	5	10	ns
Reset clock set up time	$t_{Rs}$		0.7T			ns
Reset clock pulse width	$t_{Rw}$		10			ns
Reset clock hold time	$t_{Rh}$		10			ns

■ Electrical Characteristics

• Clock input capacitance (Ta=0 to + 60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clocks A to D input capacitance	$C_{1A}, C_{1B}$ $C_{1C}, C_{1D}$ $C_{2A}, C_{2B}$ $C_{2C}, C_{2D}$	$V_{IN}=12V, f=1MHz$	—	160	—	pF
Shift register clocks E to H input capacitance	$C_{1E}, C_{1F}$ $C_{1G}, C_{1H}$ $C_{2E}, C_{2F}$ $C_{2G}, C_{2H}$		—	120	—	pF
Shift register final stage clock input capacitance	$C_{1L}$		—	10	—	pF
Reset clock input capacitance	$C_{RS}$		—	10	—	pF
Shift clocks 1, 3 input capacitance	$C_{SG1}, C_{SG3}$		—	150	—	pF
Shift clock 2 input capacitance	$C_{SG2}$		—	250	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	$I_{DD}$	$V_{DD}=+12V$	—	15	—	mA

• AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	$t_{OS}$		—	50	—	ns

## ■ Optical Characteristics

<Inspection conditions>

- Ta=25°C, V<sub>DD</sub>=12V,  
Pulse: V<sub>OH</sub>=10V, V<sub>RH</sub>=12V, V<sub>S1H</sub>=12V, V<sub>S2H</sub>=10V, V<sub>S3H</sub>=4V, f<sub>C</sub>=f<sub>R</sub>=1MHz, T<sub>int</sub> (accumulation time)=10ms
- Light source: A light source with IR cutting filter (CM-500S)
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 5000 valid pixels for each color excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R <sub>R</sub>	Note 1		1.2		V/lx·s
	R <sub>G</sub>	Note 1		1.5		
	R <sub>B</sub>	Note 1		1.3		
Photo response non-uniformity	PRNU	Note 2		10		%
Saturation output voltage	V <sub>SAT</sub>	Note 3		1.0		V
Saturation exposure	SE <sub>R</sub>	Note 4		0.83		lx·s
	SE <sub>G</sub>	Note 4		0.67		
	SE <sub>B</sub>	Note 4		0.77		
Dark signal output voltage	V <sub>DRK</sub>	Dark condition, see Note 5		0.2	2.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 6		0.1	2.0	mV
Shift register total transfer efficiency	STTE		92			%
Output impedance	Z <sub>O</sub>				1	kΩ
Dynamic range	DR	Note 7		5000		
Signal output pin DC level	V <sub>OS</sub>	(OS1, OS2, OS3) see Note 8		4.5		V
Compensation output pin DC level	V <sub>DS</sub>	Note 8		4.5		V
Signal and compensation output pin DC level difference	V <sub>OS</sub> - V <sub>DS</sub>	Note 8			300	mV

Connect all NC pins externally to V<sub>SS</sub> (GND).

### Note 1) Responsivity (R)

This is the value obtained by dividing the average output voltage (V) of all valid pixels of each of the colors R, G, and B by the exposure (lx·s). The exposure is the product of the incident light intensity (lx) and the accumulation time (s). Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

### Note 2) Photo response non-uniformity (PRNU)

This is defined by the following equation where X<sub>ave</sub> is the average output voltage of the active pixels of each of the colors R, G, and B, and Δx is the difference between the output voltage of the maximum (or minimum) output pixel and X<sub>ave</sub>, when the photodetector region is illuminated with light of a uniform illumination intensity distribution.

$$\text{PRNU} = \frac{\Delta x}{X_{\text{ave}}} \times 100 (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

### Note 3) Saturation output voltage (V<sub>SAT</sub>)

This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

### Note 4) Saturation Exposure (SE)

This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

### Note 5) Dark signal output voltage (V<sub>DRK</sub>)

This is defined as the average of the output from all the valid pixels in the dark condition at Ta=25°C, T<sub>int</sub>=10ms. Normally, the dark signal output voltage gets doubled for every 8 to 10°C increase in Ta and is proportional to T<sub>int</sub>.

### Note 6) Dark signal non-uniformity (DSNU)

This is defined as the difference between the maximum value among the output voltages of the all valid pixels at Ta=25°C and T<sub>int</sub>=10ms and V<sub>DRK</sub>.



### ■ Optical Characteristics (continued)

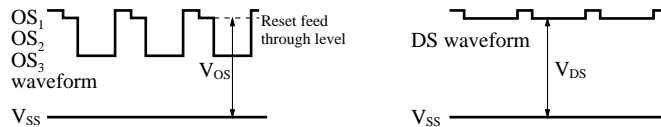
Note 7) Dynamic range (DR)

This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 8) The signal output pin DC level ( $V_{OS}$ ) and the compensation output pin DC level ( $V_{DS}$ ) are the voltage values given in the following figure.



### ■ Construction of the Image Sensor

The MN3672 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11μm floating photodiode and a 3μm channel stopper (isolation region) per pixel, and 5000 pixels' lines of each of the colors R, G, and B are arranged neighboring.
- There is a spacing of one line between B-R in the sideways scanning direction (center to center spacing of 14μm) and a similar one line spacing between R-G in the sideways scanning direction (center to center spacing of 14μm).
- The photodetector window is a rectangle of dimensions 8μm (Horizontal) × 11μm (Vertical), and the areas other than the photodetector window are optically shielded.
- The photodetector region has 24 optically shielded (black reference) pixels for each color that can be used as the black level reference.

b) CCD Transfer region (analog shift register)

- The signal charges obtained by photoelectric conversion are transferred to the CCD transfer regions of the respective colors during the period when the shift gate ( $\phi_{SG}$ ) is at the High level. The signal charges transferred to this analog shift register are successively transferred to the output region.
- A buried type CCD that can be driven by a two phase clock ( $\phi_1, \phi_2$ ) is used for the analog shift register.
- In the CCD transfer region, since each CCD shift register is


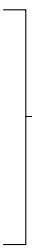
divided into four segments each of which are provided with separate  $\phi_1, \phi_2$  clock pins, it is possible to reduce the heat generation in the chip and the load on the clock driver circuit by providing separate clock driver circuit for each pin during high speed operation.

- The last gate of the CCD transfer region is connected to an independent pin ( $\phi_{IL}$ ). By driving this pin independent of the other pins by a clock driver, it is possible to speed up the flow of signal charge into the charge to voltage conversion region thereby making the output waveform rise sharply. This makes it easy to obtain margin of the signal processing time during high speed drive operation.

c) Output region

- The signal charge transferred to the output region is first sent to the charge to voltage conversion region where it is converted into a voltage level corresponding to the amount of the signal charge, and then output after impedance conversion in a two stage source follower amplifier.
- The DC level component not containing the optical signal and the clock noise component are output at the DS pin.
- It is possible to obtain a signal with a high S/N ratio with reduced clock noise, etc., by carrying out differential amplification of the OS and DS outputs externally.

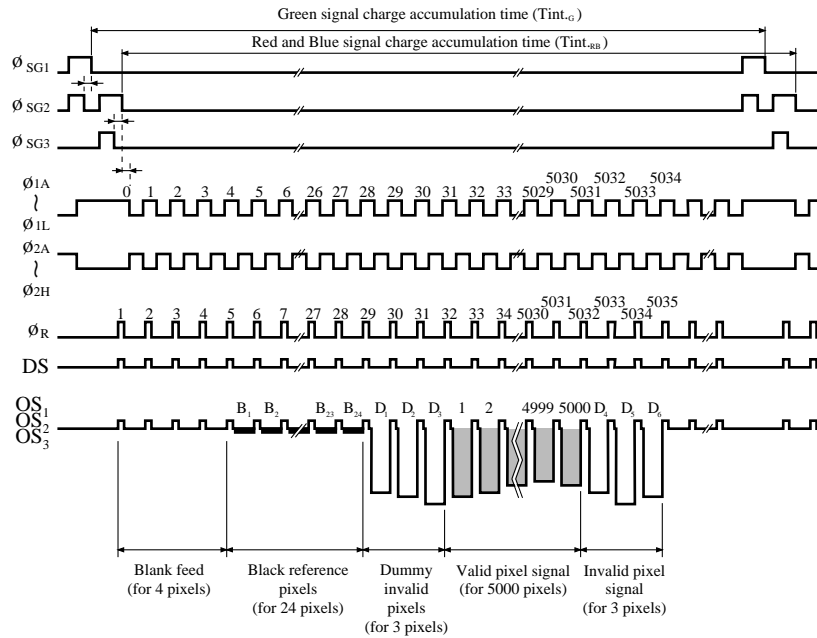
## ■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS <sub>1</sub>	Signal output 1 (Red)	Internally connected to pin 20.
2	OS <sub>2</sub>	Signal output 2 (Green)	
3	V <sub>DD</sub>	Power supply	
4	φ <sub>SG1</sub>	Shift clock gate 1	
5	V <sub>SS</sub>	Ground	
6	φ <sub>R</sub>	Reset clock	
7	NC	Non connection	 <p>All pins are independent. (Separate drivers can be used)</p>
8	φ <sub>2A</sub>	CCD clock (Phase 2)	
9	φ <sub>1A</sub>	CCD clock (Phase 1)	
10	φ <sub>1B</sub>	CCD clock (Phase 1)	
11	φ <sub>2B</sub>	CCD clock (Phase 2)	
12	φ <sub>2C</sub>	CCD clock (Phase 2)	
13	φ <sub>1C</sub>	CCD clock (Phase 1)	
14	φ <sub>1D</sub>	CCD clock (Phase 1)	
15	φ <sub>2D</sub>	CCD clock (Phase 2)	
16	SUB	Substrate	Should be left open.
17	NC	Non connection	Connected to the aluminum layer for optical shielding.
18	V <sub>SS</sub>	Ground	
19	V <sub>SS</sub>	Ground	Internally connected to pin 4.
20	φ <sub>SG1</sub>	Shift clock gate 1	
21	φ <sub>SG2</sub>	Shift clock gate 2	Internally connected to pin 37.
22	φ <sub>SG3</sub>	Shift clock gate 3	
23	NC	Non connection	 <p>All pins are independent. (Separate drivers can be used)</p>
24	NC	Non connection	
25	NC	Non connection	
26	φ <sub>2E</sub>	CCD clock (Phase 2)	
27	φ <sub>1E</sub>	CCD clock (Phase 1)	
28	φ <sub>1F</sub>	CCD clock (Phase 1)	
29	φ <sub>2F</sub>	CCD clock (Phase 2)	
30	φ <sub>2G</sub>	CCD clock (Phase 2)	
31	φ <sub>1G</sub>	CCD clock (Phase 1)	
32	φ <sub>1H</sub>	CCD clock (Phase 1)	
33	φ <sub>2H</sub>	CCD clock (Phase 2)	
34	NC	Non connection	Connected to the aluminum layer for optical shielding.
35	φ <sub>1L</sub>	CCD final stage clock (Phase 1)	
36	V <sub>SS</sub>	Ground	Internally connected to pin 22.
37	φ <sub>SG3</sub>	Shift clock gate 3	
38	V <sub>SS</sub>	Ground	
39	DS	Compensation output	
40	OS <sub>3</sub>	Signal output 3 (Blue)	

Note) Connect all NC pins externally to V<sub>SS</sub> (GND).

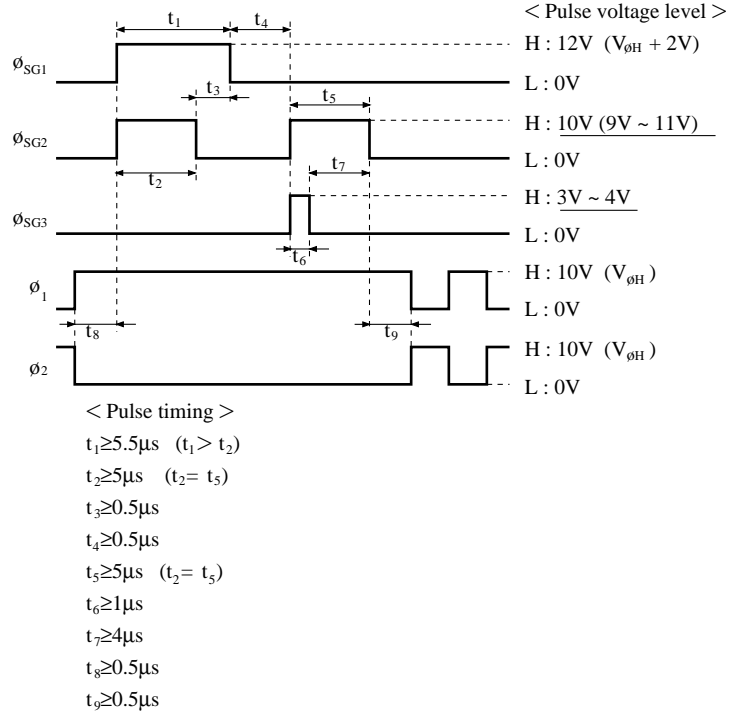
## ■ Timing Diagram

### (1) I/O timing

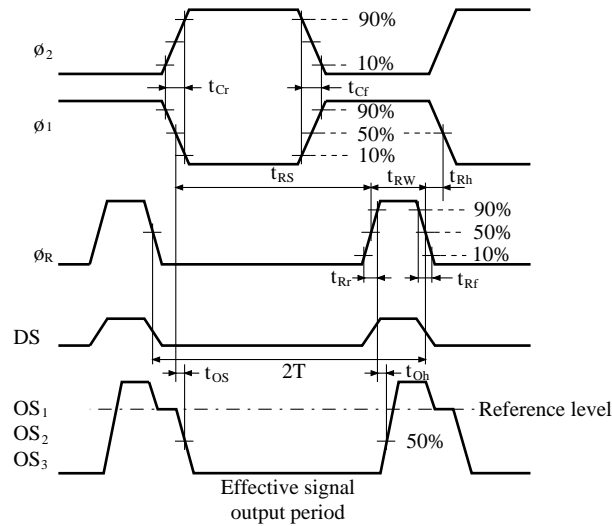


### (2) Drive timing 1

(during shifting signal charge to CCD)



(2) Drive timing 2  
(during repeated pattern)



■ Graphs and Characteristics

