Stereo Continuous Calibration DAC (CC-DAC)

TDA1311A

FEATURES

- Voltage output
- Space saving packages SO8 or DIP8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - single 4 to 5.5 V rail supply
  - output current and bias current are proportional to the supply voltage
  - integrated current-to-voltage converter
- Fast settling time permits 2, 4 and 8 × oversampling (serial input) or double-speed operation at 4 × oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement, TTL
- No zero-crossing distortion
- Cost efficient.

GENERAL DESCRIPTION

The TDA1311A; AT is a voltage-driven digital-to-analog converter and is new generation of DAC devices which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle which has an accuracy insensitive to ageing, temperature matching and process variations.

The TDA1311A; AT is fabricated in a 1.0 μm CMOS process and features an extremely low-power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1311A	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1311AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-?

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	17	30	mW

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BLOCK DIAGRAM

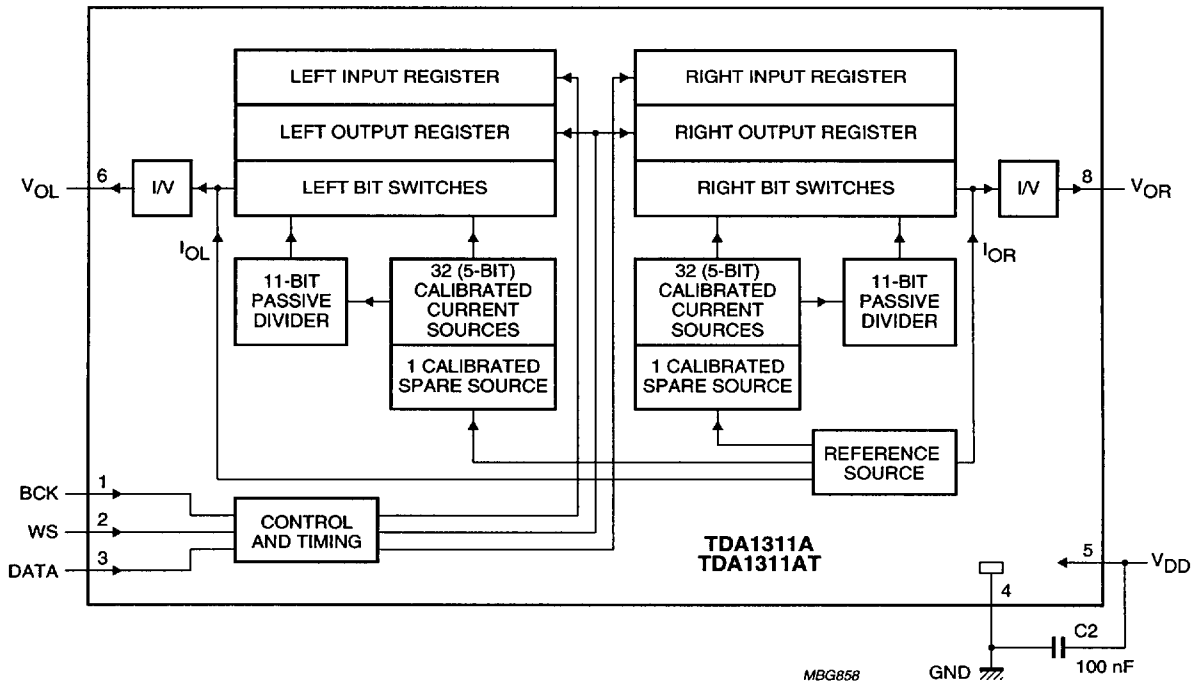

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
V_{OL}	6	left channel output
n.c.	7	not connected
V_{OR}	8	right channel output

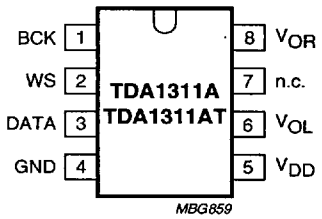

Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (see Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (see Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the OUT terminal.

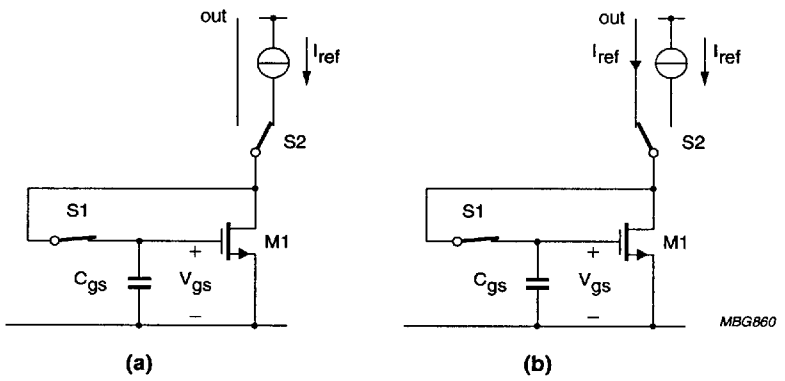
The 32 current sources and the spare current source of the TDA1311A; AT are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors.

A symmetrical offset decoding principle is incorporated that arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1311A; AT (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5.

With a HIGH level on the word select input (WS), data is placed in the left input register and with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

An internal offset voltage V_{OS} is added to the full scale output voltage V_{FS}; V_{OS} and V_{FS} are proportional to V_{DD}: $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{OS1}/V_{OS2}$.



(a) = calibration.
(b) = operation.

Fig.3 Calibration principle.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{stg}	storage temperature		–55	+150	°C
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Note

1. Human body model: C = 100 pF, R = 1500 Ω, 3 pulses positive and 3 pulses negative.
2. Machine model: C = 200 pF, L = 0.5 μH, R = 10 Ω, 3 pulses positive and 3 pulses negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIL8	100	K/W
	SO8	210	K/W

QUALITY SPECIFICATION

In accordance with SNW-FQ-0611.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.4	6.0	mA
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	μA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	μA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		1.8	2.0	2.2	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
V_{os}	offset voltage	$V_{DD} = V_{OL/ORmax}$	0.45	0.50	0.55	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 1	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level; note 1	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 1	–	–33	–	dB
			–	2	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.09	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		75	80	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 1	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB

Note

1. Measured with 1 kHz sinewave generated at sampling rate of 192 kHz.

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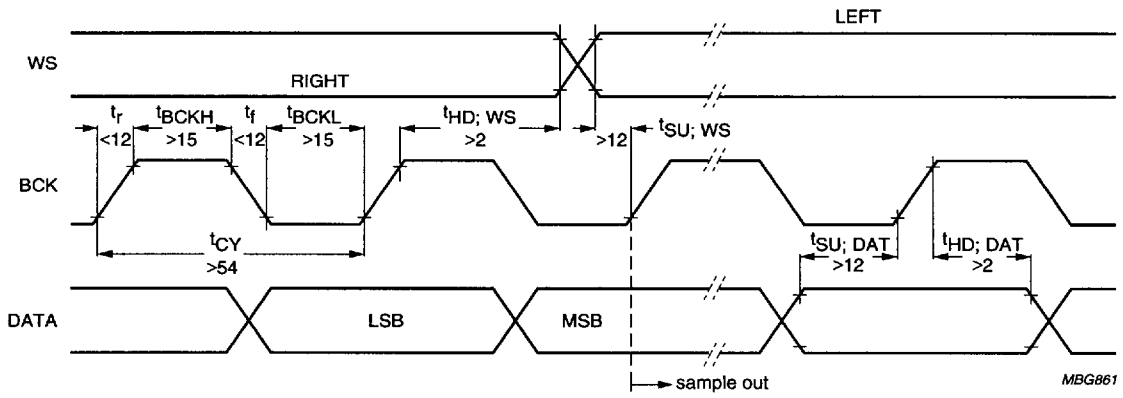

Fig.4 Timing and input signals.

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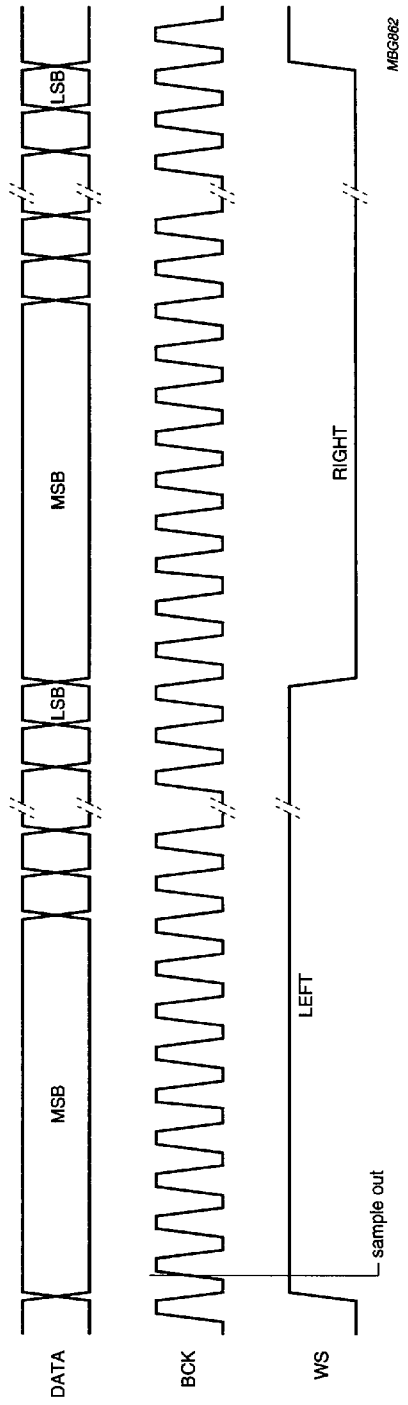

Fig.5 Format of input signals.

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APPLICATION INFORMATION

Basic application example

A typical example of a CD-application with the TDA1311A; AT is shown in Fig.6. It features typical decoupling components and a third-order analog post-filter stage providing a line output.

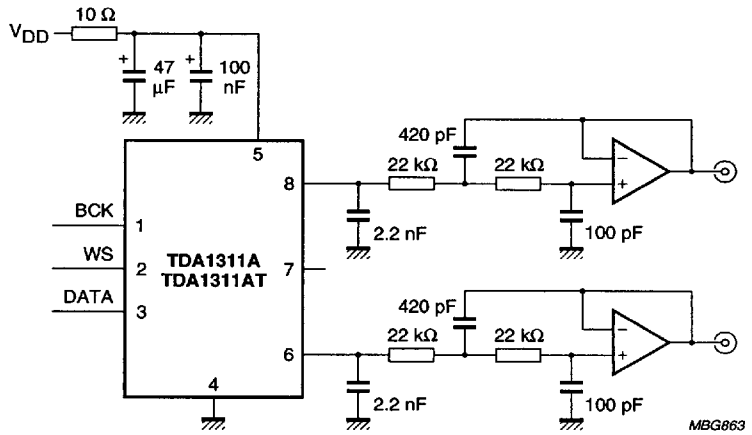

Fig.6 Example of a 3rd order filter application.

Attention to printed circuit board layout

The TDA1311A and even more so the TDA1311AT offers great ease in designing-in to printed-circuit boards due to its small size and low pin count. The TDA1311A; AT being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. Following some basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1311A; AT with a clean, noiseless V_{DD}, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns and separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives `free` additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Figure 7 shows recommended layouts for printed-circuit boards for the SO8 and DIL8 versions respectively. Both layouts use a single-interconnect layer.

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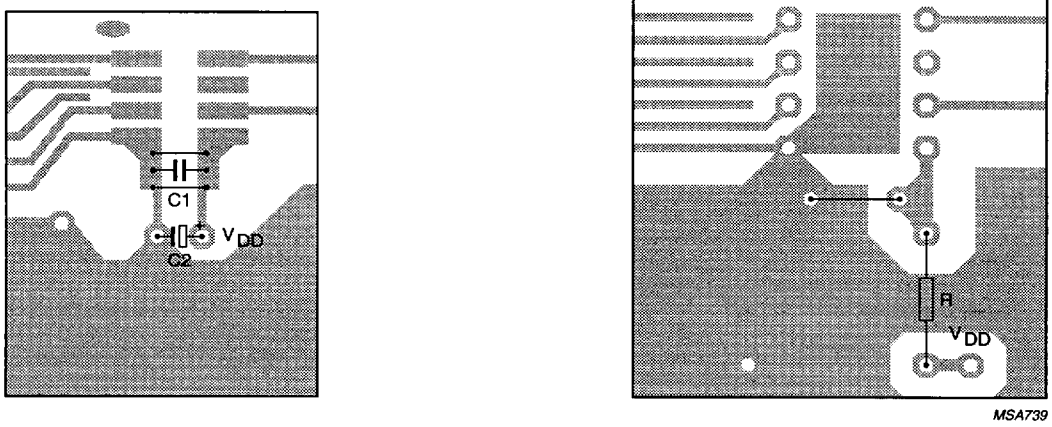

Fig.7 Recommended printed-circuit board layouts.

Interface examples

The following figures (Figs 8 to 14) show examples of connections to commonly used decoder and digital filter ICs. The digital interface part is shown only, for clarity. The diagrams are for guidance purposes only - **no** guarantee for industrial exploitation is implied.

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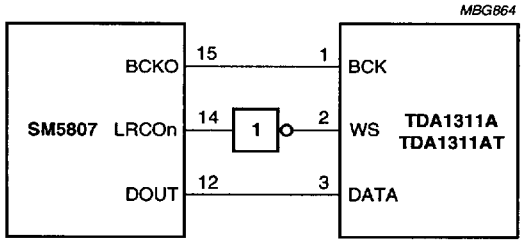
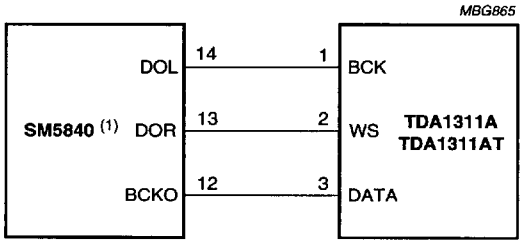
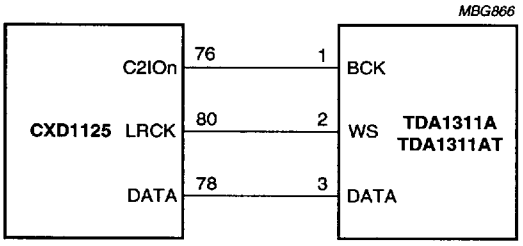


remark: SCSLn – signal SM5807 both "L" and "H" supported by TDA1311A and TDA1311AT



OMODn pin 19: "L" for 4FS operation
(1) versions A/B/G

Fig.9 NPC SM5840 digital filter (4FS).



MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H"
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.10 Sony CXD1125 decoder (1FS).

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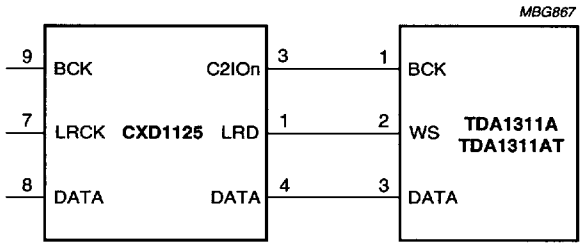
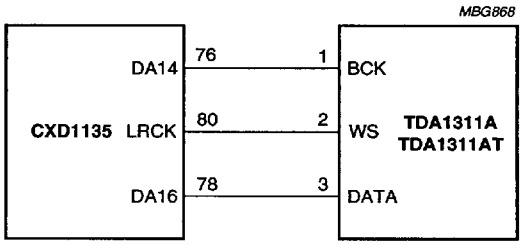


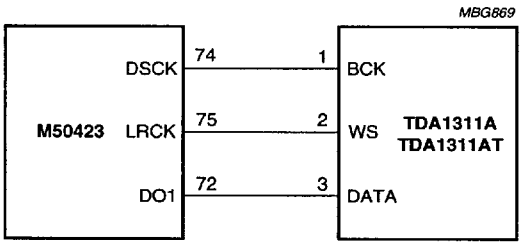
remark: CXD1162 input connectable to CXD1125 in the same way as for TDA1311A; AT to CXD1125

Fig.11 Sony CXD1162 digital filter (4FS).



MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H" for 1FS; "L" for 2FS
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.12 Sony CXD1135 decoder (1FS) and digital filter (2FS).



MODE SELECT:
DOBSEL pin 7: "L"
DASEL1 pin 8: "H"
DASEL2 pin 9: "L"
DASEL3 pin 10: "H"
DASEL4 pin 11: "L"

Fig.13 Mitsubishi M50423 decoder (1FS) and digital filter (4FS).

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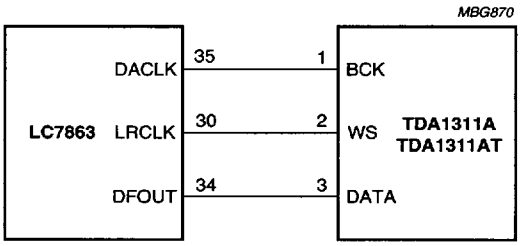

MODE SELECT:
DFOFF pin 27: "L"
MSBF pin 38: "H"

Fig.14 Sanyo LC7863 decoder (1FS).

Evaluation of audio parameters

The following measurement graphs are performed on singular engineering samples; therefore **no** guarantee of typical parameter values is implied. Measurement conditions are typical, as stated in the section Characteristics, unless otherwise indicated. The normal measurement set-up includes a 20 kHz band-limiting filter for bandwidth definition, and an A-weighting filter where indicated.

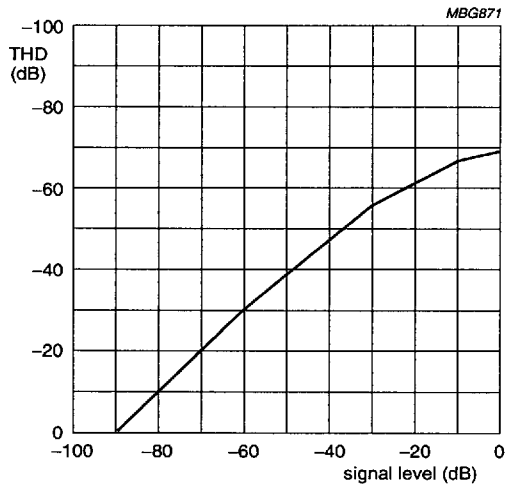

Fig.15 Total harmonic distortion plus noise as a function of signal level (4FS).

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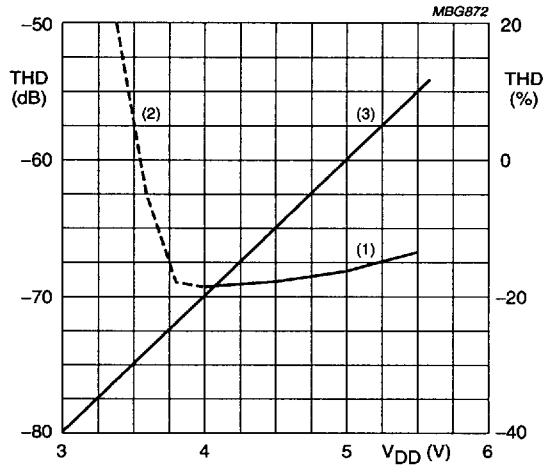
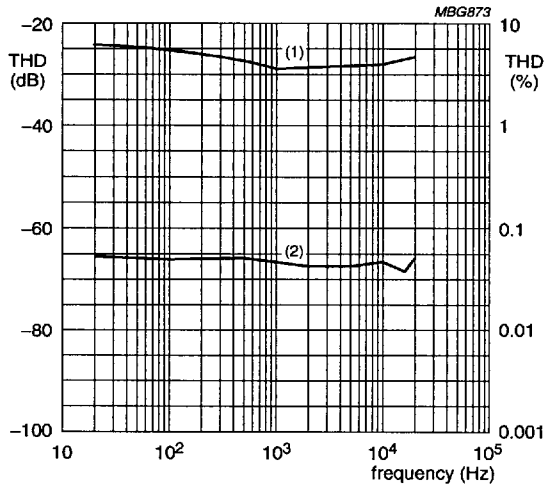


(1) Measured including all distortion plus noise within the specified operating supply voltage range.
(2) Measured including all distortion plus noise outside the specified operating supply voltage range.
(3) V_{FS} relative to nominal.

Fig.17 Total harmonic distortion plus noise as a function of supply voltage (4FS).



(1) Measured including all distortion plus noise at a signal level of −60 dB.
(2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.16 Total harmonic distortion plus noises as a function of frequency (4FS).

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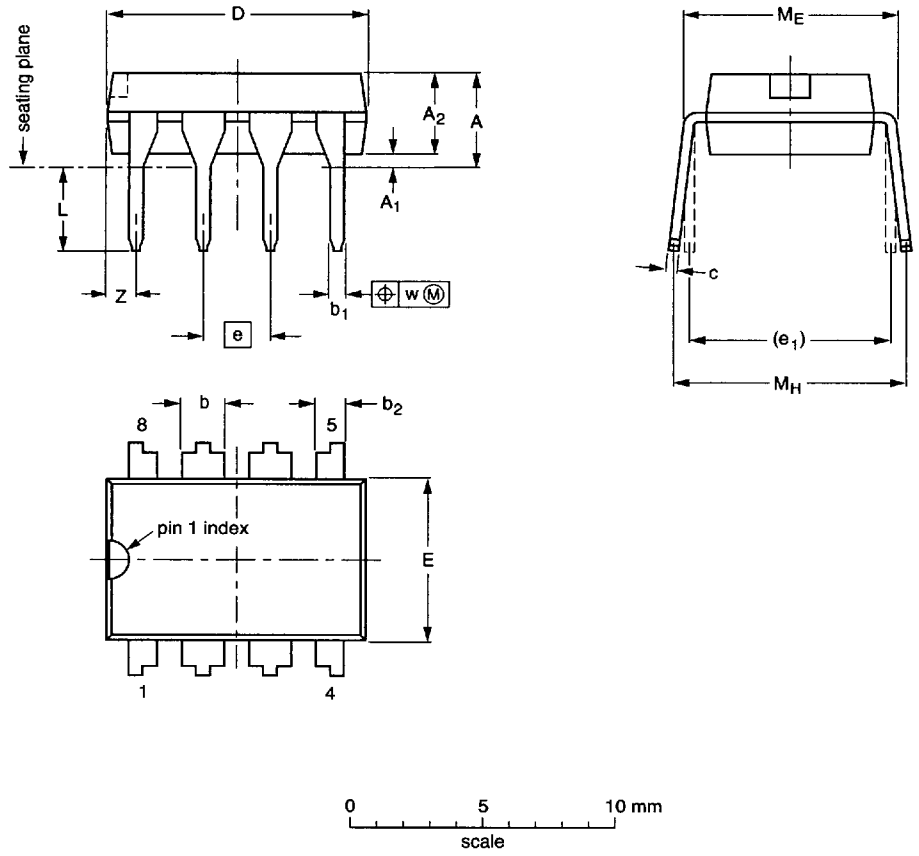
PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

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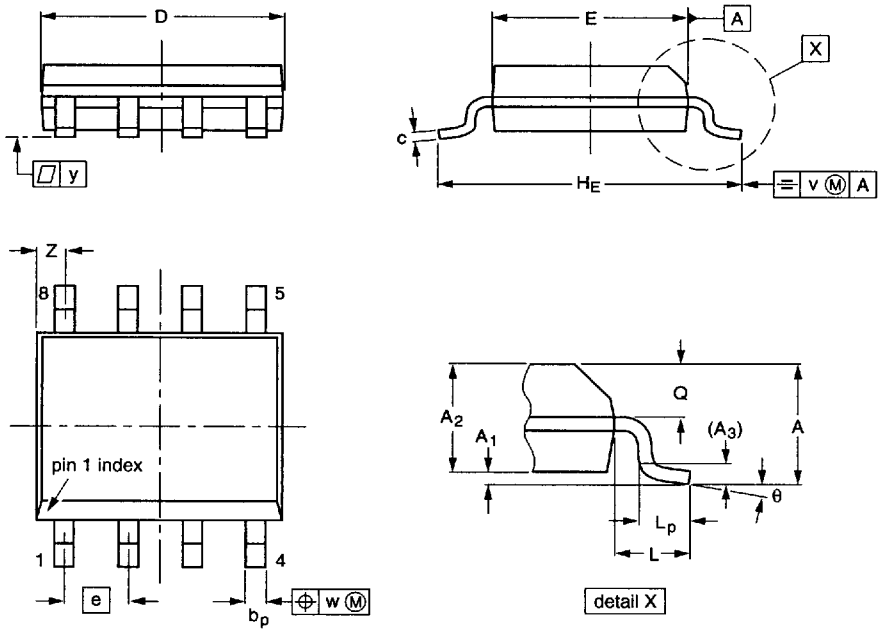
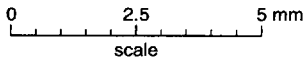
SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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