19-0394; Rev 0; 12/97

MAXIM

3-in-1 Silicon Delay Line

MXD1013

General Description

The MXD1013 contains three independent, monolithic, logic-buffered delay lines with delays ranging from 10ns to 200ns. Nominal accuracy is ±2ns for a 10ns to 60ns delay, ±3% for a 70ns to 100ns delay, and ±5% for a 150ns to 200ns delay. Relative to hybrid solutions, these devices offer enhanced performance and higher reliability, and reduce overall cost. Each output can drive up to ten standard 74LS loads.

The MXD1013 is available in multiple versions, each offering a different combination of delay times. It comes in the space-saving 8-pin µMAX package, as well as a standard 8-pin SO and DIP. It is also offered in industry-standard 16-pin SO and 14-pin DIP packaging, allowing full compatibility with the DS1013 and other delay-line products.

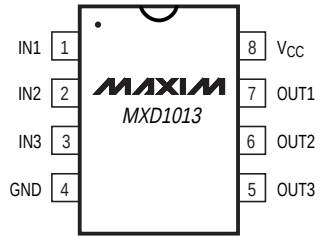
Applications

Clock Synchronization

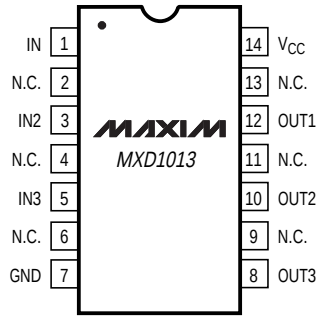
Digital Systems

Pin Configurations

TOP VIEW



DIP/SO/µMAX



DIP

Pin Configurations continued at end of data sheet.

Features

- ♦ **Improved Second Source to DS1013**
- ♦ **Available in Space-Saving 8-Pin µMAX Package**
- ♦ **20mA Supply Current (vs. Dallas' 40mA)**
- ♦ **Low Cost**
- ♦ **Three Separate Buffered Delays**
- ♦ **Delay Tolerance of ±2ns for MXD1013__010 through MXD1013__060**
- ♦ **TTL/CMOS-Compatible Logic**
- ♦ **Leading- and Trailing-Edge Accuracy**
- ♦ **Custom Delays Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXD1013C/D___	0°C to +70°C	Dice*
MXD1013PA___	-40°C to +85°C	8 Plastic DIP
MXD1013PD___	-40°C to +85°C	14 Plastic DIP
MXD1013SA___	-40°C to +85°C	8 SO
MXD1013SE___	-40°C to +85°C	16 Narrow SO
MXD1013UA___	-40°C to +85°C	8 µMAX

**Dice are tested at T_A = +25°C.*

Note: *To complete the ordering information, fill in the blank with the part number extension from the Part Numbers and Delay Times table to indicate the desired delay per output.*

Part Numbers and Delay Times

PART NUMBER EXTENSION (MXD1013___)	OUTPUT DELAY (ns)	PART NUMBER EXTENSION (MXD1013___)	OUTPUT DELAY (ns)
010	10	050	50
012	12	060	60
015	15	070	70
020	20	075	75
025	25	080	80
030	30	090	90
035	35	100	100
040	40	150	150
045	45	200	200

Functional Diagram appears at end of data sheet.

3-in-1 Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +6V
All Other Pins.....-0.5V to (V_{CC} + 0.5V)
Short-Circuit Output Current (1sec).....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.0mW/°C above +70°C) ...800mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) 696mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 2)	4.75	5.00	5.25	V
Input Voltage High	V_{IH}	(Note 2)	2.2			V
Input Voltage Low	V_{IL}	(Note 2)			0.8	V
Input Leakage Current	I_L	0V ≤ V_{IN} ≤ V_{CC}	-1		1	µA
Active Current	I_{CC}	V_{CC} = 5.25V, period = minimum (Note 3)		20	70	mA
Output Current High	I_{OH}	V_{CC} = 4.75V, V_{OH} = 4.0V			-1	mA
Output Current Low	I_{OL}	V_{CC} = 4.75V, V_{OL} = 0.5V	12			mA
Input Capacitance	C_{IN}	T_A = +25°C (Note 4)		5	10	pF

TIMING CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = +25°C, unless otherwise noted.)

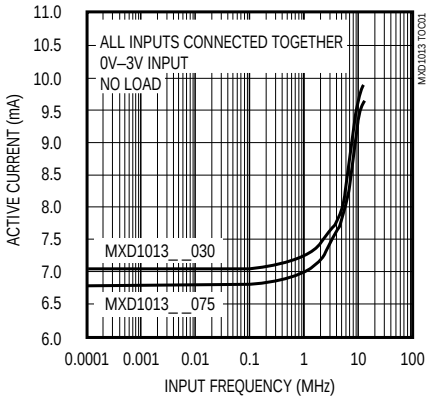
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 5)	100% of t_{PLH}			ns
Input-to-Output Delay (leading edge)	t_{PLH}	(Notes 6, 7, 8)	*See Part Number and Delay Times table*			ns
Input-to-Output Delay (trailing edge)	t_{PHL}	(Notes 6, 7, 8)	*See Part Number and Delay Times table*			ns
Power-Up Time	t_{PU}				100	ms
Period		(Note 5)	3(t_{WI})			ns

Note 1: Specifications to -40°C are guaranteed by design, not production tested.
Note 2: All voltages referenced to GND.
Note 3: Measured with outputs open.
Note 4: Guaranteed by design.
Note 5: Pulse width and/or period specifications may be exceeded, but accuracy is application sensitive (i.e., layout, decoupling, etc.).
Note 6: V_{CC} = +5V at +25°C. Typical delays are accurate on both rising and falling edges within ±2ns for delays from 10ns to 60ns, within ±3% for delays from 70ns to 100ns, and within ±5% for delays from 150ns to 200ns.
Note 7: The *Part Number and Delay Times* table provides typical delays at +25°C with V_{CC} = +5V. The delays may shift with temperature and supply variations. The combination of temperature (from +25°C to 0°C, or +25°C to +70°C) and supply variation (from 5V to 4.75V, or 5V to 5.25V) could produce an additional typical delay of ±1.5ns or ±3%, whichever is greater.
Note 8: All output delays tend to vary unidirectionally with temperature or supply voltage variations (i.e., if OUT1 slows down, all other outputs also slow down).

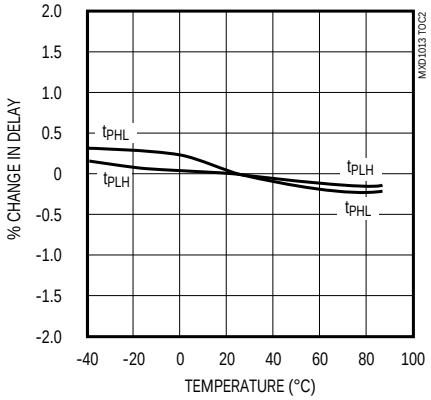
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

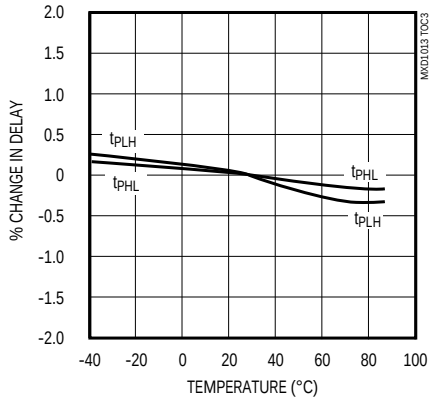
ACTIVE CURRENT vs. INPUT FREQUENCY



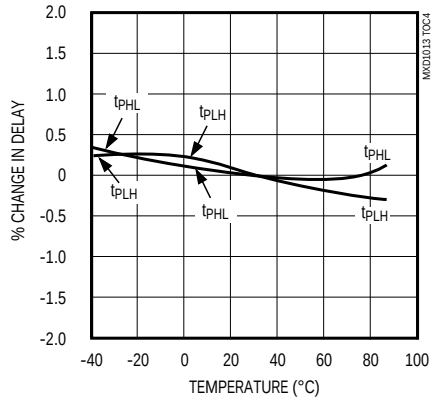
MXD1013_ _100 PERCENT CHANGE IN DELAY vs. TEMPERATURE (OUT1)



MXD1013_ _100 PERCENT CHANGE IN DELAY vs. TEMPERATURE (OUT2)



MXD1013_ _00 PERCENT CHANGE IN DELAY vs. TEMPERATURE (OUT3)



3-in-1 Silicon Delay Line

Pin Description

PIN			NAME	FUNCTION
8-PIN DIP/SO/µMAX	14-PIN DIP	16-PIN SO		
1	1	1	IN1	First Independent Input
2	3	4	IN2	Second Independent Input
3	5	6	IN3	Third Independent Input
4	7	8	GND	Device Ground
5	8	9	OUT3	Third Delayed Output
6	10	11	OUT2	Second Delayed Output
7	12	13	OUT1	First Delayed Output
8	14	16	V_{CC}	Power-Supply Input
—	2, 4, 6, 9, 11, 13	2, 3, 5, 7, 10, 12, 14, 15	N.C.	Not Connected

Definitions of Terms

Period: The time elapsed between the first pulse's leading edge and the following pulse's leading edge.

Pulse Width (t_{WI}): The time elapsed on the pulse between the 1.5V level on the leading edge and the 1.5V level on the trailing edge, or vice versa.

Input Rise Time (t_{RISE}): The elapsed time between the 20% and 80% points on the input pulse's leading edge.

Input Fall Time (t_{FALL}): The time elapsed between the 80% and 20% points on the input pulse's trailing edge.

Time Delay, Rising (t_{PLH}): The time elapsed between the 1.5V level on the input pulse's leading edge and the corresponding output pulse's leading edge.

Time Delay, Falling (t_{PHL}): The time elapsed between the 1.5V level on the input pulse's trailing edge and the corresponding output pulse's trailing edge.

Test Conditions

Ambient Temperature:	+25°C
Supply Voltage (V_{CC}):	5.0V ±0.1V
Input Pulse:	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Times:	3.0ns max
Pulse Width:	500ns max
Period:	1µs

Each output is loaded with a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edges. The time delay due to the 74F04 is subtracted from the measured delay.

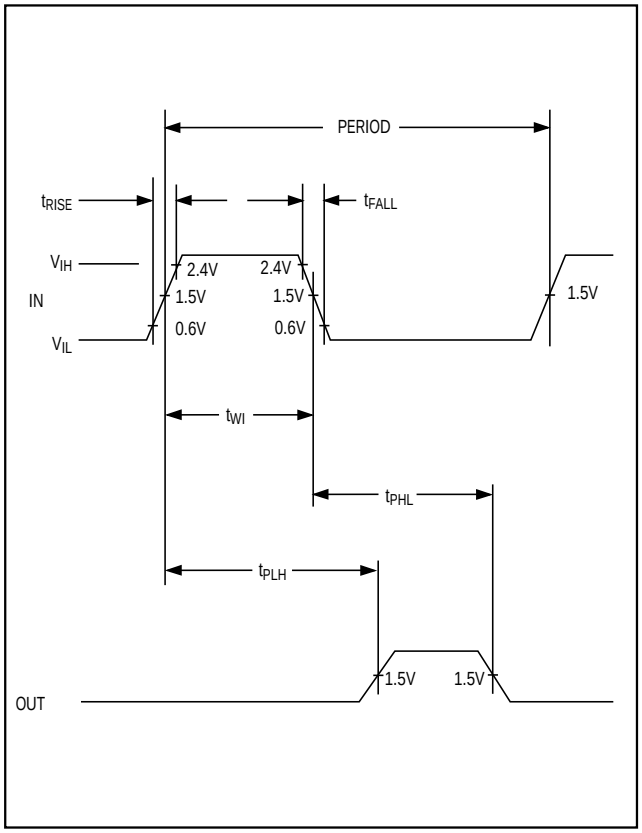


Figure 1. Timing Diagram

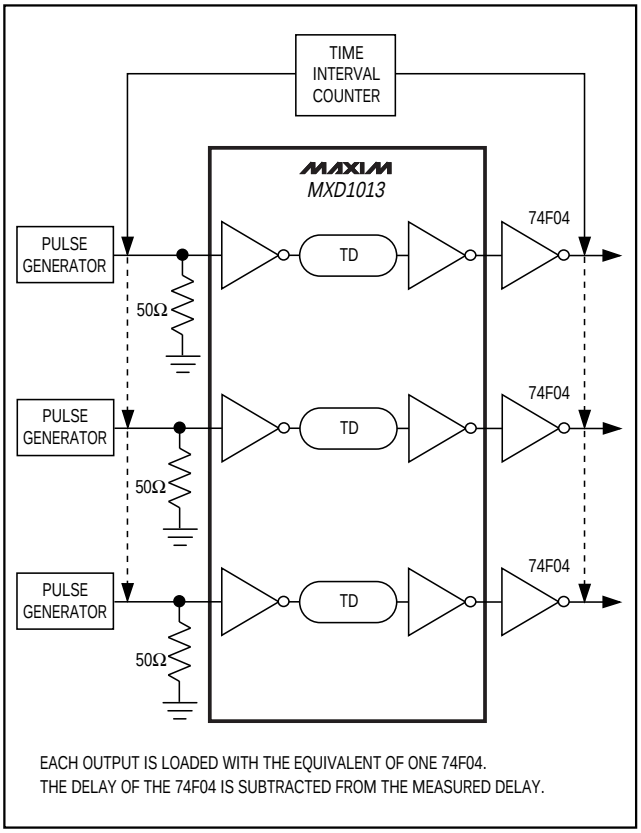


Figure 2. Test Circuit

Applications Information

Supply and Temperature Effects on Delay

Over the specified range, the MXD1013's delays are typically 2% accurate. Variations in supply voltage may affect the MXD1013's fixed output delays. Supply voltages beyond the specified range may result with larger variations. Although there might be a slight variance in delays over temperature, the MXD1013 is internally compensated to maintain its nominal values.

Loading Effect on Delay Lines

Capacitive loads increase delay times as they increase the rise and fall times of the delay lines. Other logic devices increase the capacitance at the output of the delays, which can affect device performance.

Board Layout Considerations

Bypass the MXD1013 with a 0.1µF capacitor to minimize the impact of high-speed switching on the power supply. The power supply must be able to deliver the required switching currents for proper operation.

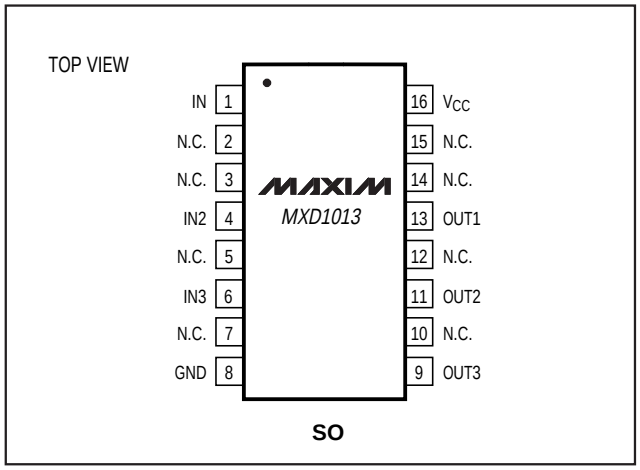
It is advisable to minimize trace lengths in order to reduce board capacitance as well as the traveling distance between devices. Sockets and wire-wrapped boards increase capacitance and should be avoided.

Chip Information

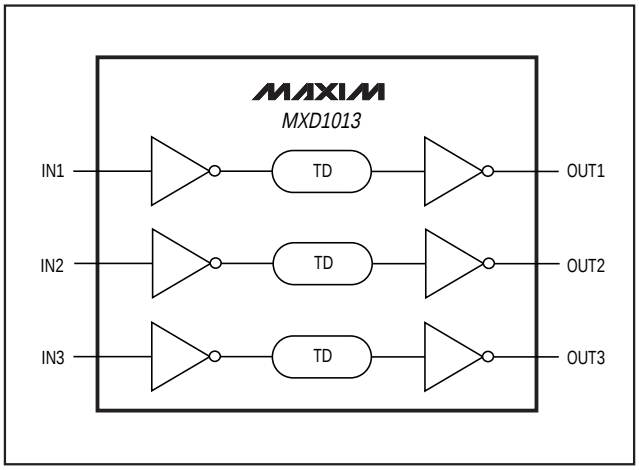
TRANSISTOR COUNT: 824

3-in-1 Silicon Delay Line

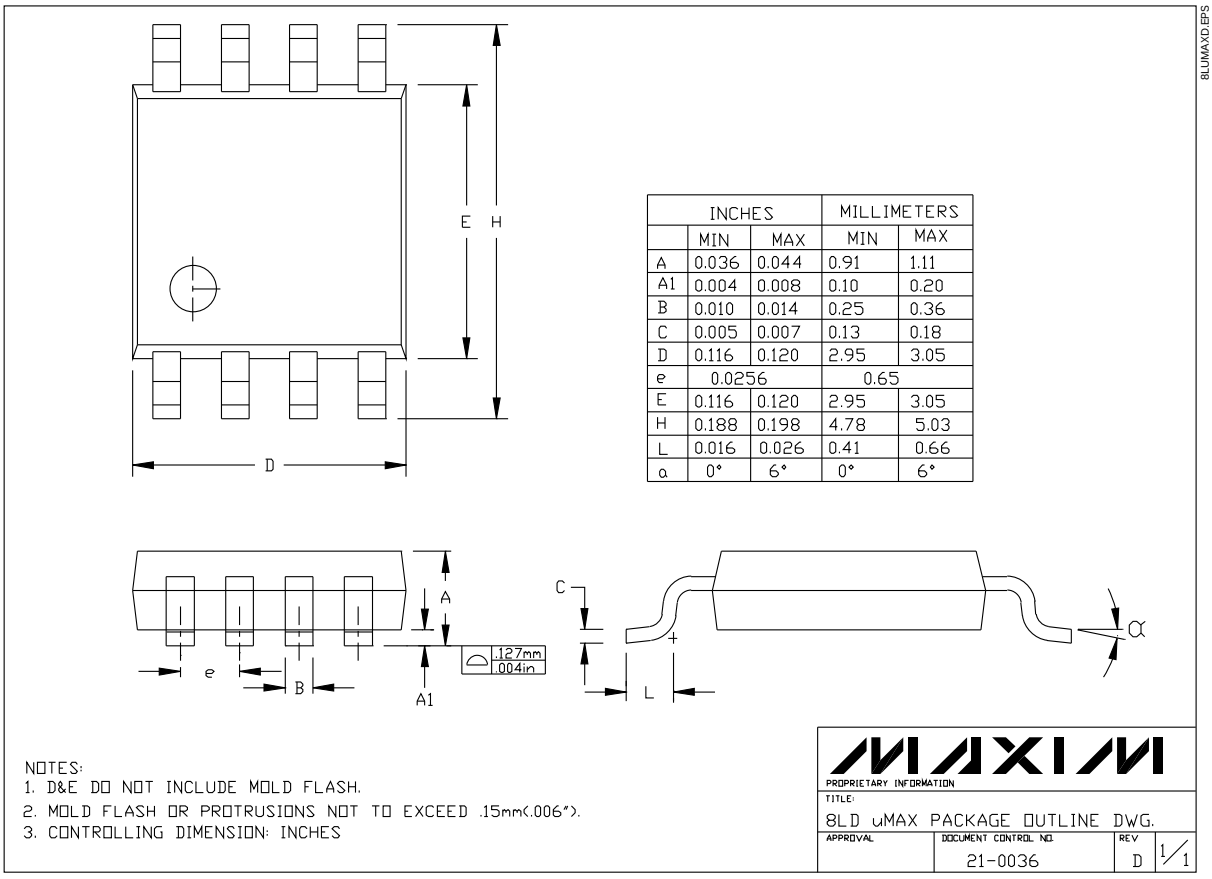
Pin Configurations (continued)



Functional Diagram



Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°