

High Performance
64K×8 3.3V
CMOS SRAM



AS7C3512
AS7C3512L

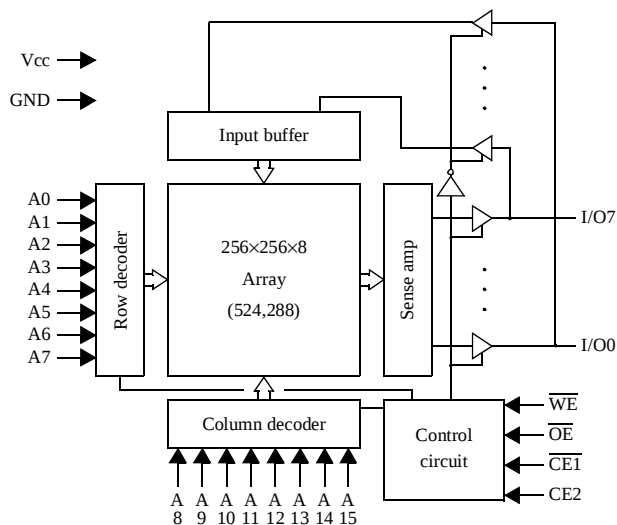
Low voltage 64K×8 CMOS SRAM

Preliminary information

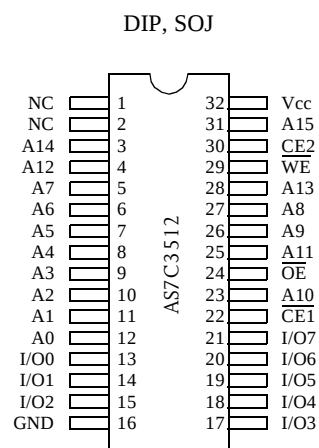
Features

- Organization: 65,536 words × 8 bits
- Single 3.3 ±0.3V power supply
- 5V tolerant I/O specification
- High speed
 - 12/15/20/25/35 ns address access time
 - 3/4/5/6/8 ns output enable access time
- Very low power consumption
 - Active: 250 mW max, 12 ns cycle
 - Standby: 9.0 mW max, CMOS I/O
1.8 mW max, CMOS I/O, L version
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- Ideal for cache and portable computing
 - 75% power reduction during CPU idle mode
- 32-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
- ESD protection >2000 volts
- Latch-up current >200 mA

Logic block diagram



Pin arrangement



Selection guide

	7C3512-12	7C3512-15	7C3512-20	7C3512-25	7C3512-35	Unit
Maximum address access time	12	15	20	25	35	ns
Maximum output enable access time	3	4	5	6	8	ns
Maximum operating current	70	65	60	55	50	mA
Maximum CMOS standby current	2.5	2.5	2.5	2.5	2.5	mA
	L	0.5	0.5	0.5	0.5	mA

Shaded areas contain advance information.



Functional description

The AS7C3512 is a 3.3V high performance CMOS 524,288-bit Static Random Access Memory (SRAM) organized as 65,536 words $\times$ 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters standby mode when $\overline{CE1}$ is HIGH or CE2 is LOW. CMOS standby mode consumes ≤ 9.0 mW (≤ 1.8 mW for the L version). Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode. Both versions of the AS7C3512 offer 2.0V data retention.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/4/5/6/8 ns are ideal for high performance applications. The active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and 5V tolerant. Operation is from a single 3.3 ± 0.3 V supply. The AS7C3512 is packaged in all high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{CC}	-0.5	+4.6	V
Input voltage relative to GND	V_{IN}	-0.5	+6.0	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-55	+150	°C
Temperature under bias	T_{bias}	-10	+85	°C
DC output current	I_{out}	—	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB} , I_{SB1})
X	L	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH



Recommended operating conditions

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input voltage	V _{IH}	2.0	-	5.5	V
	V _{IL}	-0.5 [†]	-	0.8	V

[†]V_{IL} min = -2.0V for pulse width less than t_{RC}/2.DC operating characteristics¹(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test conditions	-12		-15		-20		-25		-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	I _{LI}	V _{CC} = Max, V _{in} = GND to V _{CC}	-	1	-	1	-	1	-	1	-	1	μA
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} , V _{CC} = Max, V _{out} = GND to V _{CC}	-	1	-	1	-	1	-	1	-	1	μA
Operating power supply current	I _{CC}	CE1 = V _{IL} , CE2 = V _{IH} , f = f _{max} , I _{out} = 0 mA	-	70	-	65	-	60	-	55	-	50	mA
Standby power supply current	I _{SB}	CE1 = V _{IH} or CE2 = V _{IL} , f = f _{max}	-	30	-	25	-	20	-	20	-	15	mA
	I _{SB1}	CE1 ≥ V _{CC} -0.2V or CE2 ≤ 0.2V, V _{in} ≤ 0.2V or V _{in} ≥ V _{CC} -0.2V, f = 0	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	mA
		L	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	mA
Output voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
	V _{OH}	I _{OH} = -4 mA, V _{CC} = Min	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V

Shaded areas contain advance information.

Capacitance²(f = 1 MHz, T_a = Room temperature, V_{CC} = 3.3V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CE1, CE2, WE, OE	V _{in} = 0V	5	pF
I/O capacitance	C _{I/O}	I/O	V _{in} = V _{out} = 0V	7	pF



Read cycle^{3,9,12}

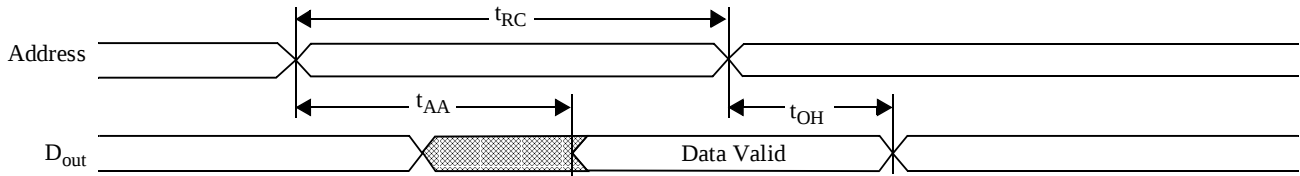
($V_{CC} = 3.3 \pm 0.3V$, $GND = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	
Address access time	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	—	12	—	15	—	20	—	25	—	35	ns	3, 12
Chip enable ($\overline{CE2}$) access time	t_{ACE2}	—	12	—	15	—	20	—	25	—	35	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	—	3	—	4	—	5	—	6	—	8	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	3	—	ns	5
Chip enable ($\overline{CE1}$) to output in Low Z	t_{CLZ1}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
Chip enable ($\overline{CE2}$) to output in Low Z	t_{CLZ2}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
Chip disable ($\overline{CE1}$) to output in High Z	t_{CHZ1}	—	3	—	4	—	5	—	6	—	8	ns	4, 5, 12
Chip disable ($\overline{CE2}$) to output in High Z	t_{CHZ2}	—	3	—	4	—	5	—	6	—	8	ns	4, 5, 12
Output enable to output in Low Z	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Output disable to output in High Z	t_{OHZ}	—	3	—	4	—	5	—	6	—	8	ns	4, 5
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 12
Chip disable to power down time	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	4, 5, 12

Shaded areas contain advance information

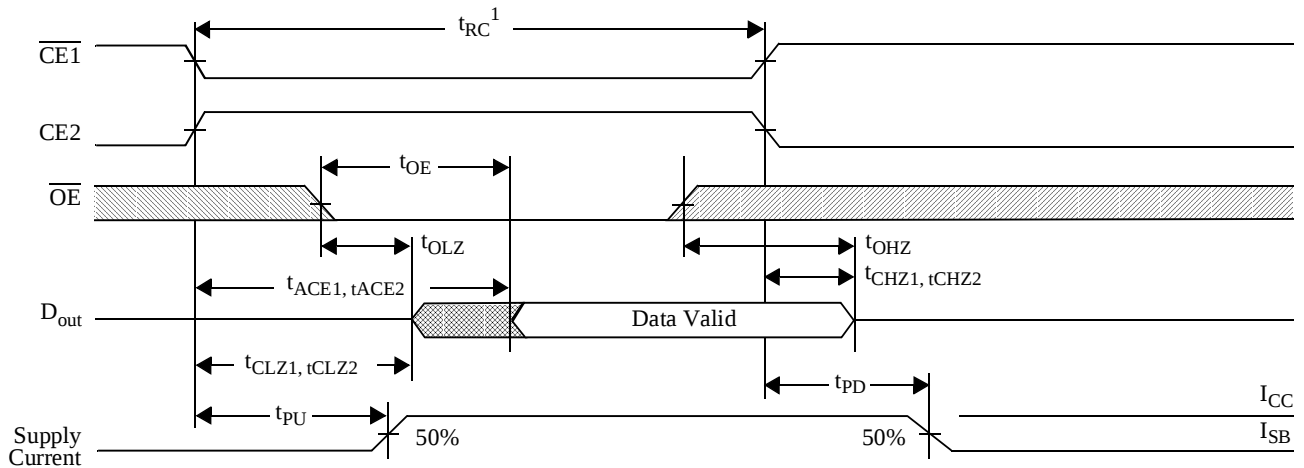
Read waveform 1^{3,6,7,9,12}

Address controlled



Read waveform 2^{3,6,8,9,12}

$\overline{CE1}$ and $\overline{CE2}$ controlled





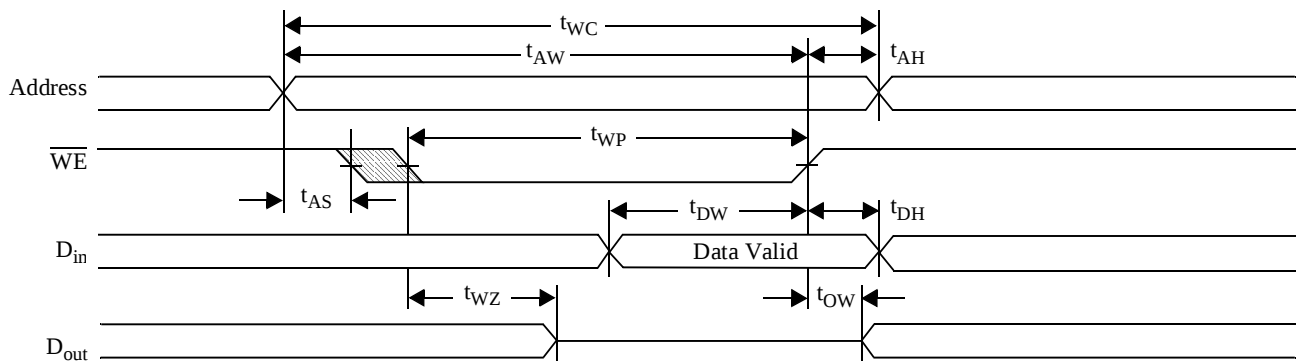
Write cycle^{11,12}

($V_{CC} = 3.3 \pm 0.3V$, GND = 0V, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	12	—	15	—	20	—	25	—	30	—	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	10	—	12	—	12	—	15	—	20	—	ns	12
Chip enable (CE2) to write end	t_{CW2}	10	—	12	—	12	—	15	—	20	—	ns	12
Address setup to write end	t_{AW}	10	—	12	—	12	—	15	—	20	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	12
Write pulse width	t_{WP}	8	—	9	—	12	—	15	—	17	—	ns	
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to write end	t_{DW}	6	—	8	—	10	—	12	—	15	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Write enable to output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	—	5	ns	4, 5
Output active from write end	t_{OW}	3	—	3	—	3	—	3	—	3	—	ns	4, 5

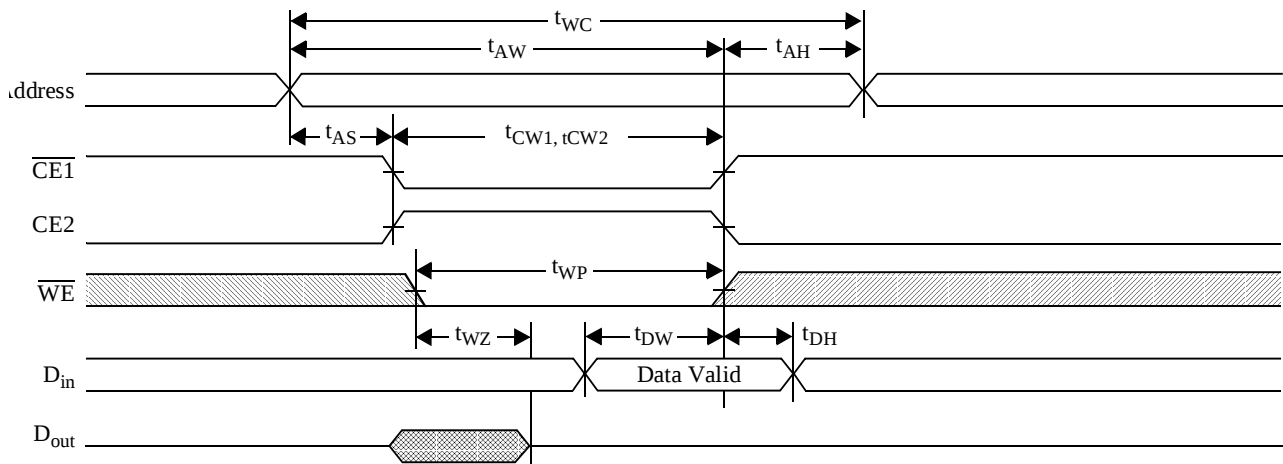
Write waveform 1^{10,11,12}

WE controlled



Write waveform 2^{10,11,12}

$\overline{CE1}$ and CE2 controlled

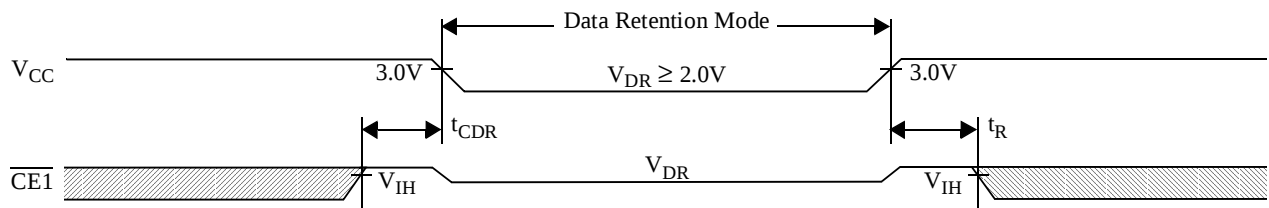




Data retention characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0V$	2.0	—	V
Data retention current	I_{CCDR}	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	—	1200	μA
Chip deselect to data retention time	t_{CDR}		—	250	μA
Operation recovery time	t_R	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	—	ns
Input leakage current	$ I_{LI} $		t_{RC}	—	ns
			—	1	μA

Data retention waveform



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

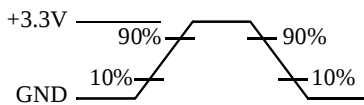


Figure A: Input Waveform

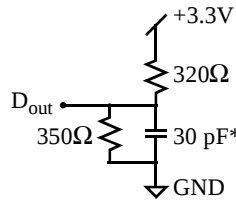


Figure B: Output Load

Thevenin equivalent:

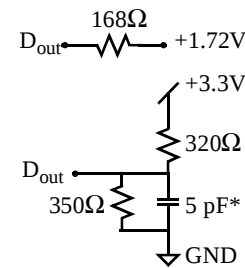


Figure C: Output Load for t_{CLZ} , t_{CHZ}

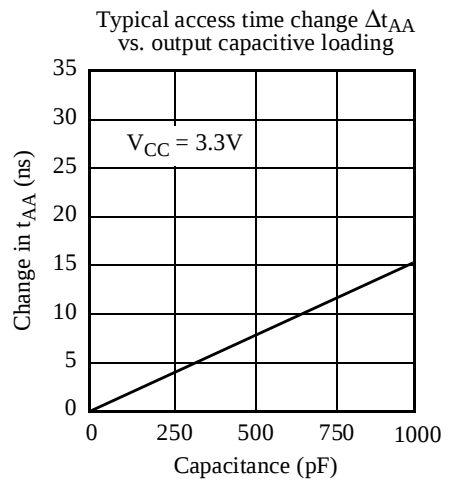
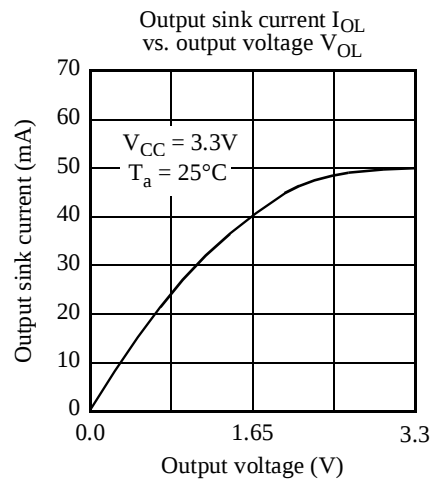
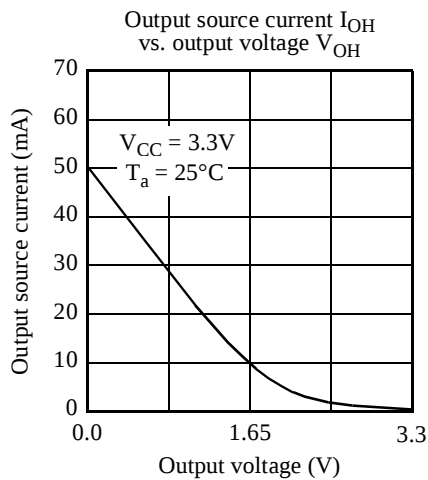
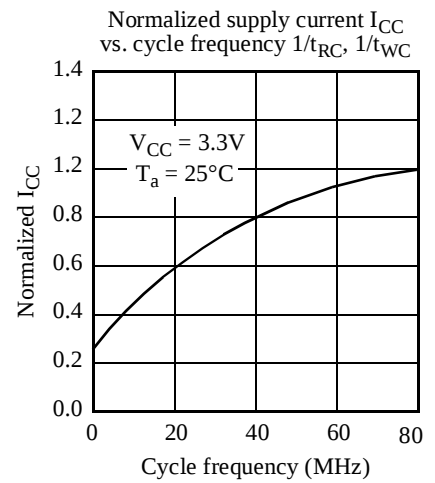
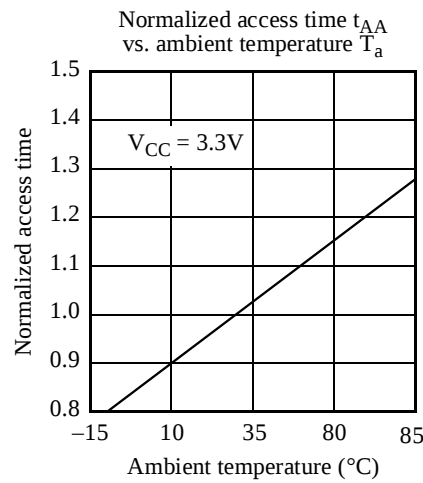
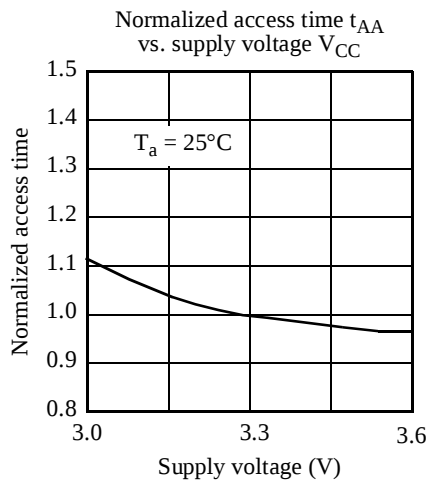
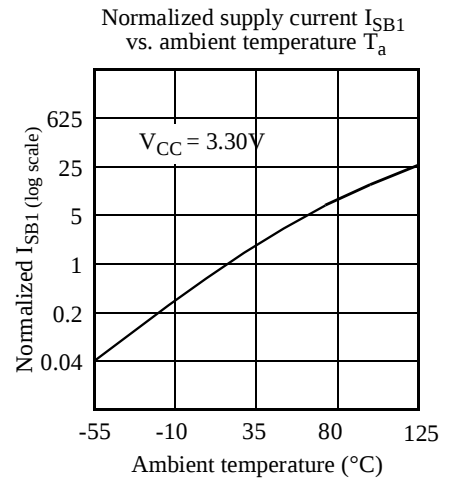
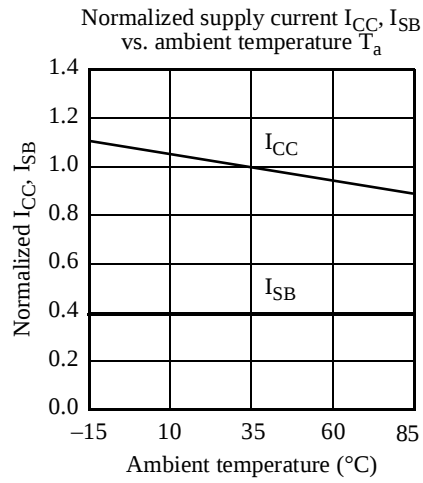
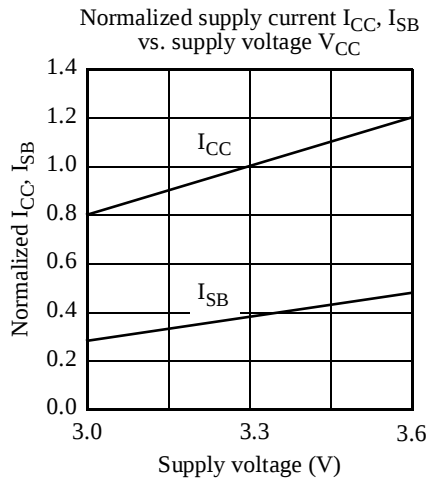
*including scope and jig capacitance

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
- 2 This parameter is sampled and not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, C.
- 4 t_{CLZ} and t_{CHZ} are specified with $CL = 5pF$ as in Figure C. Transition is measured $\pm 500mV$ from steady-state voltage.
- 5 This parameter is guaranteed but not tested.
- 6 $\overline{WE}$ is HIGH for read cycle.
- 7 $\overline{CE1}$ and $\overline{OE}$ are LOW and $CE2$ is HIGH for read cycle.
- 8 Address valid prior to or coincident with $\overline{CE1}$ transition LOW and $CE2$ transition HIGH.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or $CE2$ LOW during address transitions.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 $\overline{CE1}$ and $CE2$ have identical timing.



Typical DC and AC characteristics



AS7C3512
AS7C3512L



Ordering information

Package \ Access Time	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C3512-12PC AS7C3512L-12PC	AS7C3512-15PC AS7C3512L-15PC	AS7C3512-20PC AS7C3512L-20PC	AS7C3512-25PC AS7C3512L-25PC	AS7C3512-35PC AS7C3512L-35PC
Plastic SOJ, 300 mil	AS7C3512-12JC AS7C3512L-12JC	AS7C3512-15JC AS7C3512L-15JC	AS7C3512-20JC AS7C3512L-20JC	AS7C3512-25JC AS7C3512L-25JC	AS7C3512-35JC AS7C3512L-35JC

Shaded areas contain advance information.

Part numbering system

AS7C	3	512	-XX	X	C
SRAM prefix	Blank = 5V supply 3 = 3.3V supply	Device number	Access time	Package: P = PDIP 300 mil J = SOJ 300 mil	Commercial temperature range, 0°C to 70 °C

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