Data Sheet, DS3, June 2001

TE3-MUX
M13 Multiplexer and DS3 Framer
PEB 3445 E V2.1

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Revision History:	**2001-06-29**	DS3
Previous Version:	Preliminary Data Sheet 09.2000	

Page	Subjects (major changes since last revision)
	Changed document to new documentation guidelines.
21	Recommendation for demultiplexed bus operation added to signal LALE.
55	Added table content which was missing in previous version.
64f., 66f. 185ff., 188ff.	**Figure 16**, **Figure 17**, **Figure 18**, **Figure 19** corrected. LBHE respectively LBLE were wrong in previous version. Timings of LBHE in **Figure 24** and **Figure 25** redrawn. **Figure 27** added. Merged timings for LA and LBHE. Timings of LBLE in **Figure 28** and **Figure 29** redrawn. **Figure 31** added. Merged timings of LA and LBLE.
84, 139	Description of register bits SIDLE, SAISA, RDC extended.
91, 101, 113, 118, 127, 151, 154	Description of register bits OD, XBIT, GN, RES, T1E1 corrected.
167, 179	Major parts of register description (FHND and PHND) rewritten. Register FHND: Bits ABORT and XTF removed. Register PHND: Bit XTF removed.
177	Removed register bit XRA.
191	Section ’DMA Interface Signals’ added.
204	RTD is updated with rising edge of RTC. This is corrected in **Figure 49**.
	Some minor documentation updates (wording, syntax, ...).
	Name change M13FX -> TE3-MUX. Removed PEF version. Corrected **Table 27 "DS1/E1 Receive Data Timing" on Page 202**.
	Changed figure 25 and 27. Removed timing 35. Changed timings 101,111,151,152,195,198. Changed table 11.
	Changed FEAC FHND register to contain XTF bit.

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V2.1

1 TE3-MUX Overview

The TE3-MUX integrates a DS3 framer, with a M13 multiplexer, a tributary interchanger/ line selector and 32 serial line interfaces for DS1/E1/J1 lines with 4:28 line protection capability. It is an economical solution for applications, which require DS3 framing but no DS1/E1 framers. This is often required in a Central office where DS1/E1 from different equipment are multiplexed in a card. The TE3-MUX allows the DS1/E1 to be aggregated into DS3 without investing in the framers. Line and remote loopback capabilities can be used to trouble shoot in case of broken connections and other failures. The use of standard line interfaces to interconnect office equipment is called Office Repeater Bay (ORB) compliance.

1.1 General Features

- Integrates a M13 multiplexer and a DS3 framer operating in M13 or C-bit parity mode
- Optionally the M13 multiplexer can be disabled, which provides an integrated solution for combined channelized/unchannelized DS3 applications
- Provides 32 tributary interfaces where each interface can be switched to any of the 28DS1/21E1 tributaries of the DS3 signal
- Integrates a bit error rate tester
- Integrates a 16-/8-bit switchable Intel or Motorola style microprocessor interface which operates in multiplexed or demultiplexed bus mode
- JTAG boundary scan according to IEEE1149.1 (5 pins).
- 0.25 µm, 2.5V low power core technology
- I/Os are 3.3V tolerant and have 3.3V driving capability
- Package P-BGA-272-1 (27mm x 27mm; pitch 1.27mm)
- Full scan path and BIST of on-chip RAMs for production test
- Power consumption: 340mW (typical)
- Temperature range -40..+85°C

1.1.1 M23 Multiplexer and DS3 Framer

- Multiplexing/demultiplexing of seven DS2 into/from M13 asynchronous format according to ANSI T1.107, ANSI T1.107a
- Multiplexing/demultiplexing of seven DS2 into/from C-bit parity format according to ANSI T1.107, ITU-T G.704
- DS3 framing according to ANSI T1.107, T1.107a, ITU-T G.704
- Support of B3ZS encoded signals
- Provides access to the DS3 overhead bits and the DS3 stuffing bits via a serial clock and data interface (overhead interface)
- Insertion and Extraction of alarms according to ANSI T1.404 (remote alarm, AIS, far end receive failure)
- Supports HDLC (Path Maintenance Data Link) and bit oriented message mode (Far End Alarm and Control Channel) in C-bit parity mode. An integrated signalling controller provides 2x32 byte deep FIFO's for each direction of both channels.
- Detection of AIS and idle signal in presence of BER 10^{-3}
- Detection of excessive zeroes and LOS
- Alarm and performance monitoring with 16-bit counters for line code violations, excessive zeroes, parity error (P-bit), framing errors (F-bit errors with or without M-bit errors, far end block error (FEBE-bit) and CP-bit errors.
- Automatic insertion of severely errored frame and AIS defect indication

1.1.2 M12 Multiplexer and DS2 Framer

- Multiplexing/Demultiplexing of four asynchronous DS1 bit streams into/from M13 asynchronous format
- Multiplexing/Demultiplexing of 3 E1 signals into/from ITU G.747 compliant DS2 signal.
- DS2 line loopback detection/generation
- Framing according to ANSI T1.107, T1.107a or ITU-T G.747
- Insertion and extraction of X-bit
- Insertion and Extraction of alarms (remote alarm, AIS)
- Detection of AIS in presence of BER 10^{-3}
- Alarm and performance monitoring (framing bit errors, parity errors)
- Reframe time below 7ms (TR-TSY-000009) for DS2 format and below 1 ms for ITU G.747 format
- Bit Stuffing/Destuffing in M12 multiplex format or C-bit parity format
- Insertion of AIS in lieu of low speed tributaries

1.1.3 Bit Error Rate Tester

- User specified PRBS or Fixed Pattern with programmable length of 2 to 32 bits and programmable feedback tap (PRBS only)
- Optional Bit Inversion
- Two error insertion modes: Single or programmable bit rates

- Optional zero suppression
- 32-bit counters for errors and received bits
- Programmable bit intervals for receive measurements
- Framed DS3, framed/unframed DS2 or framed/unframed DS1/E1 error insertion
- Additional framing error counters for DS1/E1 error insertion

1.2 Logic Symbol

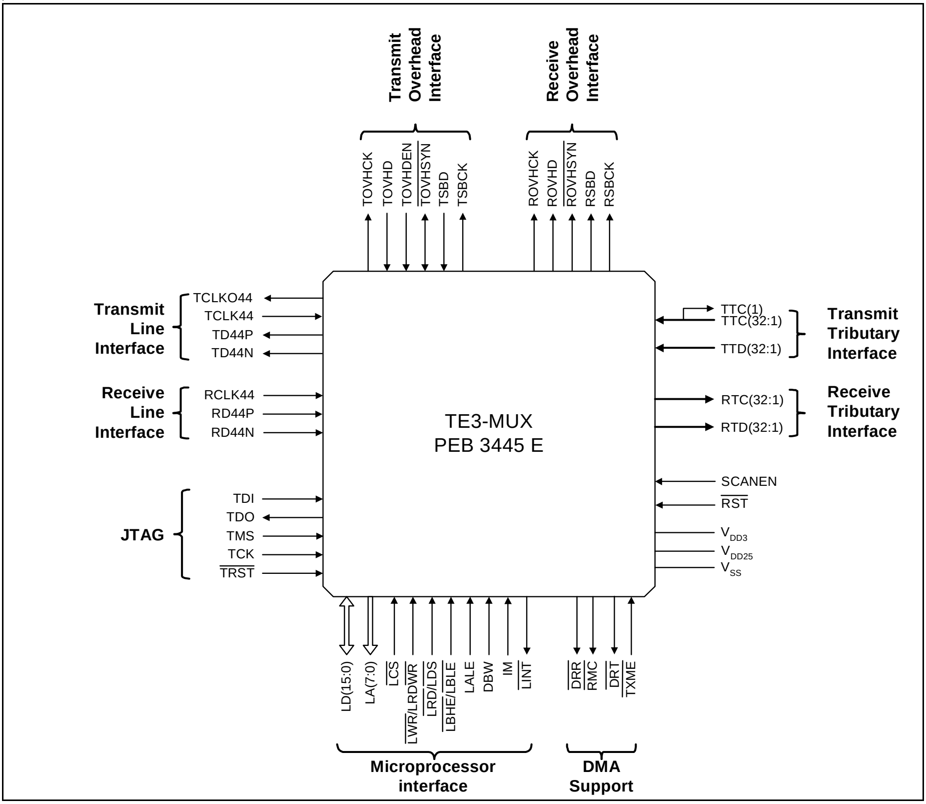


Figure 1 Logic Symbol

1.3 Typical Applications

Typical applications for the TE3-MUX support of channelized DS3 with serial line interfaces on the low speed side. The system partitioning due to ORB compliance may allow usage in following systems:

- Terminal Multiplexers with DS1/E1 and HDSL interfaces
- Add Drop Multiplexers (ADM) with DS1/E1 and HDSL interfaces
- Digital Cross Connect devices with DS1/E1 and HDSL interfaces
- DLC COT and RT
- Channelized DS3 applications

The TE3-MUX supports 32 low speed serial interfaces. These interfaces can be mapped to any of the 28 DS3 tributaries which provides for 4:28 protection.

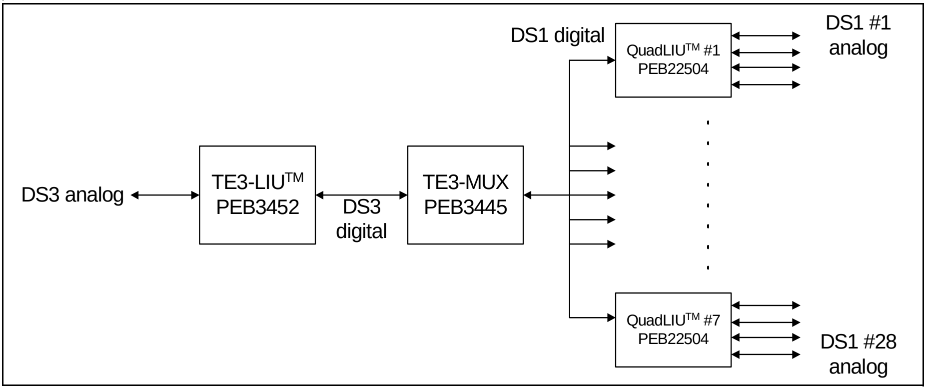


Figure 2 Typical DS3 Channelized Application

2 Pin Description

2.1 Pin Diagram

(top view)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Y	NC23	RTD(25)	VDD25	TTD(24)	TTD(23)	RTC(22)	TTC(22)	RTC(21)	RTC(20)	RTC(19)	TTD(19)	RTD(18)	RTD(17)	TTC(17)	TTD(16)	RTC(15)	RTD(14)	RTC(14)	RTC(13)	NC22
W	RTC(26)	TTD(26)	RTC(25)	RTD(24)	TTC(24)	TTC(23)	TTD(22)	RTD(21)	RTD(20)	RTD(19)	VDD25	RTC(18)	RTC(17)	RTD(16)	TTC(16)	TTD(15)	RTD(13)	TTD(13)	NC21	TTC(13)
V	RTD(27)	RTD(26)	TTC(26)	TTD(25)	RTC(24)	RTD(23)	RTD(22)	VDD25	TTC(21)	TTC(20)	TTC(19)	TTD(18)	TTD(17)	RTC(16)	RTD(15)	TTC(15)	TTC(14)	NC20	VDD25	TTD(12)
U	VDD25	TTC(27)	TTD(27)	VSS	TTC(25)	VDD33	RTC(23)	VSS	TTD(21)	TTD(20)	VDD33	TTC(18)	VSS	VDD25	VDD33	TTD(14)	VSS	RTD(12)	TTC(12)	RTC(11)
T	RTC(28)	TTD(28)	TTC(28)	RTC(27)													RTC(12)	RTD(11)	TTD(11)	RTC(10)
R	RTC(29)	TTD(29)	RTD(28)	VDD33						TE3-MUX PEB 3445 E							VDD33	TTC(11)	TTD(10)	VDD25
P	TTD(30)	TTC(30)	RTD(29)	TTC(29)													RTD(10)	TTC(10)	RTD(9)	RTC(9)
N	VDD25	RTD(30)	RTC(30)	VSS													VSS	TTD(9)	TTC(9)	RTD(8)
M	RTD(31)	RTC(31)	TTD(31)	TTC(31)					VSS	VSS	VSS	VSS					RTC(8)	TTD(8)	TTC(8)	RTD(7)
L	RTC(32)	TTC(32)	TTD(32)	VDD33					VSS	VSS	VSS	VSS					RTC(7)	TTD(7)	TTC(7)	VDD25
K	RTD(32)	$\overline{RMC}$	$\overline{TXME}$	VDD25					VSS	VSS	VSS	VSS					VDD33	RTC(6)	TTD(6)	RTD(6)
J	$\overline{LINT}$	$\overline{DRT}$	$\overline{DRR}$	IM					VSS	VSS	VSS	VSS					TTD(5)	RTC(5)	RTD(5)	TTC(6)
H	DBW	$\overline{LCS}$	$\overline{LRD}$ $\overline{LDS}$	VSS													VSS	RTC(4)	RTD(4)	TTC(5)
G	$\overline{LWR}$ $\overline{LRDWR}$	$\overline{LBHE}$ $\overline{LBLE}$	VDD25	LA(1)													TTD(3)	VDD25	TTC(4)	TTD(4)
F	LALE	NC19	LA(2)	VDD33													VDD33	TTC(3)	RTC(3)	RTD(3)
E	LA(0)	LA(3)	LA(4)	LA(7)													RTC(1)	TTD(2)	RTC(2)	RTD(2)
D	NC18	LA(5)	VDD25	VSS	$\overline{RST}$	VDD33	LD(4)	VSS	NC17	VDD33	NC16	VDD25	VSS	SCANEN	VDD33	TSBCK	VSS	TTD(1)	TTC(1)	TTC(2)
C	LA(6)	NC15	NC14	TCK	LD(1)	NC13	LD(7)	LD(9)	LD(12)	VDD25	TCLKO44	RCLK44	NC12	NC11	VDD25	TOVHDEN	ROVHCK	RSBCK	VDD25	RTD(1)
B	NC10	TDI	TMS	$\overline{TRST}$	LD(2)	LD(5)	VDD25	LD(10)	LD(13)	LD(15)	TCLK44	RD44N	NC9	NC8	NC7	TOVHCK	$\overline{TOVHSYN}$	ROVHD	$\overline{ROVHSYN}$	NC6
A	NC5	TDO	VDD25	LD(0)	LD(3)	LD(6)	LD(8)	LD(11)	LD(14)	TD44 TD44P	TD44N	RD44 RD44P	NC4	NC3	NC2	NC1	TOVHD	TSBD	RSBD	VSS

Figure 3 Pin Configuration

2.2 Pin Definitions and Functions

Signal Type Definitions:

I *Input* is a standard input- only signal.

O *Totem Pole Output* is a standard active driver.

I/O *I/O* is a bidirectional, tri-state input/output pin.

o/d *Open Drain* allows multiple devices to share a line as a wire-OR. A pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.

Signal Name Conventions:

NCn *No-connect Pin n*

Such pins are not bonded with the silicon. Although any potential at these pins will not impact the device it is recommended to leave them unconnected. No-connect pins might be used for additional functionality in later versions of the device. Leaving them unconnected will guarantee hardware compatibility to later device versions.

Reserved Reserved pins are for vendor specific use only and should be connected as recommended to guarantee normal operation.

Note: The signal type definition specifies the functional usage of a pin. This does not reflect necessarily the implementation of a pin, e.g. a pin defined of signal type 'Input' may be implemented with a bidirectional pad.

2.3 Local Microprocessor Interface

Pin No.	Symbol	Input (I) Output (O)	Function
D16	$\overline{\text{RST}}$	I	**Reset**
J17	IM	I	**Intel/Motorola** By connecting this pin to either V_{SS} or V_{DD3} the bus interface can be adapted to either Intel or Motorola environment. IM = V_{SS} selects Intel bus mode. IM = V_{DD3} selects Motorola bus mode.
H20	DBW	I	**Data Bus Width** DBW = V_{SS} selects 8-bit bus mode. DBW = V_{DD3} selects 16-bit bus mode.
E17, C20, D19, E18, E19, F18, G17, E20	LA(7:0)	I	**Address bus** These input address lines select one of the internal registers for read or write access.
B11, A12, B12, C12, A13, B13, C13, A14, C14, A15, B15, D14, A16, B16, C16, A17	LD(15:0)	I/O	**Data Bus** Bidirectional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: • 8-bit mode (DBW = 0): LD(7:0) are active. LD(15:8) are in high impedance and have to be connected to V_{DD3} or V_{SS}. • 16-bit mode (DBW = 1): LD(15:0) are active. In case of byte transfers, the active half of the bus is determined by LA(0) and $\overline{\text{LBHE}}$/$\overline{\text{LBLE}}$ and the selected bus interface mode (IM). The unused half is in high impedance. For detailed information, refer to **Chapter 5.1**.
H19	$\overline{\text{LCS}}$	I	**Chip Select** This active low signal selects the TE3-MUX for read/write operations.

Pin No.	Symbol	Input (I) Output (O)	Function
F20	LALE	I	**Address Latch Enable** The address information provided on address lines LA(7:0) is internally latched with the falling edge of LALE. This function allows the TE3-MUX to be directly connected to a multiplexed address/data bus. In this case, pins LA(7:0) must be externally connected to the data bus pins. When the TE3-MUX is operated in demultiplexed bus mode LALE shall be connected to V_{DD3}.
H18	$\overline{\text{LRD}}$ **or** $\overline{\text{LDS}}$	I I	**Read (Intel Bus Mode)** This active low signal selects a read transaction. **Data strobe (Motorola Bus Mode)** This active low signal indicates that valid data has to be placed on the data bus (read cycle) or that valid data has been placed on the data bus (write cycle).
G20	$\overline{\text{LWR}}$ **or** $\text{LRD}\overline{\text{WR}}$	I I	**Write Enable (Intel Bus Mode)** This active low signal selects a write cycle. **Read Write Signal (Motorola Bus Mode)** This input signal distinguishes write from read operations.
J20	$\overline{\text{LINT}}$	od	**Interrupt Request** This line indicates general interrupt requests of the TE3-MUX. The interrupt sources can be masked via registers.

Pin No.	Symbol	Input (I) Output (O)	Function
G19	$\overline{\text{LBHE}}$	I	**Byte High Enable (Intel Bus Mode)** If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte LD(15:8) of the data bus. In 8-bit bus interface mode this signal has no function and should be tied to V_{DD3}. Refer to **Chapter 5.1** for detailed information.
	or		
	$\overline{\text{LBLE}}$	I	**Byte Access (Motorola Bus Mode)** If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte LD(7:0) of the data bus. In 8-bit bus interface mode this signal has no function and should be tied to V_{DD3}. Refer to **Chapter 5.1** for detailed information.
J18	$\overline{\text{DRR}}$	O	**Data Request Receive** This signal indicates that the receive FIFO of the path maintenance data link channel contains a byte which has to be read by an external CPU.
K19	$\overline{\text{RMC}}$	O	**Receive Message Complete** This signal indicates that the DMA controller has to read the port status register PPSR in order to release the receive FIFO.
J19	$\overline{\text{DRT}}$	O	**Data Request Transmit** This signal indicates a request to store a new byte in the transmit FIFO of the path maintenance data link channel.
K18	$\overline{\text{TXME}}$	I	**Transmit Message End** This signal in combination with $\overline{\text{DRT}}$ indicates that the byte written to the transmit FIFO is the last byte of a HDLC message. $\overline{\text{TXME}}$ has to asserted together with the data signal LD.

2.4 Serial Interface

Pin No.	Symbol	Input (I) Output (O)	Function
DS3 Serial Interface Signals			
B10	TCLK44	I	**DS3 Transmit Clock Input** This clock provides a reference clock for the DS3 interface. The frequency of this clock is nominally 44.736 MHz.
C10	TCLKO44	O	**DS3 Transmit Clock Output** This output is a buffered version of the selected transmit clock. In normal operation mode TCLKO44 is a buffered version of TCLK44. In looped timed mode TCLKO44 is a buffered version of RCLK44.
A11	TD44 **or** TD44P	O O	**DS3 Transmit Data** This unipolar serial data output represents the DS3 signal. TD44 can be updated on the falling or the rising edge of TCLKO44. **DS3 Transmit Positive Pulse** In dual-rail mode this pin represents the positive pulse of the B3ZS encoded DS3 signal. TD44P can be updated on the falling edge or rising edge of TCLKO44.
A10	TD44N	O	**DS3 Transmit Negative Pulse** In dual-rail mode this pin represents the negative pulse of the B3ZS encoded DS3 signal. TD44N can be updated on the falling or rising edge of TCLKO44.
C9	RCLK44	I	**DS3 Receive Clock Input** This pin provides the receive clock input . The frequency of this clock is nominally 44.736 MHz.

Pin No.	Symbol	Input (I) Output (O)	Function
A9	RD44 **or** RD44P	I I	**DS3 Receive Data** This unipolar serial data input represents the DS3 signal. RD44 can be sampled on the falling or rising edge of RCLK44. **DS3 Receive Positive Pulse** In dual-rail mode this pin represents the positive pulse of the B3ZS encoded DS3 signal. RD44P can be sampled on the falling or rising edge of RCLK44.
B9	RD44N	I	**DS3 Receive Negative Pulse** In dual-rail mode this pin represents the negative pulse of the B3ZS encoded DS3 signal. RD44N can be sampled on the falling or rising edge of RCLK44.
DS3 Overhead Interface			
B5	TOVHCK	O	**Transmit Overhead Bit Clock** This signal provides the bit clock for the DS3 overhead bits of the outgoing DS3 frame. TOVHCK is nominally a 526 kHz clock.
A4	TOVHD	I	**Transmit Overhead Data** The overhead bits to be placed in the outgoing DS3 frame can be provided via TOVHD. Transmit overhead data is sampled on the rising edge of TOVHCK and those bits marked by TOVHDEN are inserted in the overhead bit positions of the outgoing DS3 frame.
C5	TOVHDEN	I	**Transmit Overhead Data Enable** The asserted TOVHDEN signal marks the bits to be inserted in the DS3 frame. TOVHDEN is sampled together with TOVHD on the rising edge of TOVHD.

Pin No.	Symbol	Input (I) Output (O)	Function
B4	TOVHSYN	I/O	**Transmit Overhead Synchronization** TOVHSYN provides the means to align TOVHD to the first M-frame of the DS3 signal or to align the first M-frame to TOVHSYN. • If operated in output mode TOVHSYN is asserted when the X-bit of the 1st subframe of the DS3 multiframe has to be inserted via TOVHD. TOVHSYN is updated on the falling edge of TOVHCK. • If operated in input mode TOVHSYN must be asserted when the X-bit of the 1st M-frame of the DS3 signal is output on TD44. TOVHSYN is sampled on the rising edge of TCLKO44.
D5	TSBCK	O	**Transmit Stuff Bit Clock** This signal provides the bit clock for DS3 transmit stuff bit data.
A3	TSBD	I	**Transmit Stuff Bit Data** Data provided via TSBD is optionally inserted in the stuffed bit positions of the DS3 signal. TSBD is sampled on the rising edge of TSBCK. This function is available in M13 asynchronous format only.
C4	ROVHCK	O	**Receive Overhead Bit Clock** This signal provides the bit clock for the received DS3 overhead bits. ROVHCK is nominally a 526 kHz clock.
B3	ROVHD	O	**Receive Overhead Data** ROVHD contains the extracted overhead bits of the DS3 frame. It is updated on the falling edge of ROVHCK.

Pin No.	Symbol	Input (I) Output (O)	Function
B2	$\overline{\text{ROVHSYN}}$	O	**Receive Overhead Synchronization** ROVHSYN is asserted while the X-bit of the 1st subframe of the DS3 signal is provided via ROVHD. It is updated on the falling edge of ROVHCK.
C3	RSBCK	O	**Receive Stuff Bit Clock** This signal provides the bit clock for DS3 receive stuff bit data.
A2	RSBD	O	**Receive Stuff Bit Data** ROVHD provides data which was inserted in the stuffed bit positions of the DS3 signal. RSBD is updated on the falling edge of RSBCK. This function is available in M13 asynchronous format only.
DS1/E1 Interface Signals, DS3 System Interface Signals			
L20, M19, N18, R20, T20, T17, W20, W18, V16, U14, Y15, Y13, Y12, Y11, W9, W8, V7, Y5, Y3, Y2, T4, U1, T1, P1, M4, L4, K3, J3, H3, F2, E2, E4	RTC(32:1) **or**	O	**DS1/E1 Receive Clock** This interface provides the receive clock for each of the low speed interfaces. Dependent on the tributary (DS1/E1) this clock has a nominal frequency of 1.544 MHz or 2.048 MHz. Due to the destuffing and demultiplexing process the receive clock contains gaps.
E4	RTC(1)	O	**DS3 Receive Clock** When the TE3-MUX is operated in unchannelized mode (DS3 framer mode) this interface provides the DS3 receive payload clock. It is derived from the receive clock RCLK44 and has clock gaps on the DS3 bit positions containing the overhead bits.

Pin No.	Symbol	Input (I) Output (O)	Function
K20, M20, N19, P18, R18, V20, V19, Y19, W17, V15, V14, W13, W12, W11, Y9, Y8, W7, V6, Y4, W4, U3, T3, P4, P2, N1, M1, K1, J2, H2, F1, E1, C1	RTD(32:1) **or**	O	**DS1/E1 Receive Data** The data stream of the DS1/E1 tributary is directly feeded to this output. RTD(x) is updated on the rising or falling edge of RTC(x).
C1	RTD(1)	O	**DS3 Receive Data** When the TE3-MUX is operated in unchannelized mode (DS3 framer mode) the payload of the incoming DS3 signal is output on RTD(1). RTD(1) is updated on the falling edge of RTC(1).

Pin No.	Symbol	Input (I) Output (O)	Function
L19, M17, P19 , P17, T18, U19, V18, U16, W16, W15, Y14, V12, V11, V10, U9, Y7, W6, V5, V4, W1, U2, R3, P3, N2, M2, L2, J1, H1, G2, F3, D1, D2	TTC(32:1) **or**	I	**DS1/E1 Transmit Clock** Transmit data is sampled on the rising edge of TTC(x) and inserted into the assigned DS1/E1 tributary of the DS3 signal. Dependent on the tributary type TTC(x) has a clock frequency of 1.544 MHz or 2.048 MHz.
D2	TTC(1)	O	**DS3 Transmit Clock** When the TE3-MUX is operated in unchannelized mode (DS3 framer mode) this interface provides the DS3 transmit payload clock. It is derived from the transmit clock TCLKO44 and has clock gaps on the DS3 bit positions containing the overhead bits.
L18, M18, P20, R19, T19, U18, W19, V17, Y17, Y16, W14, U12, U11, Y10, V9, V8, Y6, W5, U5, W3, V1, T2, R2, N3, M3, L3, K2, J4, G1, G4, E3, D3	TTD(32:1) **or**	I	**DS1/E1 Transmit Data** TTD(x) provides the DS1/E1 data stream to be inserted in the assigned DS1/E1 tributary of the DS3 signal. TTD(x) can be sampled on the rising or falling edge of TTC(x).
D3	TTD(1)	I	**DS3 Transmit Data** When the TE3-MUX is operated in unchannelized mode (DS3 framer mode) the payload of the outgoing DS3 signal needs to be provided via TTD(1). TTD(1) is sampled on the rising edge of TTC(1)

2.5 Test interface

Pin No.	Symbol	Input (I) Output (O)	Function
C17	TCK	I	**JTAG Test Clock** This pin is connected with an internal pull-up resistor.
B18	TMS	I	**JTAG Test Mode Select** This pin is connected with an internal pull-up resistor.
B19	TDI	I	**JTAG Test Data Input** This pin is connected with an internal pull-up resistor.
A19	TDO	O	**JTAG Test Data Output**
B17	$\overline{\text{TRST}}$	I	**JTAG Test Reset** This pin is connected with an internal pull-up resistor.
D7	SCANEN	I	**Full Scan Path Test Enable** When connected to V_{DD3} the TE3-MUX works in a vendor specific test mode. It is recommended to connect this pin to V_{SS}.

2.6 Power Supply, Reserved Pins and No-connect Pins

Pin No.	Symbol	Input (I) Output (O)	Function
A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	V_{SS}	I	**Ground** 0V All pins must have the same level.
A18, B14, C2, C6, C11, D9, D18, G3, G18, K17, L1, N20, R1, U7, U20, V13, V2, W10, Y18	V_{DD25}	I	**Supply Voltage** 2.5V ± 0.25V All pins must have the same level.
D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	V_{DD3}	I	**Supply Voltage** 3.3V ± 0.3V All pins must have the same level.
A5, A6, A7, A8, A20, B1, B6, B7, B8, B20, C7, C8, C15, C18, C19, D10, D12, D20, F19, V3, W2, Y1, Y20	NC1..23		**No-connect Pins 1..23** **It is recommended not to connect these pins.**

3 General Overview

3.1 Block Diagram

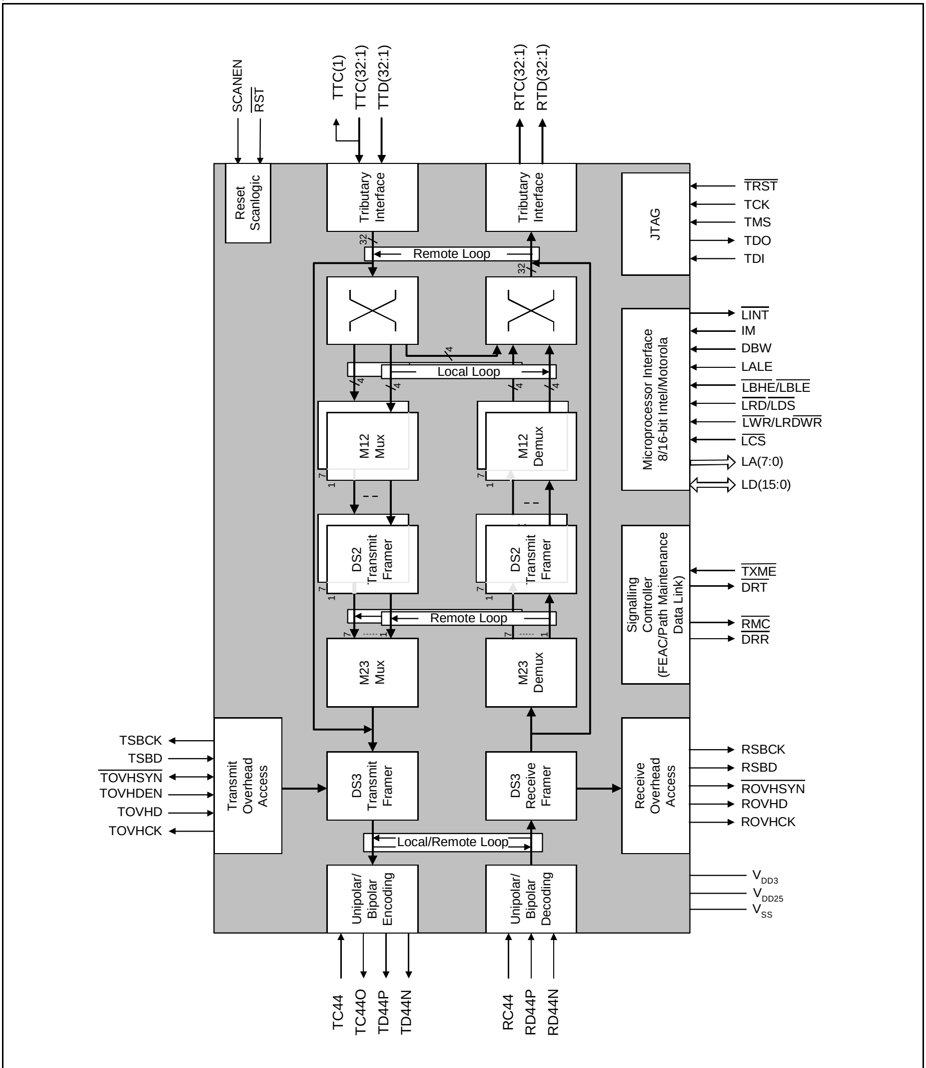


Figure 4 Block Diagram

3.2 Block Description

32 port line selector/tributary mapper

This structure allows the user to connect any DS1/E1 signal to a specified tributary of any M12 module. Therefore it maps 32 DS1/E1 signals into 28 DS1 time slots or 21 E1 time slots of the DS3 signal.

The four remaining spare ports can be used for microcontroller based protection, e.g. they can be operated in stand-by mode. They can also be used to interface an external test unit to test any DS1/E1.

M12 multiplexer/demultiplexer and DS2 framer

There are seven independent M12 multiplexer/demultiplexer modules in the chip. Each module can operate in either ANSI T1.107, ANSI T1.107a or ITU-T G.747 mode. In other words, a module can either map 4 DS1/J1 to one DS2 or 3 E1 to one DS2. When mapping DS1 signals into DS2 signals the M12 multiplexer performs inversion of the second and fourth DS1 signal. The DS2 framer performs frame and multi-frame alignment in receive direction and vice versa inserts the framing bits according to ANSI T1.107, ANSI T1.107a or ITU-T G.747. It detects loopback requests or enables insertion of loopback requests under microprocessor control.

M23 multiplexer/demultiplexer and DS3 framer

In channelized operating mode the M23 multiplexer/demultiplexer maps/demaps seven DS2 signals (generated by the M12 multiplexer/demultiplexer and DS2 framer) into/from M13 asynchronous format or C-bit parity format. In unchannelized mode one logical input stream is mapped into the information bits of the DS3 stream according to ANSI T1.107, ANSI T1.107a. The DS3 framer performs frame and multiframe alignment in receive direction and inserts the frame and multiframe alignment bits. Access to the DS3 overhead bits is provided by an additional overhead interface or via internal registers. An integrated signalling controller supports the Far End Alarm and Control Channel and the C-bit Parity Path Maintenance Data Link in DMA or interrupt mode. Performance monitoring provides counting of framing bit errors, parity errors, CP-bit errors, far end block errors, excessive zeros and line code violations. The framer detects loopback requests and allows insertion of loopbacks under microprocessor control.

BERT/PRBS generator/detector

The device has an integrated bit error rate tester. It is a programmable pseudo random bit sequence generator/monitor capable of supporting any smart jack loopback code from 2 to 32 bits in length and with a programmable feedback tap. The monitor can detect the incoming pattern and transmit the same pattern towards the far end of any low speed/ high speed port.

The test unit also has single/multi bit error insertion for testing and diagnostics and supports framed DS3, framed/unframed DS2 and framed/unframed DS1/E1 error insertion.

4 Functional Description

4.1 Remote and Local Loops

4.1.1 Local Loops

Local loops are provided on DS3 and DS1 level on a per port/tributary basis. In the local loop the outgoing bit stream of a port/tributary is mirrored to the receive data path. This allows to provide data via the low speed tributaries which is processed by the TE3-MUX in transmit direction, mirrored to the respective receiver and send back to the originating source. In order to ensure that the local port loop works even without incoming receive clock, each line looped uses the corresponding transmit clock.

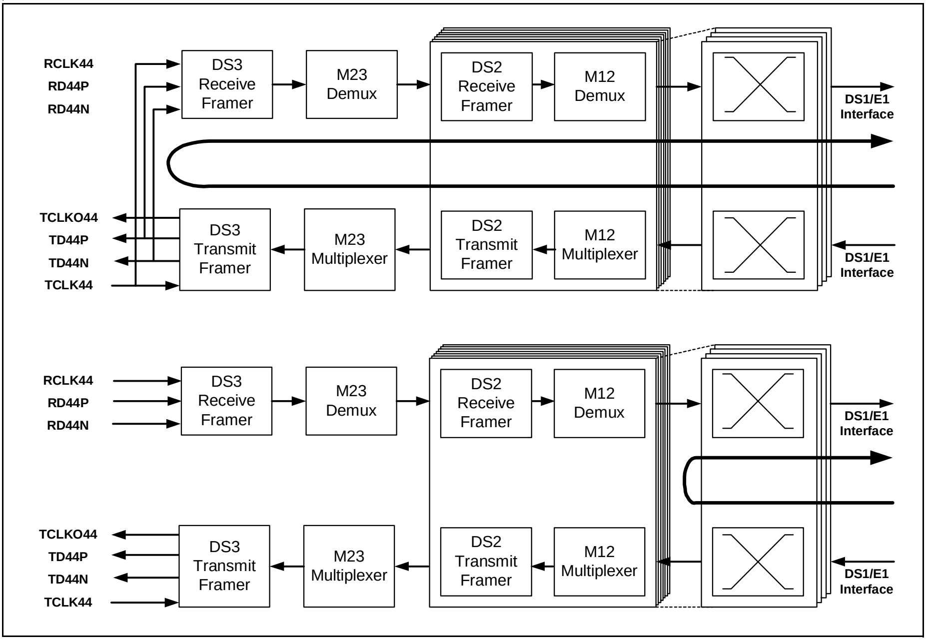


Figure 5 Local Loops

4.1.2 Remote Loops

The TE3-MUX supports remote loops in different stages of the M13 data path. In DS3 line loopback mode the incoming DS3 signal is mirrored and placed on the DS3 signal output. While operating in DS3 line loopback mode, the incoming receive clock RCLK44 is used to update outgoing transmit data. In DS2 line loopback mode one or more selectable DS2 signals are looped after the M23 stage the of the TE3-MUX. Finally the DS1/E1 line loopback mode mirrors one or more incoming lines. Tributary data provided via the low speed serial interface is replaced by the mirrored data stream.

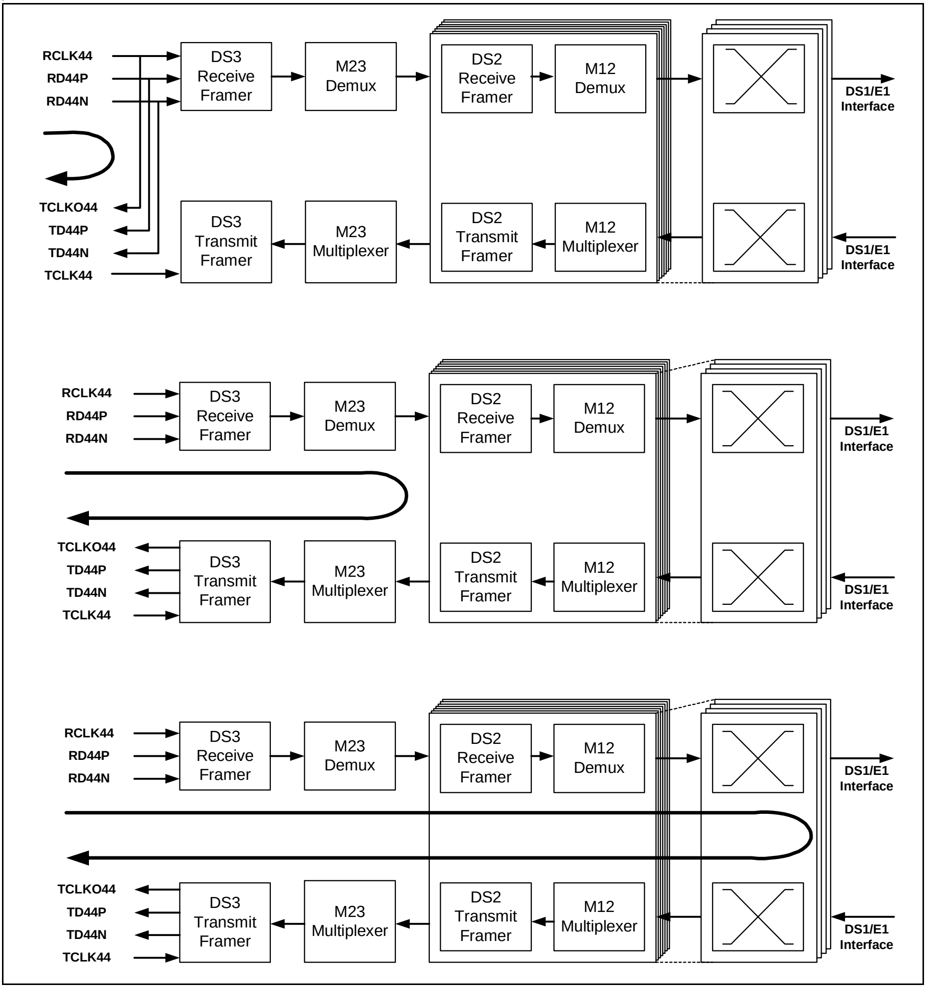


Figure 6 Remote Loops

4.2 B3ZS Code

In the B3ZS line code each block of three consecutive zeros is replaced by either of two replacements codes which are B0V and 00V, where B represents a pulse which applies to the bipolar rule (‘+1’ or ‘-1’) and V represents a bipolar violation (two consecutive ‘+1’ or ‘-1’ bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

The receive line decoder decodes the incoming B3ZS dual rail data signal and changes the replacement patterns to the original three-zeros pattern. Pattern sequences violating these rules are reported as bipolar violation errors.

4.3 Tributary Mapper

The tributary mapper connects any of the 28 low speed tributaries to any of the 32 DS1/ E1 low speed interfaces. A DS3 tributary consists of seven DS2 tributaries. Each DS2 tributaries consists of four DS1 tributaries when operated in DS1 format or three E1 tributaries when operated in ITU-T G.747 format. When a DS2 tributary is operated in ITU-T G.747 format the first three tributaries of a M12 multiplexer are accessible only. The fourth tributary of that M12 multiplexer is not used.

Mapping of the tributaries to the serial interfaces can be done independently in receive and transmit direction. After reset the tributary mapper maps the tributaries 1..28 to the port interfaces 1..28 and the spare lines 29..32 to the port interfaces 29..32.

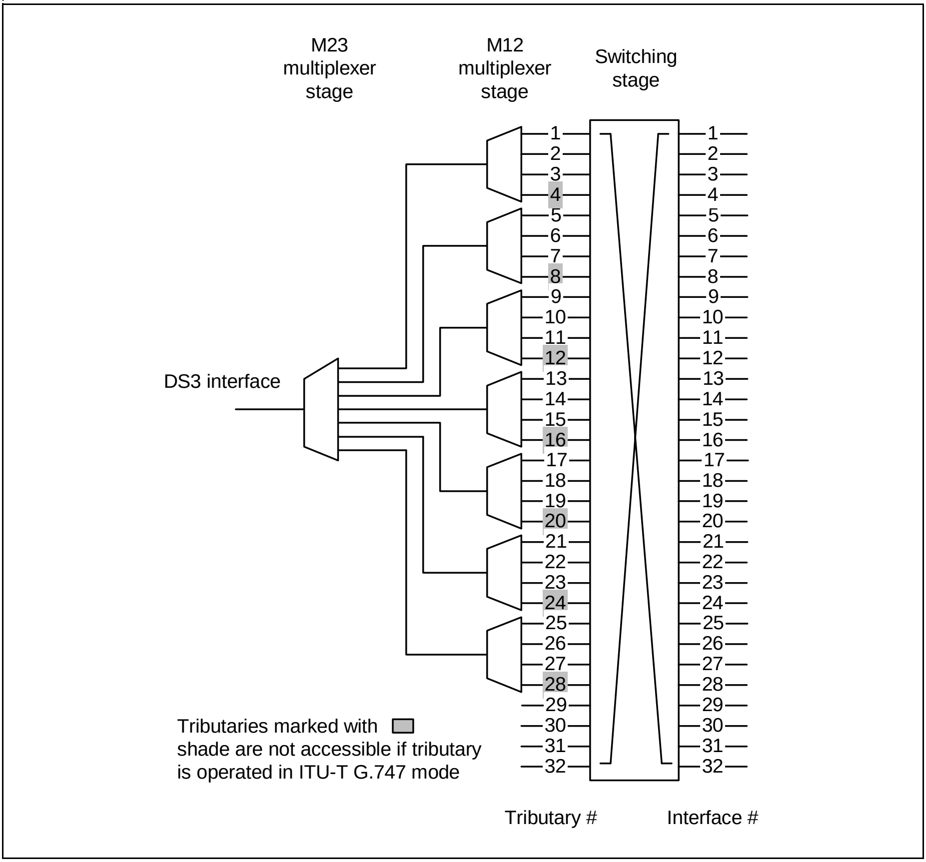


Figure 7 Tributary Mapper

Transmit Path

Figure 8 shows the DS1/E1 transmit part of the TE3-MUX. Each M12 multiplexer is assigned one input switch which maps 4 out of 32 input signals to the four inputs of the M12 multiplexer. The multiplexer as well as the switch to be programmed are selected via D2TSEL.GN. Then the four outputs of the switch are configured using register D2TTM0..3. Additionally each line can be switched into remote loop mode or one selected line can be fed via the integrated bit error rate tester.

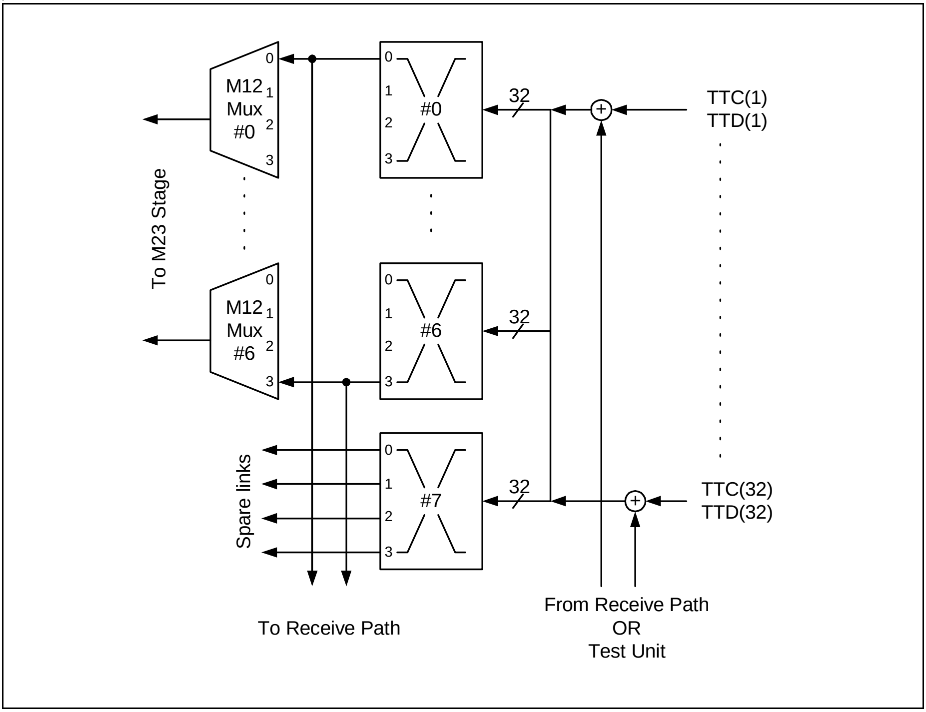


Figure 8 Tributary Mapper (Transmit Direction)

Receive Path

In receive direction a group of four consecutive output ports is assigned to one output switch (see **Figure 9**). This output switch maps any of the 28 M12 demultiplexer outputs or any of the four internal spare links to its four outputs. The output multiplexer to be programmed is selected via D2RSEL.GN. Then the four outputs of the switch are programmed via D2RTM0..3.

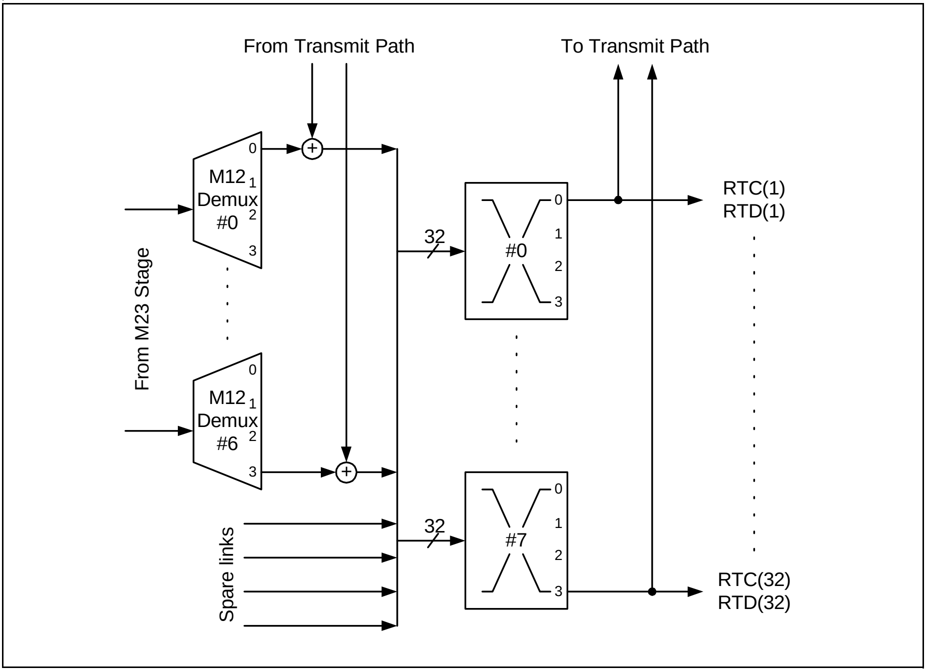


Figure 9 Tributary Mapper (Receive Direction)

4.4 M12 Multiplexer/Demultiplexer and DS2 framer

The M12 multiplexer and the DS2 framer can be operated in two modes:

- M12 multiplex format according to ANSI T1.107
- ITU-T G.747 format

4.4.1 M12 multiplex format

The framing structure of the M12 signal is shown in **Table 1**. A DS2 multiframe consists of four subframes. Each subframe combines 6 blocks with 49 bits each. The first bit of each block contains an overhead (OH) bit and 48 information bits. The 48 information bits are formed by bit-by-bit interleaving of the four DS1 signals or a total of 12 bits from each DS1 signal. The first bit is assigned to the 1st tributary DS1 signal, the second bit is assigned to the 2nd tributary DS1 signal and so on.

Table 1 M12 multiplex format

	Subframe	Block 1 through 6 of a subframe					
		1	2	3	4	5	6
DS2-Multiframe	1	M_0 [48]	C_{11} [48]	F_0 [48]	C_{12} [48]	C_{13} [48]	F_1 [48]
	2	M_1 [48]	C_{21} [48]	F_0 [48]	C_{22} [48]	C_{23} [48]	F_1 [48]
	3	M_1 [48]	C_{31} [48]	F_0 [48]	C_{32} [48]	C_{33} [48]	F_1 [48]
	4	X [48]	C_{41} [48]	F_0 [48]	C_{42} [48]	C_{43} [48]	F_1 [48]

M_0, M_1

M_0 and M_1 form the multiframe alignment signal. Each DS2 multiframe consists of three M-bits and they are located in bit 0 of subframe one through three. The multiframe alignment signal is ’011’.

X

This bit is the fourth bit of the multiframe alignment signal and can be set to either ’0’ or ’1’. It is accessible via an internal register.

F_0, F_1

F_0 and F_1 form the frame alignment pattern. Each DS2 multiframe consists of eight F-bits, two per subframe in block 3 and 6. F_0 and F_1 form the pattern ’01’. This pattern is repeated in every subframe.

$C_{11}..C_{43}$

The C-bits control the bit stuffing procedure of the multiplexed DS1 signals.

[48]

These bits represent a data block, which consists of 48 bits. [48] consists of four time slots of 12 bit and each time slot is assigned to one of four participating DS1 signals.

4.4.1.1 Synchronization Procedure

The integrated DS2 framer searches for the frame alignment pattern ’01’ and the multiframe alignment pattern in each of the seven DS2 frames which are contained in a DS3 signal. Frame alignment is declared, when the DS2 framer has found the basic frame alignment pattern (F-bit) and the multiframe alignment pattern (M-bit).

Loss of frame is declared, when 2 out of 4 or 3 out of 5 incorrect F-bits are found or when one or more incorrect M-bits are found in 3 out of 4 subframes.

4.4.1.2 Multiplexer/Demultiplexer

Demultiplexer

The demultiplexer extracts four DS1 signals out of each DS2 signal. If two out of three bits of C_{i1}, C_{i2}, C_{i3} are set to ’1’ the first information bit in the i^{th} subframe and the 6^{th} block which is assigned to the i^{th} DS1 signal is discarded.

The demultiplexer performs inversion of the 2^{nd} and 4^{th} tributary DS1 signal.

Multiplexer

The multiplexer combines four DS1 signals to form a DS2 signal. Stuffing bits are inserted and the C_{i1}-, C_{i2}-, C_{i3}-bits, which are assigned to the i^{th} DS1 signal, are set to ’1’ in case that not enough data is available.

The 2^{nd} and 4^{th} DS1 signal are automatically inverted in transmit direction.

4.4.1.3 Loopback Control

Detection

Loopback requests encoded in the C-bits of the DS2 signal are flagged when they are repeated for at least five DS2 multiframes. Loops must be initiated by an external microprocessor.

Generation

A loopback request, which is transmitted in lieu of the C-bits, can be placed in each DS2 signal.

4.4.1.4 Alarm Indication Signal

Detection

AIS is declared, when the AIS condition (the received DS2 data stream contains an all ‘1’ signal with less then 3/9 zeros within 3156 bits while the DS2 framer is out of frame) is present within a time interval that is determined by register D2RAP.

Generation

The alarm indication signal is an all ’1’ unframed signal and will be transmitted if enabled.

4.4.2 ITU-T G.747 format

The multiplexing frame structure is shown in **Table 2**.

Table 2 ITU-T G.747 format

	Set	Content	Bit
ITU-T G.747 Frame	I	Frame Alignment Signal 111010000	1 to 9
		Bits from tributaries	10 to 168
	II	Alarm indication to the remote multiplex equipment	1
		Parity Bit	2
		Reserved	3
		Bits from tributaries	4 to 168
	III	Justification control bits C_{j1}	1 to 3
		Bits from tributaries	4 to 168
	IV	Justification control bits C_{j2}	1 to 3
		Bits from tributaries	4 to 168
	V	Justification control bits C_{j3}	1 to 3
		Bits from tributaries available for justification	4 to 6
		Bits from tributaries	7 to 168

4.4.2.1 Synchronization Procedure

The integrated framer searches for the frame alignment pattern ’111010000’ in each of the seven DS2 frames which are contained in a DS3 signal. Frame alignment is declared, when the framer has found three consecutive correct frame alignment signals. If the frame alignment signal has been received incorrectly in one of the following frames after the receiver found the first correct frame alignment signal a new frame search is started.

Loss of frame is declared, when four consecutive frame alignment signals have been received incorrectly.

4.4.2.2 Multiplexer/Demultiplexer

Demultiplexer

The demultiplexer extracts three E1 signals from each 6.312 MHz signal. If two out of three bits of C_{j1}, C_{j2}, C_{j3} are set to ’1’ the available justification bit of the j^{th} E1 signal is discarded.

Multiplexer

The multiplexer combines three E1 signals to form a DS2 signal. Stuffing bits are inserted and the C_{j1}-, C_{j2}-, C_{ij}-bits, which are assigned to the j^{th} E1 signal, are set to '1' in case that not enough data is available.

4.4.2.3 Parity Bit

Detection

The receiver optionally calculates the parity of all tributary bits and compares this value with the received parity bit. Differences are counted in the parity error counter.

Generation

The parity bit is automatically calculated according to ITU-T G.747 or programmable to a fixed value under microprocessor control.

4.4.2.4 Remote Alarm Indication

Detection

Remote alarm is reported when bit 1 of "set II" (see **Table 2 "ITU-T G.747 format" on Page 43**) changes and when the change persists for at least three multiframes.

Generation

Remote alarm is transmitted in bit 2 of "set II" and can be inserted under microprocessor control.

4.4.2.5 Alarm Indication Signal

Detection

AIS is declared, when the AIS condition (the received DS2 data stream contains an all '1' signal with less then 5/9 zeros within two consecutive multiframes while the DS2 framer is out of frame) is present within a time interval that is determined by register D2RAP.

Generation

The alarm indication signal is an all '1' unframed signal and will be transmitted if enabled.

4.5 M23 multiplexer and DS3 framer

The DS3 path of the TE3-MUX can be operated in three modes:

- M23 multiplex format
- C-bit parity format with modified M23 multiplex operation
- Full payload rate format

4.5.1 M23 multiplex format

The framing structure of the M23 multiplex signal is shown in **Table 3**. Each DS3 multiframe consists of 7 subframes and each subframe of eight blocks. One block consists of 85 bits, where the first bit is the overhead (OH) bit and the remaining 84 bits contain the information bits. The 84 information bits are formed by bit-by-bit interleaving of the seven DS2 signals or a total of 12 bits from each DS2 signal. The first bit is assigned to the 1st tributary DS2 signal, the second bit is assigned to the 2nd tributary DS2 signal and so on.

Table 3 M23 multiplex format

	Sub-frame	**Block 1 through 8 of a subframe**							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
DS3-Multi-frame	1	X [84]	F_1 [84]	C_{11} [84]	F_0 [84]	C_{12} [84]	F_0 [84]	C_{13} [84]	F_1 [84]
	2	X [84]	F_1 [84]	C_{21} [84]	F_0 [84]	C_{22} [84]	F_0 [84]	C_{23} [84]	F_1 [84]
	3	P [84]	F_1 [84]	C_{31} [84]	F_0 [84]	C_{32} [84]	F_0 [84]	C_{33} [84]	F_1 [84]
	4	P [84]	F_1 [84]	C_{41} [84]	F_0 [84]	C_{42} [84]	F_0 [84]	C_{43} [84]	F_1 [84]
	5	M_0 [84]	F_1 [84]	C_{51} [84]	F_0 [84]	C_{52} [84]	F_0 [84]	C_{53} [84]	F_1 [84]
	6	M_1 [84]	F_1 [84]	C_{61} [84]	F_0 [84]	C_{62} [84]	F_0 [84]	C_{63} [84]	F_1 [84]
	7	M_0 [84]	F_1 [84]	C_{71} [84]	F_0 [84]	C_{72} [84]	F_0 [84]	C_{73} [84]	F_1 [84]

F_0, F_1

F_0 and F_1 form the frame alignment pattern. Each DS3 frame consists of 28 F-bits, four per subframe in block 2, 4, 6 and 8. F_0 and F_1 form the pattern ’1001’. This pattern is repeated in every subframe.

M_0, M_1

M_0 and M_1 form the multiframe alignment signal. The M-bit is contained in the OH-bit of the first block in subframe 5,6 and 7. The multiframe alignment signal is ’010’.

C_{11}..C_{73}

The C-bits control the bit stuffing procedure of the multiplexed DS2 signals.

P

The P-bits contain parity information and are calculated as even parity on all information bits of the previous DS3 frame. Both P-bits are identical.

X

The X-bits are used for transmission of asynchronous in-service messages. Both X-bits must be identical and may not change more than once every second.

[84]

These bits represent a data block, which consists of 84 bits.

[84] consists of seven time slots with 12 bits each and they are assigned to one of the seven participating DS2 signals.

4.5.1.1 Synchronization Procedure

The integrated DS3 framer searches for the frame alignment pattern ’1001’ and when found for the multiframe alignment pattern in each of the seven DS3 subframes. When the multiframe alignment pattern is found in three consecutive DS3 frames while frame alignment is still valid frame alignment is declared. The P-bits and the X-bits are ignored during synchronization.

Loss of frame is declared, when 3 out of 8 or 3 out of 16 incorrect F-bits are found or when one or more incorrect M-bits are found in 3 out of 4 subframes.

4.5.1.2 Multiplexer/Demultiplexer

Demultiplexer

The demultiplexer extracts seven DS2 signals from the incoming DS3 signal. If two or three bits out of C_{i1}, C_{i2}, C_{i3} are set to ’1’ the first bit following the F_1 bit in the i^{th} subframe which is assigned to the i^{th} DS2 signal is discarded.

Multiplexer

The multiplexer combines seven DS2 signals to form a DS3 signal. If not sufficient data is available for a DS2 signal, it automatically inserts a stuffing bit and sets the bits C_{i1}, C_{i2}, C_{i3} assigned to the i^{th} DS2 signal to ’1’.

4.5.1.3 X-bit

The TE3-MUX provides access to the X-bit via an internal register. Data written to the X-bit register is copied to an internal shadow register which is then locked for one second after each write access.

4.5.1.4 Alarm Indication Signal, Idle Signal

Detection

Alarm indication signal or Idle signal is declared, when the selected signal format was received with less than 8/15 bit errors (selectable via bit D3RAP.AIS) for at least one multiframe. The alarm indication signal can be selected as:

- Unframed all ’1’s
- Framed ’1010’ sequence, starting with a binary ’1’ after each OH-bit. C-bits are set to ‘0’. X-bit can be checked as ‘1’ or X-bit check can be disabled.

The idle signal is a

- Framed ’1100’ sequence, starting with a binary ’11’ after each OH-bit. C-bits are set to ‘0’ in M-subframe 3. X-bit can be checked as ‘1’ or X-bit check can be disabled.

Generation

The alarm indication signal or idle signal will be generated according to the selected signal format. X-bit needs to be set separately to ‘1’.

4.5.1.5 Loss of Signal

Detection

Loss of signal is declared, when the incoming data stream contains more than 175 consecutive ’0’s.

Recovery

Loss of signal is removed, when two or more ones are detected in the incoming data stream.

4.5.1.6 Performance Monitor

The following conditions are counted:

- Line code violations
- Excessive zeroes
- P-bit errors, CP-bit errors
- Framing bit errors
- Multiframe bit errors
- Far end block errors

4.5.2 C-bit parity format

The framing structure of the C-bit parity format is shown in **Table 3**. The assignment of the information bits [84] is identical to the M23 multiplex format, but the function of the C-bits is redefined for path maintenance and data link channels.

Table 4 C-bit parity format

	Sub-frame	Block 1 through 8 of a subframe															
		1		2		3		4		5		6		7		8	
DS3-Multi-frame	1	X	[84]	F_1	[84]	AIC	[84]	F_0	[84]	N_r	[84]	F_0	[84]	FEAC	[84]	F_1	[84]
	2	X	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]
	3	P	[84]	F_1	[84]	CP	[84]	F_0	[84]	CP	[84]	F_0	[84]	CP	[84]	F_1	[84]
	4	P	[84]	F_1	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_1	[84]
	5	M_0	[84]	F_1	[84]	DL_t	[84]	F_0	[84]	DL_t	[84]	F_0	[84]	DL_t	[84]	F_1	[84]
	6	M_1	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]
	7	M_0	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]

F_0, F_1

F_0 and F_1 form the frame alignment pattern. Each DS3 frame consists of 28 F-bits, four per subframe in block 2, 4, 6 and 8. F_0 and F_1 form the pattern ’1001’. This pattern is repeated in every subframe.

M_0, M_1

M_0 and M_1 form the multiframe alignment signal. The M-bit is contained in the OH-bit of the first block in subframe 5,6 and 7. The multiframe alignment signal is ’010’.

N_r

Reserved. Set to ’1’ in transmit direction.

AIC

Application Identification Channel.

DL_t

The terminal-to-terminal path maintenance data link uses the HDLC protocol. Access to the DL_t bits is possible via the integrated signalling controller.

DL

Reserved. Access to the DL-bits is possible via the spare bit registers.

FEAC

The alarm or status information of a far end terminal is sent back over the far end and control channel. This bit also contains DS3 or DS1 line loopback requests. Messages are sent in bit oriented mode. The far end alarm and control channel can be accessed via the internal signalling controller.

FEBE

The far end block error bits indicate a CP-bit parity error or a framing error. They are used to monitor the performance of a DS3 signal. Upon detection of either error in the incoming data stream the FEBE-bits are set automatically to ’000’ in the outgoing direction. Received far end block errors are counted.

CP

The CP-bits are used to carry path parity information and are set to the same value as the P-bits. In receive direction the CP-bits are checked against the calculated parity and differences are counted.

P

The P-bits contain parity information and are automatically calculated as even parity on all information bits of the previous DS3 frame.

X

The X-bits are used for transmission of asynchronous in-service messages. Both X-bits must be identical and may not change more than once every second. Access to the X-bits is possible via a register.

[84]

These bits represent a data block, which consists of 84 bits. [84] consists of seven time slots with 12 bits each and they are assigned to one of the seven participating DS2 signals.

4.5.2.1 Synchronization Procedure

The integrated DS3 framer searches for the frame alignment pattern ’1001’ and when found for the multiframe alignment pattern in each of the seven DS3 subframes. Frame alignment is declared when the multiframe alignment pattern is found in three consecutive DS3 frames. The P-bits and the X-bits are ignored during synchronization.

Loss of frame is declared, when 3 out of 8 or 3 out of 16 incorrect F-bits are found or when one or more incorrect M-bits are found in 3 out of 4 subframes.

4.5.2.2 Multiplexer/Demultiplexer

Demultiplexer

The demultiplexer extracts seven DS2 signals from the incoming DS3 signal. Since the DS3 signal is always stuffed the stuffing bit assigned to each DS2 signal is discarded.

Multiplexer

The multiplexer combines seven DS2 signals to form a DS3 signal and automatically inserts a stuffing bit for each DS2 signal.

4.5.2.3 X-bit

The TE3-MUX provides access to the X-bits via internal registers.

4.5.2.4 Far End Alarm and Control Channel

The Far End Alarm and Control Channel is handled via an internal BOM controller (see Chapter 4.6, Signalling Controller). The following byte format is assumed (the left most bit is received first):

$111111110xxxxxx0_B$

The far end alarm and control channel uses the FF_H byte for synchronization. Message words start and end with a ‘0’.

4.5.2.5 Loopback Control

Detection

Loopback requests are encoded in the messages of the far end alarm and control channel. The microprocessor has access to the messages as described in **Chapter 4.5.2.4**.

Generation

A loopback request can be initiated via the far end alarm and control channel.

4.5.2.6 Alarm Indication Signal, Idle Signal

Detection

Alarm indication signal or Idle signal is declared, when the selected signal format was received with less than 8/15 bit errors (selectable via bit D3RAP.AIS) for at least one multiframe. The alarm indication signal can be selected as:

- Unframed all ’1’s
- Framed ’1010’ sequence, starting with a binary ’1’ after each OH-bit. C-bits are set to ‘0’. X-bit can be checked as ‘1’ or X-bit check can be disabled.

The idle signal is a

- Framed ’1100’ sequence, starting with a binary ’11’ after each OH-bit. C-bits are set to ‘0’ in M-subframe 3. X-bit can be checked as ‘1’ or X-bit check can be disabled.

Generation

The alarm indication signal or idle signal will be generated according to the selected signal format. X-bit needs to be set separately to ‘1’.

4.5.2.7 Loss of Signal

Detection

Loss of signal is declared, when the incoming data stream contains more than 175 consecutive '0's.

Recovery

Loss of signal is removed, when two or more ones are detected in the incoming data stream.

4.5.2.8 Performance Monitor

The following conditions are counted:

- Line code violations
- Excessive zeroes
- P-bit errors, CP-bit errors
- Framing bit errors
- Multiframe bit errors
- Far end block errors

4.5.3 Full Payload Rate Format

In full payload rate format the DS3 multiframe structure can be selected according to M13 multiplex structure or C-bit parity structure. In either case the data blocks [84] carry one continuous data stream which is provided via the tributary interface one.

Multiplexing/Demultiplexing of the data block [84] does NOT apply.

4.6 Signalling Controller

The signalling controller provides access to the Far End Alarm and Control Channel and to the C-bit Parity Path Maintenance Data Link Channel.

Note: The C-bit parity path maintenance data link channel and the far end alarm and control channel support the same register structure. Registers assigned to the C-bit parity path maintenance data link channel start with a 'P', registers assigned to the Far End Alarm and Control Channel start with a 'F'.

4.6.1 C-bit Parity Path Maintenance Data Link Channel

The TE3-MUX performs the FLAG generation, CRC generation, zero bit-stuffing and programmable idle code generation. Buffering of transmit/receive data is done in 2x32 byte deep FIFOs.

The TE3-MUX additionally supports DMA support signals for operation of the C-bit parity path maintenance data link channel.

Shared Flags

The closing flag of a previously transmitted frame simultaneously becomes the opening flag of the following frame if there is one to be transmitted. The shared flag feature is enabled by setting PXCR.SF.

CRC check

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits PRCFG.CRCDIS and PXCFG.DISCRC.

- Receive Direction
  The received CRC checksum is always assumed to be in the last two bytes of a frame, immediately preceding a closing flag. If PRCFG.CRCDIS is set, the received CRC checksum will be written to the receive FIFO where it precedes the frame status byte. The received CRC checksum is additionally checked for correctness.
- Transmit Direction
  If PXCFG.DISCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (PXFF.XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a (closing) flag.

4.6.2 Far End Alarm And Control Channel (BOM)

The BOM controller supports the Far End Alarm and Control Channel according to ANSI T1.404.

Data Transmission

Transmission of BOM data is done by using a transparent mode of the signalling controller. After having written 1 to 32 bytes to the transmit FIFO, the command 'Start Transmission, Enable Automatic Repetition' via the handshake register FHND forces the TE3-MUX to repeatedly transmit the data stored in the transmit FIFO to the remote end.

The cyclic transmission continues until a reset command (FHND.XRES) is issued or until the command 'Stop Transmission, Disable Automatic Repetition' is written to the handshake register FHND. Afterwards an all '1' pattern is transmitted.

The transmitter does not insert FF_H itself. Data stored in the transmit FIFO has to include the FF_H byte as well and has to follow the following byte format:

$111111110xxxxxx0_B$

Data Reception BOM Regular Mode

The following byte format is assumed (the left most bit is received first):

$111111110xxxxxx0_B$

The signalling controller uses the first two FF_H bytes for synchronization, the next byte is stored in the receive FIFO (first bit received: LSB) if it starts and ends with a '0', that is the receiver automatically removes the FF_H synchronization byte. Bytes starting or ending with a '1' are not stored. If the message word $7E_H$ (similar to HDLC flag) is received or when more than four times FF_H is received byte sampling is stopped and a 'Receive Message End' interrupt vector is generated. Byte sampling starts again when the synchronization byte FF_H is received two times.

After detecting 32 bits of '1's, byte sampling is stopped, the receive status byte marking the end of a BOM frame is stored in the receive FIFO and a 'BOM Idle' interrupt is generated. The same interrupt is generated when not eight consecutive ones where received in 32 bits.

Data Reception BOM Filter Mode

In BOM filter mode the received BOM data is validated and then filtered. If same valid BOM pattern is received for 7 out of 10 patterns, then BOM data is written to the receive FIFO along with the status byte indicating that filtered BOM data was received.

Filtered BOM mode will be exited if one of the following conditions occurs:

- 4 valid BOM patterns are consecutively received but none of these equals the BOM data received earlier.
- 4 times idle pattern is received.

4.6.3 Signalling controller FIFO operation

Access to the FIFO's of the signalling controllers is handled via registers. The corresponding FIFO's for receive and transmit direction of the C-bit parity Path

Maintenance data link channel are named PRFF and PXFF respectively. The FIFOs of the Far End Alarm and Control Channel are named FRFF and FXFF. FIFO status and commands are exchanged using the port status registers PPSR (FPSR) and the handshake register PHND (FHND). The C-bit parity Path Maintenance Data Link Channel supports an external DMA controller via the signals $\overline{\text{DRR}}$, $\overline{\text{RME}}$ or $\overline{\text{DRT}}$ and $\overline{\text{TXME}}$. Additional interrupts inform the system software about protocol status and FIFO status.

4.6.3.1 Interrupt Driven Microprocessor Operation

Receive Direction

In receive direction there are different interrupt indications associated with the reception of data:

- A 'Receive Pool Full' (RPF) interrupt indicates that a data block can be read from the receive FIFO and the received message is not yet complete. It is generated, when the amount of data bytes has reached the programmed threshold.
- A 'Receive Message End' (RME) or 'Receive Message Idle' interrupt indicates that the reception of one message is completed. After this interrupt system software has to read the corresponding port status register in order to get the number of bytes stored in the receive FIFO. This number includes the status byte which is written into the receive FIFO as the last byte after the received frame. The status byte includes information about the CRC result, valid frame indication, abort sequence or data overflow. The format of the status byte is shown in the table below:

7 6	5	4 0
SMODE(1:0)	0	STAT(4:0)

SMODE Receiver Status Mode

STAT Receive FIFO Status
This bit field reports the status of the data stored in the receive FIFO. The content of the status byte is dependent on the channel.

	C-bit Parity Path Maintenance Data Link	**Far End Alarm and Control Channel**
00000_B	Valid HDLC Frame	BOM Filtered data declared
00001_B	Receive Data Overflow	BOM Data Available
00010_B	Receive Abort	Flag $7E_H$ Received

	C-bit Parity Path Maintenance Data Link	Far End Alarm and Control Channel
00011_B	Not Octet	BOM Filtered Data Undeclared
00100_B	CRC Error	BOM Idle
00101_B	Channel Off	n/a

Note: For a description of the status information refer to ***Page 165*** *and* ***Page 177****.*

After the received data has been read from the FIFO, the receive FIFO has to be released by the CPU with the command 'Receive Message Complete' (FHND.RMC, PHND.RMC). The CPU has to process a 'Receive Pool Full' interrupt and issue the 'Receive Message Complete' command before the second page of the FIFO becomes full. Otherwise a 'Receive Data Overflow' condition will occur. This time is dependent on the threshold programmed (smaller threshold results in shorter time).

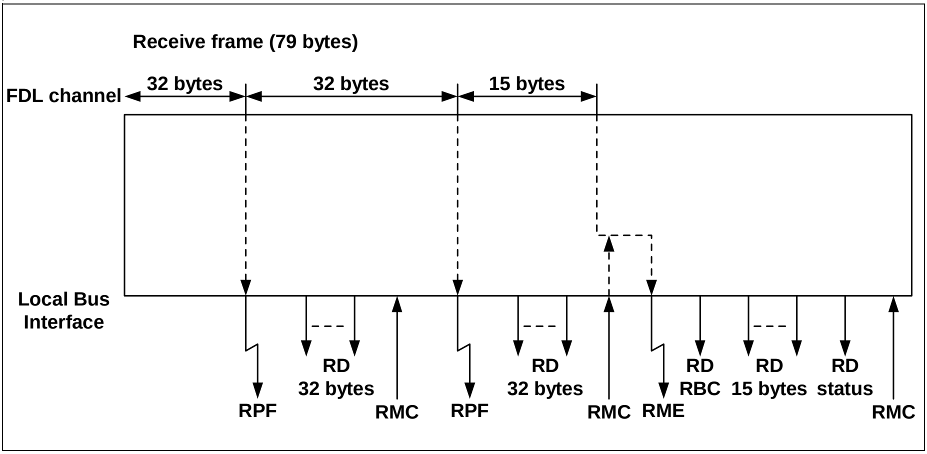


Figure 10 Interrupt Driven Reception Sequence Example (32-byte Receive Threshold)

Transmit Direction

In the transmit direction after checking the transmit FIFO status by polling the transmit FIFO write enable bit (FPSR.XFW, PPSR.XFW) or after a 'Transmit Pool Ready' interrupt, up to 32 bytes may be written to the transmit FIFO (bit field FXFF.XFIFO, PXFF.XFIFO) by the CPU. Transmission of a frame can be started by issuing a 'Start Transmission' command (see register FHND on **Page 167** for Far End Alarm and Control Channel and register PHND on **Page 179** for C-bit parity Path Maintenance Data

Link). If the transmit command does not include a 'Transmit Message End' indication (FHND.XME, PHND.XME), the signalling controller will repeatedly request for the next data block by means of a XPR interrupt as soon as the transmit FIFO becomes free. This process will be repeated until the local CPU writes the last bytes to the transmit FIFO. End of transmission is by issuing the command 'Stop Transmission'. In case of C-bit Parity Path Maintenance Data Link channel CRC and closing flag sequence is appended after the last byte was sent.

C-bit parity path maintenance data link channel only: Consecutive frames may share a flag (enabled via bit PXCR.SF) or may be transmitted as back-to-back frames, if service of transmit FIFO is quick enough. In case that no more data is available in the transmit FIFO prior to the arrival of PHND.XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified via a 'Transmit Data Underrun' interrupt (XDU). The frame may also be aborted per software by setting the XAB bit in the handshake register PHND.

In case of messages longer than 32 bytes the transmit FIFO has to be filled up in blocks of 32 bytes. The last block of the message can be smaller than 32 bytes. If the transmit FIFO is not filled up in time a transmit abort (C-bit parity Path Maintenance Data Link) is inserted or gaps between BOM messages (Far End Alarm and Control Channel) may occur.

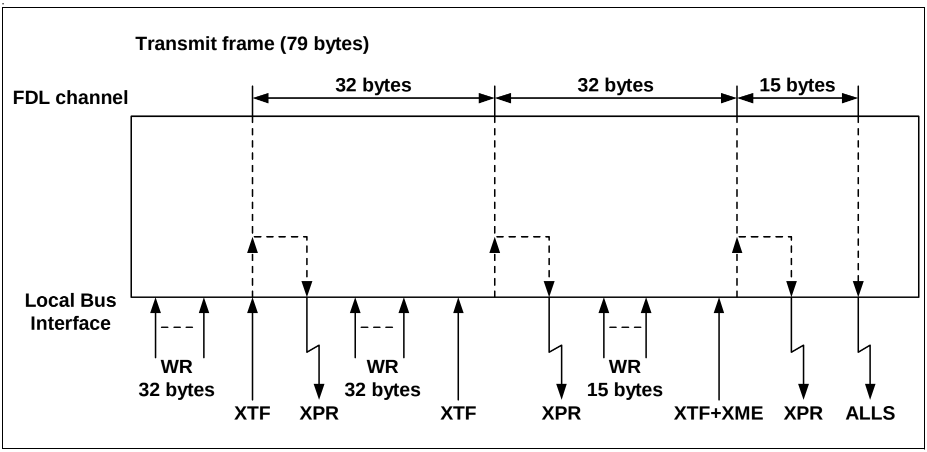


Figure 11 Interrupt Driven Transmit Sequence Example

Note: Data bus is 16 bit wide. In the given example writing 32 bytes requires 16 write accesses. Writing 15 bytes requires 8 accesses.

4.6.3.2 DMA Supported Data Transmission

The C-bit parity Path Maintenance Data Link Channel supports additionally DMA signals to optimize data transfers to and from the internal FIFOs. Request signals for transmit and receive direction indicate free respectively available channel data. The RME (Receive Message End) signal and the TXME (Transmit Message Complete) signal indicates the end of a message.

Receive Direction

Data reception can be initiated by enabling the HDLC controller and setting the DMA functionality in register PRCFG. As soon as there is a data byte in the receiver the TE3-MUX autonomously requests a data transfer by activating the DRR line. This indicates to the DMA controller to read a data byte out of the receive FIFO PRFF. This sequence continuous until the last byte is transferred via the DMA controller. The last byte in the receive FIFO is always the status byte which contains the frame status information, e.g. 'Receive Abort' or 'CRC error'. When the last byte of a message was read out of the receive FIFO the signal RME is asserted to indicate that the port status register PPSR needs to be read in order to free the internal buffer.

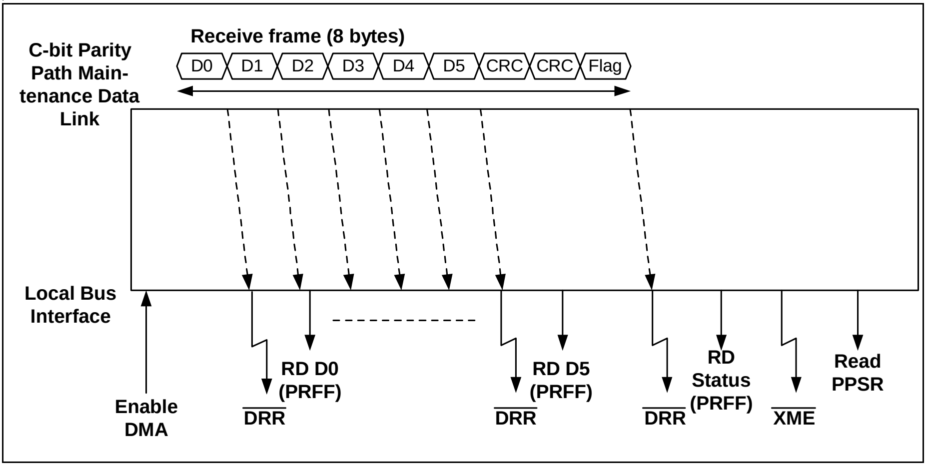


Figure 12 DMA Supported Receive Sequence

Transmit Direction

Prior to data transmission the HDLC controller has to be enabled and the DMA support must be activated via the register PXCFG. As long as there is free space in the transmit FIFO the signalling controller requests data by asserting the DRT line which indicates that the external DMA controller can write data to the transmit FIFO. While writing the last byte of a message the external DMA must assert the signal TXME, that is the signal must be asserted while the data byte is on the microprocessor bus. Then the next data transfer is the first byte of a new message. The TE3-MUX automatically appends the CRC and the flags between messages.

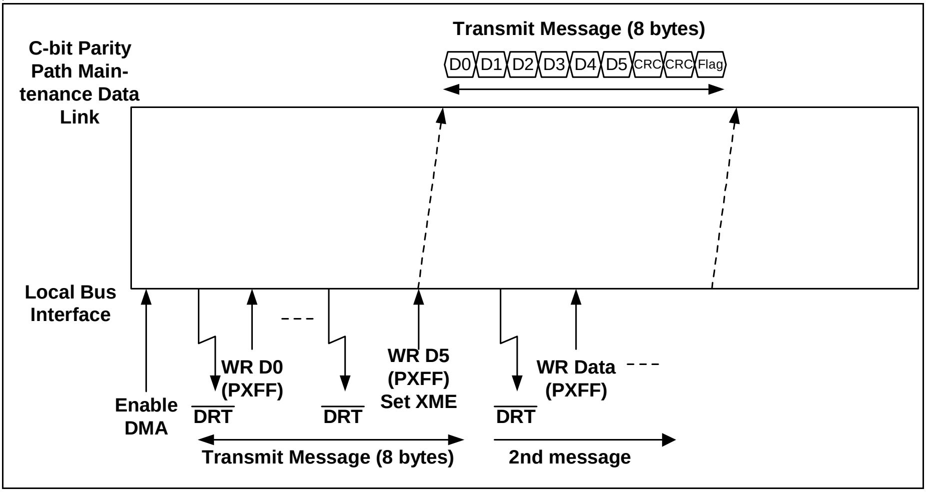


Figure 13 DMA supported Transmit Sequence

4.7 Test Unit

The test unit of the TE3-MUX incorporates a test pattern generator and a test pattern synchronizer which can be attached to different test points as shown in **Figure 14**. Controlled by a small set of registers it can generate and synchronize to polynomial pseudorandom test patterns or repetitive fixed length test patterns.

Test patterns can be generated in the following modes:

- Framed DS3
- Unframed DS2
- Framed DS2
- Unframed DS1/E1
- Framed DS1/E1

Note: When the test unit is operated in framed DS1 mode, the bit error rate must be below 1/100.

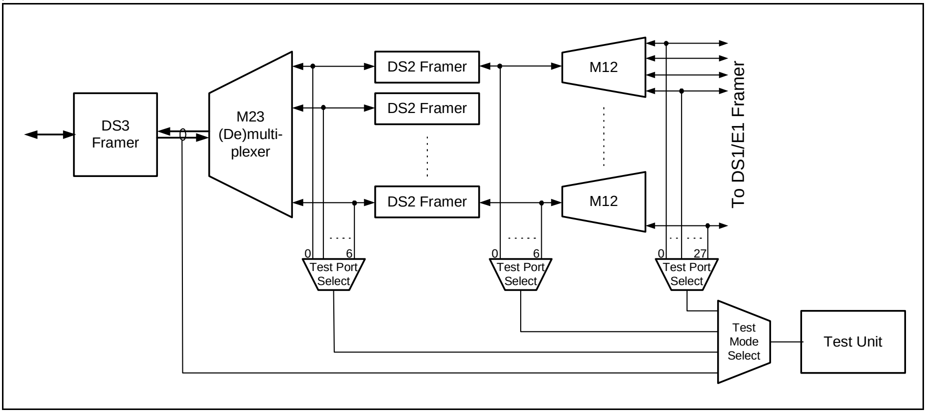


Figure 14 Test Unit Access Points

In pseudorandom test mode the receiver tries to achieve synchronization to a test pattern which satisfies the programmed receiver polynomial. In fixed pattern mode it synchronizes to a repetitive pattern with a programmable length. An all ’1’ pattern or an all ’0’ pattern, which satisfies this condition, is flagged. Measurement intervals as well as receiver synchronization can be controlled by the user. When a test is finished an interrupt is generated and the bit count and the bit error count are readable.

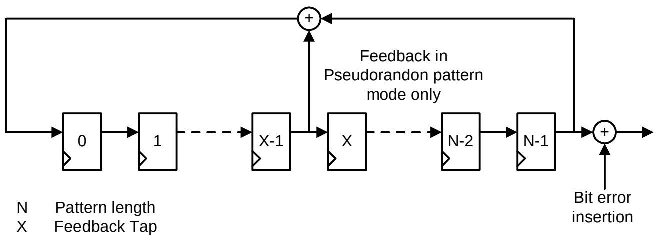


Figure 15 Pattern Generator

Bit Error Insertion

The test unit provides the optional capability to insert bit errors in the range of 10^{-7} (1 error in 10.000.000 bits) up to 10^{-1} bit errors (1 error in 10 bits).

External Bit Error Test

Four of the 32 low speed tributary interfaces can be used for protection switching or to connect an external bit error rate tester to one of the 28 DS1/21E1 tributaries.

4.8 Interrupt Interface

Special events in the TE3-MUX are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull, active low/high), which requests the CPU to read status information or to transfer to/from the TE3-MUX.

Since only one interrupt output is provided the cause of an interrupt must be determined by the external CPU by reading the interrupt status register D3RINTV which indicates the interrupt reason and the interrupt source. Status changes of the test unit, the DS2 framer or the DS3 framer require a second read of register D3RINTC while loopback code changes of the DS2 receiver require a read of register D3RINTL.

The interrupt pin is deactivated when register D3RINTV was read and no further interrupts are pending. As long as further interrupts are pending the interrupt pin remains asserted and the process as described above needs to be repeated until all pending interrupts are resolved.

5 Interface Description

5.1 Local Microprocessor Interface

The Local Microprocessor Interface is a demultiplexed/multiplexed switchable Intel or Motorola style interface with an 8- or 16-bit bus interface.

5.1.1 Intel Mode

The Intel mode supports a 16- or 8-bit bus interface with demultiplexed or multiplexed bus operation. For multiplexed bus operation LA(7:0) must be connected to LD(7:0). The TE3-MUX uses the port pins LA(7:0) for the 8 bit address and the port pins LD(15:0) for 16/8 bit data or LD(7:0) in 8-bit interface mode. A read/write access is initiated by placing an address on the address bus and then asserting $\overline{\text{LCS}}$. The external processor then activates the respective command signal ($\overline{\text{LRD}}$, $\overline{\text{LWR}}$). Data is driven onto the data bus either by the TE3-MUX (for read cycles) or by the external processor (for write cycles). After a period of time, which is determined by the access time to the internal registers valid data is placed on the bus.

In multiplexed bus operation a falling edge of LALE indicates a valid address on LA(7:0) and the corresponding byte enable on $\overline{\text{LBHE}}$. If operated in demultiplexed operated LALE must be connected to V_{DD3}.

Note: $\overline{\text{LCS}}$ need not to be deasserted between two subsequent cycles to the same device.

Read cycles

Input data can be latched and the command signal can be deactivated now. This causes the TE3-MUX to remove its data from the data bus which is then tri-stated again.

Write cycles

The command signal can be deactivated now. If a subsequent bus cycle is required, the external processor can place the respective address on the address bus.

Table 5 Data Bus Access 16-bit Intel Mode

$\overline{\text{LBHE}}$	LA(0)	Register Access	Data Pins Used
0	0	Word access (16 bit)	LD(15:0)
0	1	Byte access (8 bit), odd address	LD(15:8)
1	0	Byte access (8 bit), even address	LD(7:0)
1	1	No data transfer	-

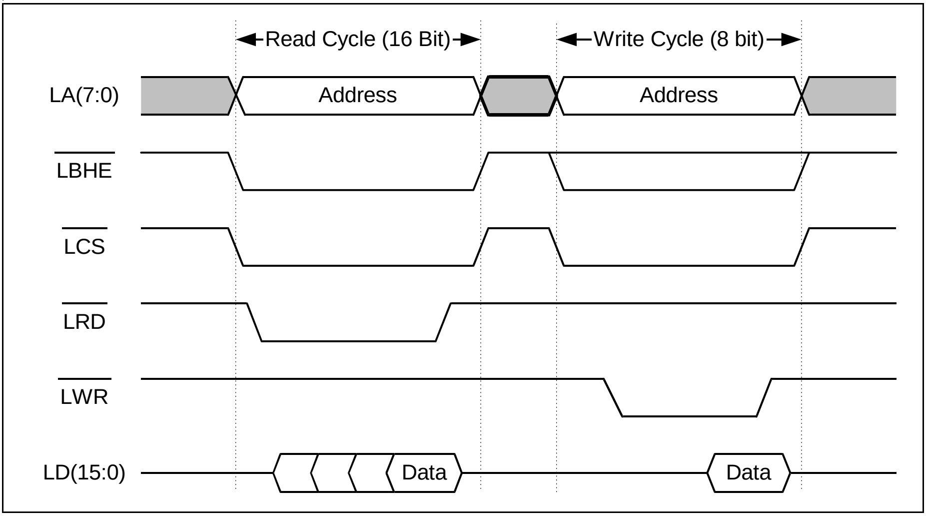


Figure 16 Intel Bus Mode (Demultiplexed Bus Operation)

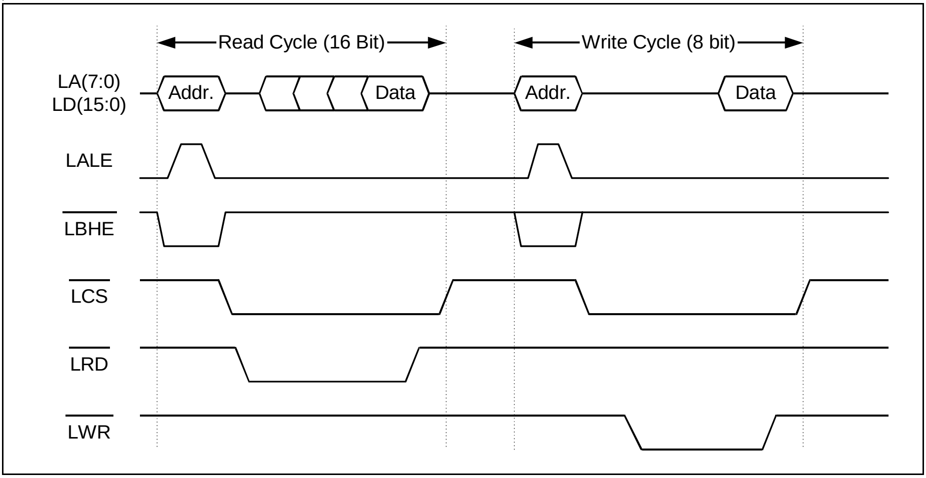


Figure 17 Intel Bus Mode (Multiplexed Bus Operation)

5.1.2 Motorola Mode

The Motorola bus mode supports a 16- or 8-bit bus interface with demultiplexed or multiplexed bus operation. For multiplexed bus operation LA(7:0) must be connected to LD(7:0). The TE3-MUX uses the port pins LA(7:0) for the 8 bit address and the port pins LD(15:0) for 16/8 bit data or LD(7:0) in 8-bit interface mode. A read/write access is initiated by placing an address on the address bus and asserting LCS together with the command signal LRDWR (see **"Motorola Bus Mode (Demultiplexed Bus Operation)" on Page 66**). The data cycle begins when the signal LDS is asserted. Data is driven onto the data bus either by the TE3-MUX (for read cycles) or by the external processor (for write cycles). After a period of time, which is determined by the access time to the internal registers valid data is placed on the bus.

In multiplexed bus operation a falling edge of LALE indicates a valid address on LA(7:0)and the corresponding byte enable signal on LBLE. If operated in demultiplexed bus mode LALE must be connected to V_{DD3}.

Note: LCS need not to be deasserted between two subsequent cycles to the same device.

Read cycles

Input data can be latched and the data strobe signal can be deactivated now. This causes the TE3-MUX to remove its data from the data bus which is then tri-stated again.

Write cycles

The data strobe signal can be deactivated now. If a subsequent bus cycle is required, the external processor can place the respective address on the address bus.

Table 6 Data Bus Access 16-bit Motorola Mode

LBLE	LA(0)	Register Access	Data Pins Used
0	0	Word access (16 bit)	LD(15:0)
0	1	Byte access (8 bit), even address	LD(15:8)
1	0	Byte access (8 bit), odd address	LD(7:0)
1	1	no data transfer	-

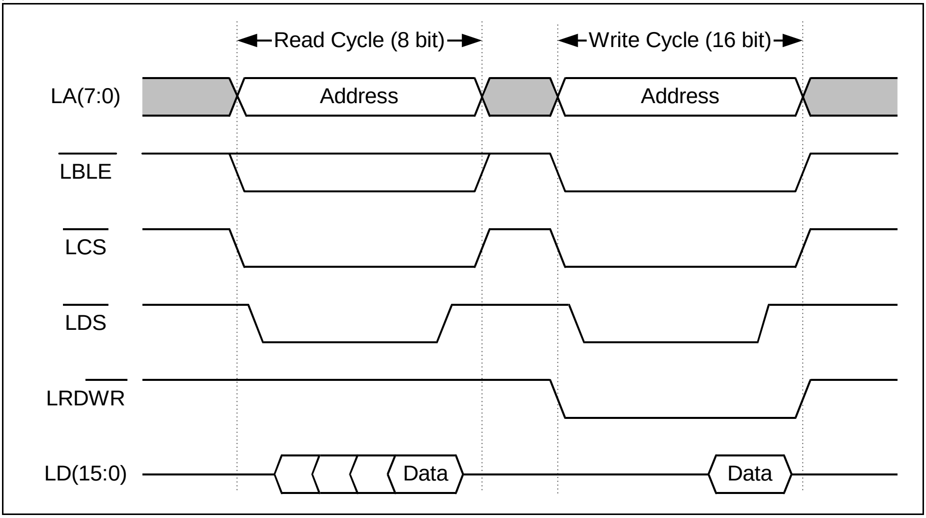


Figure 18 Motorola Bus Mode (Demultiplexed Bus Operation)

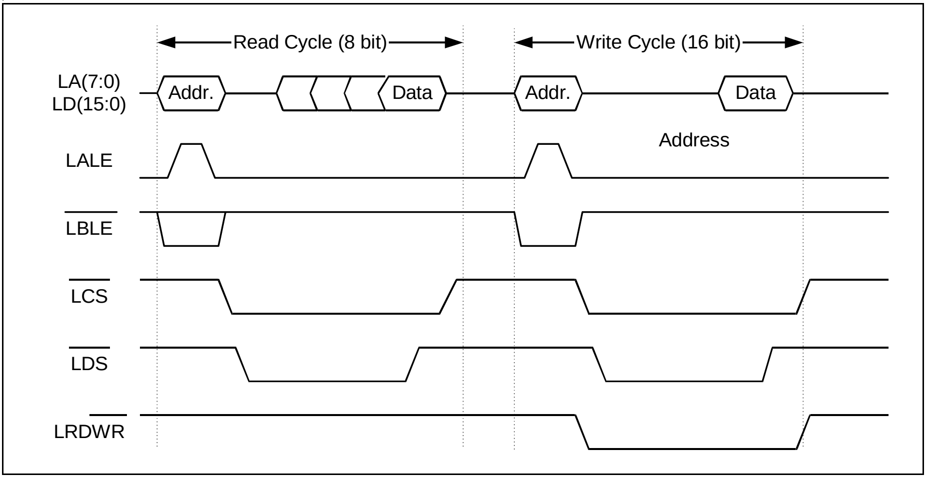


Figure 19 Motorola Bus Mode (Multiplexed Bus Operation)

5.2 Serial Interface Timing

5.2.1 DS3 Interface

The DS3 interface of the TE3-MUX consists of one receive port and one transmit port. The receive port provides a clock input (RCLK44) and one (RD44) or two data inputs (RD44P, RD44N) for unipolar or dual-rail input signals. Receive data can be sampled on the rising or falling edge of the receive clock. In transmit direction the port interface consists of two clock signals, the transmit clock input TCLK44 and a clock output signal TCLKO44. The data signals consists of one (TD44) or two data outputs (TD44P, TD44N) for unipolar or dual-rail output signals. The transmit port can be clocked by the receive clock RCLK44 or by the transmit clock TCLK44. The selected clock is provided as an output on TCLKO44. Transmit data is updated on the rising or falling edge of TCLKO44.

The TE3-MUX provides two additional serial interfaces, one for DS3 overhead bit access and one for DS3 stuff bit access (M13 asynchronous format only).

The overhead access is provided via an overhead clock signal (ROVHCK, TOVHCK), an overhead data signal (ROVHD, TOVHD) and an synchronization signal (ROVHSYN, TOVHSYN) which marks the X overhead bit of the first subframe of a DS3 signal. In transmit direction the overhead enable signal (TOVHDEN) marks those bits which shall be inserted in the overhead bits of the DS3 signal. Overhead signals are updated on the falling edge or sampled on the rising edge of the corresponding overhead clock. See **Figure 20** and **Figure 21** for details.

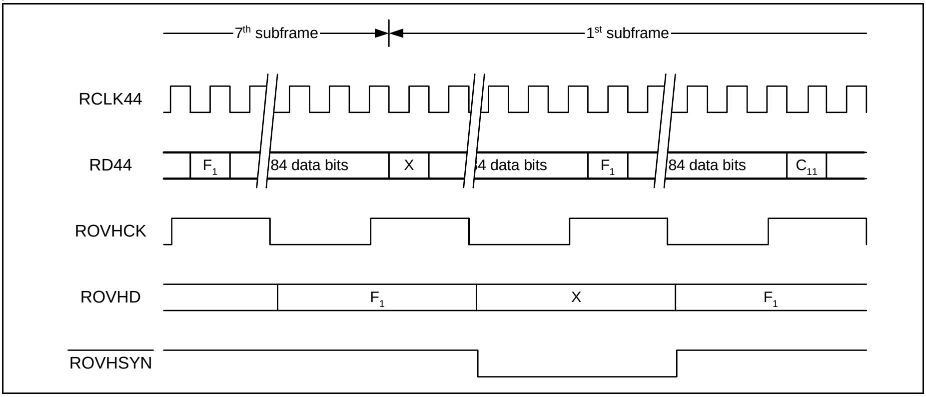


Figure 20 Receive Overhead Access

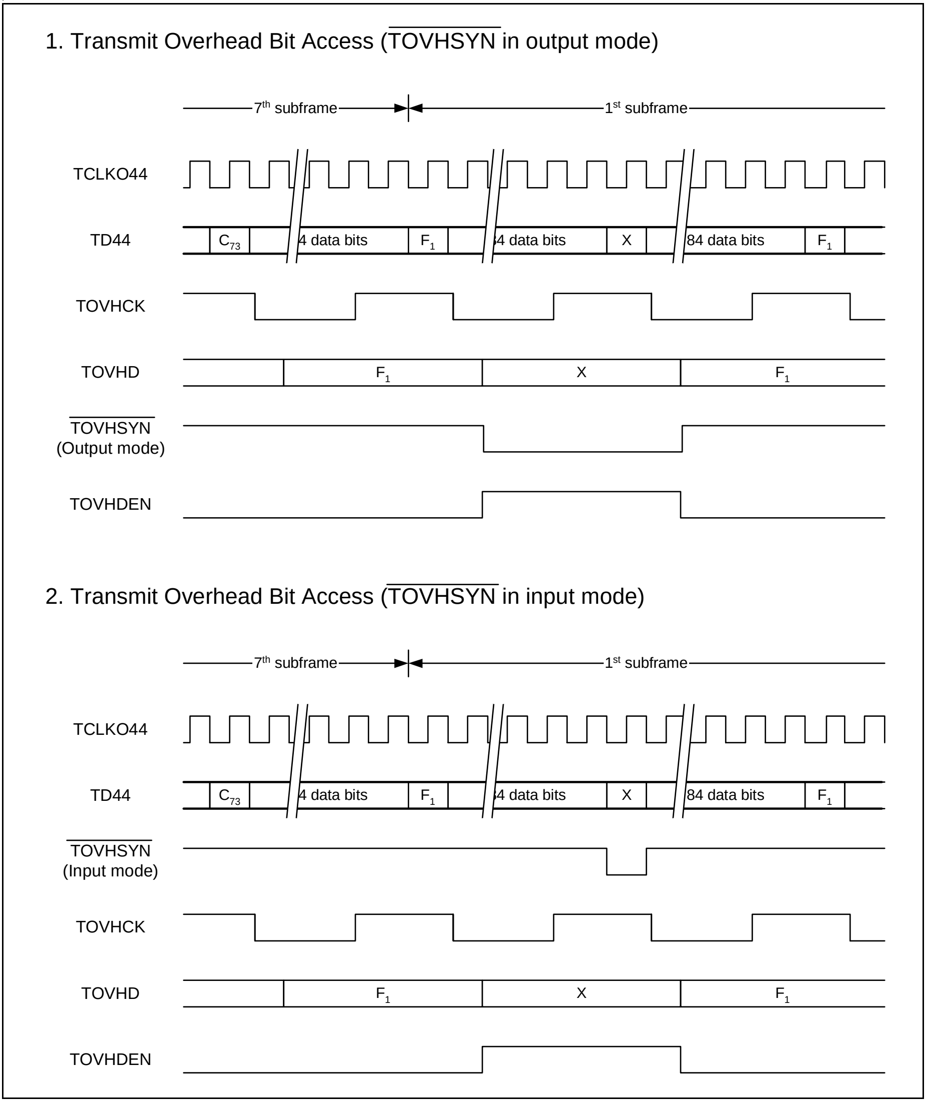


Figure 21 Transmit Overhead Access

The stuff bit access is provided via a receive and transmit stuff bit clock (RSBCK, TSBCK) and the two stuff bit signals RSBD and TSBD. Stuff bits are updated on the falling edge and sampled on the rising edge of the corresponding stuff bit clock.

5.2.2 DS1/E1 Interface/DS3 System Interface

Dependent on the selected operational mode the TE3-MUX operates in channelized mode, where the M13 multiplexer is enabled, or in unchannelized mode where the M13 multiplexer is disabled. In unchannelized mode the first tributary interface is used to transfer DS3 payload data.

5.2.2.1 DS1/E1 Interface

In receive direction (DS3 --> DS1/E1) each port consists of a clock output RTC(x) and the corresponding data output RTD(x). The receive clock is nominally a 1.544 MHz (DS1) respectively a 2.048 MHz (E1) clock. Due to the demultiplexing and destuffing process this clock contains clock gaps. Each port can be mapped independently to any of the 28 tributaries of the T3 signal.

In transmit direction (DS1/E1--> DS3) each port consists of a clock input TTC(x) and the corresponding data input TTD(x). This clock is nominally a 1.544 MHz (DS1 mode) respectively a 2.048 MHz (E1) clock.

5.2.2.2 DS3 System Interface

In unchannelized mode the first DS1/E1 interface is used to transfer DS3 payload data. The DS3 payload clocks are derived from the DS3 receive respectively the DS3 transmit clock. In receive direction the overhead bits are extracted and the receive clock is gapped on those positions which contain the overhead bits. In transmit direction clock #1 (TTC(1)) is switched to output direction and transmit data needs to be provided via TTD(1). TTC(1) is gapped on those positions where the overhead bits need to be inserted by the TE3-MUX.

5.3 JTAG Interface

A test access port (TAP) is implemented in the TE3-MUX. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 22** gives an overview about the TAP controller.

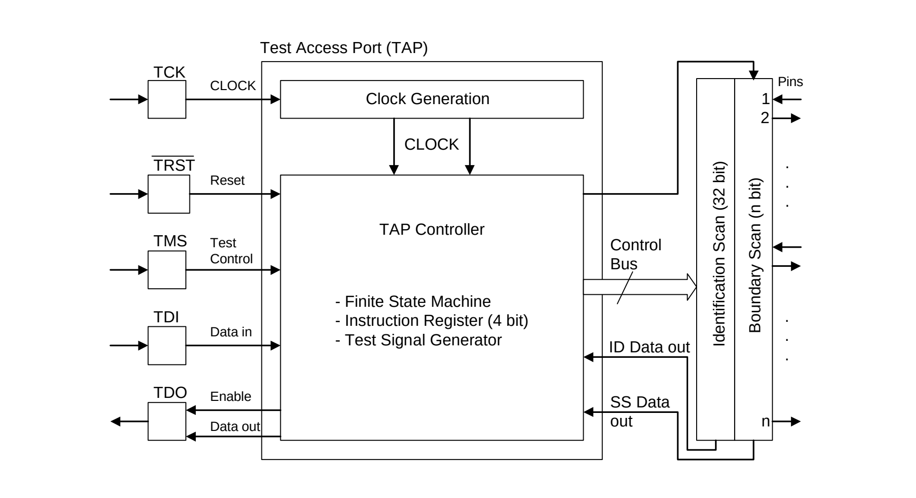


Figure 22 Block Diagram of Test Access Port and Boundary Scan Unit

If no boundary scan operation is planned $\overline{\text{TRST}}$ has to be connected to V_{SS}. TMS and TDI do not need to be connected since pull- up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put the unused inputs to defined levels. In this case, if the JTAG is not used:
TMS = TCK = ‘1’ is recommended.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, i. e. $\overline{\text{TRST}}$ is connected to V_{DD3} or $\overline{\text{TRST}}$ input is open in which case internal pull sets $\overline{\text{TRST}}$ to V_{DD3}. Test data at TDI are loaded with a clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to another; constant ‘1’ on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out, enable) and an I/O-pin (I/O) uses three cells (data in, data out, enable). Note that most functional output and input pins of the TE3-MUX are tested as I/O pins in boundary scan, hence using three cells. The boundary scan unit of the TE3-MUX contains a total of n = 484 scan cells. The desired test mode is selected by serially loading a 4-bit instruction code into the instruction register via TDI (LSB first).

EXTEST is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values (‘0’ or ‘1’). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

INTEST supports internal testing of the chip, i. e. the output pins capture the current level on the corresponding internal line whereas all input pins are held on constant values (‘0’ or ‘1’). The resulting boundary scan vector is shifted to TDO. The next test vector is serially loaded via TDI. Then all input pins are updated for the following test cycle.

SAMPLE/PRELOAD is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ‘1’.

The ID code field is set to

Version : 1_H

Part Number : 0078_H

Manufacturer : 083_H (including LSB, which is fixed to ’1’)

Note: Since in test logic reset state the code ‘0011’ is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state.

BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

CLAMP allows the state of signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. Signals driven from the TE3-MUX will not change while the CLAMP instruction is selected.

HIGHZ places all of the system outputs in an inactive drive state.

6 Reset and Initialization procedure

Since the term “initialization” can have different meanings, the following definition applies:

Chip Initialization

Generating defined values in all on-chip registers, RAMs (if required), flip-flops etc.

Mode Initialization

Software procedure, that prepares the device to its required operation, i.e. mainly writing on-chip registers to prepare the device for operation in the respective system environment.

Operational programming

Software procedures that setup, maintain and shut down operational modes, i.e. initialize logical channel or maintain framing operations on selected ports.

6.1 Chip Initialization

Reset phase

The hardware reset $\overline{\text{RST}}$ has to be applied to the device. Chip input $\overline{\text{TRST}}$ must be activated prior to or while asserting $\overline{\text{RST}}$ and should be held asserted as long as the boundary scan operation is not required. During reset:

- All I/Os and all outputs are tri-state.
- All registers, state machines, flip-flops etc. are set asynchronously to their reset values and all internal modules are set to their initial state.
- All interrupts are masked.

After hardware reset ($\overline{\text{RST}}$ deasserted) the transmit clock TCLK44 is assumed to be running. Tributary clocks must be low/high or running. The local bus interface goes into its operational state.

6.2 Mode Initialization

After reset the TE3-MUX is configured in C-bit parity mode. System software has to setup the device for the required function.

7 Register Description

The register description of the TE3-MUX is divided into two parts, an overview of all internal registers and in the second part a detailed description of all internal registers.

7.1 Register Overview

Note: Register locations not contained in the following register tables are “reserved”. In general all write accesses to reserved registers are discarded and read access to reserved registers result in 0000$_H$ (16-bit bus mode) or 00$_H$ (8-bit bus mode). Nevertheless, to allow future extensions, system software shall access documented registers only, since writes to reserved registers may result in unexpected behavior. The read value of reserved registers shall be handled as don’t care.
Unused and reserved bits are marked with a gray box. The same rules as given for register accesses apply to reserved bits, except that system software shall write the documented default value in reserved bit locations.

Note: The lower 8 bits (bits 7..0) of a register correspond to even address, the upper 8 bits (bits 15..8) correspond to an odd address.

Table 7 Register Overview

Register	Access	Address	Reset value	Comment	Page
DS3 Clock Configuration and Status Register					
D3CLKCS	R/W	00$_H$	00$_H$	DS3 Clock Configuration and Status	78
TUCLKC	R/W	01$_H$	00$_H$	Test Unit Clock Configuration	80
DS3 Transmit Control Registers					
D3TCFG	R/W	02$_H$	0000$_H$	Transmit Configuration	81
D3TCOM	R/W	04$_H$	70$_H$	Transmit Command	83
D3TLPB	R/W	05$_H$	00$_H$	Remote DS2 Loopback	85
D3TLPC	R/W	06$_H$	00$_H$	Transmit Loopback Code Insertion	86
D3TAIS	R/W	07$_H$	00$_H$	Transmit AIS Insertion	87
D3TFINS	R/W	08$_H$	00$_H$	Transmit Fault Insertion Control	88
D3TTUC	R/W	09$_H$	00$_H$	Transmit Test Unit Control	89
D3TSDL	R/W	0A$_H$	01FF$_H$	Transmit Spare Data Link	90

Register	Access	Address	Reset value	Comment	Page
DS3 Receive Control/Status Registers					
D3RCFG	R/W	10_H	0000_H	Receive Configuration	91
D3RCOM	R/W	12_H	00_H	Receive Command	94
D3RAP	R/W	13_H	00_H	Alarm Timer Parameters	96
D3RIMSK	R/W	14_H	$0FFF_H$	Receive Interrupt Mask	97
D3RESIM	R/W	16_H	00_H	Receive Error Simulation	98
D3RTUC	R/W	17_H	00_H	Receive Test Unit Control	99
D3RSTAT	R	18_H	0001_H	Receive Status	100
D3RLPCS	R	$1A_H$	00_H	Receive Loopback Code Status	103
D3RSDL	R	$1C_H$	$01FF_H$	Receive Spare Data Link	104
D3RCVE	R/W	$1E_H$	0000_H	Receive B3ZS Code Violation Error Counter	105
D3REXZ	R/W	$2E_H$	0000_H	Receive Excessive Zero Counter	105
D3RFEC	R/W	20_H	0000_H	Receive Framing Error Counter	106
D3RPEC	R/W	22_H	0000_H	Receive Parity Error Counter	106
D3RCPEC	R/W	24_H	0000_H	Receive Path Parity Error Counter	107
D3RFEBEC	R/W	26_H	0000_H	Receive FEBE Error Counter	107
D3RINTV	R	28_H	00_H	Interrupt Vector	108
D3RINTC	R	$2A_H$	0000_H	Interrupt Status	111
D3RINTL	R	$2C_H$	00_H	Interrupt Loopback Code Status	112
DS2 Transmit Control Registers					
D2TSEL	R/W	30_H	00_H	DS2 Transmit Group Select	113
D2TCFG	R/W	31_H	00_H	Transmit Configuration	114
D2TCOM	R/W	32_H	00_H	Transmit Command	115
D2TLPC	R/W	33_H	00_H	Remote DS1/E1 Loopback Loopback Code Insertion	116
D2TTM0	R/W	34_H	00_H	Tributary Map Registers	117
D2TTM1	R/W	35_H	00_H		
D2TTM2	R/W	36_H	00_H		
D2TTM3	R/W	37_H	00_H		

Register	Access	Address	Reset value	Comment	Page
DS2 Receive Control Registers					
D2RSEL	R/W	40_H	00_H	DS2 Receive Group Select	118
D2RCFG	R/W	41_H	00_H	Receive Configuration	119
D2RCOM	R/W	42_H	00_H	Receive Command	121
D2RIMSK	R/W	43_H	00_H	Receive Interrupt Mask	123
D2RTM0	R/W	44_H	00_H	Tributary Map Registers	124
D2RTM1	R/W	45_H	00_H		
D2RTM2	R/W	46_H	00_H		
D2RTM3	R/W	47_H	00_H		
D2RLAIS	R	48_H	00_H	Local DS1/E1 Loopback AIS Insertion Register	125
D2RSTAT	R	49_H	00_H	Receive Status	126
D2RLPCS	R	$4A_H$	00_H	Receive Loopback Code Status	128
D2RAP	R/W	$4B_H$	00_H	Alarm Timer Parameters	129
D2RFEC	R/W	$4C_H$	0000_H	Receive Framing Bit Error Counter	131
D2RPEC	R/W	$4E_H$	0000_H	Receive Parity Bit Error Counter (G.747)	131
Test Unit Transmit Registers					
TUTCFG	R/W	50_H	0000_H	Transmit Configuration	132
TUTCOM	W	52_H	00_H	Transmit Command	133
TUTEIR	R/W	53_H	00_H	Transmit Error Insertion Rate	135
TUTFP0	R/W	54_H	0000_H	Transmit Fixed Pattern	136
TUTFP1	R/W	56_H	0000_H		
Test Unit Receive Registers					
TURCFG	R/W	58_H	0000_H	Receive Configuration	137
TURCOM	W	$5A_H$	00_H	Receive Command	139
TURERMI	R/W	$5B_H$	00_H	Receive Error Measurement Interval	141
TURIMSK	R/W	$5C_H$	$1F1F_H$	Receive Interrupt Mask	142
TURSTAT	R	$5E_H$	0001_H	Receive Status	143

Register	Access	Address	Reset value	Comment	Page
TURBC0	R	60_H	0000_H	Receive Bit Counter	145
TURBC1	R	62_H	0000_H		
TUREC0	R	64_H	0000_H	Receive Error Counter	147
TUREC1	R	66_H	0000_H		
TURFP0	R	68_H	0000_H	Receive Fixed Pattern	149
TURFP1	R	$6A_H$	0000_H		
Test Unit Framer Registers					
TUTFCFG	R/W	70_H	00_H	Transmit Framer Configuration	150
TUTFCOM	R/W	71_H	00_H	Transmit Framer Command	152
TURFCFG	R/W	74_H	00_H	Receive Framer Configuration	153
TURFCOM	R/W	75_H	00_H	Receive Framer Command	155
TURFSTAT	R	76_H	00_H	Receive Framer Status Register	156
TURFFEC	R	78_H	0000_H	Receive Framing Error Counter	157
TURFCEC	R	$7A_H$	0000_H	Receive Framer CRC Error Counter	158
TURFEBC	R	$7C_H$	0000_H	Receive Framer Errored Block Counter	159
Far End Alarm and Control Channel (BOM)					
FRCFG	R/W	80_H	0000_H	Receive Configuration Register	160
FRFF	R	82_H	0000_H	Receive FIFO	162
FXCFG	R/W	84_H	00_H	Transmit Configuration Register	163
FXFF	W	86_H	0000_H	Transmit FIFO	164
FPSR	R	88_H	2000_H	Port Status Register	165
FHND	W	$8A_H$	0000_H	Handshake Register	167
FMSK	R/W	$8C_H$	00_H	Interrupt Mask Register	170
C-Bit Path Maintenance Channel (HDLC)					
PRCFG	R/W	90_H	0000_H	Receive Configuration Register	171
PRFF	R	92_H	0000_H	Receive FIFO	173
PXCFG	R/W	94_H	0000_H	Transmit Configuration Register	174
PXFF	W	96_H	0000_H	Transmit FIFO	176
PPSR	R	98_H	2000_H	Port Status Register	177

Register	Access	Address	Reset value	Comment	Page
PHND	W	$9A_H$	0000_H	Handshake Register	179
PMSK	R/W	$9C_H$	00_H	Interrupt Mask Register	181

7.2 Detailed Register Description

7.2.1 DS3 Control and Status Registers

D3CLKCS
DS3 Clock Configuration and Status Register

Access : read/write
Address : 00_H
Reset Value : 00_H

7	6	5	4	3	2	1	0
0	RCA	TCA	RRX	RTX	T2RL	R2TL	TXLT

RCA Receive Clock Activity
This bit monitors the receive clock activity (RCLK44).
0 No receive DS3 clock since last read of this register.
1 At least one receive DS3 clock since last read of this register.

TCA Transmit Clock Activity
This bit monitors the transmit clock activity (TCLK44).
0 No transmit DS3 clock since last read of this register.
1 At least one transmit DS3 clock since last read of this register.

RRX Reset receiver
This bit resets the receiver.
0 Normal operation.
1 Reset DS3 receiver. This bit is self clearing.

RTX Reset transmitter
This bit resets the transmitter.
0 Normal operation.
1 Reset DS3 transmitter. This bit is self clearing.

T2RL	Transmit to Receive Loop (Local DS3 Loopback)
	This bit enables the local DS3 loop where the outgoing DS3 bit stream is mirrored to the DS3 input.
	0 Disable local loop.
	1 Enable local loop.
R2TL	Receive to Transmit Loop (Remote DS3 Loopback)
	This bit enables the remote DS3 line loop where the complete incoming DS3 bit stream is mirrored to the transmitter.
	0 Disable remote loop.
	1 Enable remote loop.
TXLT	Transmit Loop Timing Mode
	This bit enables DS3 looped timing where the transmitter uses the receivers DS3 input clock.
	0 Disable looped timing.
	1 Enabled looped timing.

TUCLKC
Test Unit Clock Configuration Register

Access : read/write

Address : 01_H

Reset Value : 00_H

7						1	0
0	0	0	0	0	0	RTUR	TUL

RTUR Reset Test Unit Receiver

This bit resets the test unit receiver.

0 Normal operation.

1 Reset Receiver (automatically removed). This bit is self clearing.

TUL Test Unit Transmit to Receive Loop

This bit switches a local loop from the test unit transmitter to the test unit receiver. While operating in loop mode the test unit is operated with TCLK44.

0 Normal operation.

1 Test unit transmitter output connected to test unit receiver input.

D3TCFG
DS3 Transmit Configuration Register

Access : read/write

Address : 02_H

Reset Value : 0000_H

15					10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	ITRCK	ITRD	FAM	ITCK	ITD	UTD	AISC	LPC(1:0)		FPL	CBP

ITRCK Invert DS1/E1 Interface Clock

This bit sets the clock edge for data sampling on the low speed interfaces.

- 0 Sample data on the falling edge of TTC(x).
- 1 Sample data on the rising edge of TTC(x).

ITRD Invert DS1/E1 Data

This bit enables inversion of sampled data.

- 0 No inversion of data sampled on TTD(x).
- 1 Invert data sampled on TTD(x).

FAM $\overline{\text{TOVHSYN}}$ Mode

This bit switches between input mode and output mode of the signal pin $\overline{\text{TOVHSYN}}$. If $\overline{\text{TOVHSYN}}$ is operated in input mode it marks the position of the X-bit. Therefor the outgoing DS3 frame is aligned to $\overline{\text{TOVHSYN}}$. If TOVHSYN is switched to output mode $\overline{\text{TOVHSYN}}$ is asserted when the X-bit needs to be inserted via the transmit overhead interface.

- 0 $\overline{\text{TOVHSYN}}$ switched to input.
- 1 $\overline{\text{TOVHSYN}}$ switched to output.

ITCK Invert DS3 Transmit Clock

This bit sets the clock edge on which transmit data TD44P/TD44N is updated with respect to the transmit clock TCLKO44.

- 0 Update transmit data on the rising edge of the transmit clock.
- 1 Update transmit data on the falling edge of transmit clock.

ITD	Invert DS3 Transmit Data This bit enables inversion of DS3 transmit data. 0 Transmit data is logic high (not inverted). 1 Transmit data is logic low (inverted).	
UTD	Unipolar data mode This bit sets the port mode to dual-rail mode or unipolar mode. 0 B3ZS (dual rail data). 1 Unipolar mode (single rail data).	
AISC	AIS Code Type This bit field sets the AIS code. 0 Set AIS to '1010... ' between overhead bits, C-bits all '0's. The X-bits needs to be set via D3TCOM.TXBIT. 1 Set AIS to unframed all '1's (non-standard).	
LPC	Loopback Code. This bit field selects the C-bit which will be inverted when loopback requests are transmitted. 00 Invert 1st C-bit. 01 Invert 2nd C-bit. 10 Invert 3rd C-bit.	
FPL	Full Payload Mode This bit enables the M23 multiplex operation or the full payload rate format. 0 Enable M23 multiplex operation. Payload is formed by interleaving 7 asynchronous DS2 tributaries. 1 Enable full payload rate format. The payload is one single, high speed data stream without stuffing.	
CBP	C-bit parity mode This bit enables M13 asynchronous mode or C-bit parity mode. 0 M13 asynchronous mode. 1 C-bit parity mode.	

D3TCOM
DS3 Transmit Command Register

Access : read/write

Address : 04_H

Reset Value : 70_H

7	6	5	4	3	2	1	0
0	TAIC	TN_rB	TXBIT	SIDLE	SAISA	SAIS	0

TAIC Transmitted AIC-bit

This bit sets the value to be transmitted in the DS3 overhead bit of block 3, subframe 1. This function is available in C-pit parity format only.

0 AIC-bit = ‘0’.

1 AIC-bit = ‘1’.

TN_rB Transmitted N_r-bit

This bit sets the value to be transmitted in the DS3 overhead bit of block 5, subframe 1. This function is available in C-pit parity format only.

0 N_r-bit = ‘0’.

1 N_r-bit = ‘1’.

TXBIT Transmitted X-bits

This bit sets the value to be transmitted in the DS3 overhead bit of block 1, subframes 1 and 2.

TXBIT is synchronized to the DS3 multiframe. Both X-bits in a multiframe are guaranteed identical. Software should limit changes to maximum of 1 per second.

Note: Setting TXBIT to ‘0’ results in transmission of remote alarm indication even when SIDLE, SAISA or SAIS are set.

0 X-bit = ‘0’.

1 X-bit = ‘1’.

SIDLE Send DS3 Idle Code

This bit enables transmission of the DS3 idle code ('1100' between overhead bits, C-bits all '0's). The X-bits must be set to '1' independently by setting TXBIT to '1'.

0 Normal operation.

1 Send DS3 idle code.

SAISA Send AIS in DS3 output and on DS3 loop

This bit enables transmission of AIS on the DS3 output. If the DS3 is additionally switched to local DS3 loopback mode the DS3 signal including AIS is mirrored to the receiver. The AIS code transmitted depends on D3TCFG.AISC. The X-bits must be set to '1' independently by setting TXBIT to '1'.

0 Normal operation.

1 Enable transmission of AIS.

SAIS Send AIS at DS3 output

This bit enables transmission of AIS on the DS3 output. If the DS3 signal is switched into local DS3 loopback mode the DS3 signal **without** AIS code is mirrored to the DS3 receiver. The AIS code transmitted depends on D3TCFG.AISC. The X-bits must be set to '1' independently by setting TXBIT to '1'.

0 Normal operation.

1 Enable transmission of AIS.

D3TLPB
DS3 Transmit Remote DS2 Loopback Register

Access : read/write

Address : 05_H

Reset Value : 00_H

7	6 … 0
0	LPB(6:0)

LPB Remote DS2 Loopback

Setting LPB(x) enables the remote DS2 loopback of tributary x. In this mode the demultiplexed DS2 tributary is internally looped and multiplexed into the outgoing DS3 signal.

0 Normal operation.

1 Enable remote DS2 loopback of tributary x.

D3TLPC
DS3 Transmit Loopback Code Insertion Register

Access : read/write

Address : 06_H

Reset Value : 00_H

7	6 ... 0
0	LPC(6:0)

LPC — Send Loopback

Setting LPC(x) enables transmission of the loopback code in tributary x of the DS3 signal. The loopback code inserted depends on D3TCFG.LPC.

0 Normal operation.

1 Enable transmission of loopback code in tributary x.

D3TAIS
DS3 Transmit AIS Insertion Register

Access : read/write
Address : 07_H
Reset Value : 00_H

7	6 ... 0
AISE	AIS(6:0)

AISE — AIS Error Insertion

Toggling this bit inserts one ‘0’ in all DS3 tributaries which transmit AIS.

AIS — Send DS2 Alarm Indication Signal

Setting AIS(x) enables insertion of the DS2 alarm indication signal in the outgoing tributary x of the DS3 signal. AIS is an all ’1’ signal.

0 Normal operation.

1 Enable transmission of AIS in tributary x.

D3TFINS
DS3 Transmit Fault Insertion Control Register

Access : read/write
Address : 08_H
Reset Value : 00_H

7				3 0
0	0	0	0	FINSC(3:0)

FINSC Fault Insertion Code.

Fault insertion is service affecting and is intended for testing only. Codes are not self clearing, i.e. errors are continuously generated as indicated until bit cleared. A single FEBE, P, CP, or code violation is guaranteed to be inserted if the respective code is written and then immediately cleared.

0 Normal operation (no fault insertion).
1 Insert FEBE event every multiframe (106 µsec).
2 Insert P-bit errors every 2nd multiframe (212 µsec).
3 Insert CP-bit errors every 2nd multiframe (212 µsec).
4 Insert 4 F-bit errors/multiframe (satisfies 3 out of 15 threshold trigger).
5 Insert 5 F-bit errors/multiframe (satisfies 3 out of 7 threshold trigger).
6 Insert 3 M-bit errors/multiframe (caution: receiver can frame on emulator).
7 Force DS3 output to all ‘0’s.
8 Insert B3ZS violation/multiframe (violation of alternate polarity rule).
9 Insert 3 zero string/multiframe (B3ZS code word suppressed).

D3TTUC
DS3 Transmit Test Unit Control Register

Access : read/write

Address : 09_H

Reset Value : 00_H

7	6		4	3	2	1	0
EN	TUDS2(2:0)			TUDS1(1:0)		TUIM	

EN — Enable Test Unit Insertion

Setting this bit enables insertion of the test unit data.

- 0 Normal operation.
- 1 Enable insertion of test unit data.

TUDS2 — Test Unit DS2 Group

This bit field selects the DS2 group the test unit is attached to. Only valid if TUIM is 10_B, 01_B or 00_B.

- 0..6 Selects DS2 group 0..6.

TUDS1 — Test Unit DS1 Tributary

This bit field selects the DS1 tributary the test unit is attached to. Only valid if TUIM is 00_B. The DS2 group is selected via TUDS2.

- 0..3 DS1/E1 tributary

TUIM — Bit Error Rate Test Unit (TU) Insertion Mode

This bit field selects the interface the test unit is attached to.

- 00_B Insert test stream into DS1/E1 tributary.
- 01_B Insert test stream into DS2 tributary (unframed, bypass M12).
- 10_B Insert test stream into DS2 payload (framed).
- 11_B Insert test stream into DS3 payload (framed).

D3TSDL
DS3 Transmit Spare Data Link Register

Access : read/write

Address : $0A_H$

Reset Value : $01FF_H$

15							8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DL77	DL75	DL73	DL67	DL65	DL63	DL27	DL25	DL23

Multiframe buffer for spare DL bits transmitted in blocks 3, 5, and 7 of subframes 2, 6, and 7. If enabled, the M13 will generate an interrupt every multiframe to request a refresh of this register. The software must write these registers within 106 µsec to avoid an underrun.

DL(S)(B) Overhead bit for block B of subframe S

These bits store the DL bits to be transmitted in blocks 3, 5, and 7 of subframes 2, 6, and 7. If enabled, the M13 will generate an interrupt every multiframe to request a refresh of this register.

D3RCFG
DS3 Receive Configuration Register

Access : read/write

Address : 10_H

Reset Value : 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CVM	ITRCK	ITRD	OD	IL	STTM	ECM	FEBM	0	AISX	MFM	MDIS	FFM	IRCK	IRD	URD

Note: M13 mode, Full payload mode, loopback code, and AIS mode are controlled by bits CBP, FPL, LPC, and AISC in register DS3 transmit configuration register D3TCFG.

CVM B3ZS Code Word (“00V” or “10V” Acceptance Condition)

This bit selects the B3ZS violations alternate polarity to maintain line balance.

- 0 Convert all B3ZS codeword patterns to “000” regardless of polarity.
- 1 Convert codeword only if alternate violation polarity rule is satisfied.

ITRCK Invert Tributary Clock

This bit sets the clock edge for data update on the low speed tributaries.

- 0 Update data on the rising edge of RTC(x).
- 1 Update data on the falling edge of RTC(x).

ITRD Invert Tributary Data

This bit enables inversion of tributary data.

- 0 No inversion of data provided via RTD(x).
- 1 Invert data provided via RTD(x).

OD Interrupt Open Drain

This bit selects the operating mode of the interrupt pin.

- 0 Open Drain.
- 1 Push-Pull.

IL — Interrupt Active Level

This bit selects the active level of the interrupt pin.

0 Active Low.

1 Active High.

STTM — Select Transmit Tributary Monitoring for receive test unit

This bit selects the DS1/E1 tributary observed by the test unit receiver. The test unit can be connected to the upstream DS1/E1 tributary (DS1/E1 tributary going towards the DS3 interface) or to the downstream DS1/E1 tributary (DS1/E1 tributary coming from the DS3 interface).

0 Monitor downstream DS1/E1 tributary.

1 Monitor upstream DS1/E1 tributary.

ECM — Error Counter Mode

DS3 errors are counted in background and copied to foreground (error counter registers) when condition selected via ECM is met.

0 Counter values are copied to foreground when copy command is executed. See also register DS3COM.

1 The counter values are copied to the foreground register in one second intervals. At the same time the background registers are reset to zero. This operation is synchronous with the periodic one second interrupt which alerts software to read the register.

FEBM — Far End Block Error (FEBE) Mode

This bit selects the event which leads to FEBE indication. It is available in C-bit parity mode only.

0 Receive multiframe parity error.

1 Receive multiframe parity error or framing error.

AISX — AIS X-bit Check Disable

This bit disables checking of the X-bit for AIS and idle detection.

0 Check X-bit.

1 Disable check of X-bit.

MFM	Multiframe Framing Mode
	This bit selects the M-bit error condition which triggers the DS3 framer to start a new frame search. To enable reframing in case of M-bit errors MDIS must be set to ‘0’.
	0 Start new F-frame search if M-bit errors are detected in two out of four consecutive M-frames.
	1 Start new F-frame search if M-bit errors are detected in three out of four consecutive M-frames.
MDIS	Multiframe Reframe Disable
	This bit disables reframing due to M-bit errors.
	0 Enable reframe due to M-bit errors.
	1 Disable reframe due to M-bit errors.
FFM	F Framing Mode
	This bit selects the F-bit error condition which triggers the DS3 framer to start a new frame search.
	0 A new frame search is started when 3 out of 8 contiguous F-bits are in error.
	1 A new frame search is started when 3 out of 16 contiguous F-bits are in error.
IRCK	Invert Receive Clock
	This bit sets the clock edge for data sampling.
	0 Sample data on rising edge of receive clock.
	1 Sample data on falling edge of receive clock.
IRD	Invert Receive Data
	This bit enables inversion of receive data.
	0 Receive data is logic high (not inverted).
	1 Receive data is logic low (inverted).
URD	Unipolar Receive Data
	This bit sets the port mode to dual-rail mode or unipolar mode.
	0 B3ZS (dual rail data input).
	1 Unipolar mode (single rail data input).

D3RCOM
DS3 Receive Command Register

Access : read/write

Address : 12_H

Reset Value : 00_H

7			4	3	2	1	0
0	0	0	C3NC	C3C	CNCA	CCA	FRS

C3NC Copy DS3 Error Counters

Values of DS3 background registers are copied to foreground. Background registers are NOT cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

Note: Usage of this function in not recommend in 'One Second' error counter mode (D3RCFG.ECM = '1').

0 No operation.

1 Copy background counters to foreground.

C3C Copy and Clear DS3 Error Counters

Values of DS3 background registers are copied to foreground. Background registers are cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

0 No operation.

1 Copy background counters to foreground. Clear background counters.

Note: Usage of this function in not recommend in 'One Second' error counter mode (D3RCFG.ECM = '1').

CNCA Copy Error Counters

Only valid for counters which are not operating in 'One Second' error counter mode. Values of DS2 and DS3 background registers are copied to foreground. Background registers are NOT cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

0 No operation.

1 Copy background counters to foreground.

CCA Copy and Clear DS2/DS3 Error Counters

Only valid for counters which are not operating in 'One Second' error counter mode. Values of DS2 and DS3 background registers are copied to foreground. Background registers are cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

0 No operation.

1 Copy background counters to foreground. Clear background counters.

FRS Force Resynchronization

This bit enables a new frame search on the DS3 input. The command is self clearing after frame search has begun.

0 Normal operation.

1 Force new frame search.

D3RAP
DS3 Receive Alarm Timer Parameters Register

Access : read/write

Address : 13_H

Reset Value : 00_H

7	5	0
AIS	0	CV(5:0)

AIS — AIS criteria

This bits sets the error rate for AIS detection. Declaration of AIS depends on value defined in bit field CV.

0 — AIS is recognized when the alarm indication signal is received with less than 8 errors per multiframe.

1 — AIS is recognized when the alarm indication signal is received with less than 15 errors per multiframe.

CV — Counter Value

This bit specifies the number of frames when the TE3-MUX declares AIS, RED or Idle.

0..63 — Counter Value.

D3RIMSK
DS3 Receive Interrupt Mask Register

Access : read/write

Address : 14_H

Reset Value : $0FFF_H$

15				11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RSDL	TSDL	LPCS	1SEC	N_r	AIC	XBIT	IDLES	AISS	REDS	LOSS	FAS

This register provides the interrupt mask for DS3 status interrupts and DS3 loopback code interrupts. See register D3RSTAT and D3RLPCS for interrupt conditions.

The following definition applies:

1	The corresponding interrupt will not be generated by the device.
0	The corresponding interrupt will be generated.

RSDL	Mask ’Receive Spare Data Link Transfer Buffer Full’
TSDL	Mask ’Transmit Spare Data Link Transfer Buffer Empty’
LPCS	Mask ’Loopback Code Status’ (flagged in D3RLPCS)
1SEC	Mask ’1 Second Interrupt’
N_r	Mask ’N_r-bit Image’ (C-bit parity mode only)
AIC	Mask ’AIC-bit Image’ (C-bit parity mode)
XBIT	Mask ’X-bit Image’
IDLES	Mask ’DS3 Idle Signal State’
AISS	Mask ’DS3 Alarm Indication Signal State’
REDS	Mask ’DS3 Red Alarm State’
LOSS	Mask ’DS3 Input Signal State’
FAS	Mask ’DS3 Frame Alignment State’

D3RESIM
DS3 Receive Error Simulation Register

Access : read/write

Address : 16_H

Reset Value : 00_H

7			4		2		0
0	0	0	FTMR	0	ESIMC(2:0)		

FTMR Fast Timer

This bit enables alarm timer test function (manufacturing test only).

0 Normal Operation.

1 Test Operation.

DS3 RED/AIS/Idle timer period reduced by 56.

DS2 READ/AIS timer period reduced by 24.

Second interrupt period reduced to 140 µsec

ESIMC Error Simulation Code

This bit enables error simulation. During error simulation the device generates error interrupts and error status messages. Nevertheless the service is not affected.

0 Normal operation (no error simulation).

1 Simulate one F-bit error/multiframe (106 µsec).

2 Simulate M-bit error in every other multiframe.

3 Simulate FEBE event/multiframe (106 µsec).

4 Simulate P/CP event/multiframe (106 µsec).

5 Simulate Loss of DS3 input (all zeros).

6 Simulate B3ZS code violations.

7 Simulate Loss of Receive Clock.

D3RTUC
DS3 Receive Test Unit Control Register

Access : read/write

Address : 17_H

Reset Value : 00_H

7	6	5	4	3	2	1	0
EN	TUDS2(2:0)			TUDS1(1:0)		TURM(1:0)	

EN Enable Test Unit Receive Clock

This bit enables the receive clock of the test unit. The clock speed is dependent on the selected test mode.

0 Receive clock disabled.

1 Receive clock enabled.

TUDS2 Test Unit DS2 Group

This bit field selects the DS2 group the test unit is attached to. Only valid if TURM is 10_B, 01_B, or 00_B.

0..6 Selects DS2 group 0..6.

TUDS1 Test Unit DS1/E1 Tributary

This bit field selects the DS1/E1 tributary the test unit is attached to. Only valid if TURM is 00_B. The DS2 group is selected via TUDS2.

0..3 DS1/E1 tributary

TURM Test Unit Receive Mode

This bit field selects the interface the test unit is attached to.

00_B DS1/E1 tributary

01_B DS2 tributary (unframed, bypass M12)

10_B DS2 payload (framed)

11_B DS3 payload (framed)

D3RSTAT
DS3 Receive Status Register

Access : read

Address : 18_H

Reset Value : 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	RSDL	TSDL	LPCD	1SEC	N_r/ AICC	AIC	XBIT	IDLES	AISS	REDS	LOSS	COFA	FAS

Each bit in the DS3 framer receive status register declares a specific condition dependent on the selected modes. The following convention applies to the individual bits:

0 The named status is not or no longer existing.

1 The named status is currently effective.

Except for COFA every bit can be used to generate an interrupt. Interrupts can be masked in register D3RIMSK.

RSDL Receive Spare Data Link Buffer Full

This bit indicates that the spare data link receive buffer (register D3RSDL) is full.

TSDL Transmit Spare Data Link Buffer Empty

This bit indicates that the spare data link transmit buffer (register D3TSDL) is empty.

LPCD Loopback Code Detected

This bit indicates changes in register D3RLPCS.

1SEC 1 Second Flag

This bit toggles every second synchronously with the one second interrupt. It can be used by software to synchronize 1 second events when the ’One second interrupt’ is masked.

N_r/AICC	N_r-bit Image (C-bit parity format only) This bit contains an image of the DS3 frame overhead bit in block 5 of subframe 1. It is updated only if its state persists for 3 multiframes and DS3 frame is aligned. AIC-bit Changed (M13 asynchronous format) This bit indicates a change of the AIC-bit (first C-bit of the first subframe) since the last read of this register.
AIC	AIC-bit Image (DS3 frame overhead bit in block 3 of subframe 1) This bit contains an image of the DS3 frame overhead bit in block 3 of subframe 1. It is updated only if its state persists for 3 multiframes and DS3 frame is aligned.
XBIT	X-bit Image (DS3 frame overhead bit in block 1 of subframes 1 and 2) This bit contains an image of the DS3 frame overhead bit in block 1 of subframes 1 and 2. It is updated only if both overhead have the same value, when its state persists for 3 multiframes and when the DS3 frame is aligned.
IDLES	DS3 Idle Signal State This bit indicates that the idle pattern (framed ...1100... with C-bits='0' in subframe 3 and X-bits='1') was persistent as per alarm timing parameters defined in register D3RAP. Idle is considered active in a multiframe when fewer than 15 errors are detected. At 10^{-3} error rates, 5 errors per multiframe are typical. The exact time necessary to change the flag could be greater if the FAS flag is not constant. The frame alignment state is integrated by incrementing or decrementing a counter at the end of each multiframe when the FAS flag is set or cleared respectively.
AISS	DS3 Alarm Indication Signal State This bit indicates the AIS alarm state. AIS can be a framed '..1010..' pattern with C-bits='0' and X-bits='1' or an unframed all '1' pattern. This is determined by D3TCFG.AISC. AIS is considered active in a multiframe when fewer than 15 errors are detected and is declared when it was persistent as per alarm timing parameters defined in register D3RAP. At 10^{-3} error rates, 5 errors per multiframe are typical. The exact time necessary to change the flag could be greater if the FAS flag is not constant. The frame alignment state is integrated by incrementing or decrementing a counter at the end of each multiframe when the FAS flag is set or cleared respectively.

REDS	DS3 Red Alarm State (Loss of Frame Alignment) This bit indicates that red alarm was persistent as per alarm timing parameter defined in register D3RAP. The red alarm flag nominally changes when loss of frame alignment condition persists for either 32 or 128 multiframes. The exact time necessary to change the flag could be greater if the FAS flag is not constant. The frame alignment state is integrated by incrementing or decrementing a counter at the end of each multiframe when the FAS flag set or cleared respectively.
LOSS	DS3 Input Signal State This bit indicates that the received DS3 bit stream contained at least 175 consecutive ‘0’s. It is deasserted when 59 ‘1’ bits are detected in 175 clocks (1/3 density). Following removal of LOS, a 10 msec guard timer is started. If a new LOS occurs, the release condition is extended so that the 1/3 density condition must persist for at least 10 msec. This prevents chatter and excessive interrupts.
COFA	Change of Frame Alignment This bit indicates a change of frame alignment event. It is set when the DS3 framer found a new frame alignment and when the new frame position differs from the expected frame position.
FAS	DS3 Frame Alignment State This bit indicates that the DS3 framer is not aligned.

D3RLPCS
DS3 Receive Loopback Code Status Register

Access : read

Address : $1A_H$

Reset Value : 00_H

7	6	5	4	3	2	1	0
0	LPCD(6:0)						

LPCD Loopback Detected

LPCD(x) indicates that a loopback request was received. A loopback request for tributary x is indicated by inverting one of the 3 C-bits of the x^{th} subframe. The C-bit is determined by D3TCFG.LPC. A command state change must persist for 5 contiguous multiframes before it will be reported. This function is available in M13 asynchronous mode only.

0 No loopback code being received

1 Loopback code being received

D3RSDL
DS3 Receive Spare Data Link Register

Access : read
Address : $1C_H$
Reset Value : $01FF_H$

15							8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DL77	DL75	DL73	DL67	DL65	DL63	DL27	DL25	DL23

DL(S)(B) Overhead Bit for Block B of Subframe S

These bits buffer the spare DL bits received in blocks 3, 5, and 7 of subframes 2, 6, and 7. If enabled, the M13 will generate an interrupt every multiframe to synchronize reading of this register. The register must be read within 106 µsec to avoid an overrun.

D3RCVE
DS3 Receive B3ZS Code Violation Error Counter

Access : read/write
Address : $1E_H$
Reset Value : 0000_H

15	0
CVE(15:0)	

CVE(15:0) B3ZS Code Violation Errors

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

Register D3RCVE counts line code violations. The error counter will not be incremented during asynchronous state.

D3REXZ
DS3 Receive Excessive Zeroes Counter

Access : read/write
Address : $2E_H$
Reset Value : 0000_H

15	0
EXZ(15:0)	

EXZ(15:0) Excessive Zeroes

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

Violations are 3 zero strings. The error counter will not be incremented during asynchronous state.

D3RFEC
DS3 Receive Framing Bit Error Counter

Access : read/write

Address : 20_H

Reset Value : 0000_H

15	0
FEC(15:0)	

FEC(15:0) Framing Bit Error Counter

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

Count of F-bit and M-bit errors. Errors are not counted in out of frame state.

D3RPEC
DS3 Receive Parity Error Counter

Access : read/write

Address : 22_H

Reset Value : 0000_H

15	0
PE(15:0)	

PE(15:0) Parity Bit Error Counter

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

Count of parity errors (P-bits in DS3 overhead bits). The P-bit is duplicated in the DS3 frame structure but only single error maximum is counted per multiframe. Errors are not counted in out of frame state.

D3RCPEC
DS3 Receive Path Parity Error Counter

Access	: read/write
Address	: 24_H
Reset Value	: 0000_H

15	0
CPE(15:0)	

CPE(15:0) Path Parity Error Counter

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

Count of path parity errors (CP bits in DS3 C-bit parity overhead bits). CP-bits are triplicated in the DS3 frame structure but only single error maximum is counted per multiframe. Errors are not counted in out of frame state.

D3RFEBEC
DS3 Receive FEBE Error Counter

Access	: read/write
Address	: 26_H
Reset Value	: 0000_H

15	0
FEBE(15:0)	

FEBE(15:0) FEBE Error Events

Error counter mode (Clear on Read or Errored Second) depends on register D3RCFG.ECM.

This register counts the occurrence of a received ‘not all ‘1’s’. FEBE-bits are triplicated in the DS3 frame structure but only one single error maximum is counted per multiframe. Errors are not counted in out of frame state.

D3RINTV
Interrupt Vector Register

Access : read

Address : 28_H

Reset Value : 00_H

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">TYPE</td><td colspan="6">STATUS</td></tr>
<tr><td colspan="2">00</td><td>0</td><td>LBR</td><td>SR</td><td colspan="3">GN(2:0)</td></tr>
<tr><td colspan="2">01</td><td>0</td><td>0</td><td>RDL</td><td>TDL</td><td>TU</td><td>1S</td></tr>
<tr><td colspan="2">10</td><td rowspan="2">ALLS</td><td rowspan="2">XDU</td><td rowspan="2">XPR</td><td rowspan="2">RPF</td><td rowspan="2">RME</td><td>RMI</td></tr>
<tr><td colspan="2">11</td><td>0</td></tr>
</table>

Four vectors are defined and differentiated by the type field (bits 6 and 7). The interrupt status information contained in the status field (bits 5 down to 0) is dependent on the type information.

TYPE Interrupt Type Information

This bit field defines the content of the following interrupt status field.

- 00 This code defines loopback code changes or status changes of the DS2 or DS3 framer. Subsequently the changes can be read in register D3RINTC or D3RINTL.
- 01 This code defines general status informations.
- 10 This code defines interrupts of the Far End Alarm and Control Channel.
- 11 This code defines interrupts of the C-bit parity Path Maintenance Data Link Channel.

STATUS Status Information

The status information is dependent on the value of the type bit field.

The following section defines the meaning of the status bits:

LBR Loopback Code Status Change

This bit indicates a change of received DS3 or DS2 loopback code status. The loopback code status is shown in register D3RINTL. The related port is indicated in bit field GN.

SR	Status Register Change This bit indicates a change in DS3 or DS2 status. The status is shown is register D3RINTC. The related port is indicated in bit field GN.
GN	Group Number This bit field indicates the port where a status change or loopback code change occurred. 0..6 Status change of DS2 framer 0..6. 7 Status change of DS3 framer.
RDL	Receive Spare Data Link Buffer Full This bit indicates that new DL bits have been received in register D3RSDL. If enabled it is generated with every multiframe to synchronize reading of register D3RSDL.
TDL	Transmit Spare Data Link Buffer Empty This bit indicates that new DL bits shall be written to register D3TSDL. If enabled it is generated with every multiframe to synchronize writing of register D3RSDL.
TU	Test Unit Status Change This bit indicates a status change of the test unit. Subsequently the status can be read in register D3RINTC.
1S	1 Second The 'One Second' interrupt is generated every second.
ALLS	All Sent The 'All Sent' interrupt is generated, when the last bit of a frame to be transmitted is completely sent out and XFF.XFIFO is empty.
XDU	Transmit Data Underrun The 'Transmit Data Underrun' interrupt is generated, when the transmit FIFO of the corresponding channel runs out of data during transmission of a frame. The protocol controller terminates the affected frame.
XPR	Transmit Pool Ready The 'Transmit Pool Ready' interrupt is generated, when a new data block of up to 32 bytes can be written to transmit FIFO. 'Transmit Pool Ready' is the fastest way to access the transmit FIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flag.
RPF	Receive Pool Full This bit is set, when the receive threshold is reached and data has to be read from the receive FIFO. The frame is not yet completely received.

RME	Receive Message End
	This bit is set, when one complete message of length less than 32 bytes or the last part of a frame is stored in the receive FIFO. The number of bytes in RFF.RFIFO can be determined reading the port status register F/PPSR.
RMI	Receive Message Idle/Incorrect
	This bit is set, when four flags (FF_H) or no eight consecutive '1's are detected within 32 bits.

D3RINTC
Interrupt Status Register

Access : read

Address : $2A_H$

Reset Value : 0000_H

This register must be read after register D3RINTV and dependent on the content of register D3RINTV it contains a copy of register D3RSTAT, D2RSTAT or TURSTAT.

D3RINTL
Interrupt Loopback Code Status Register

Access : read

Address : $2C_H$

Reset Value : 0000_H

This register must be read after register D3RINTV and dependent on the content of register D3RINTV this register contains a copy of register D3RLPCS or D2RLPCS.

7.2.2 DS2 Control and Status Registers

D2TSEL
DS2 Transmit Group Select Register

Access : read/write

Address : 30_H

Reset Value : 00_H

7					2		0
0	0	0	0	0	GN(2:0)		

Note: This register is an indirect access register, which must be programmed before accessing the register DS2 transmit registers.

GN Group Number

This bit field selects the DS2 group, which can be accessed via the DS2 transmit registers.
Please refer to section **“Tributary Mapper” on Page 37** for a detailed description of the tributary mapper and to **Page 117** for programming examples.

0..6 Tributary Group Number.

7 Spare Line Group

D2TCFG
DS2 Transmit Configuration Register

Access : read/write

Address : 31_H

Reset Value : 00_H

7					2	1	0
0	0	0	0	0	LPC(1:0)		E1

LPC Loopback Code

This bit selects the C-bit which will be inverted when loopback requests are transmitted.

00 Invert 1^{st} C-bit.

01 Invert 2^{nd} C-bit.

10 Invert 3^{rd} C-bit.

E1 G.747 Select

This bit selects the operation mode of the low speed multiplexer.

0 Select M12 mode (4 DS1 into DS2).

1 Select ITU-T G.747 mode (3 E1 into DS2).

D2TCOM
DS2 Transmit Command Register

Access : read/write

Address : 32_H

Reset Value : 00_H

7 – 4	3 – 2	1	0
IAIS(3:0)	FINSC(1:0)	SRA	RES

IAIS Insert DS1/E1 AIS

Setting IAIS(x) enables transmission of the alarm indication signal in tributary x of the DS2 signal. AIS is an all ‘1’ signal.

- 0 Normal operation.
- 1 Insert AIS in low speed tributary x.

FINSC Fault Insertion Code

This bit enables transmission of faults for testing purposes.

- 0 No fault insertion.
- 1 Insert F-bit errors at low rate (2 out of 5 F-bits).
- 2 Insert F-bit errors at high rate (2 out of 4 F-bits).
- 3 Insert M-bit framing bit error (DS1 mode) or P-bit error (ITU-T G.747)

SRA Set Remote Alarm

This bit enables transmission of the DS3 remote alarm. In DS1 modes remote alarm is transmitted in subframe 4, block 1 overhead bit and in ITU-T G.747 remote alarm is transmitted in bit 2 of “set II”.

- 0 Normal operation.
- 1 Enable transmission of remote alarm.

RES ITU-T G.747 Reserved Bit

This bit sets the value to be transmitted in the reserved bit of ITU-T G.747 format.

- 0 Transmit reserved bit as ’0’.
- 1 Transmit reserved bit as ’1’.

D2TLPC
DS2 Transmit DS1/E1 Remote Loopback/Loopback Code Insertion Register

Access : read/write

Address : 33_H

Reset Value : 00_H

7 4	3 0
R2T(3:0)	LPC(3:0)

R2T DS2 Tributary Receive to Transmit Loop (remote loop)

Setting bit R2T(x) enables the remote loop for tributary x where the incoming tributary x is mirrored to the DS2 transmitter.

0 Disable remote loop.

1 Enable remote loop.

LPC Send Loopback Code for Tributary N

Setting LPC(x) enables transmission of the loopback code in tributary x. The loopback code inserted is specified in D2TCFG.LPC.

0 Disable transmission of loopback code.

1 Enable transmission of loopback code.

D2TTM0, D2TTM1, D2TTM2, D2TTM3
DS2 Transmit Tributary Map Register

Access	: read/write
Address	: 34_H, 35_H, 36_H, 37_H
Reset Value	: 00_H

7			4	0
0	0	0	TN(4:0)	

TN Tributary Number

A (transmit) tributary map register specifies the data and clock source for the seven M12 multiplexers and the four internal spare links (please refer to section **"Tributary Mapper" on Page 37** for a detailed description of the tributary mapper).

The M12 multiplexer to be programmed is selected via D2TSEL.GN. where GN can be in the range of 0..6. To program the four internal spare links GN must be set to 7.

Now each of the four inputs of the selected M12 multiplexer (or the four spare links) can be programmed by the four tributary map registers D2TTM0..3 (D2TTM0 programs the first input, .., D2TTM3 programs the fourth input). This process maps any of the incoming 32 inputs to the selected input of the M12 multiplexer.

After reset interfaces 1..32 are mapped to tributaries 1..32.

Example (please refer to Figure 7 on page 37):

The interface 14 (TTC(14), TTD(14)) shall be connected to tributary 7 (the third input of the second M12 multiplexer).

1. Write 01_H to D2TSEL.GN.
   This command selects the second M12 multiplexer (GN counts from 0..7).
2. Write $0D_H$ (= 13_D) to D2TTM2.TN.
   This command assigns interface 14 (TN counts from 0..31) to the third input of the second M12 multiplexer.

D2RSEL
DS2 Receive Group Select Register

Access : read/write

Address : 40_H

Reset Value : 00_H

7					2		0
0	0	0	0	0	GN(2:0)		

Note: This register is an indirect access register, which must be programmed before accessing the register DS2 transmit registers.

GN Group Number

This bit field selects the DS2 group number, which can be accessed via the DS2 receive registers.
Please refer to section **"Tributary Mapper" on Page 37** for a detailed description of the tributary mapper and to **Page 124** for programming examples.

0..7 Group Number.

D2RCFG
DS2 Receive Configuration Register

Access : read/write

Address : 41_H

Reset Value : 00_H

7				3	2	1	0
0	0	0	0	ECM	AAIS	MFM	FFM

Note: ITU-T G.747 mapping and loop back codes are controlled by bits E1 and LPC in the DS3 transmit configuration register D2TCFG.

DS1/E1 and loopback codes are controlled by E1 and LPC fields of the D2TCFG register.

ECM — Error Counter Mode

DS2 errors are counted in background and copied to foreground (error counter registers) when condition selected via ECM is met.

0 — Counter values are copied to foreground when copy command is executed. See also register DS3COM.

1 — The counter values are copied to the foreground register in one second intervals. At the same time the background registers are reset to zero. This operation is synchronous with the periodic one second interrupt which alerts software to read the register.

AAIS — Automatic AIS Insertion

This bit enables automatic insertion of AIS in downstream direction if DS2 framer OR DS3 framer is out of frame.

0 — Disable automatic insertion of AIS.

1 — Enable automatic insertion of AIS.

MFM — Multiframe Framing Mode

This bit selects the M-bit error condition which triggers the DS2 framer to start a new frame search. It is valid in DS1 mode only.

0 — F-frame search started if 3 contiguous multiframes have M-bit errors.

1 — Inhibit new F-frame search due to M-bit errors.

FFM	F-Framing Mode
	This bit selects the F-bit error condition which triggers the DS2 framer to start a new frame search.
	0 A new frame search is started when 2 out of 4 contiguous F-bits are in error.
	1 A new frame search is started when 2 out of 5 contiguous F-bits are in error.

D2RCOM
DS2 Receive Command Register

Access : read/write

Address : 42_H

Reset Value : 00_H

7	6		4			1	0
0	ESIMC(2:0)			0	0	C2NC	C2C

ESIMC — Error Simulation Code

This bit field enables error simulation. During error simulation the device generates error interrupts and error status messages. Nevertheless the service is not affected.

0 Normal operation (no error simulation)

1 Simulate 2 receive F-bit errors/multiframe (186 µsec)

2 Simulate
2 receive M-bit errors/multiframe (186 µsec) (DS-1 mode)
Receive parity error/multiframe (133 µsec) (ITU-T G.747 mode)

3 Simulate remote alarm

4 Simulate loss of frame (RED alarm timer)

Note: This simulation is service affecting if automatic AIS insertion is enabled.

5 Simulate AIS (AIS alarm timer)

6 Simulate receive loop command

C2NC — Copy DS2 Error Counters

Only valid when D2RCFG.ECM is set to ‘0’. Values of DS2 background registers are copied to foreground. Background registers are NOT cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

0 No operation.

1 Copy background counters to foreground.

C2C	Copy and Clear DS2 Error Counters Only valid when D2RCFG.ECM is set to ‘0’. Values of DS2 background registers are copied to foreground. Background registers are cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer. 0 No operation. 1 Copy background counters to foreground. Clear background counters.

D2RIMSK
DS2 Receive Interrupt Mask Register

Access : read/write

Address : 43_H

Reset Value : $3F_H$

7		5	4	3	2	1	0
0	0	LPCD	AISS	REDS	RES	RAS	FAS

This register provides the interrupt mask for DS2 status interrupts and DS2 loopback code interrupts. See register D2RSTAT and D2RLPCS for interrupt conditions.

The following definition applies:

1	The corresponding interrupt vector will not be generated by the device.
0	The corresponding interrupt vector will be generated.

LPCS	Mask 'Loopback Code Status' (flagged in D2RLPCS)
AIS	Mask 'AIS Alarm State'
REDS	Mask 'Red Alarm State'
RES	Mask 'Reserved Bit'
RAS	Mask 'DS2 Remote Alarm State'
FAS	Mask 'DS2 Frame Alignment State'

D2RTM0, D2RTM1, D2RTM2, D2RTM3
DS2 Receive Tributary Map Register

Access	: read/write
Address	: 44_H, 45_H,46_H, 47_H
Reset Value	: 00_H

7			4				0
0	0	0	TN(4:0)				

TN — Tributary Number

A (receive) tributary map register specifies the data and clock source for one of the 32 DS1/E1 outputs (please refer to section **"Tributary Mapper" on Page 37** for a detailed description of the tributary mapper).

The outputs are divided into eight groups where each group represents four consecutive output ports, i.e. 1..4, 5..8, .. , 29..32. The group to be programmed is selected via D2RSEL.GN.

Now each of the four outputs of the selected group can be programmed by the four tributary map registers D2RTM0..3. This process maps any of the incoming 28 tributaries of the DS3 signal or any of the four internal spare links to an output.

After reset interfaces 1..32 are mapped to tributaries 1..32.

Example (please refer to Figure 7 on page 37):

The interface 22 (RTC(22), RTD(22)) shall be connected to the tributary 7 (the third output of the second M12 demultiplexer).

1. Write 05_H to D2RSEL.GN.
   This command selects the output group 5 consisting of the output pins 21..24 and in this case the registers D2RTM0..D2RTM3 represent the output pins 21..24.
2. Write 06_H to D2RTM1.TN.
   This command assigns tributary seven (TN counts from 0..31) to output 22.

D2RLAIS
DS2 Receive Local DS1/E1 Loopback/AIS Insertion Register

Access : read

Address : 48_H

Reset Value : 00_H

7 ... 4	3 ... 0
IAIS(3:0)	T2R(3:0)

IAIS — Insert AIS

Setting bit x of bit field IAIS(x) enables insertion of AIS in tributary x of the demultiplexed DS2 signal in downstream direction.

0 No function.

1 Enable insertion of AIS in tributary x of demultiplexed DS2 tributary.

T2R — Enable loopback

Setting bit x of bit field T2R enables loopback from transmit to receive of tributary x (local loop of DS1/E1 tributary).

0 No loopback.

1 Enable loopback from transmit to receive.

D2RSTAT
DS2 Receive Status Register

Access : read

Address : 49_H

Reset Value : 00_H

7		5	4	3	2	1	0
0	0	AISS	REDS	RES	RAS	COFA	FAS

Each bit in the DS2 framer receive status register declares a specific condition dependent on the selected modes. The following convention applies to the individual bits:

0 The named status is not or no longer existing.

1 The named status is currently effective.

Except for COFA every bit can be used to generate an interrupt. Interrupts can be masked in register D2RIMSK.

AISS DS2 AIS Alarm State (unframed all ‘1’s pattern)

AIS is considered valid in a multiframe when fewer than 5 zeros are detected. At 10^{-3} error rates, 1 zero per multiframe is typical. A valid DS2 signal without any bit errors has at least 5 zeros.

The AIS flag nominally changes when the AIS condition is persistent as per alarm timing parameters defined in register D2RAP. The exact time necessary to change the flag could be greater in extremely high error rates. The AIS state is integrated by incrementing or decrementing a counter at the end of each multiframe depending on the AIS condition being valid or invalid respectively.

REDS DS2 Red Alarm State (loss of frame alignment).

The red alarm flag nominally changes when loss of frame alignment condition is persistent as per alarm timing parameters defined in register D2RAP. The exact time necessary to change the flag could be greater if the FAS flag is not constant because the frame alignment state is integrated by incrementing or decrementing a counter at the end of each multiframe when the FAS flag set or cleared respectively. Note that the framer's verification algorithm is designed to prevent a bouncing FAS flag.

RES	Reserved Bit This bit indicates the status of bit 3 in set II of ITU-T G.747 mode. Is it updated if the DS2 framer is aligned and when its state persists for at least 8 multiframes.
RAS	DS2 Remote Alarm State This bit indicates that remote alarm is active. Changes are reported when they persist for 3 multiframes. In DS1 mode changes on M_X bit are reported, in ITU-T G.747 mode changes of bit 1 of set II are reported.
COFA	Change of Frame Alignment This bit indicates a change of frame alignment event. It is set when the DS2 framer found a new frame alignment and when the new frame position differs from the expected frame position.
FAS	DS2 Frame Alignment State This bit indicates that the DS2 framer is not aligned.

D2RLPCS
DS2 Receive Loopback Code Status Register

Access	: read
Address	: $4A_H$
Reset Value	: 00_H

7				3 0
0	0	0	0	LPCD(3:0)

LPCD(N) Loopback Command Detected

LPCD(x) indicates that a loopback request was received. A loopback request for tributary x is indicated by inverting one of the 3 C-bits of the x^{th} subframe. The C-bit is determined by D2TCFG.LPC. A command state change must persist for 5 contiguous multiframes before it will be reported.

0 No loopback code being received.

1 Loopback code being received.

D2RAP
DS2 Receive Alarm Timer Parameters

Access : read/write

Address : $4B_H$

Reset Value : 00_H

7	6	5 ... 0
AIS	CM	CV(5:0)

AIS — AIS criteria

This bits sets the error rate for AIS detection. Declaration of AIS is specified by bits CM and CV.

ITU-T G.747:

0 AIS condition is recognized when the alarm indication signal is received with less than 5 errors in each of 2 consecutive multiframes.

1 AIS condition is recognized when the alarm indication signal is received with less than 9 errors in each of 2 consecutive multiframes.

M12 format:

0 AIS condition is recognized when the alarm indication signal is received with less than 3 errors in 3156 bits.

1 AIS condition is recognized when the alarm indication signal is received with less than 9 errors in 3156 bits.

CM — Counter Mode

This bit selects the alarm timer mode. If counter mode is set to multiframes (‘0’) the value in CV determines the number of multiframes after which the TE3-MUX declares AIS or RED. When counter mode is set to ‘½ milliseconds’ (‘1’) the value in CV determines the time in CV x 0.5 ms after which AIS or RED is declared.

0 Multiframes.

1 ½ Milliseconds.

CV	Counter Value
	Dependent on bit CM the counter value specifies the number of frames or the time in multiples of 0.5 milliseconds when AIS or RED is declared, i.e. setting CV to 20 and CM to '1' sets the alarm integration time to 10 milliseconds.
	0..63 Counter Value.

D2RFEC
DS2 Receive Framing Bit Error Counters

Access	: read/write
Address	: $4C_H$
Reset Value	: 0000_H

15	0
FE(15:0)	

FE(15:0) Framing Bit Errors

Error counter mode (Clear on Read or Errored Second) depends on register D2RCFG.ECM.

For DS1 mode framing bit errors include F-bit and M-bit errors. For G747 mode, individual bits in the Frame Alignment Signal (FAS) are counted. Errors are not counted in out of frame state.

D2RPEC
DS2 Receive Parity Bit Error Counter

Access	: read/write
Address	: $4E_H$
Reset Value	: 0000_H

15	0
PE(15:0)	

PE(15:0) Parity Errors in ITU-T G.747 mode

Error counter mode (Clear on Read or Errored Second) depends on register D2RCFG.ECM. Errors are not counted in out of frame state.

7.2.3 Test Unit Registers

TUTCFG
Test Unit Transmit Configuration Register

Access : read/write

Address : 50_H

Reset Value : 0000_H

15		13	12					8	6				2	1	0
0	0	INV	FBT(4:0)					0	LEN(4:0)					ZS	MD

INV Invert output

This bit enables inversion of the test unit output. Bit inversion is done after the zero suppression insertion point.

0 No inversion

1 Invert pattern generator output

FBT Feedback Tap

This bit field sets the feedback tap in pseudorandom pattern mode. PRBS shift register input bit 0 is XOR of shift register bits LEN and FBT.

LEN Pattern Generator Length

This bit field sets the pattern generator length to 1..32.

ZS Enable Zero Suppression

This bit enables zero suppression where a ’1’ bit is inserted at the output if the next 14 bits in the shift register are ’0’.

0 No zero suppression

1 Zero suppression.

MD Generator Mode

This bit selects the generator mode of the test unit to be either PRBS or fixed pattern mode.

0 Pseudorandom Pattern (PRBS)

1 Fixed Pattern

TUTCOM
Test Unit Transmit Command Register

Access : write

Address : 52_H

Reset Value : 00_H

7				3	2	1	0
0	0	0	0	LDER	IN1E	STOP	STRT

Note: All commands are self clearing i.e. user does not have to clear command. The maximum command rate is limited by clock rate of unit under test and the associated synchronization process. Write interval should be > 4 transmit clock periods e.g. 2.6 µs for DS1 tributary test or 634 ns for T2 tributary test.

LDER — Load Error Rate Register

This bit loads the value of the error rate register TUTEIR to the test unit transmitter. The command can be given while the transmitter is running.

0 No function.

1 Copy value of register TUTEIR to transmit clock region.

IN1E — Insert One Error in Output

This bit enables a single error insertion in the next bit after command was written.

0 No function

1 Single error insertion.

STOP — Stop Pattern Generation.

This bit stops the test unit transmitter. When stopped output becomes all '1'.

0 No function.

1 Stop pattern generation.

STRT Start Transmitter.

This bit starts the test unit transmitter with the parameters defined in register TUTCFG. In fixed pattern mode the pattern needs to be programmed via register TUTFP0/1 prior to starting the transmitter.

0 No operation.

1 Start test unit.

TUTEIR
Test Unit Transmit Error Insertion Rate Register

Access : read/write
Address : 53_H
Reset Value : 00_H

7				3	2		0
0	0	0	0	MTST	TXER(2:0)		

MTST Manufacturing test.
Must be written to '0' for normal operation.

TXER Transmit Error Insertion Rate.
This bit field determines the error insertion rate of the test unit transmitter.

000	No errors	
001	10^{-1} (1 in	10)
010	10^{-2} (1 in	100)
011	10^{-3} (1 in	1 000)
100	10^{-4} (1 in	10 000)
101	10^{-5} (1 in	100 000)
110	10^{-6} (1 in	1 000 000)
111	10^{-7} (1 in	10 000 000)

TUTFP0
Test Unit Transmit Fixed Pattern Low Word

Access : read/write
Address : 54_H
Reset Value : 0000_H

15	0
FP(15:0)	

FP — Fixed Pattern Low Word
See description below.

TUTFP1
Test Unit Transmit Fixed Pattern High Word

Access : read/write
Address : 56_H
Reset Value : 0000_H

15	0
FP(31:15)	

FP — Fixed pattern High Word
The 32 bit fixed pattern is distributed over two 16 bit registers and contains the pattern which is transmitted repetitively from bit FP(TUTCFG.LEN) down to FP(0) when test unit is operated in fixed pattern generator mode.

TURCFG
Test Unit Receive Configuration Register

Access : read/write

Address : 58_H

Reset Value : 0000_H

15		13	12 … 8		6 … 2	1	0
AIM	0	DAS	FBT(4:0)	0	LEN(4:0)	ZS	MD

AIM Auxiliary Interrupt Mode

This bit field enables the auxiliary interrupt mask AIM of register TURIMSK. In normal operation and if not masked every status event generates an interrupt event. In auxiliary interrupt mode an individual status event generates one interrupt event and further status events of the same class, i.e. 'Bit Error Detected', are masked via an internal mask. This prevents excessive interrupt floods. See register TURIMSK for further details.

0 Normal Operation

1 Auxiliary Interrupt Mode

DAS Disable Automatic Synchronization

This bit disables automatic resynchronization in case of high bit error rates. If automatic resynchronization is enables the receiver automatically tries to resynchronize to the received test pattern.

0 Enable automatic resynchronization.

1 Disable automatic resynchronization.

FBT Feedback Tap

This bit field sets the feedback tap of the test unit synchronizer (receiver) in pseudorandom pattern mode. Next input to PRBS reference shift register (bit 0) is XOR of shift register bits LEN and FBT.

LEN Reference shift register length

This bit field sets the length of the receiver's test pattern register.

ZS Enable Zero Suppression

This bit enables zero suppression at the test unit receiver. A ’1’ is expected and inserted at the input if the next 14 bits in the shift register are set to ’0’.

0 No zero suppression.

1 Enable zero suppression.

MD Generator Mode

This bit sets the generator mode of the test unit to either PRBS or fixed pattern.

0 Pseudorandom Pattern (PRBS)

1 Fixed Pattern

TURCOM
Test Unit Receive Command Register

Access : write

Address : $5A_H$

Reset Value : 00_H

7		5	4	3	2	1	0
0	0	FRS	RDF	RDC	CAIM	STOP	STRT

Note: All commands are self clearing i.e. user does not have to clear command. The maximum command rate is limited by clock rate of unit under test and the associated synchronization process. Write interval should be > 4 transmit clock periods e.g. 2.6 µs for DS1 tributary test or 634 ns for T2 tributary test.

FRS — Force resynchronization.

This bit forces the receiver to resynchronize to the received bit stream. Only applicable if **TURCFG.DAS = ’1’.**

0 No function.

1 Force resynchronization of receiver.

RDF — Copy Receiver’s 32 bit Pattern

This bit loads the test units internal receiver pattern to register TURFP in fixed pattern mode. In synchronous state TURFP will be loaded with the pattern received. In asynchronous state TURFP with a 32-bit sample of the last received bit stream.

0 No function.

1 Update register TURFP with synchronizer pattern.

RDC — Copy bit counter and error counter

This bit loads the test units internal bit counter and error counter to registers TURBC0,1 and TUREC0,1. Afterwards the bit counter and the error counter is cleared.

0 No function.

1 Copy counter.

CAIM	Clear Auxiliary Interrupt Masks.
	This bit resets the internal auxiliary mask. See TURCFG.AIM.
	0 No operation
	1 Clear auxiliary interrupts
STOP	Stop Receiver
	Setting this bit stopes the test unit receiver.
STRT	Start Receiver.
	This bit loads and starts the test unit receiver with the parameters defined in register TURCFG.
	0 No operation.
	1 Load/Start test unit receiver.

TURERMI
Test Unit Receive Error Measurement Interval Register

Access : read/write

Address : $5B_H$

Reset Value : 00_H

7				3	2	0
0	0	0	0	TST	RXMI(2:0)	

TST — Test Mode

This bit enables test of the measurement interval timer.

0 Normal operation

1 Auto test of measurement interval function. End of Measurement interrupt should be asserted after approximately 4250 receive clock cycles (if enabled). The lower three bits of register FPAT should be “111”.

RXMI — Receive Error Rate Measurement Interval

This bit field defines the measurement interval in terms of input bits for measurement of receive bit error rate.

At the end of the measurement window, contents of background error counter are automatically copied to foreground error counter and reset for next measurement interval. An interrupt can be generated at the end of each measurement interval.

000_B Max measurement interval of 2^{32}-1

001_B 10^3 bits

010_B 10^4 bits

011_B 10^5 bits

100_B 10^6 bits

101_B 10^7 bits

110_B 10^8 bits

111_B 10^9 bits

TURIMSK
Test Unit Receive Interrupt Mask Register

Access	: read/write
Address	: $5C_H$
Reset Value	: $1F1F_H$

15	14	13	12–8	7	6	5	4	3	2	1	0
0	0	0	AIM(4:0)	0	0	0	ERXM	BED	ALL1	LOS	SYN

This register provides the interrupt mask for test unit interrupts. See register TURSTAT.

The following definition applies:

1	The corresponding interrupt vector will not be generated by the device.
0	The corresponding interrupt vector will be generated.

ERXM	Mask 'End of Receive Error Rate Measurement'
BED	Mask 'Bit Error Detected'
ALL1	Mask 'All '1' Pattern Received'
LOS	Mask 'Loss of Signal'
SYN	Mask 'Change in Receiver Synchronization State'

AIM flags have same layout as the above five mask but are internal masks that are set automatically following the interrupt in the AIM mode. This mask prevents excessive bus load in error conditions. AIM flags are cleared by the **TURCOM.CAIM** command. They are “read only” flags in this register.

TURSTAT
Test Unit Receive Status Register

Access : read

Address : $5E_H$

Reset Value : 0001_H

15							8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	INVS	LA1	LA0	LOOS	EMI	LBE	A1	A0	OOS

INV — Inverted Pattern

This bit indicates that the received PRBS sequence is inverted.

0 Not Inverted.

1 Inverted.

LA1 — Latched 'Input all '1''

This bit indicates that the condition 'Input all '1'' was active since last status register read.

LA0 — Latched 'Input all '0''

This bit indicates that the condition 'Input all '0'' was active since last status register read.

LOOS — Latched Out of Synchronization.

This bit indicates that the receiver was out of synchronization since last status register read.

EMI — End of Measurement Interval

This bit indicates that the end of the measurement internal was reached since last read of error counter or that command TURCMD.RDC was given. The results of the bit error rate test are available in register TURBC0,1 and TUREC0,1. This flag is cleared when the error counter is read. Counters will not be overwritten while EMI is '1'.

LBE — Latched Bit Error Detected Flag.

This bit indicates that at least '1' one bit error occurred since last read of this register. It is cleared by status register read.

A1 — Input all '1's

This bit indicates that the input contained all '1' during the last 32 bits. It is reset if at least one '0' occurs in 32 bits.

A0 Input all ‘0’s

This bit indicates that the input contained all ’0’ during the last 32 bits. It is reset if at least one ’1’ occurs in 32 bits.

OOS Receiver Out of Synchronization

This bit indicates the status of the test unit synchronizer.

TURBC0
Test Unit Receive Bit Counter Low Word

Access : read
Address : 60_H
Reset Value : 0000_H

15	0
BC(15:0)	

BC(31:0) Bit Counter

See description below.

TURBC1
Test Unit Receive Bit Counter High Word

Access : read
Address : 62_H
Reset Value : 0000_H

15	0
BC(31:16)	

BC(31:0) Bit Counter

BC is a 32 bit counter which is split between two 16 bits registers. It counts receive clock slots when the receiver is enabled. Bits are counted in a background register which is not directly readable. The values are transferred to the two 16 bit foreground (readable) registers and cleared in one of the two ways:

1. Assert command TURCOM.RDC.
2. Automatically at end of measurement interval.

The background register is transferred to the foreground register and cleared in the same way as the bit error counter (see previous section).

When the error registers are read in response to the “End of Measurement Interval” interrupt vector, reading this register is not necessary because the measurement interval would be known. However the user could assert command TURCOM.RDC to terminate the measurement interval early and transfer the current bit error count and bit count to the foreground registers (polling mode).

TUREC0
Test Unit Receive Error Counter Low Word

Access	: read
Address	: 64_H
Reset Value	: 0000_H

15	0
EC(15:0)	

EC(31:0) Error Counter

See description below.

TUREC1
Test Unit Receive Error Counter High Word

Access	: read
Address	: 66_H
Reset Value	: 0000_H

15	0
EC(31:16)	

EC(31:0) Error Counter

This 32 bit counter counts receive errors detected when receiver is enabled and in synchronized state. When the 'Bit Error Detected' interrupt is enabled, it will be asserted and then automatically masked when this counter is incremented.

Errors are counted in a background register (not directly readable) until:
1. The user asserts command TURCOM.RDC.
2. The end of measurement interval is reached and the last result was read.

In both cases the value of the background register is copied to TUREC.EC and the measured values are accessible. An 'End of

Receive Error Rate Measurement' interrupt vector is optionally generated.

TURFP0
Test Unit Receive Fixed Pattern Low Word

Access : read

Address : 68_H

Reset Value : 0000_H

15	0
FP(15:0)	

FP(31:0) Fixed pattern

See description below.

TURFP1
Test Unit Receive Fixed Pattern High Word

Access : read

Address : $6A_H$

Reset Value : 0000_H

15	0
FP(31:16)	

FP(31:0) Fixed Pattern

This 32 bit field is distributed over two 16 bit registers and is used in the fixed pattern mode (TURCFG.MD='1'). The TURCOM.RDF command will copy the current state of the receiver's 32 bit pattern generator to this register. If the receiver is synchronized, bits FP(TURCFG.LEN:0) contain the fixed pattern being received. Bit 0 is the most recently received. If not synchronized, the register contains a 32 bit sample of input data.

7.2.4 Test Unit Framer Registers

TUTFCFG
Test Unit Transmit Framer Configuration Register

Access : read/write

Address : 70_H

Reset Value : 00_H

7			4	3	2	1	0
0	0	0	OM	SRAF	FM	T1E1	EF

OM — Overwrite mode

This bit enables test pattern overwrite mode. While in overwrite mode the generated PRBS sequence will be overwritten by the frame bits. When overwrite is disabled the generated PRBS sequence is placed into the payload field of the DS1/E1 signal.

0 Disable overwrite mode.

1 Enable overwrite mode.

SRAF — Select Remote (Yellow) Alarm Format

Setting this bit enables the remote alarm format in DS1 mode. This bit has no function in E1 mode.

DS1: F12

0 Bit 2 = 0 in every channel.

1 FS bit of frame 12.

FM — Framer Mode

This bit selects the frame format of DS1 or E1 mode.

DS1

0 Select ESF (F24) format.

1 Select SF (F12) format.

E1

0 Select double frame format.

1 Select multiframe format.

T1E1	Select DS1/E1 mode	
	This bit switches between DS1 and E1 mode.	
	0	Select DS1 mode.
	1	Select E1 mode.
EF	Enable framer	
	This bit enables the framer for framed DS1/E1 error insertion mode.	
	0	Disable framer. (Unframed bit error rate test)
	1	Enable framer. (Framed bit error rate test)

TUTFCOM
Test Unit Transmit Framer Command Register

Access : read/write
Address : 71_H
Reset Value : 00_H

7				3	2	1	0
0	0	0	0	EBIT	CRC	FE	RA

EBIT Set active E-bit (E1 mode)
This bit inserts an active E-bit. EBIT is self clearing.
0 Normal operation.
1 Set active E-bit.

CRC Insert CRC error
This bit enables insertion of CRC error. CRC is self clearing.
0 Normal operation.
1 Insert CRC error.

FE Insert frame error
This bit enables insertion of framing errors. FE is self clearing.
0 Normal operation.
1 Insert frame error.

RA Send remote alarm
This bit enables insertion of remote alarm.
0 Disable remote alarm.
1 Send remote alarm.

TURFCFG
Test Unit Receive Framer Configuration Register

Access : read/write

Address : 74_H

Reset Value : 00_H

7			4	3	2	1	0
0	0	0	OM	RRAM	FM	T1E1	EF

OM Overwrite mode

This bit enables test pattern overwrite. In overwrite mode the test unit discards the generated bits while the F-bit (DS1 mode) respectively time slot 0 (E1 mode) is received. When overwrite mode is disabled the complete test pattern is expected in the payload of the frame.

0 Disable overwrite mode.

1 Enable overwrite mode.

RRAM Receive Remote Alarm Mode

The condition for remote (yellow) alarm detection in DS1-SF mode can be selected via this bit. Remote alarm detection is flagged in register TURFSTAT.RRA.

0 Detection:
Bit 2 = ‘0’ in every speech channel per frame.

Release:
The alarm will be reset when above conditions are no longer detected.

1 Detection:
FS-bit of frame 12 is forced to ‘1’.

Release:
The alarm will be reset when above conditions are no longer detected.

FM Framer Mode

This bit selects the frame format of DS1 or E1 mode.

DS1

0 Select ESF (F24) format.

1 Select SF (F12) format.

E1

0 Select double frame format.

1 Select multiframe format.

T1E1 Select DS1/E1 mode

This bit switches between DS1 and E1 mode.

0 Select DS1 mode.

1 Select E1 mode.

EF Enable framer

This bit enables the framer for framed DS1/E1 error detection mode.

0 Disable framer. (Unframed DS1/E1 bit error rate test)

1 Enable framer. (Framed DS1/E1 bit error rate test)

TURFCOM
Test Unit Receive Framer Command Register

Access : read/write

Address : 75_H

Reset Value : 00_H

7							0
0	0	0	0	0	0	0	CC

CC — Copy and Clear Framer Error Counters

Values of framer background registers are copied to foreground. Background registers are cleared. Command is self clearing and completes before next register access is possible i.e. software can write command and then immediately read the counters without starting a delay timer.

0 No operation.

1 Copy background counters to foreground. Clear background counters.

TURFSTAT
Test Unit Receive Framer Status Register

Access : read

Address : 76_H

Reset Value : 00_H

7						1	0
0	0	0	0	0	0	RRA	LFA

RRA Received Remote Alarm (Yellow Alarm)

Condition for receive remote alarm is defined by bit TURFCFG.RRAM. The flag is set after detecting remote alarm (yellow alarm).

LFA Loss of Frame Alignment

This bit reports loss of frame alignment.

In DS1 mode loss of frame alignment is reported when 2 out of 4 framing bit errors are detected.

TURFFEC
Test Unit Receive Framing Error Counter

Access	: read
Address	: 78_H
Reset Value	: 00_H

15 … 0
FE(15:0)

FE Framing Error Counter

The counter will not be incremented during asynchronous state. The error counter is cleared on read.

DS1: F12

The counter will be incremented when incorrect FT and FS bits are received.

DS1: ESF

The counter will be incremented when incorrect FAS bits are received.

E1

The counter will be incremented when incorrect FAS words are received.

TURFCEC
Test Unit Receive Framer CRC Error Counter

Access : read

Address : $7A_H$

Reset Value : 00_H

15	0
CR(15:0)	

CR CRC Errors

The counter will not be incremented during asynchronous state. The error counter is cleared on read.

DS1: F12

No function.

DS1: ESF

The counter will be incremented when a multiframe has been received with a CRC error.

E1: Doubleframe

No function.

E1: CRC-4 Multiframe

In CRC-4 multiframe mode the counter will be incremented when a submultiframe has been received with a CRC error.

TURFEBC
Test Unit Receive Framer Errored Block Counter

Access : read

Address : $7C_H$

Reset Value : 00_H

15 ... 0
EB(15:0)

EB E-Bit counter

The counter will not be incremented during asynchronous state. The error counter is cleared on read.

DS1

No function.

E1: Doubleframe

No function.

E1: CRC-4 Multiframe

The counter will be incremented each time the framer receives a CRC-4 multiframe with S_i bit in frame 13 or frame 15 set to zero.

7.2.5 Far End Alarm and Control Channel (BOM) Registers

FRCFG
FEAC Receive Configuration Register

Access : read/write

Address : 80_H

Reset Value : 0000_H

15								7 6				2	1	0
0	0	0	0	0	0	0	0	RTF(1:0)	0	0	0	BFE	BRM	RON

RTF RFIFO Threshold Level

This bit field sets the threshold of the receive FIFO and is applied to both pages of the receive FIFO. A 'Receive Pool Full' interrupt vector will be generated, when the programmed threshold is reached. The threshold value is given as follows:

00_B 32 byte threshold

01_B 16 byte threshold

10_B 4 byte threshold

11_B 2 byte threshold

BFE Enable BOM Filter Mode

This bit selects, that byte oriented messages have to be filtered. The BOM is reported only if 7 out 10 data is received.

0 Disable BOM filter mode.

1 Enable BOM filter mode.

BRM BOM Receive Mode

This bit switches between continuous and 10 byte packet reception of the receive signalling controller. In 10 byte packet mode a receive FIFO full interrupt is generated after 10 bytes. In continuous reception mode a receive message interrupt is generated when the receive FIFO threshold level is reached.

0 Enable 10 byte packets.

1 Enable continuous reception.

RON Receiver On/Off

This bit switches the receiver of the Far End Alarm and Control channel to operational (on) or inoperational state (off).

It is recommended to issue a 'Receive Message Complete' command after the receiver was initialized (FHND.RMC = '1') in order to clear arbitrary receive FIFO contents.

0 Switch receiver off.

1 Switch receiver on.

FRFF
FEAC Receive FIFO Register

Access : read
Address : 82_H
Reset Value : 0000_H

15								7							0
RFIFO(15:0)															
0	0	0	0	0	0	0	0	RFIFO(7:0)							

RFIFO — Receive FIFO Data

This bit field contains the first 16 bit word of the receive FIFO of the signalling controller. The receive FIFO itself consists of two pages with 32 bytes. One page is always used in background and is not visible to the microprocessor. The microprocessor sees one FIFO of 32 bytes only. Thus a maximum of 16 words is stored inside the receive FIFO at a time. Data stored in the receive FIFO can be read in 8- or 16-bit accesses. Nevertheless if the port status register indicates an odd byte count the higher byte of the last word is not valid. Port status and FIFO operations can be accessed via register FPSR and register FHND.

The first bit received is stored in bit 0.

FXCFG
FEAC Transmit Configuration Register

Access : read/write

Address : 84_H

Reset Value : 00_H

7							0
0	0	0	0	0	0	0	XON

XON Transmitter On/Off

This bit switches the transmitter of the facility data link to operational (on) or inoperational state (off).

0 Switch transmitter off.

1 Switch transmitter on.

FXFF
FEAC Transmit FIFO

Access : write
Address : 86_H
Reset Value : 0000_H

15								7	0
XFIFO(15:0)									
0	0	0	0	0	0	0	0	XFIFO(7:0)	

XFIFO Transmit FIFO Data

This bit field contains the first 16 bit word of the transmit FIFO of the signalling controller. The transmit FIFO itself consists of two pages with 32 bytes. One page is always used in background and is not visible to the microprocessor. The microprocessor sees one FIFO of 32 bytes only. Thus a maximum of 16 words can be stored inside the transmit FIFO at a time. Data stored in the transmit FIFO can be written in 8- or 16-bit accesses. Nevertheless if the user wants to transfer an odd number of bytes the last access to the transmit FIFO register must be a byte access. Port status and FIFO operations can be accessed via register FPSR and register FHND.

Data written to the transmit FIFO is sent starting with bit 0 up to bit 15.

Note: The FEAC transmitter does not automatically insert 'FF' between message bytes. The 'FF' bytes have to be provided as part of the message to be transmitted. Thus messages stored in the transmit FIFO must have the following structure: $11111111_B 0XXXXXX0_B$.

Note: *If the transmit FIFO is not completely filled (32 bytes stored in the FIFO page) the transmitter may insert gaps between the packet stored in the current FIFO page and the packet stored in the following FIFO page. Thus in order to sent BOM sequences longer than 32 bytes the transmit FIFO has to filled in blocks of 32 bytes except for the last part of the sequence which may not completely occupy a FIFO page.*

FPSR
FEAC Port Status register

Access : read
Address : 88_H
Reset Value : 2000_H

15	14	13	12				8		5	4				0
0	XRA	XFW	RBC(4:0)					-	-	BRFO	STAT(4:0)			

XRA Transmit Repeat Active

This bit indicates that the transmit signalling controller is operating in repeat mode.

0 Normal operation

1 Repeat operation

XFW Transmit FIFO Write Enable

This bit indicates that data can be written to XFF.XFIFO. This bit is for polling use with the same meaning as the 'Transmit Pool Ready' interrupt vector.

RBC Receive Byte Count

This bit field indicates the amount of data stored in the receive FIFO. Valid after a 'Receive Message End' interrupt vector is generated. Receive byte count will be cleared, when a 'Receive Message Clear' command is executed via register HND.

Note: A zero byte count in combination with a 'Receive Pool Full' or 'Receive Message End' interrupt vector means that 32 bytes are available in the receive FIFO. However evaluating RBC is not necessary when the 'Receive Pool Full' interrupt was received.

BRFO BOM Receive FIFO Overflow

0 No overflow

1 RFF overflow

The status word will be cleared after a 'Receive Message Clear' command is issued.

STAT Receive FIFO Status

This bit field reports the status of the data stored in the receive FIFO.

00000_B BOM Filtered Data Declared

This status is reported when ‘BOM Filtered Data’ is enabled, and 7 out of 10 BOM data are received (see also register bit FRCFG.BFE).

00001_B BOM Data Available

BOM data received is continuously written to the receive FIFO. If '10 byte packet mode' is enabled then this status byte is sent after 10 bytes are written into fifo. Otherwise, whenever the receive fifo is full, this status byte is generated.

00010_B BOM 7E

This status reported when the HDLC flag $7E_H$ was detected.

00011_B BOM Filtered Data Undeclared

This is sent only if 'BOM FIltered Mode' is enabled. This is sent whenever 3 valid BOM data is received but all these data is not same as the BOM data for which the status 'BOM Filtered Data declared' was sent earlier. Basically, this means that 7 out of 10 condition is no longer valid. This status is useful, when BOM data pattern changes from one valid pattern to another and BOM Filtered data is enabled.

00100_B BOM Idle

This message is generated when the receiver was not able to detect a BOM message in the last 32 bits, e.g. the idle pattern (all ‘1’) was sent.

FHND
FEAC Handshake Register

Access : write

Address : $8A_H$

Reset Value : 0000_H

15							8		6	5	4			1	0
0	0	0	0	0	0	0	RMC	0	0	XRES	XREP	0	0	XTF	XME

Note: Receive command (bit 8) and transmit commands (bit 5 down to bit 0) can not be issued at the same time. Doing so will cause the facility data link to omit the transmit commands.

RMC Receive Message Complete

This bit is a confirmation from CPU that a data block has been read from RFIFO following a 'Receive Pool Full' or 'Receive Message End' interrupt vector and that the occupied page can now be released.

Note: If this bit is set, the low byte (transmit commands) of the register HND is ignored.

0 No function

1 Release page of receive FIFO.

XRES Transmitter Reset

This bit resets the signalling controller transmit. However, the contents of the control register will not be reset.

0 Normal operation

1 Transmitter reset

XREP Transmission Repeat

Setting this bit together with bit XTF indicates that the contents stored in XFF.XFIFO shall be repeatedly transmitted by the TE3-MUX.

0 No cyclic transmission.

1 Enable cyclic transmission.

XTF Transmit transparent frame

Setting this bit indicates that the contents written to XFF.XFIFO shall be transmitted in transparent mode.

	0	No function
	1	Transmit data stored in XFF.XFIFO fully transparent, i.e. without bit stuffing and CRC.

XME — Transmit Message End

Setting this bit indicates that the last data block written to XFF.XFIFO completes the current message.

Table 8 Far End Alarm and Control Transmit Commands

XRES	XREP	XTF	XME	Function
1	-	-	-	**Reset Port**
0	0	1	0	**Start Transmission** Send FIFO content in BOM channel.
0	0	1	1	**Stop Transmssion** Stop transmission of FIFO contents. Transmission ends when content of transmit FIFO has been sent completely.
0	1	1	0	**Start Transmission, Enable automatic Repetition** Send FIFO content BOM channel. Automatically repeat transmission of FIFO content.
0	1	1	1	**Stop Transmission, Disable Automatic Repetition** Stop transmission after last byte stored in FIFO has been sent. This command is issued when transmission started by command '**Start Transmission, Enable automatic Repetition**' shall be stopped.

FMSK
FEAC Interrupt Mask Register

Access	: read/write
Address	: $8C_H$
Reset Value	: 00_H

7		5	4	3	2	1	0
0	0	ALLS	XDU	XPR	RPF	RME	RMI

For each facility data link interrupt vector an interrupt vector generation mask is provided. Generation of an interrupt vector itself does not necessarily result in assertion of the interrupt pin. For description of interrupt concept refer to section **"Interrupt Interface" on Page 62**.

The following definition applies:

1	The corresponding interrupt vector will not be generated by the device.
0	The corresponding interrupt vector will be generated.

Facility Data Link Interrupt Vector Transmit

ALLS	Mask 'All Sent'
XDU	Mask ''Transmit Data Underrun'
XPR	Mask 'Transmit Pool Ready'

Facility Data Link Interrupt Vector Receive

RPF	Mask 'Receive Pool Full'
RME	Mask 'Receive Message End'
RMI	Mask 'BOM Idle'

7.2.6 C-Bit Path Maintenance (HDLC) Registers

PRCFG
HDLC Receive Configuration Register

Access : read/write

Address : 90_H

Reset Value : 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	RMCP	DRRP	DMA	RTF(1:0)		0	INV	RIFTF	XCRC	CRC DIS	RON

RMCP $\overline{RMC}$ Polarity

This bit sets the polarity of the $\overline{RMC}$ signal.

0 Set polarity to active low.

1 Set polarity to active high.

DRRP $\overline{DRR}$ Polarity

This bit sets the polarity of the $\overline{DRR}$ signal.

0 Set polarity to active low.

1 Set polarity to active high.

DMA Activate DMA

This bit enables the DMA functionality of the C-bit parity Path Maintenance Data Link receiver. While DMA is active new data is indicated by an asserted DRR signal. The end of a message is indicated by an asserted $\overline{RMC}$ signal.

0 Disable DMA.

1 Enable DMA.

RTF RFIFO Threshold Level

This bit field sets the threshold of the receive FIFO and is applied to both pages of the receive FIFO. A 'Receive Pool Full' interrupt vector will be generated, when the programmed threshold is reached. The threshold value is given as follows:

00_B 32 byte threshold

01_B 16 byte threshold

10_B 4 byte threshold

11_B 2 byte threshold

INV Invert data input from Receive Framer

This bit enables data inversion between receive framer and receive signalling controller.

0 Disable data Inversion.

1 Enable data inversion.

RIFTF Report Interframe Time-fill Change

This bit selects, that interframe time-fill changes should be reported.

0 Disable IFF status messages.

1 Enable IFF status messages.

XCRC Transfer CRC to RFIFO

This bit defines, that CRC of incoming data packets shall be transferred to the receive FIFO or not.

0 No transfer of CRC to RFIFO.

1 Transfer of CRC to RFIFO.

CRCDIS CRC Check Disable

This bit enables or disables the CRC check of incoming data packets.

0 Enable CRC check.

1 Disable CRC check.

RON Receiver On/Off

This bit switches the receiver of the facility data link channel to operational (on) or inoperational state (off).

It is recommended to issue a ’Receive Message Complete’ command after the receiver was initialized (PHND.RMC = ‘1’) in order to clear arbitrary receive FIFO contents.

0 Switch receiver off.

1 Switch receiver on.

PRFF
HDLC Receive FIFO Register

Access : read
Address : 92_H
Reset Value : 0000_H

15								7							0
RFIFO(15:0)															
0	0	0	0	0	0	0	0	RFIFO(7:0)							

RFIFO Receive FIFO Data

This bit field contains the first 16 bit word of the receive FIFO of the signalling controller. The receive FIFO itself consists of two pages with 32 bytes. One page is always used in background and is not visible to the microprocessor. The microprocessor sees one FIFO of 32 bytes only. Thus a maximum of 16 words is stored inside the receive FIFO at a time. Data stored in the receive FIFO can be read in 8- or 16-bit accesses. Nevertheless if the port status register indicates an odd byte count the higher byte of the last word is not valid. Port status and FIFO operations can be accessed via register PPSR and register PHND.

The first bit received is stored in bit 0.

PXCFG
HDLC Transmit Configuration Register

Access : read/write

Address : 94_H

Reset Value : 0000_H

15					10	9	8	7				3	2	1	0
0	0	0	0	0	TXMEP	DRTP	DMA	0	0	0	0	INV	DIS CRC	SF	XON

TXMEP — $\overline{\text{TXME}}$ Polarity

This bit sets the polarity of the $\overline{\text{TXME}}$ signal.

0 Set polarity to active low.

1 Set polarity to active high.

DRTP — $\overline{\text{DRT}}$ Polarity

This bit sets the polarity of the $\overline{\text{DRT}}$ signal.

0 Set polarity to active low.

1 Set polarity to active high.

DMA — Activate DMA

This bit enables the DMA functionality of the C-bit parity Path Maintenance Data Link transmitter. While DMA is active a data request is indicated by an asserted $\overline{\text{DRT}}$ signal. The end of a message is indicated by the user with an asserted $\overline{\text{TXME}}$ signal.

0 Disable DMA.

1 Enable DMA.

INV — Invert Data

This bit enables data inversion between transmit signalling controller and transmit framer.

0 Disable data Inversion.

1 Enable data inversion.

DISCRC	Disable CRC	
	This bit enables CRC generation and transmission on transmission of HDLC packets.	
	0	Enable CRC generation.
	1	Disable CRC generation.
SF	Shared Flags	
	This bit enables transmission of protocol data with shared flags.	
	0	Disable shared flags.
	1	Enable shared flags.
XON	Transmitter On/Off	
	This bit switches the transmitter of the facility data link to operational (on) or inoperational state (off).	
	0	Switch transmitter off.
	1	Switch transmitter on.

PXFF
HDLC Transmit FIFO Register

Access : write

Address : 96_H

Reset Value : 0000_H

15							7		0
XFIFO(15:0)									
0	0	0	0	0	0	0	0	XFIFO(7:0)	

XFIFO Transmit FIFO Data

This bit field contains the first 16 bit word of the transmit FIFO of the signalling controller. The transmit FIFO itself consists of two pages with 32 bytes. One page is always used in background and is not visible to the microprocessor. The microprocessor sees one FIFO of 32 bytes only. Thus a maximum of 16 words can be stored inside the transmit FIFO at a time. Data stored in the receive FIFO can be written in 8- or 16-bit accesses. Nevertheless if the user wants to transfer an odd number of bytes the last access to the transmit FIFO register must be a byte access. Port status and FIFO operations can be accessed via register PPSR and register PHND.

Data written to the transmit FIFO is sent starting with bit 0 up to bit 15.

PPSR
HDLC Port Status register

Access : read
Address : 98_H
Reset Value : 2000_H

15	14	13	12				8	7	6	5	4				0
0	0	XFW	RBC(4:0)					-	-	0	STAT(4:0)				

XFW Transmit FIFO Write Enable

This bit indicates that data can be written to XFF.XFIFO. This bit is for polling use with the same meaning as the 'Transmit Pool Ready' interrupt vector.

RBC Receive Byte Count

This bit field indicates the amount of data stored in the receive FIFO. Valid after a 'Receive Message End' interrupt vector is generated. Receive byte count will be cleared, when a 'Receive Message Clear' command is executed via register HND.

Note: A zero byte count in combination with a 'Receive Pool Full' or 'Receive Message End' interrupt vector means that 32 bytes are available in the receive FIFO. However evaluating RBC is not necessary when the 'Receive Pool Full' interrupt was received.

STAT — Receive FIFO Status

This bit field reports the status of the data stored in the receive FIFO.

00000_B Valid HDLC Frame

This status is reported whenever a valid frame with valid CRC was received.

00001_B Receive Data Overflow

This status indicates a receive buffer overflow while the frame was received.

00010_B Receive Abort

Indicates a frame which was aborted while being received.

00011_B Not Octet

The frame length is not a multiple of eight bits.

00100_B CRC Error

HDLC frame was received with CRC error.

00101_B Channel Off

This status is generated when the receiver was disabled while a frame was being received. It reports the first ’7E’ flag which was received after the receiver was disabled.

PHND
HDLC Handshake Register

Access : write
Address : $9A_H$
Reset Value : 0000_H

15							8		6	5	4		2	1	0
0	0	0	0	0	0	0	RMC	0	ABORT	XRES	0	0	XHF	0	XME

Note: Receive command (bit 8) and transmit commands (bit 5 down to bit 0) can not be issued at the same time. Doing so will cause the facility data link to omit the transmit commands.

RMC Receive Message Complete

This bit is a confirmation from CPU that a data block has been read from RFIFO following a 'Receive Pool Full' or 'Receive Message End' interrupt vector and that the occupied page can now be released.

Note: If this bit is set, the low byte (transmit commands) of the register HND is ignored.

0 No function

1 Release page of receive FIFO.

ABORT Abort Frame

Setting this bit aborts HDLC frames which are transmitted.

0 Normal operation

1 Abort HDLC frame.

XRES Transmitter Reset

This bit resets the signalling controller transmit. However, the contents of the control register will not be reset.

0 Normal operation

1 Transmitter reset

XHF Transmit HDLC frame

Setting this bit indicates that the contents written to XFF.XFIFO shall be transmitted as HDLC frame. If data written to XFF.XFIFO completes a HDLC frame, bit XME must be set together with XHF in order to generate CRC and flag.

0 No function

1 Transmit data stored in XFF.XFIFO in HDLC format.

XME Transmit Message End

Setting this bit indicates that the last data block written to XFF.XFIFO completes the current frame. The signalling controller terminates the transmission properly by appending CRC and the closing flag to the data sequence.

Table 9 Path Maintenance Transmit Commands

XRES	XHF	XME	Function
1	-	-	**Reset Port**
0	1	0	**Start Transmission** Send FIFO content. This command has to be issued in case frames are longer than 32 bytes. In case frames length is equal to or smaller than 32 bytes the command 'End Transmission' is sufficient.
0	1	1	**End Transmission** Send FIFO content. CRC (if enabled) and flag are sent after the last byte which was stored in the transmit FIFO was sent.

PMSK
Interrupt Mask Register

Access	: read/write
Address	: $9C_H$
Reset Value	: 00_H

7		5	4	3	2	1	0
0	0	ALLS	XDU	XPR	RPF	RME	0

For each facility data link interrupt vector an interrupt vector generation mask is provided. Generation of an interrupt vector itself does not necessarily result in assertion of the interrupt pin. For description of interrupt concept refer to section **"Interrupt Interface" on Page 62**.

The following definition applies:

1	The corresponding interrupt vector will not be generated by the device.
0	The corresponding interrupt vector will be generated.

Facility Data Link Interrupt Vector Transmit

ALLS	Mask 'All Sent'
XDU	Mask ''Transmit Data Underrun'
XPR	Mask 'Transmit Pool Ready'

Facility Data Link Interrupt Vector Receive

RPF	Mask 'Receive Pool Full'
RME	Mask 'Receive Message End'

8 Electrical Characteristics

8.1 Important Electrical Requirements

Both V_{DD3} and V_{DD25} can take on any power-on sequence. Within 50 milliseconds of power-up the voltages must be within their respective absolute voltage limits. At power-down, within 50 milliseconds of either voltage going outside its operational range, both voltages must be returned below 0.1V.

8.2 Absolute Maximum Ratings

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min	max	
Ambient temperature under bias	T_A	-40	85	°C
Junction temperature under bias	T_J		125	°C
Storage temperature	T_{stg}	-65	125	°C
Voltage on any pin with respect to ground	V_S	-0.4	V_{DD3}+0.4	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.3 DC Characteristics

a) Power Supply Pins

Table 11 DC Characteristics

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Core Supply Voltage		V_{DD25}	2.375	2.5	2.75	V	
I/O Supply Voltage		V_{DD3}	3.0	3.3	3.6	V	
Core supply current V_{DD25}	operational	I_{CC25}		75	100	mA	
	power down (no clocks)	I_{CCPD25}			100	µA	
I/O supply current V_{DD3}	operational	I_{CC3}		45	70	mA	Inputs at V_{SS}/ V_{DD3} No output loads.
	power down (no clocks)	I_{CCPD3}			200	µA	
Input leakage for each pin:							$V_{DD25}=V_{DD3}$=max
Input leakage low		I_{IL}	-1			µA	V_{in}=0V;
Input leakage high		I_{IH}			5		V_{in}=3.6V;
Input leakage low bscan		I_{IIL_BS}	-200				V_{in}=0V;
Input leakage high bscan		I_{IIH_BS}			5		V_{in}=3.6V;
Power Dissipation		P		340		mW	

b) Interface Pins

Table 12 DC Characteristics

T_A = -40 to 85°C, V_{DD3} = 3.3 V ± 0.3 V, V_{DD25} = 2.5 V + 0.25 V - 0.125 V, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	-0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD3}+0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{QL} = 2 mA
H-output voltage	V_{OH}	2.4		V	I_{QH} = -400 µA

8.4 AC Characteristics

T_A = -40 to 85°C, V_{DD3} = 3.3 V ± 0.3 V, V_{DD25} = 2.5 V + 0.25 V - 0.125 V, V_{SS} = 0 V

Inputs are driven to 2.4 V for a logical '1' and to 0.4 V for a logical '0'. Timing measurements are made at 2.0 V for a logical '1' and at 0.8 V for a logical '0'.

The AC testing input/output waveforms are shown below.

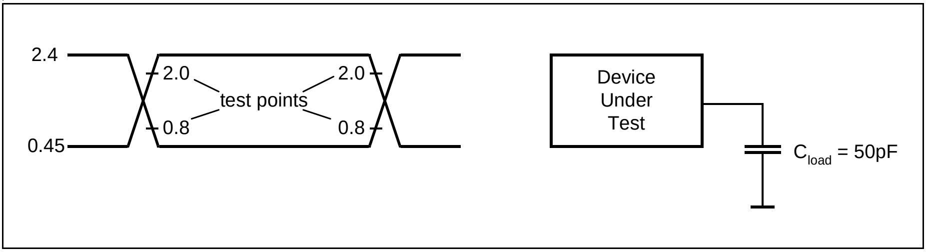


Figure 23 Input/Output Waveform for AC Tests

8.4.1 Local Microprocessor Interface Timing

8.4.1.1 Intel Bus Interface Timing

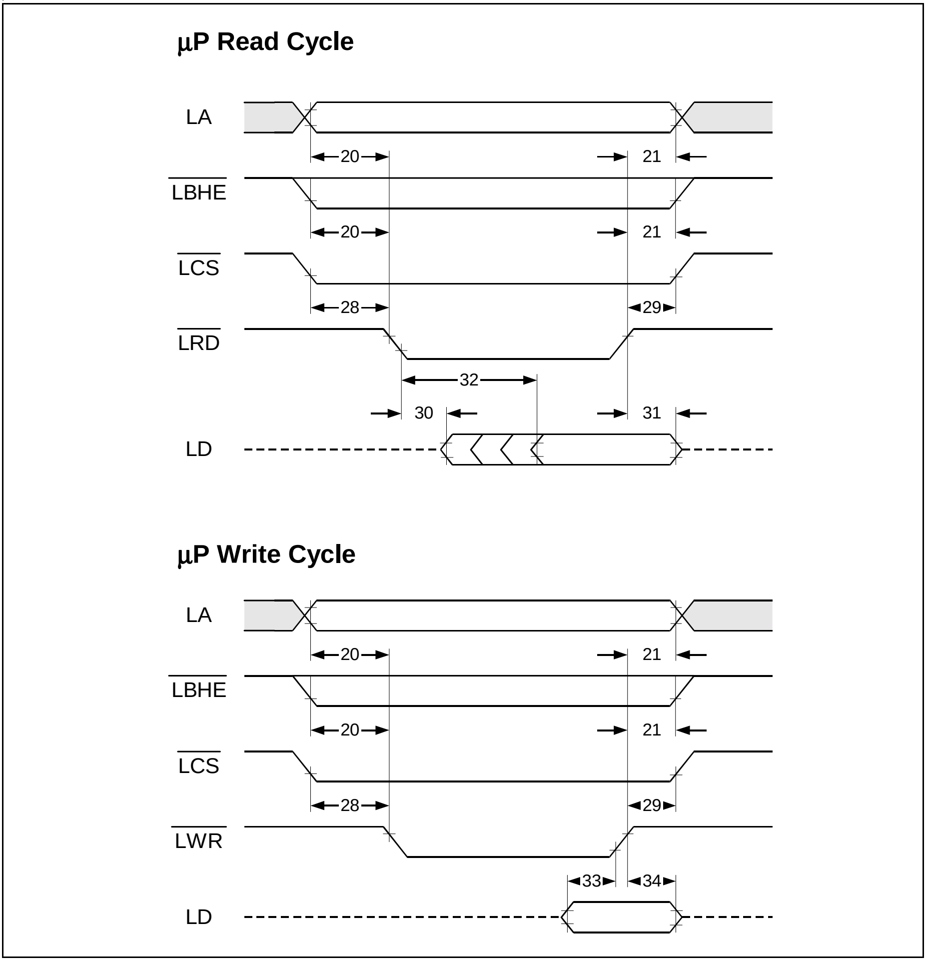


Figure 24 Intel Demultiplexed Bus Timing

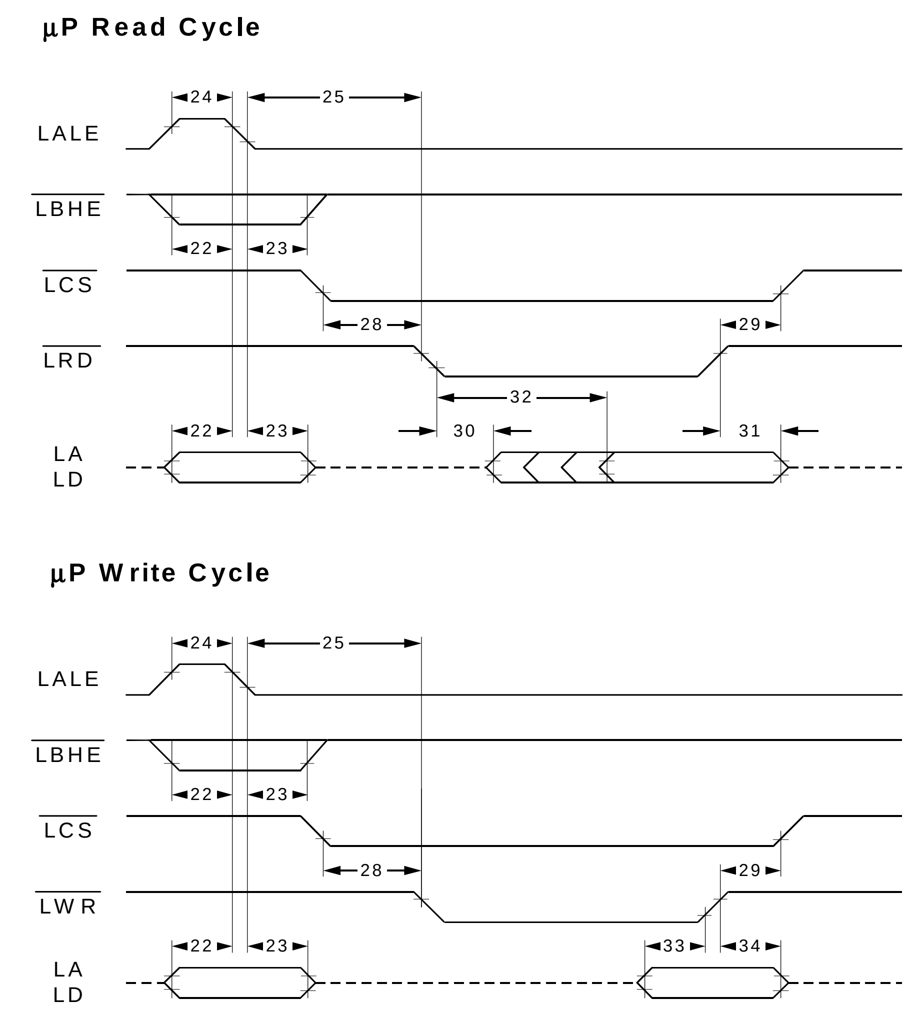


Figure 25 **Intel Multiplexed Bus Timing**

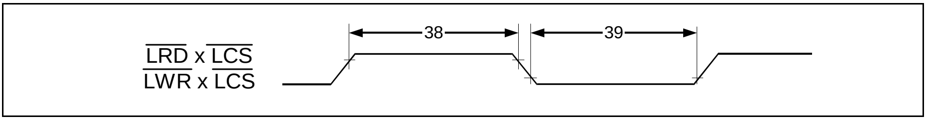


Figure 26 Read, Write Control Interval in Demultiplexed Bus Mode

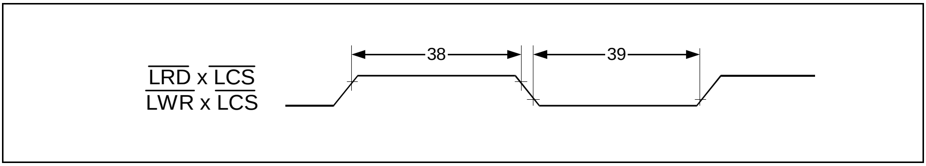


Figure 27 Read, Write Control Interval in Multiplexed Bus Mode

Table 13 Intel Bus Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
20	LA, $\overline{LBHE}$ to $\overline{LRD}$, $\overline{LWR}$ setup time	10		ns
21	LA, $\overline{LBHE}$ to $\overline{LRD}$, $\overline{LWR}$ hold time	0		ns
22	LA, $\overline{LBHE}$ to LALE falling setup time	10		ns
23	LA, $\overline{LBHE}$ to LALE falling hold time	5		ns
24	LALE minimum high time	15		ns
25	LALE falling to $\overline{LRD}$, $\overline{LWR}$ setup time	10		ns
28	$\overline{LCS}$ to $\overline{LRD}$, $\overline{LWR}$ setup time	10		ns
29	$\overline{LCS}$ to $\overline{LRD}$, $\overline{LWR}$ hold time	0		ns
30	$\overline{LRD}$ low to LD active delay		20	ns
31	$\overline{LRD}$ high to LD float delay		5	ns
32	$\overline{LRD}$ low to LD valid delay		100	ns
33	LD to $\overline{LWR}$ setup time	20		ns
34	LD to $\overline{LWR}$ hold time	5		ns
38	Read, Write inactive control interval	60		ns
39	Read, Write active control interval	100		ns

8.4.1.2 Motorola Bus Interface Timing

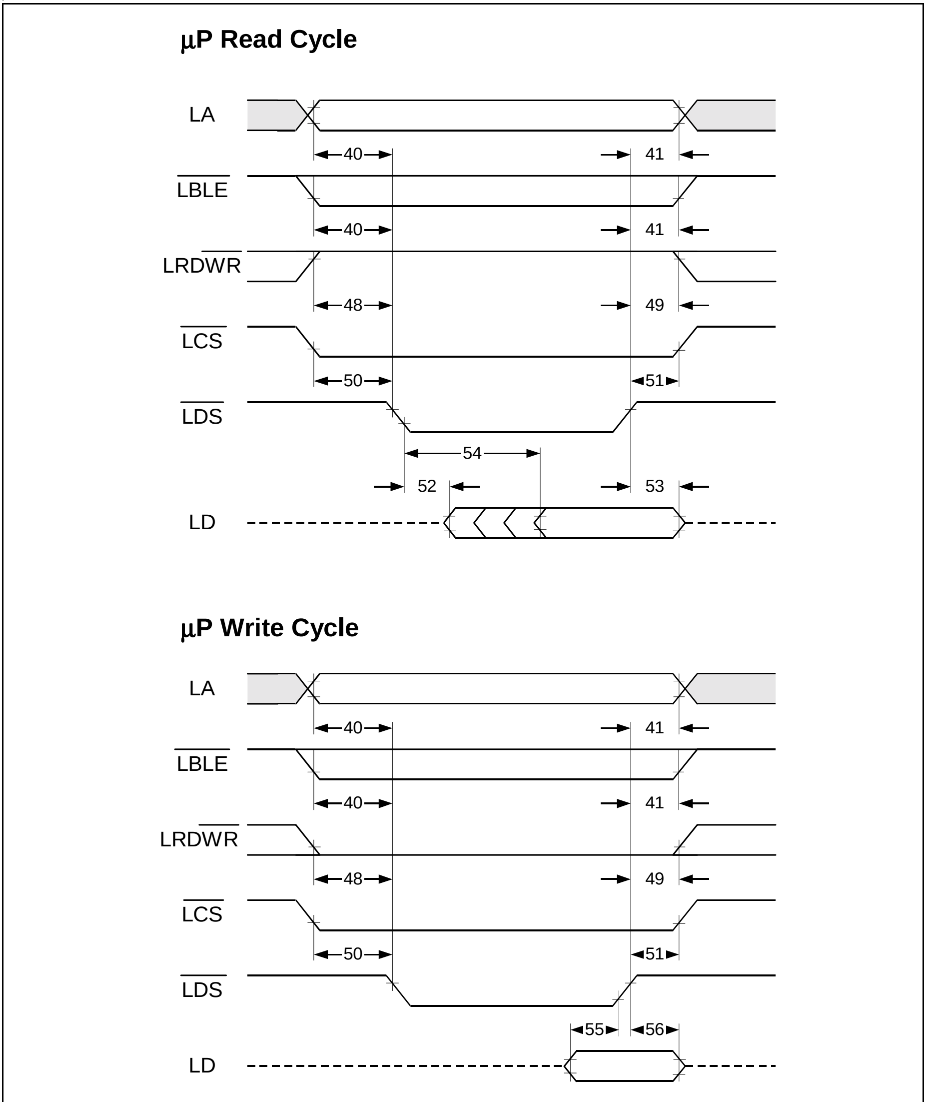


Figure 28 Motorola Demultiplexed Bus Timing

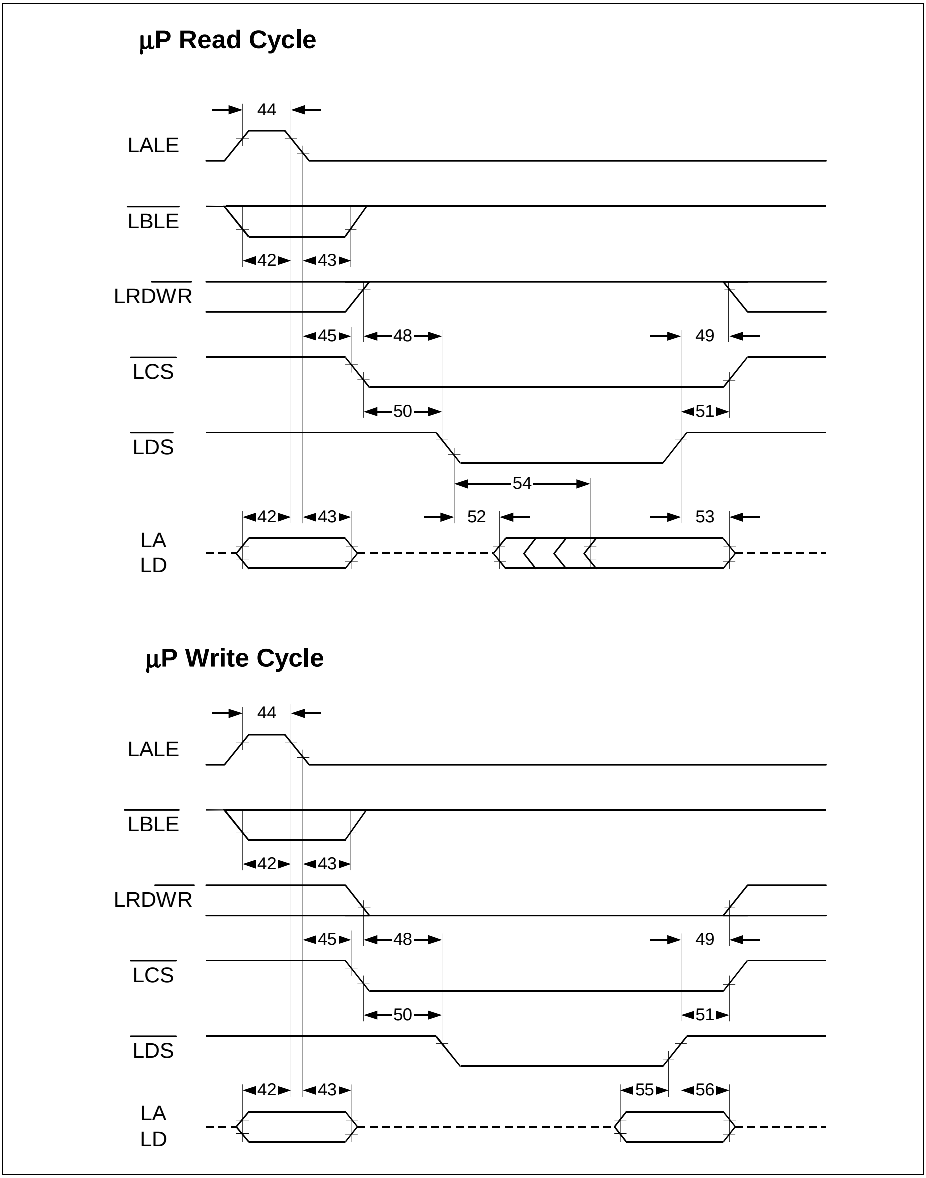


Figure 29 Motorola Multiplexed Bus Timing

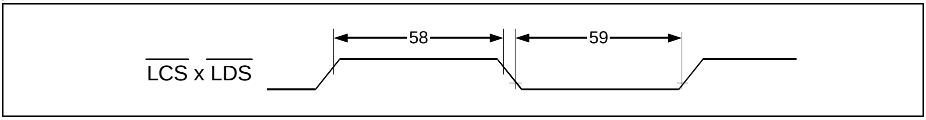


Figure 30 Read, Write Control Interval in Demultiplexed Bus Mode

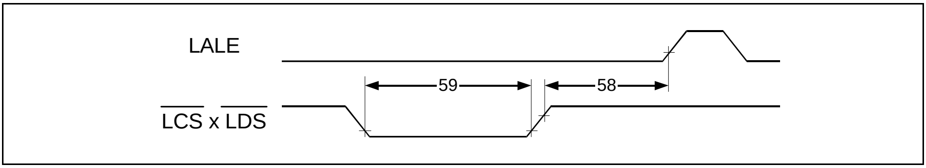


Figure 31 Read, Write, ALE Control Interval in Multiplexed Bus Mode

Table 14 Motorola Bus Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
40	LA to $\overline{\text{LDS}}$ setup time	10		ns
41	LA to $\overline{\text{LDS}}$ hold time	0		ns
42	LA to LALE falling setup time	10		ns
43	LA to LALE falling hold time	5		ns
44	LALE minimum high time	15		ns
45	LALE falling to $\overline{\text{LCS}}$ setup time	10		ns
48	LRD$\overline{\text{WR}}$ to $\overline{\text{LDS}}$ setup time	10		ns
49	LRD$\overline{\text{WR}}$ to $\overline{\text{LDS}}$ hold time	5		ns
50	$\overline{\text{LCS}}$ to $\overline{\text{LDS}}$ setup time	10		ns
51	$\overline{\text{LCS}}$ to $\overline{\text{LDS}}$ hold time	0		ns
52	$\overline{\text{LDS}}$ low to LD active delay		20	ns
53	$\overline{\text{LDS}}$ high to LD float delay		5	ns
54	$\overline{\text{LDS}}$ low to LD valid delay		100	ns
55	LD to $\overline{\text{LDS}}$ setup time	20		ns
56	LD to $\overline{\text{LDS}}$ hold time	5		ns
58	Read, Write inactive control interval	60		ns
59	Read, Write active control interval	100		ns

8.4.2 DMA Interface Signals

8.4.2.1 DMA Receive Timing

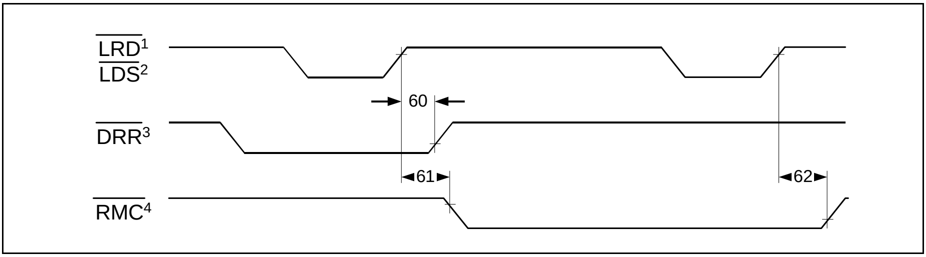


Figure 32 DMA Receive Timing

Note:

1 Intel Mode

2 Motorola Mode

3 $\overline{\text{DRR}}$ is asserted asynchronously as soon as there is data in the receive FIFO.

4 $\overline{\text{RMC}}$ is asserted when the last data belonging to a message was read.

Table 15 DMA Receive Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
60	$\overline{\text{LRD}}$, $\overline{\text{LDS}}$ inactive to $\overline{\text{DRR}}$ inactive delay			ns
61	$\overline{\text{LRD}}$, $\overline{\text{LDS}}$ inactive to $\overline{\text{RMC}}$ active delay			ns
62	$\overline{\text{LRD}}$, $\overline{\text{LDS}}$ inactive to $\overline{\text{RMC}}$ inactive delay			ns

8.4.2.2 DMA Transmit Timing

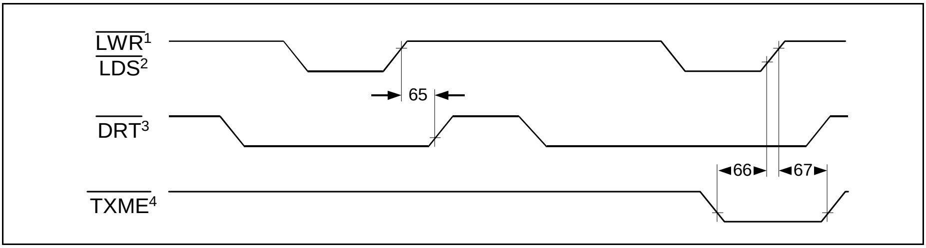


Figure 33 DMA Transmit Timing

Note:

1 Intel Mode

2 Motorola Mode

3 DRT is asserted asynchronously as soon as there is free space in the transmit FIFO.

4 TXME has to be asserted while the last byte of a message is written to the transmit FIFO.

Table 16 DMA Transmit Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
65	LRD, LDS inactive to DRT inactive delay			ns
66	TXME to LDS setup time	20		ns
67	TXME to LDS hold time	5		ns

8.4.3 Serial Interface Timing

8.4.3.1 DS3 Serial Interface Timing

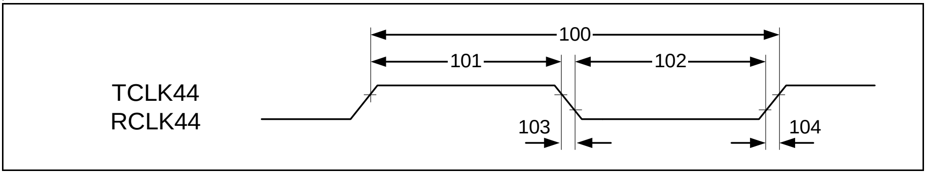


Figure 34 Clock Input Timing

Table 17 Clock Input Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
100	Clock period	nom. 44.736		MHz
101	Clock high timing	7.5		ns
102	Clock low timing	7.5		ns
103	Clock fall time		2	ns
104	Clock rise time		2	ns

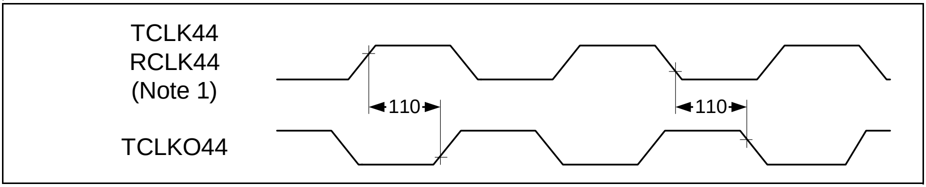


Figure 35 DS3 Transmit Cycle Timing

Note:

1. *Actual clock reference depends on selected clock mode:*

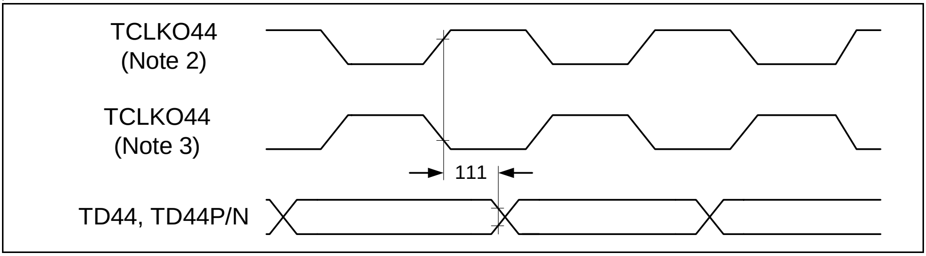


Figure 36 DS3 Transmit Data Timing

Note:

2. *Timing for transmit data which is updated on the rising edge of TCLKO44.*
3. *Timing for transmit data which is updated on the falling edge of TCLKO44.*

Table 18 DS3 Transmit Cycle Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
110	RCLK44, TCLK44 to TCLKO44 delay	2	15	ns
111	TCLKO44 to TD44, TD44P/TD44N delay	0	5	ns

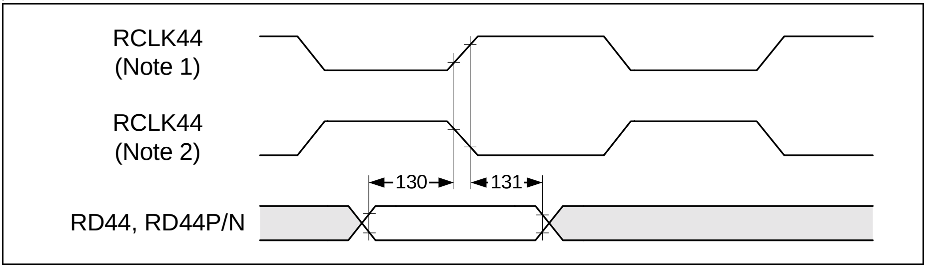


Figure 37 DS3 Receive Cycle Timing

Note:

1. *Timing for data which is sampled on the rising edge of the receive clock.*
2. *Timing for data which is sampled on the falling edge of the receive clock.*

Table 19 DS3 Receive Cycle Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
130	RD44, RD44P, RD44N to RCLK44 setup time	5		ns
131	RD44, RD44P, RD44N to RCLK44 hold time	5		ns

8.4.3.2 Overhead Bit Timing

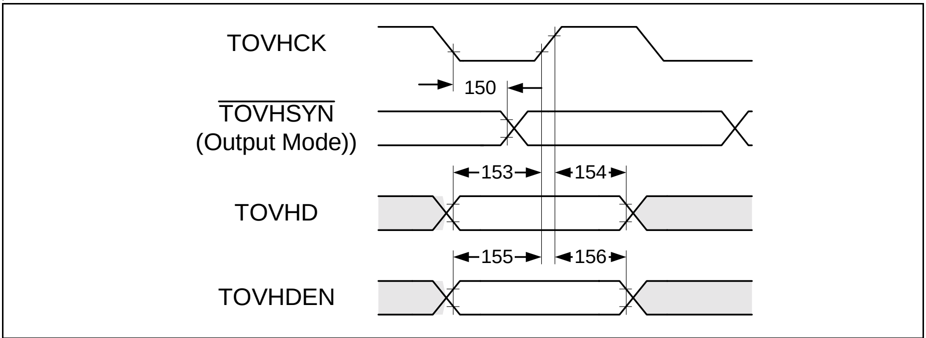


Figure 38 DS3 Transmit Overhead Timing

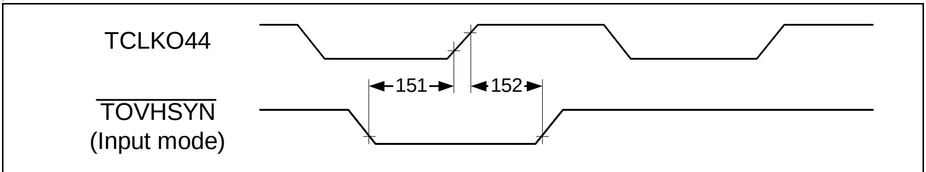


Figure 39 DS3 Transmit Overhead Synchronization Timing

Table 20 DS3 Transmit Overhead Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
150	TOVHCK to $\overline{\text{TOVHSYN}}$ delay		75	ns
151	$\overline{\text{TOVHSYN}}$ to TCLKO44 setup time	7		ns
152	$\overline{\text{TOVHSYN}}$ to TCLKO44 hold time	7		ns
153	TOVHD to TOVHCK setup time	25		ns
154	TOVHD to TOVHCK hold time	5		ns
155	TOVHDEN to TOVHCK setup time	25		ns
156	TOVHDEN to TOVHCK hold time	5		ns

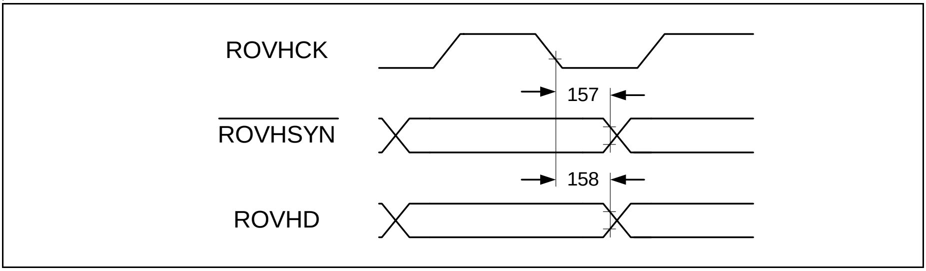


Figure 40 DS3 Receive Overhead Timing

Table 21 DS3 Receive Overhead Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
157	ROVHCK to $\overline{\text{ROVHSYN}}$ delay		75	ns
158	ROVHCK to ROVHD delay		75	ns

8.4.3.3 Stuff Bit Timing

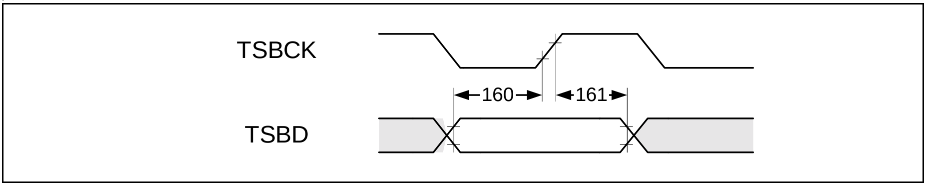


Figure 41 DS3 Transmit Stuff Bit Timing

Table 22 DS3 Transmit Stuff Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
160	TSBD to TSBCK setup time	25		ns
161	TSBD to TSBCK hold time	5		ns

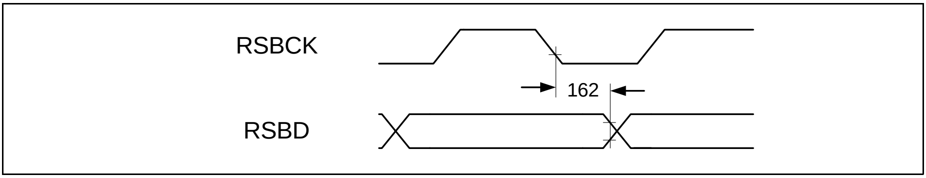


Figure 42 DS3 Receive Stuff Bit Timing

Table 23 DS3 Receive Stuff Bit Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
162	RSBCK to RSBD delay		75	ns

8.4.3.4 DS1/E1 Interface Timing

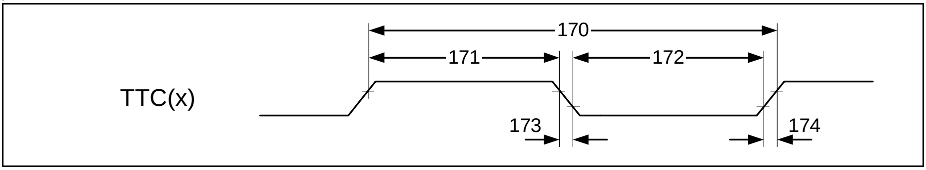


Figure 43 DS1/E1 Transmit Clock Timing

Table 24 DS1/E1 Transmit Clock Timing

No.	Parameter	Limit Values			Unit
		min.	typ	max.	
Interface operated in E1 Mode					
170	Clock period	2.048 MHz ± 50 ppm			
171	Clock high timing	100			ns
172	Clock low timing	100			ns
173	Clock fall time			10	ns
174	Clock rise time			10	ns
Interface operated in DS1 Mode					
170	Clock period	1.544 MHz ± 130 ppm			
171	Clock high timing	100			ns
172	Clock low timing	100			ns
173	Clock fall time			10	ns
174	Clock rise time			10	ns

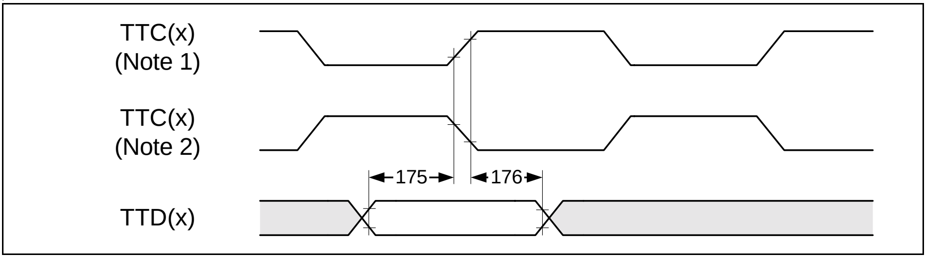


Figure 44 DS1/E1 Transmit Data Timing

Note:

1. *Timing for transmit data sampled on the rising edge of TTC(x).*
2. *Timing for transmit data sampled on the falling edge of TTC(x).*

Table 25 DS1/E1 Transmit Data Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
175	TTD(x) to TTC(x) setup time	25		ns
176	TTD(x) to TTC(x) hold time	75		ns

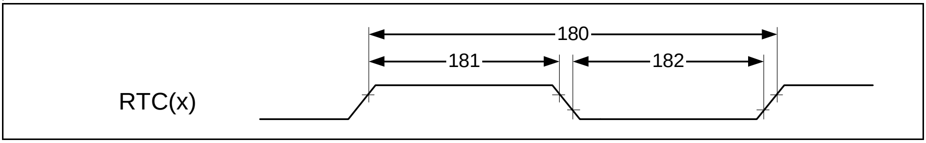


Figure 45 DS1/E1 Receive Clock Timing

Table 26 DS1/E1 Receive Clock Timing

No.	Parameter	Limit Values			Unit
		min.	typ	max.	
Interface operated in E1 Mode					
180	Clock period	469		2056	ns
181	Clock high timing	156		335	ns
182	Clock low timing	312		1900	ns
Interface operated in DS1 Mode					
180	Clock period	625		1587	ns
181	Clock high timing	310		495	ns
182	Clock low timing	310		1275	ns

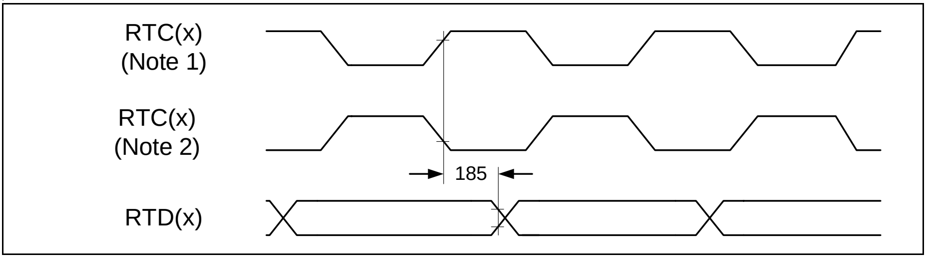


Figure 46 DS1/E1 Receive Data Timing

Note:

1. *Timing for receive data updated on the rising edge of RTC(x).*
2. *Timing for receive data updated on the falling edge of RTC(x).*

Table 27 DS1/E1 Receive Data Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
185	RTC(x) to RTD(x) delay	25	75	ns

8.4.3.5 DS3 System Interface Timing

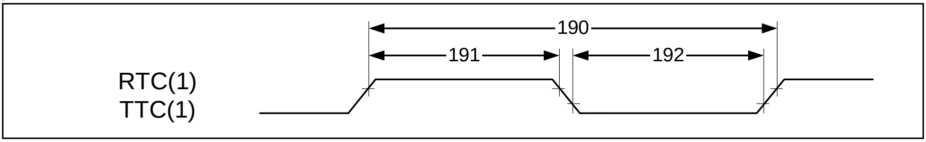


Figure 47 DS3 System Clock Timing

Table 28 DS3 System Clock Timing

No.	Parameter	Limit Values			Unit
		min.	typ	max.	
190	Clock period		22.35	44.7	ns
191	Clock high timing	7.5			ns
192	Clock low timing	7.5			ns

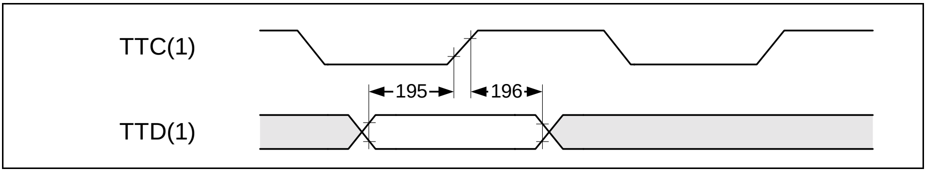


Figure 48 DS3 System Transmit Data Timing

Table 29 DS3 System Transmit Data Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
195	TTD(1) to TTC(1) setup time	7		ns
196	TTD(1) to TTC(1) hold time	5		ns

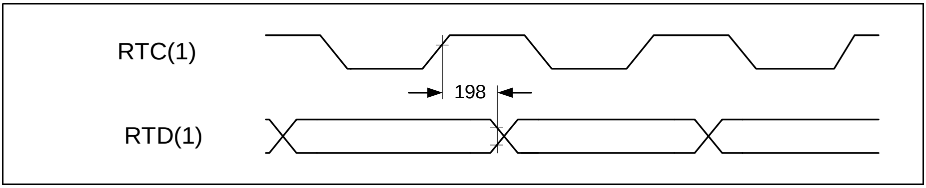


Figure 49 DS3 System Receive Data Timing

Table 30 DS3 System Receive Data Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
198	RTC(1) to RTD(1) delay	-5	7	ns

8.4.4 JTAG Interface Timing

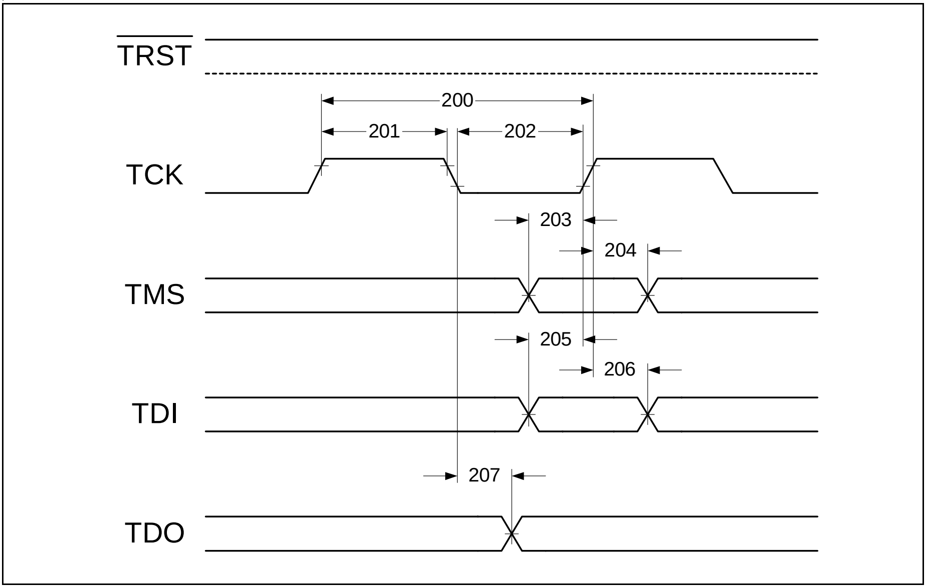


Figure 50 JTAG Interface Timing

Table 31 JTAG Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
200	TCK period	120		ns
201	TCK high time	60		ns
202	TCK low time	60		ns
203	TMS setup time	20		ns
204	TMS hold time	20		ns
205	TDI setup time	20		ns
206	TDI hold time	20		ns
207	TDO valid time	50		ns

8.4.5 Reset Timing

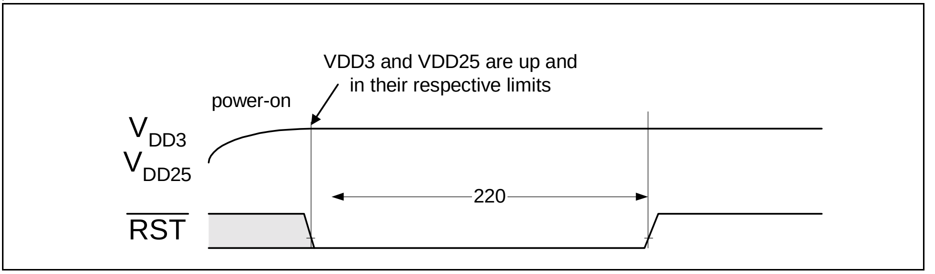
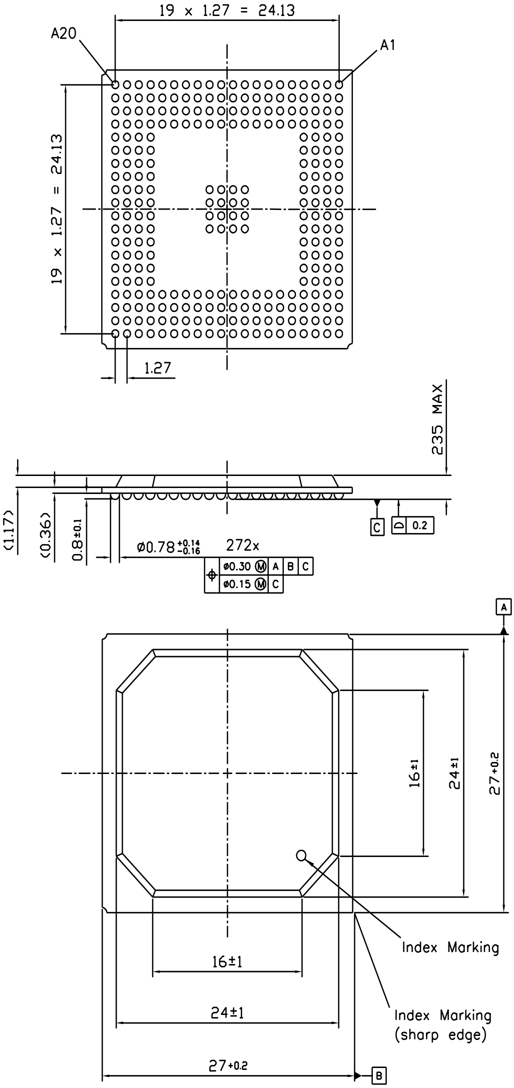


Figure 51 Reset Timing

Table 32 Reset Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
220	$\overline{\text{RST}}$ pulse width	1		µs

9 Package Outline



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