M29W800AT
M29W800AB

8 Mbit (1Mb x8 or 512Kb x16, Boot Block) Low Voltage Single Supply Flash Memory

FEATURES SUMMARY

- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 80ns
- PROGRAMMING TIME: 10µs typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte or Word-by-Word
  - Status Register bits and Ready/Busy Output
- SECURITY PROTECTION MEMORY AREA
- INSTRUCTION ADDRESS CODING: 3 digits
- MEMORY BLOCKS
  - Boot Block (Top or Bottom location)
  - Parameter and Main blocks
- BLOCK, MULTI-BLOCK and CHIP ERASE
- MULTI BLOCK PROTECTION/TEMPORARY UNPROTECTION MODES
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- LOW POWER CONSUMPTION
  - Stand-by and Automatic Stand-by
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M29W800AT: D7h
  - Bottom Device Code, M29W800AB: 5Bh

Figure 1. Packages

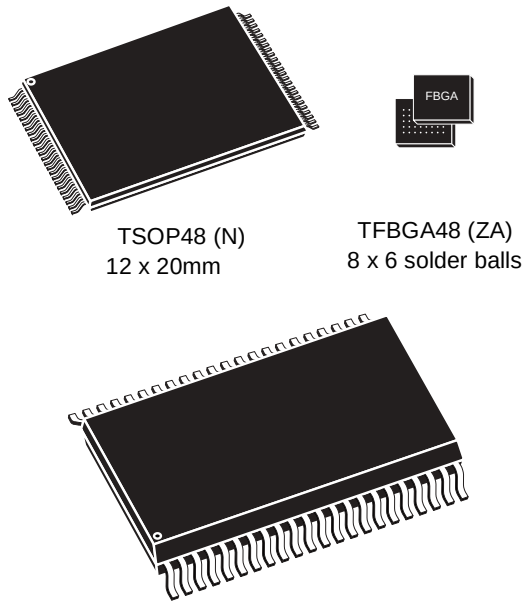
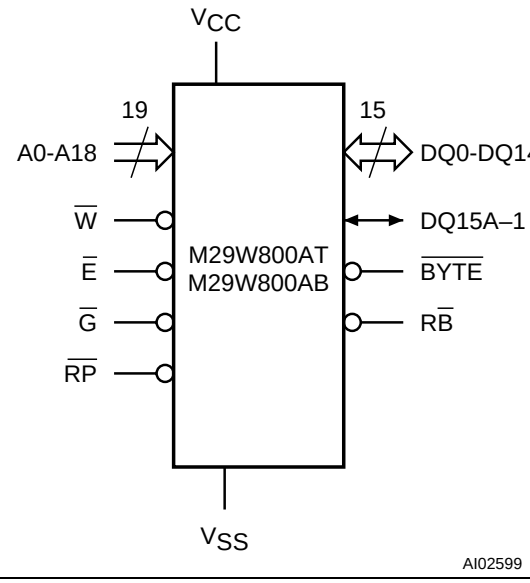


Figure 2. Logic Diagram



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DESCRIPTION

The M29W800A is a non-volatile memory that may be erased electrically at the block or chip level and programmed in-system on a Byte-by-Byte or Word-by-Word basis using only a single 2.7V to 3.6V V_{CC} supply. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed in standard programmers.

The array matrix organisation allows each block to be erased and reprogrammed without affecting other blocks. Blocks can be protected against programing and erase on programming equipment, and temporarily unprotected to make changes in the application. Each block can be programmed and erased over 100,000 cycles.

Instructions for Read/Reset, Auto Select for reading the Electronic Signature or Block Protection status, Programming, Block and Chip Erase, Erase Suspend and Resume are written to the device in cycles of commands to a Command Interface using standard microprocessor write timings.

The device is offered in TSOP48 (12 x 20mm), SO44 and TFBGA48 0.8 mm ball pitch packages.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input/Outputs, Command Inputs
DQ8-DQ14	Data Input/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Organisation

The M29W800A is organised as 1M x8 or 512K x16 bits selectable by the BYTE signal. When BYTE is Low the Byte-wide x8 organisation is selected and the address lines are DQ15A–1 and A0-A18. The Data Input/Output signal DQ15A–1 acts as address line A–1 which selects the lower or upper Byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain at High impedance. When BYTE is High the memory uses the address inputs A0-A18 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable E, Output Enable G and Write Enable W inputs.

A Reset/Block Temporary Unprotection $\overline{RP}$ tri-level input provides a hardware reset when pulled Low, and when held High (at V_{ID}) temporarily unprotects blocks previously protected allowing them to be programed and erased. Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on DQ7 provides a Data Polling signal, and DQ6 and DQ2 provide Toggle signals to indicate the state of the P/E.C operations. A Ready/Busy $\overline{RB}$ output indicates the completion of the internal algorithms.

Memory Blocks

The devices feature asymmetrically blocked architecture providing system memory integration. Both M29W800AT and M29W800AB devices have an array of 19 blocks, one Boot Block of 16 KBytes or 8 KWords, two Parameter Blocks of 8 KBytes or 4 KWords, one Main Block of 32 KBytes or 16 KWords and fifteen Main Blocks of 64 KBytes or 32 KWords. The M29W800AT has the Boot Block at the top of the memory address space and the M29W800AB locates the Boot Block starting at the bottom. The memory maps are showed in Tables 2 and 3.

Each block can be erased separately, any combination of blocks can be specified for multi-block erase or the entire chip may be erased. The Erase operations are managed automatically by the P/E.C. The block erase operation can be suspended in order to read from or program to any block not being erased, and then resumed.

Block protection provides additional data security. Each block can be separately protected or unprotected against Program or Erase on programming equipment. All previously protected blocks can be temporarily unprotected in the application.

Bus Operations

The following operations can be performed using the appropriate bus cycles: Read (Array, Electronic Signature, Block Protection Status), Write command, Output Disable, Stan-by, Reset, Block Protection, Unprotection, Protection Verify, Unprotection Verify and Block Temporary Unprotection. See Table 5., Read Electronic Signature (following AS instruction or with A9 = V_{ID}) and Table 6., Read Block Protection with AS Instruction.

Command Interface

Instructions, made up of commands written in cycles, can be given to the Program/Erase Controller through a Command Interface (C.I.). For added data protection, program or erase execution starts after 4 or 6 cycles. The first, second, fourth and fifth cycles are used to input Coded cycles to the C.I. This Coded sequence is the same for all Program/Erase Controller instructions. The 'Command' itself and its confirmation, when applicable, are given on the third, fourth or sixth cycles. Any incorrect command or any improper command sequence will reset the device to Read Array mode.

Instructions

Seven instructions are defined to perform Read Array, Auto Select (to read the Electronic Signature or Block Protection Status), Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume.

The internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle, Error bits and the RB output may be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions are composed of up to six cycles. The first two cycles input a Coded sequence to the Command Interface which is common to all instructions (see Table 8).

The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data, Electronic Signature or Block Protection Status for Read operations. In order to give additional data protection, the instructions for Program and Block or Chip Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (Block or Chip), the fourth and fifth cycles input a further Coded sequence before the Erase confirm command on the sixth cycle. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

Figure 3. TSOP Connections

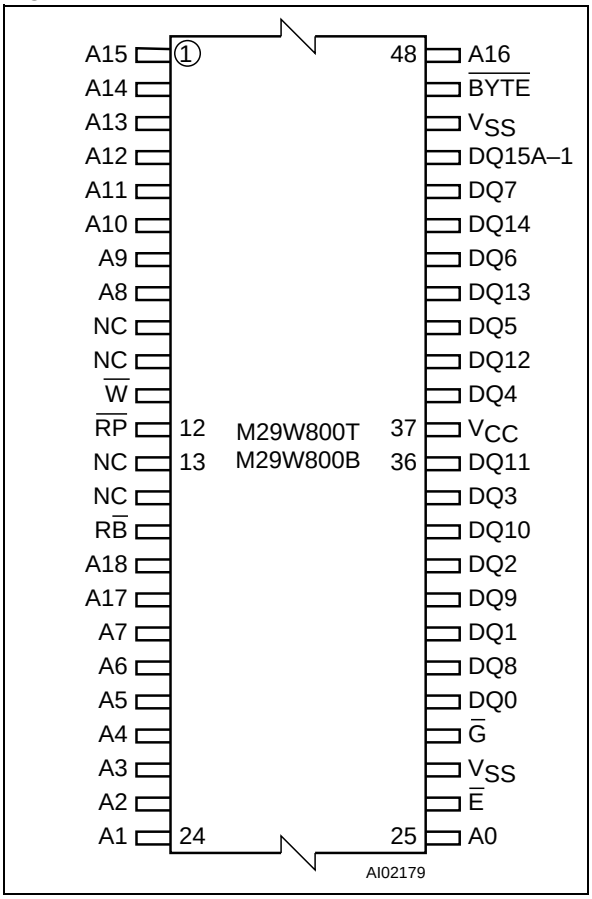


Figure 4. SO Connections

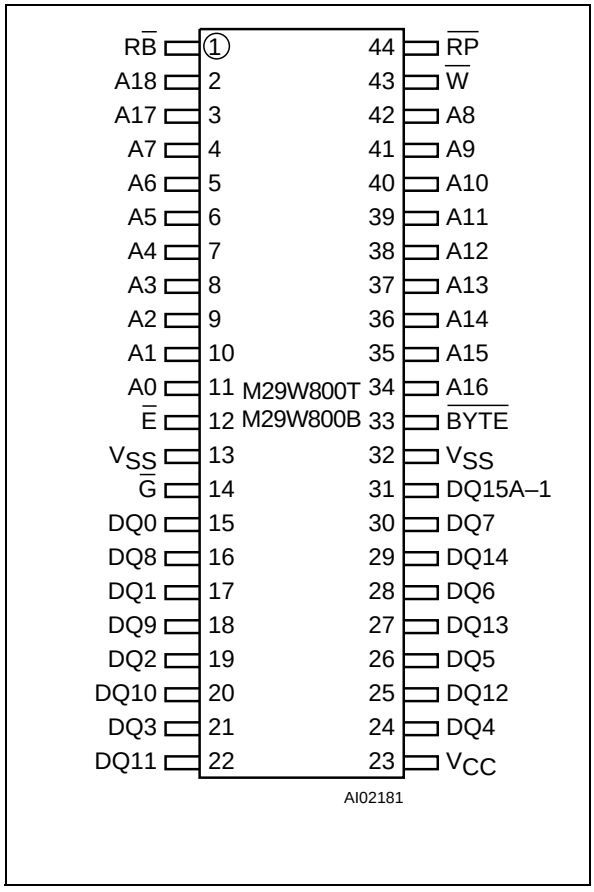


Figure 5. TFBGA Connections (Top view through package)

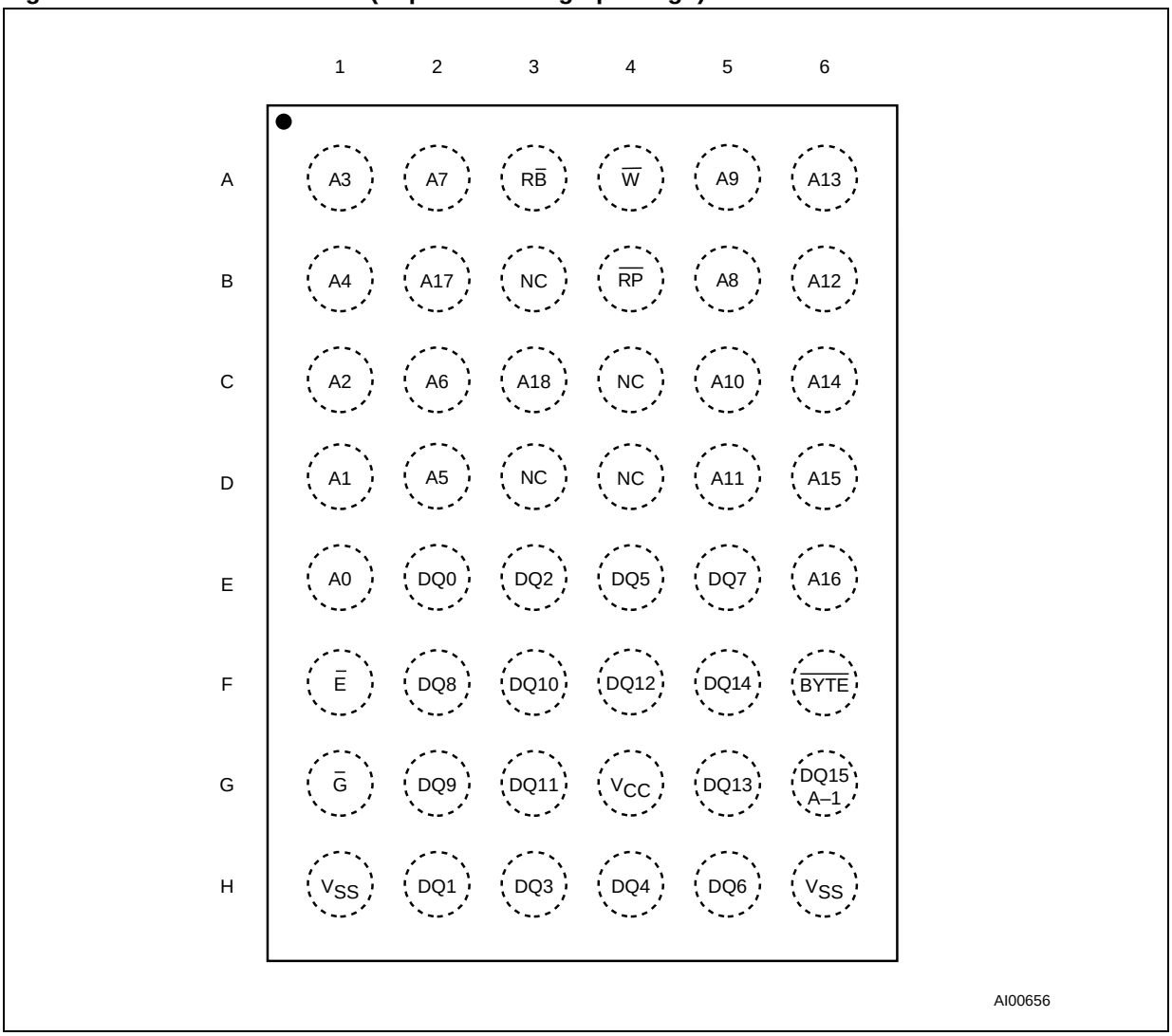


Table 2. Top Boot Block Addresses, M29W800AT

#	Size (Kbytes)	Address Range (x8)	Address Range (x16)
18	16	FC000h-FFFFFh	7E000h-7FFFFh
17	8	FA000h-FBFFFh	7D000h-7DFFFh
16	8	F8000h-F9FFFh	7C000h-7CFFFh
15	32	F0000h-F7FFFh	78000h-7BFFFh
14	64	E0000h-EFFFFh	70000h-77FFFh
13	64	D0000h-DFFFFh	68000h-6FFFFh
12	64	C0000h-CFFFFh	60000h-67FFFh
11	64	B0000h-BFFFFh	58000h-5FFFFh
10	64	A0000h-AFFFFh	50000h-57FFFh
9	64	90000h-9FFFFh	48000h-4FFFFh
8	64	80000h-8FFFFh	40000h-47FFFh
7	64	70000h-7FFFFh	38000h-3FFFFh
6	64	60000h-6FFFFh	30000h-37FFFh
5	64	50000h-5FFFFh	28000h-2FFFFh
4	64	40000h-4FFFFh	20000h-27FFFh
3	64	30000h-3FFFFh	18000h-1FFFFh
2	64	20000h-2FFFFh	10000h-17FFFh
1	64	10000h-1FFFFh	08000h-0FFFFh
0	64	00000h-0FFFFh	00000h-07FFFh

Table 3. Bottom Boot Block Addresses, M29W800AB

#	Size (Kbytes)	Address Range (x8)	Address Range (x16)
18	64	F0000h-FFFFFh	78000h-7FFFFh
17	64	E0000h-EFFFFh	70000h-77FFFh
16	64	D0000h-DFFFFh	68000h-6FFFFh
15	64	C0000h-CFFFFh	60000h-67FFFh
14	64	B0000h-BFFFFh	58000h-5FFFFh
13	64	A0000h-AFFFFh	50000h-57FFFh
12	64	90000h-9FFFFh	48000h-4FFFFh
11	64	80000h-8FFFFh	40000h-47FFFh
10	64	70000h-7FFFFh	38000h-3FFFFh
9	64	60000h-6FFFFh	30000h-37FFFh
8	64	50000h-5FFFFh	28000h-2FFFFh
7	64	40000h-4FFFFh	20000h-27FFFh
6	64	30000h-3FFFFh	18000h-1FFFFh
5	64	20000h-2FFFFh	10000h-17FFFh
4	64	10000h-1FFFFh	08000h-0FFFFh
3	32	08000h-0FFFFh	04000h-07FFFh
2	8	06000h-07FFFh	03000h-03FFFh
1	8	04000h-05FFFh	02000h-02FFFh
0	16	00000h-03FFFh	00000h-01FFFh

SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram and Table 1., Signal Names.

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation on the falling edge at Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. In Word-wide organisation the address lines are A0-A18, in Byte-wide organisation DQ15A–1 acts as an additional LSB address line. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code, Block Protection Status or a Write Block Protection or Block Unprotection is enabled depending on the combination of levels on A0, A1, A6, A12 and A15.

Data Input/Outputs (DQ0-DQ7). These Inputs/Outputs are used in the Byte-wide and Word-wide organisations. The input is data to be programmed in the memory array or a command to be written to the C.I. Both are latched on the rising edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. The output is data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection Status or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is at a Low level.

Data Input/Outputs (DQ8-DQ14 and DQ15A–1). These Inputs/Outputs are additionally used in the Word-wide organisation. When $\overline{BYTE}$ is High DQ8-DQ14 and DQ15A–1 act as the MSB of the Data Input or Output, functioning as described for DQ0-DQ7 above, and DQ8-DQ15 are 'don't care' for command inputs or status outputs. When $\overline{BYTE}$ is Low, DQ0-DQ14 are high impedance, DQ15A–1 is the Address A–1 input.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the stan-by level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. The Chip Enable must be forced to V_{ID} during the Block Unprotection operation.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ is High the outputs are High impedance. $\overline{G}$ must be forced to V_{ID} level during Block Protection and Unprotection operations.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Address and Data latches.

Byte/Word Organization Select ($\overline{BYTE}$). The $\overline{BYTE}$ input selects the output configuration for the device: Byte-wide (x8) mode or Word-wide (x16) mode. When $\overline{BYTE}$ is Low, the Byte-wide mode is selected and the data is read and programmed on DQ0-DQ7. In this mode, DQ8-DQ14 are at high impedance and DQ15A–1 is the LSB address. When $\overline{BYTE}$ is High, the Word-wide mode is selected and the data is read and programmed on DQ0-DQ15.

Ready/Busy Output ($\overline{RB}$). Ready/Busy is an open-drain output and gives the internal state of the P/E.C. of the device. When $\overline{RB}$ is Low, the device is Busy with a Program or Erase operation and it will not accept any additional program or erase instructions except the Erase Suspend instruction. When $\overline{RB}$ is High, the device is ready for any Read, Program or Erase operation. The $\overline{RB}$ will also be High when the memory is put in Erase Suspend or Stan-by modes.

Reset/Block Temporary Unprotect Input ($\overline{RP}$). The $\overline{RP}$ Input provides hardware reset and protected block(s) temporary unprotection functions. Reset of the memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPX}. When the reset pulse is given, if the memory is in Read or Stan-by modes, it will be available for new operations in t_{PHEL} after the rising edge of $\overline{RP}$. If the memory is in Erase, Erase Suspend or Program modes the reset will take t_{PLYH} during which the $\overline{RB}$ signal will be held at V_{IL}. The end of the memory reset will be indicated by the rising edge of $\overline{RB}$. A hardware reset during an Erase or Program operation will corrupt the data being programmed or the sector(s) being erased. See Tables 15 and 16, Read AC Characteristics and Figure 13., Data Polling DQ7 AC Waveforms.

Temporary block unprotection is made by holding $\overline{RP}$ at V_{ID}. In this condition previously protected blocks can be programmed or erased. The transition of $\overline{RP}$ from V_{IH} to V_{ID} must slower than t_{PHPHH}. See Tables 17 and 18, Write AC Characterisics and Figure 13., Data Polling DQ7 AC Waveforms. When $\overline{RP}$ is returned from V_{ID} to V_{IH} all blocks temporarily unprotected will be again protected.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

DEVICE OPERATIONS

See Table 4., User Bus Operations (1), Table 5., Read Electronic Signature (following AS instruction or with A9 = V_{ID}) and Table 6., Read Block Protection with AS Instruction.

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register or the Block Protection Status. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. A new operation is initiated either on the following edge of Chip Enable $\overline{E}$ or on any address transition with $\overline{E}$ at V_{IL}.

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Stan-by. The memory is in stan-by when Chip Enable $\overline{E}$ is High and the P/E.C. is idle. The power consumption is reduced to the stan-by level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Stan-by. After 150ns of bus inactivity (no address transition, CE = V_{IL}) and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-stan-by mode where consumption is reduced to the CMOS stan-by value, while outputs still drive the bus (if $\overline{G}$ = V_{IL}).

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory. The manufacturer's code for STMicroelectronics is 20h, the device code is D7h for the M29W800AT (Top Boot) and 5Bh for the M29W800AB (Bottom Boot). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the M29W800A. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 is Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7.

The Electronic Signature can also be read, without raising A9 to V_{ID}, by giving the memory the Instruction AS. If the Byte-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ14 at High impedance; if the Word-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h.

Block Protection. Each block can be separately protected against Program or Erase on programming equipment. Block protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are raised to V_{ID} and an address in the block is applied on A12-A18. Block protection is initiated on the edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100µs, the edge of $\overline{W}$ rising to V_{IH} ends the protection operations. Block protection verify is achieved by bringing $\overline{G}$, $\overline{E}$, A0 and A6 to V_{IL} and A1 to V_{IH}, while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A12-A18 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Block Temporary Unprotection. Any previously protected block can be temporarily unprotected in order to change stored data. The temporary unprotection mode is activated by bringing $\overline{RP}$ to V_{ID}. During the temporary unprotection mode the previously protected blocks are unprotected. A block can be selected and data can be modified by executing the Erase or Program instruction with the $\overline{RP}$ signal held at V_{ID}. When $\overline{RP}$ is returned to V_{IH}, all the previously protected blocks are again protected.

Block Unprotection. All protected blocks can be unprotected on programming equipment to allow updating of bit contents. All blocks must first be protected before the unprotection operation. Block unprotection is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID} and A12, A15 at V_{IH}. Unprotection is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the unprotection operation will end. Unprotection verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A0 is at V_{IL}, A6 and A1 are at V_{IH} and A9 remains at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs A12-A18 has been successfully unprotected. Each block must be separately verified by giving its address in order to ensure that it has been unprotected.

Table 4. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	A0	A1	A6	A9	A12	A15	DQ0-DQ7	DQ8-DQ14	DQ15 A–1
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	A0	A1	A6	A9	A12	A15	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	A0	A1	A6	A9	A12	A15	Data Output	Hi-Z	Address Input
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	A0	A1	A6	A9	A12	A15	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	A12	A15	Data Input	Hi-Z	Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Stan-by	V_{IH}	X	X	V_{IH}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Block Protection (2,4)	V_{IL}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	X	X	X	X	X
Blocks Unprotection (4)	V_{ID}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	X
Block Protection Verify (2,4)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{ID}	A12	A15	Block Protect Status(3)	X	X
Block Unprotection Verify (2,4)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{ID}	A12	A15	Block Protect Status(3)	X	X
Block Temporary Unprotection	X	X	X	V_{ID}	X	X	X	X	X	X	X	X	X	X

Note: 1. X = V_{IL} or V_{IH}.
2. Block Address must be given an A12-A18 bits.
3. See Table 6., Read Block Protection with AS Instruction.
4. Operation performed on programming equipment.

Table 5. Read Electronic Signature (following AS instruction or with A9 = V_{ID})

Org.	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A1	Other Addresses	DQ0-DQ7	DQ8-DQ14	DQ15 A–1
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Don't Care	20h	00h	0
	Device Code	M29W800AT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	D7h	00h	0
		M29W800AB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	5Bh	00h	0

Table 6. Read Block Protection with AS Instruction

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A12-A18	Other Addresses	DQ0-DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	00h

INSTRUCTIONS AND COMMANDS

The Command Interface latches commands written to the memory. Instructions are made up from one or more commands to perform Read Memory Array, Read Electronic Signature, Read Block Protection, Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made of address and data sequences. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the instruction. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Instructions are initialised by two initial Coded cycles which unlock the Command Interface. In addition, for Erase, instruction confirmation is again preceded by the two Coded cycles.

See Table 7., Commands for a summary of Commands.

Coded Cycles

The two Coded cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The Coded cycles consist of writing the data AAh at address AAAh in the Byte-wide configuration and at address 555h in the Word-wide configuration during the first cycle. During the second cycle the Coded cycles consist of writing the data 55h at address 555h in the Byte-wide configuration and at address 2AAh in the Word-wide configuration. In the Byte-wide configuration the address lines A–1 to A10 are valid, in Word-wide A0 to A11 are valid, other address lines are 'don't care'. The Coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Chip Erase Confirm
20h	Reserved
30h	Block Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Block Protection Status
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. A wait state of 10µs is necessary after Read/Reset prior to any valid read if the memory was in an Erase mode when the RD instruction is given. The Read/Reset command is not accepted during Erase and erase Suspend.

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address AAAh in the Byte-wide configuration or address 555h in the Word-wide configuration for command set-up. A subsequent read will output the manufacturer code and the device code or the block protection status depending on the levels of A0 and A1. The manufacturer code, 20h, is output when the addresses lines A0 and A1 are Low, the device code, EEh for Top Boot, EFh for Bottom Boot is output when A0 is High with A1 Low.

The AS instruction also allows access to the block protection status. After giving the AS instruction, A0 is set to V_{IL} with A1 at V_{IH}, while A12-A18 define the address of the block to be verified. A read in these conditions will output a 01h if the block is protected and a 00h if the block is not protected.

Program (PG) Instruction. This instruction uses four write cycles. Both for Byte-wide configuration and for Word-wide configuration. The Program command A0h is written to address AAAh in the Byte-wide configuration or to address 555h in the Word-wide configuration on the third cycle after two Coded cycles. A fourth write operation latches the Address on the falling edge of W or E and the Data to be written on the rising edge and starts the P/E.C. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend. In this case, DQ2 will toggle at the address being programmed.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address AAAh in the Byte-wide configuration or address 555h in the Word-wide configuration on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional block Erase Confirm commands and

block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. The erase will start after the erase timeout period (see Erase Timer Bit DQ3 description).

Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C. is erasing the Block(s). If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before to erasing to FFh. Read operations after the sixth rising edge of W or E output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the Erase Suspend ES instruction. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit DQ2 and DQ6 toggle during the erase operation. They stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit DQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the P/E.C.

Chip Erase (CE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address AAAh in the Byte-wide configuration or the address 555h in the Word-wide configuration on the third cycle after the two Coded cycles. The Chip Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing it to FFh. Read operations after the sixth rising edge of W or E output the Status Register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure.

Erase Suspend (ES) Instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command B0h without any specific address. No Coded cycles are required. It permits reading of data from another block and programming in another block while an erase operation is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle bit DQ6 stops toggling when the P/E.C. is suspended. The Toggle bits will stop toggling between 0.1µs and 15µs after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions. A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in both DQ2 and DQ6 toggling when the data is being programmed.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any Coded cycles.

Table 8. Instructions (1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (2,4)	Read/Reset Memory Array	1+	Addr. (3,7)		X	Read Memory Array until a new write cycle is initiated.					
			Data		F0h						
		3+	Addr. (3,7)	Byte	AAAh	555h	AAAh	Read Memory Array until a new write cycle is initiated.			
				Word	555h	2AAh	555h				
			Data		AAh	55h	F0h				
AS (4)	Auto Select	3+	Addr. (3,7)	Byte	AAAh	555h	AAAh	Read Electronic Signature or Block Protection Status until a new write cycle is initiated. See Note 5 and 6.			
				Word	555h	2AAh	555h				
			Data		AAh	55h	90h				
PG	Program	4	Addr. (3,7)	Byte	AAAh	555h	AAAh	Program Address	Read Data Polling or Toggle Bit until Program completes.		
				Word	555h	2AAh	555h				
			Data		AAh	55h	A0h	Program Data			
BE	Block Erase	6	Addr. (3,7)	Byte	AAAh	555h	AAAh	AAAh	555h	Block Address	Additional Block (8)
				Word	555h	2AAh	555h	555h	2AAh		
			Data		AAh	55h	80h	AAh	55h	30h	30h
CE	Chip Erase	6	Addr. (3,7)	Byte	AAAh	555h	AAAh	AAAh	555h	AAAh	Note 9
				Word	555h	2AAh	555h	555h	2AAh	555h	
			Data		AAh	55h	80h	AAh	55h	10h	
ES (10)	Erase Suspend	1	Addr. (3,7)		X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data		B0h						
ER	Erase Resume	1	Addr. (3,7)		X	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time.					
			Data		30h						

Note: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation (see Tables 15, 16 and Figure 13).
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1, at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output Device code.
6. Block Protection Address: A0, at V_{IL}, A1 at V_{IH} and A15-A18 within the Block will output the Block Protection status.
7. For Coded cycles address inputs A11-A18 are don't care.
8. Optional, additional Blocks addresses must be entered within the erase timeout delay after last write entry, timeout statuscan be verified through DQ3 value (see Erase Timer Bit DQ3 description). When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
9. Read Data Polling, Toggle bits or $\overline{RB}$ until Erase completes.
10. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

STATUS REGISTER

P/E.C. status is indicated during execution by Data Polling on DQ7, detection of Toggle on DQ6 and DQ2, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked. See Table 10., Status Register Bits and Table 9., Polling and Toggle Bits.

Data Polling Bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth W pulse for programming or after the sixth W pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. If all the blocks selected for erasure are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed memory data value. See Figure 15., Data Polling Flowchart and Figure 13., Data Polling DQ7 AC Waveforms. DQ7 will also flag the Erase Suspend mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. For a Read Operation in Erase Suspend mode, DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During Program operation in Erase Suspend Mode, DQ7 will have the same behavior as in the normal program execution outside of the suspend mode.

Toggle Bit (DQ6). When Programming or Erasing operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either G, or E when G is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit DQ6 is valid only during P/E.C. operations, that is after the fourth W pulse for programming or after the sixth W pulse for Erase. If the blocks selected for erasure are protected, DQ6 will toggle for about 100µs and then return back to Read. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different to the block in Erase Suspend. Either E or G toggling will cause DQ6 to toggle. See Figure 16., Data Toggle Flowchart and Figure 14., Data Toggle DQ6, DQ2 AC Waveforms.

Error Bit (DQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming, block erase, or chip erase that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occurred or to which the programmed data belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0'.

Erase Timer Bit (DQ3). This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50µs to 90µs, DQ3 returns to '1'.

Toggle Bit (DQ2). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. It can also be used to identify the block being erased. During Erase or Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will set DQ2 to '1' during erase and to DQ2 during Erase Suspend. During Chip Erase a read operation will cause DQ2 to toggle as all blocks are being erased. DQ2 will be set to '1' during program operation and when erase is complete. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Table 9. Polling and Toggle Bits

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	Note 1
Erase Suspend Read (in Erase Suspend block)	1	1	Toggle
Erase Suspend Read (outside Erase Suspend block)	DQ7	DQ6	DQ2
Erase Suspend Program	$\overline{DQ7}$	Toggle	N/A

Table 10. Status Register Bits

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES).
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C.
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase Suspend on the currently addressed block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block
		1	Program on-going, Erase on-going on another block or Erase Complete	
		DQ	Erase Suspend read on non Erase Suspend block	
1	Reserved			
0	Reserved			

Note: 1. Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.
2. Toggle if the address is within a block being erased.
'1' if the address is within a block not being erased.

MAXIMUM RATING

Table 11. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
$V_{(A9, \overline{E}, \overline{G}, \overline{RP})}$ (2)	A9, $\overline{E}$, $\overline{G}$, $\overline{RP}$ Voltage	–0.6 to 13.5	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns during transitions.
3. Depends on range.

DC AND AC CHARACTERISTICS

Figure 6. AC Testing Input Output Waveform

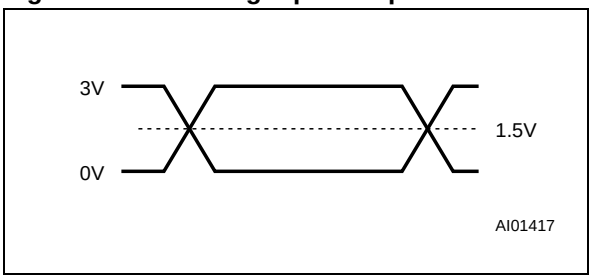


Figure 7. AC Testing Load Circuit

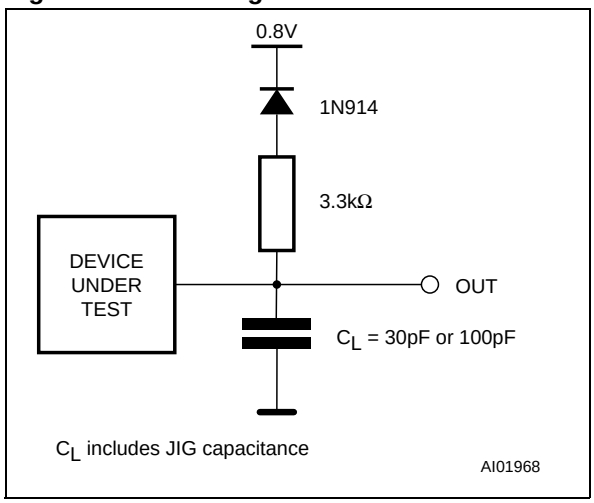


Table 12. AC Measurement Conditions

Input Rise and Fall Times	≤10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Table 13. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 14. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply Current (Read by Word)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		3	10	mA
I_{CC2}	Supply Current (Read by Word)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 6MHz		4.5	10	mA
I_{CC3}	Supply Current (Stan-by)	$\overline{E} = V_{CC}$ ±0.2V		30	100	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Byte program, Block or Chip Erase in progress			20	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V			V
V_{ID}	A9 Voltage (Electronic Signature)		11.5		12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		30	100	µA
V_{LKO} (1)	Supply Voltage (Erase and Program lock-out)		2.0		2.3	V

Note: 1. Sampled only, not 100% tested.

Table 15. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	Test Condition	M29W800AT / M29W800AB				Unit
				80		90		
				V_{CC} = 3.0V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 30pF		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	80		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80		90	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Valid			50		50	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z			50		50	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		30	ns
t_{ELBH} t_{ELBL}	t_{ELFH} t_{ELFL}	Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		30	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{PHEL}	t_{RH}	$\overline{RP}$ High to Chip Enable Low		50		50		ns
t_{PLYH} (1, 3)	t_{RRB} t_{READY}	$\overline{RP}$ Low to Read Mode			10		10	µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width		500		500		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. To be considered only if the Reset pulse is given while the memory is in Erase or Program mode.

Table 16. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	Test Condition	M29W800AT / M29W800AB				Unit
				100		120		
				V_{CC} = 2.7V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 100pF		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Valid			50		60	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z			50		60	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		30	ns
t_{ELBH} t_{ELBL}	t_{ELFH} t_{ELFL}	Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		30	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{PHEL}	t_{RH}	$\overline{RP}$ High to Chip Enable Low		50		50		ns
t_{PLYH} (1, 3)	t_{RRB} t_{READY}	$\overline{RP}$ Low to Read Mode			10		10	µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width		500		500		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. To be considered only if the Reset pulse is given while the memory is in Erase or Program mode.

Figure 8. Read Mode AC Waveforms

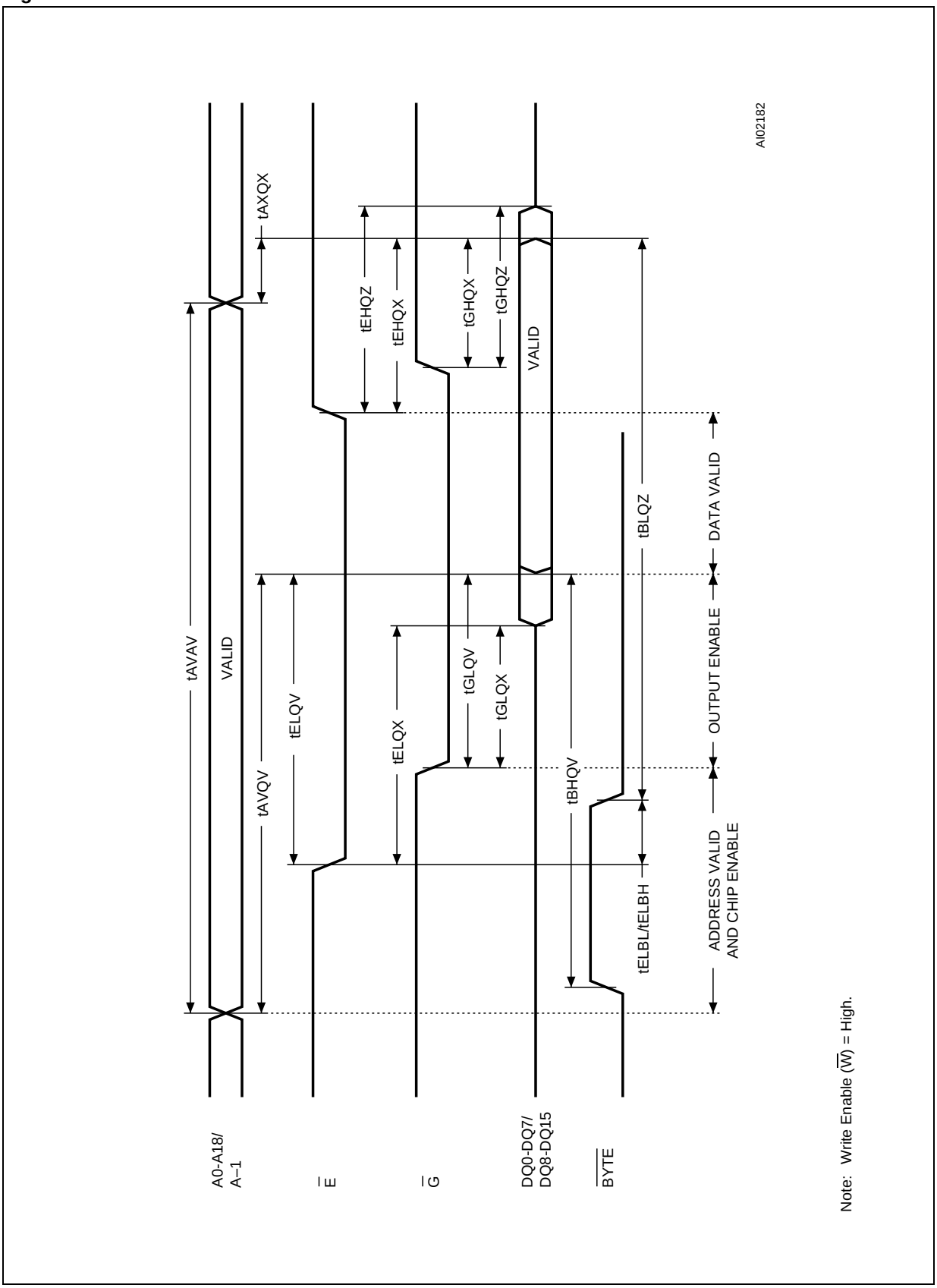


Table 17. Write AC Characteristics, $\overline{W}$ Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W800AT / M29W800AB				Unit
			80		90		
			V_{CC} = 3.0V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 30pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	80		90		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	35		45		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{PHPHH} (1, 2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHRL} (1)	t_{BUSY}	Program Erase Valid to $\overline{RB}$ Delay		90		90	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		35		ns

Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Table 18. Write AC Characteristics, $\overline{W}$ Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W800AT / M29W800AB				Unit
			100		120		
			V_{CC} = 2.7V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 100pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{PHPHH} (1, 2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHRL} (1)	t_{BUSY}	Program Erase Valid to $\overline{RB}$ Delay		90		90	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		50		ns

Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Table 19. Write AC Characteristics, $\overline{E}$ Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W800AT / M29W800AB				Unit
			80		90		
			V_{CC} = 3.0V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 30pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	80		90		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	35		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{EHRL} (1)	t_{BUSY}	Program Erase Valid to $\overline{RB}$ Delay		80		90	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		35		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{PHPHH} (1, 2)	t_{VIDR}	$\overline{RP}$ Rise TIme to V_{ID}	500		500		ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns

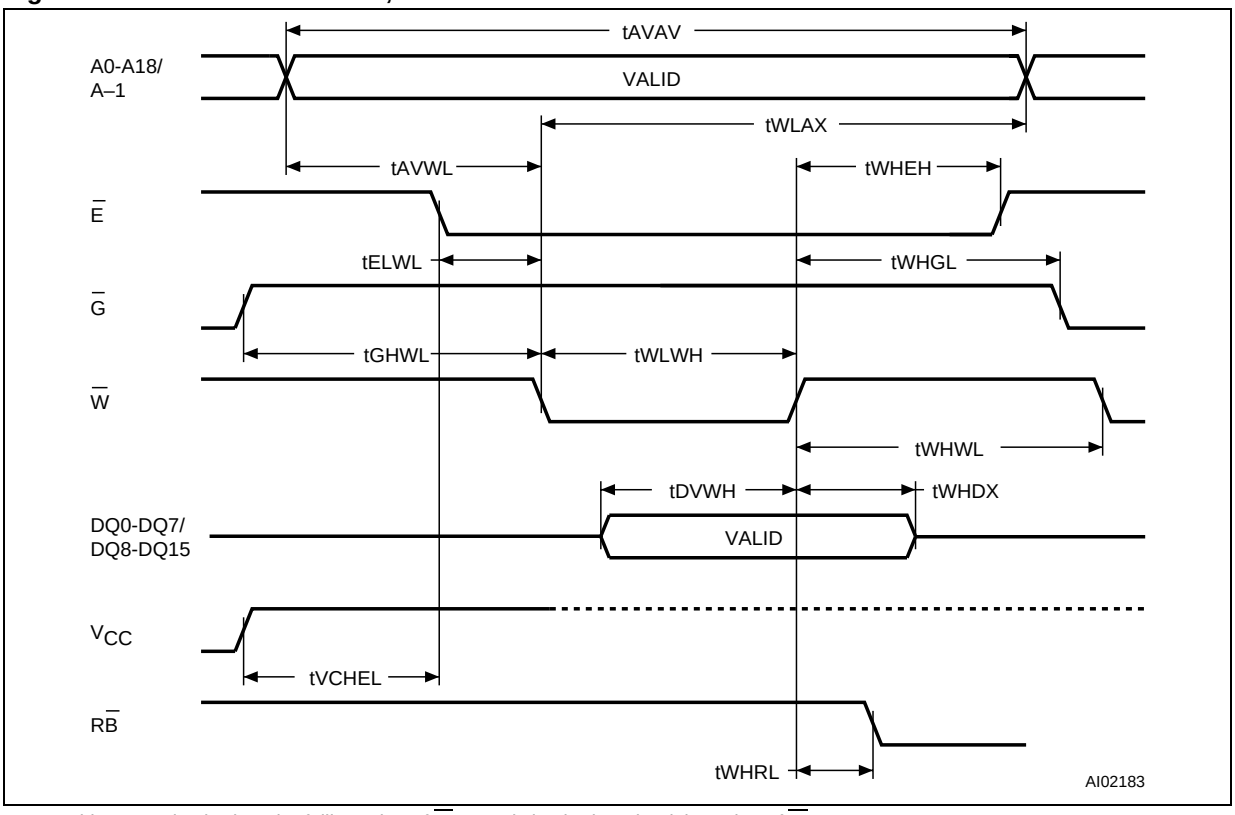
Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Table 20. Write AC Characteristics, $\overline{E}$ Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W800AT / M29W800AB				Unit
			100		120		
			V_{CC} = 2.7V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 100pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	45		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{EHRL} (1)	t_{BUSY}	Program Erase Valid to $\overline{RB}$ Delay		90		90	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		50		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise TIme to V_{ID}	500		500		ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns

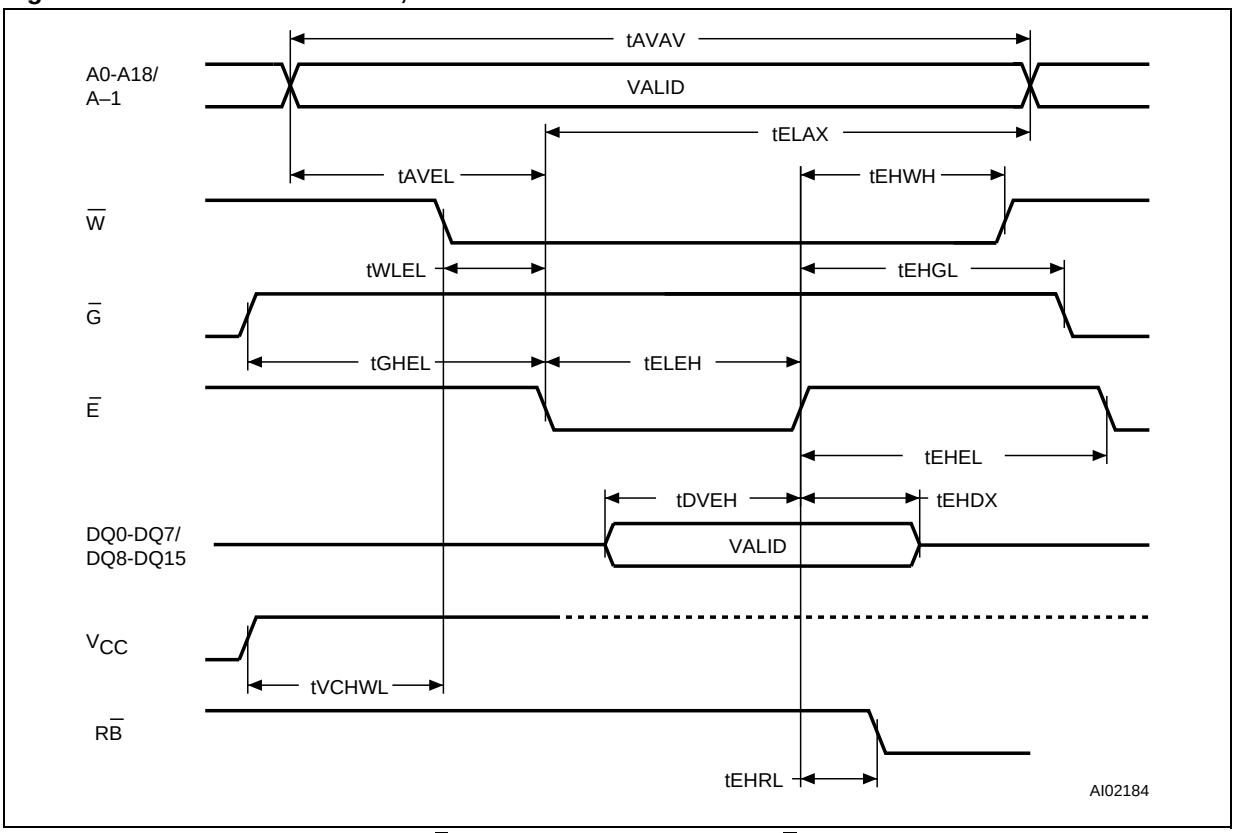
Note: 1. Sampled only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Figure 9. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

Figure 10. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Figure 11. Read and Write AC Characteristics, $\overline{RP}$ Related

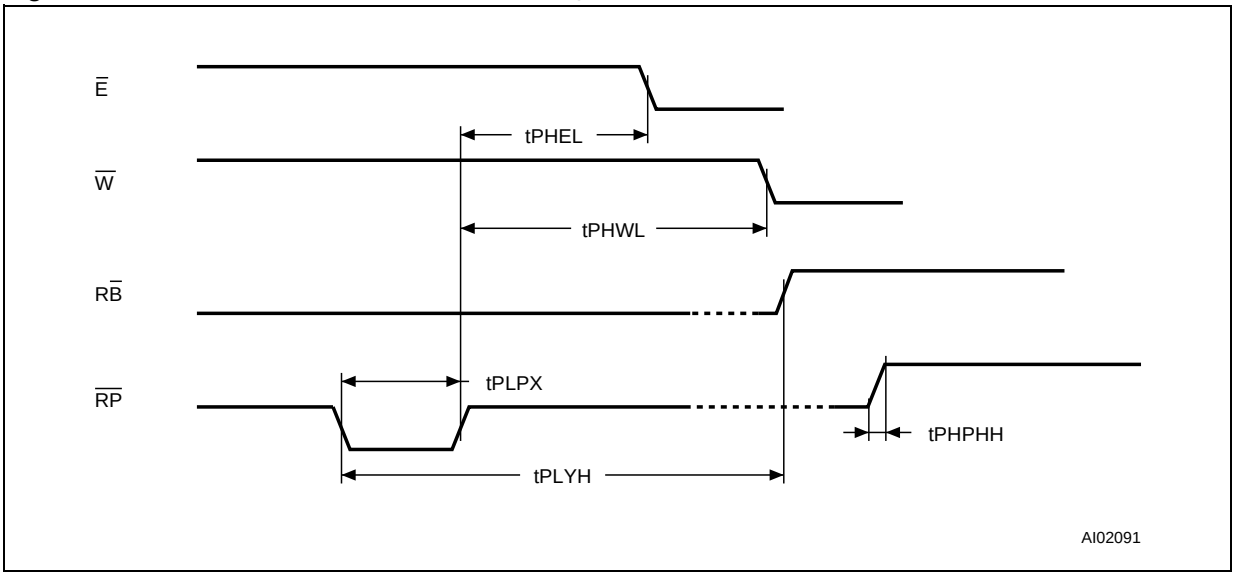


Figure 12. Data Polling and Toggle Bit AC Characteristics (1)

(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Parameter	M29W800AT / M29W800AB				Unit
		80		90		
		V_{CC} = 3.0V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 30pF		
		Min	Max	Min	Max	
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, E Controlled)	10	2400	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, E Controlled)	1.0	60	1.0	60	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		35		35	ns
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, W Controlled)	10	2400	10	2400	ms
	Write Enable High to DQ7 Valid (Chip Erase, W Controlled)	1.0	60	1.0	60	sec
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Table 21. Data Polling and Toggle Bit AC Characteristics (1)

(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Parameter	M29W800AT / M29W800AB				Unit
		100		120		
		V_{CC} = 2.7V to 3.6V CL = 30pF		V_{CC} = 2.7V to 3.6V CL = 100pF		
		Min	Max	Min	Max	
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, E Controlled)	10	2400	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, E Controlled)	1.0	60	1.0	60	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		40		50	ns
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, W Controlled)	10	2400	10	2400	ms
	Write Enable High to DQ7 Valid (Chip Erase, W Controlled)	1.0	60	1.0	60	sec
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1.0	60	1.0	60	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 13. Data Polling DQ7 AC Waveforms

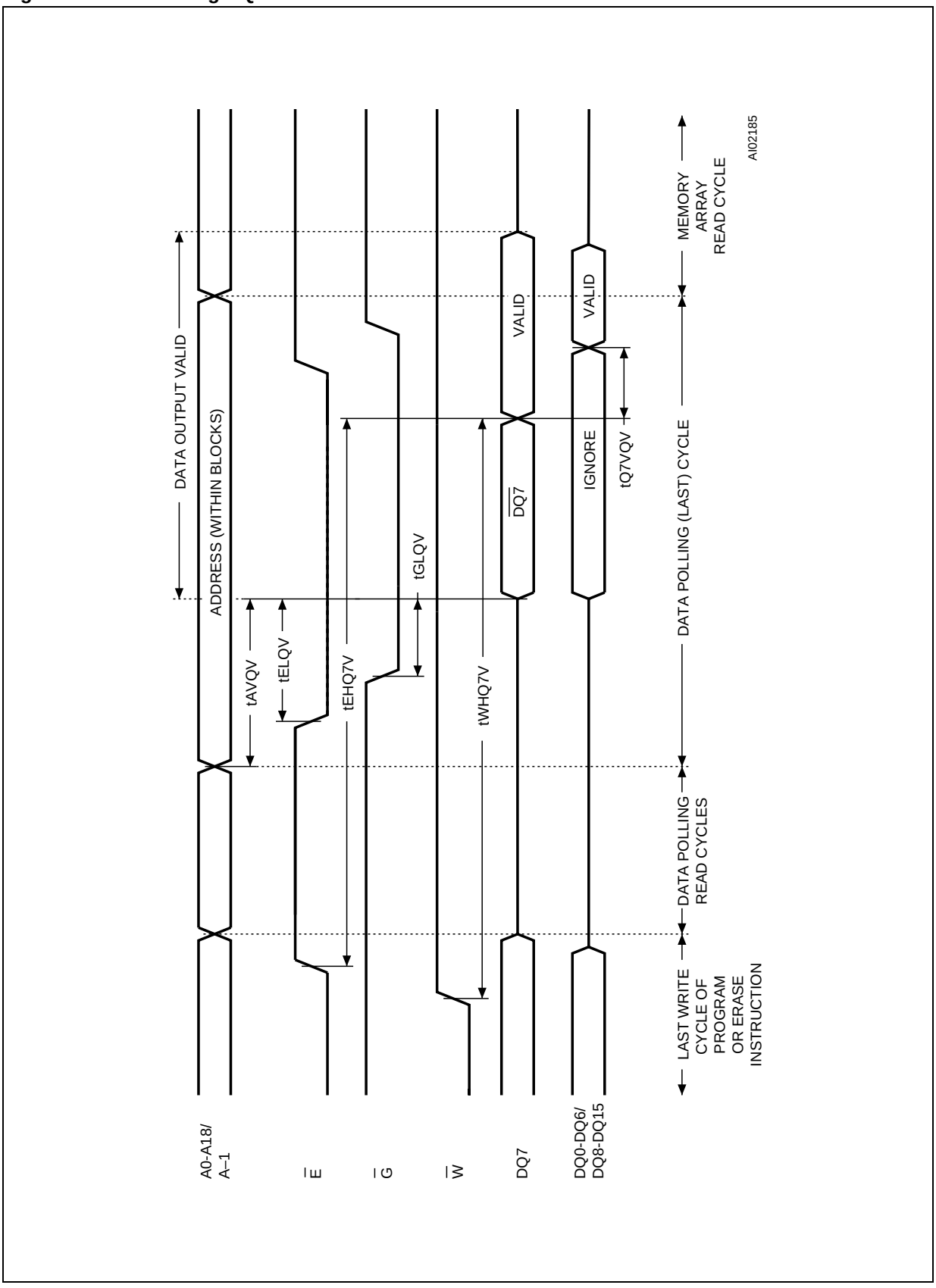


Figure 14. Data Toggle DQ6, DQ2 AC Waveforms

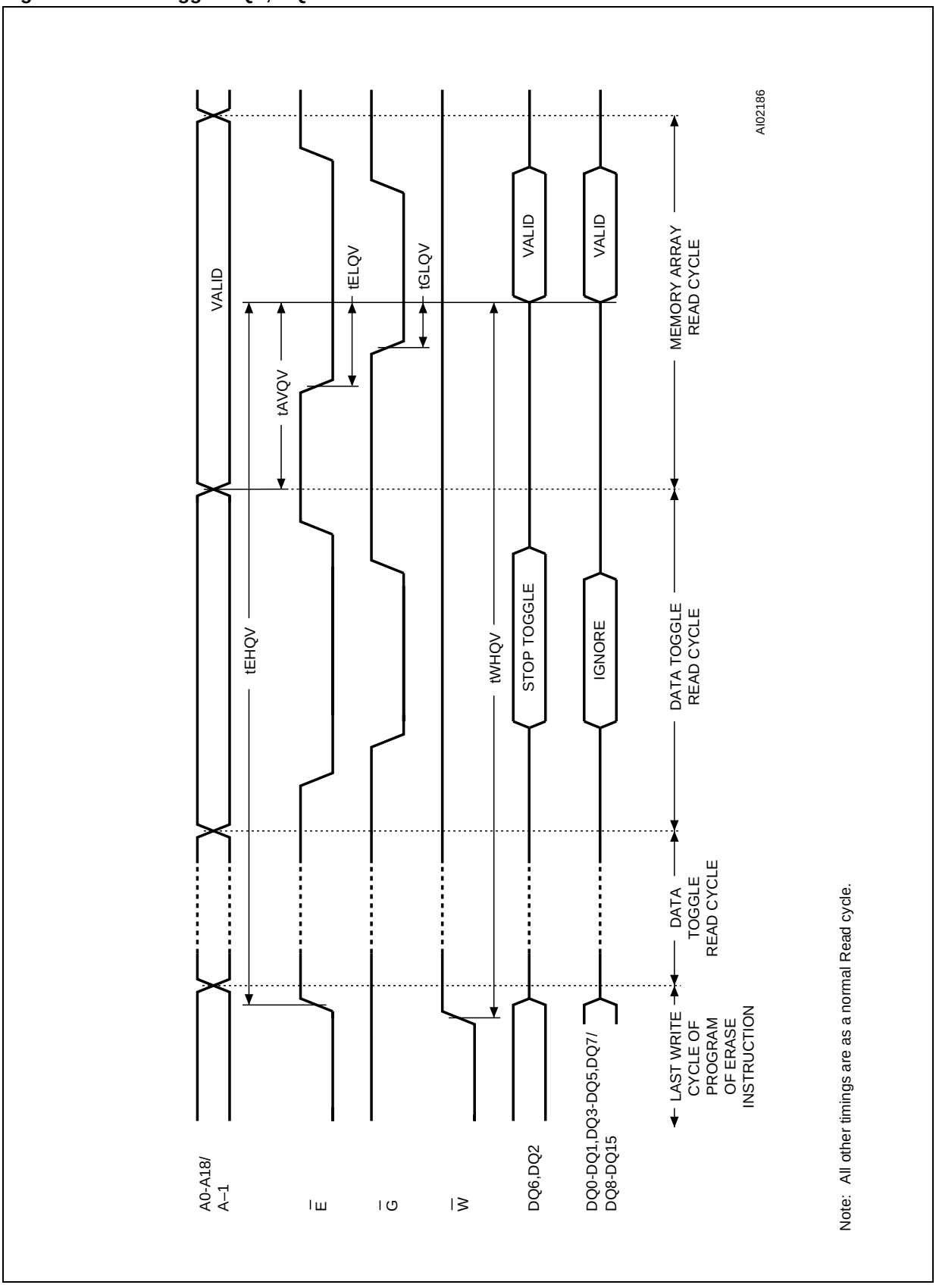


Figure 15. Data Polling Flowchart

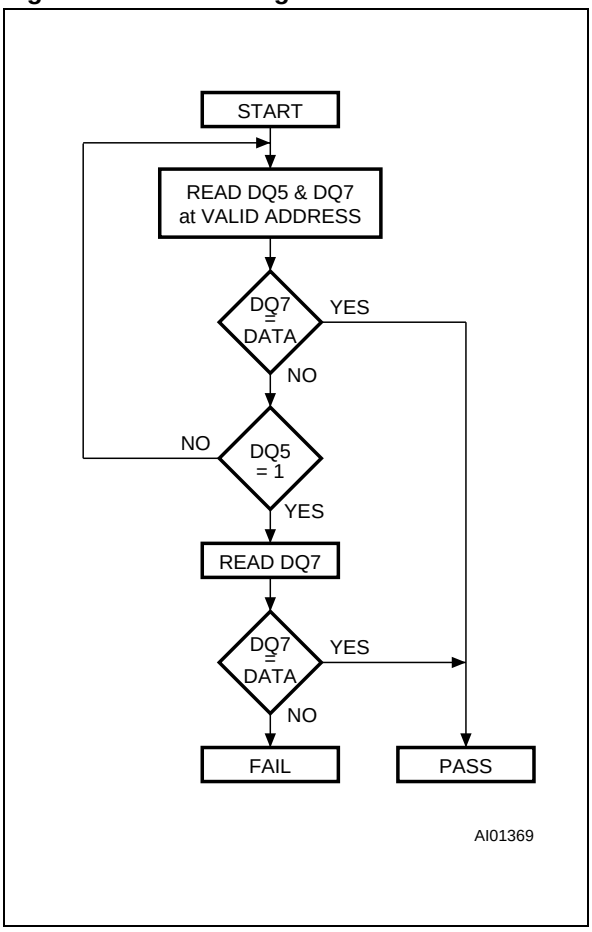


Figure 16. Data Toggle Flowchart

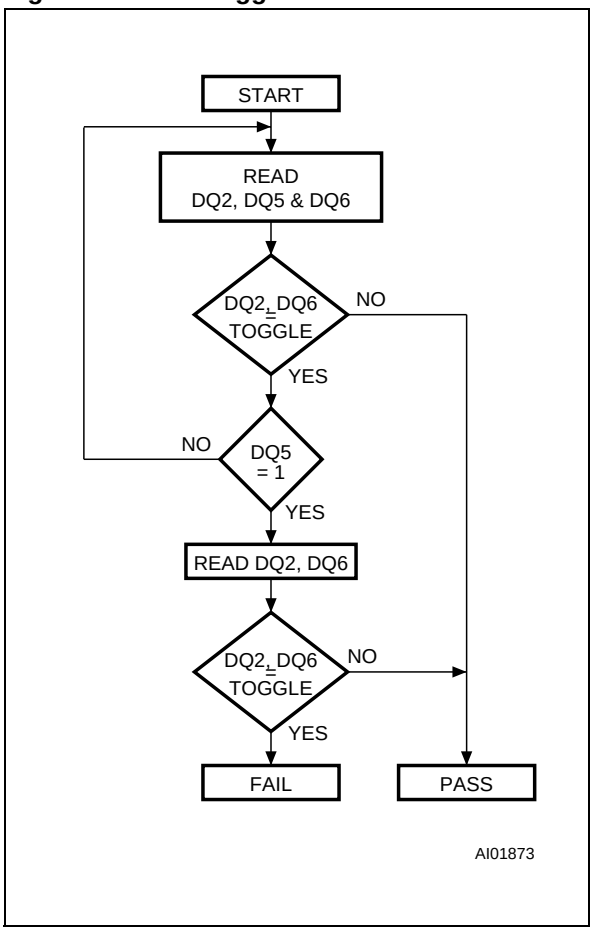


Table 22. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 2.7V to 3.6V)

Parameter	M29W800AT / M29W800AB				Unit
	Min	Typ	Typical after (1) 100k W/E Cycles	Max	
Chip Erase (Preprogrammed, V_{CC} = 2.7V)		10	10		sec
Chip Erase (V_{CC} = 2.7V)		15	15		sec
Main Block Erase (V_{CC} = 2.7V)		1.5		15	sec
Chip Program (Byte) (1)		10	10		sec
Chip Program (Word) (1)		5	5		sec
Byte/Word Program		10	10		µs
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. Excluded the time required to execute bus cycles sequence for program operation.

POWER SUPPLY

Power Up

The memory Command Interface is reset on power up to Read Array. The device does not accept commands on the first rising edge of W, if both W and $\overline{E}$ are at V_{IL} with $\overline{G}$ at V_{IH} during power-up. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

SECURITY PROTECTION MEMORY AREA

The M29W800A features a security protection memory area. It consists of a memory block of 256 bytes or 128 words which is programmed in the ST factory to store a unique code that uniquely identifies the part.

This memory block can be read by using the Read Security Data instruction (RDS) as shown in Table 23.

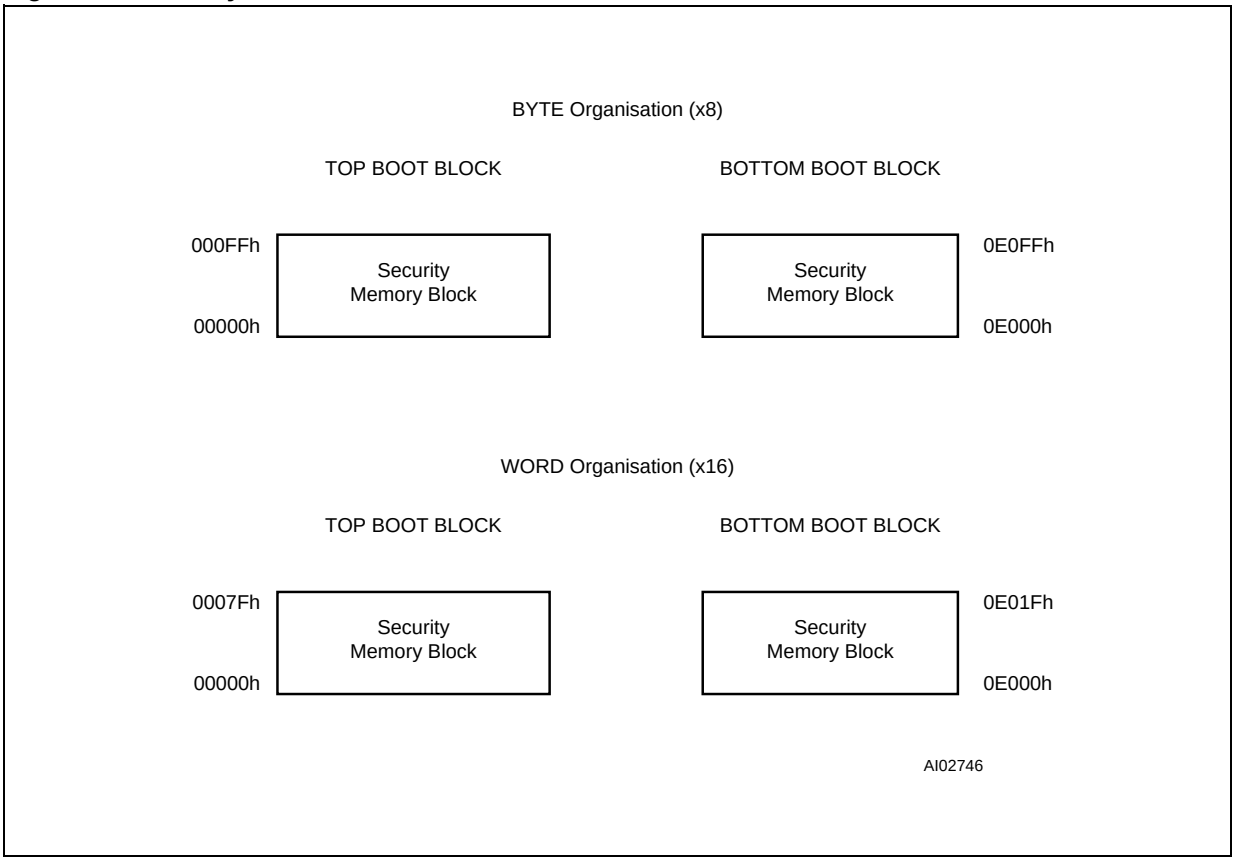
Read Security Data (RDS) Instruction. This RDS uses a single write cycle instruction: the command B8h is written to the address AAh. This sets the memory to the Read Security mode. Any successive read attempt will output the addressed Security byte until a new write cycle is initiated.

Table 23. Security Block Instruction

Mne.	Instr.	Cyc.		Unlock Cycle	2nd Cyc.
				1st Cyc.	
RDS	Read Security Data	1	Addr. (1)	AAh	Read OTP Data until a new write cycle is initiated.
			Data (2)	B8h	

Note: 1. Address bits A10-A19 are don't care for coded address inputs.
2. Data bits DQ8-DQ15 are don't care for coded address inputs.

Figure 17. Security Block Address Table



PACKAGE MECHANICAL

Figure 18. TSOP48, 48 Lead Plastic Thin Small Outline, 12x20 mm - Package Outline

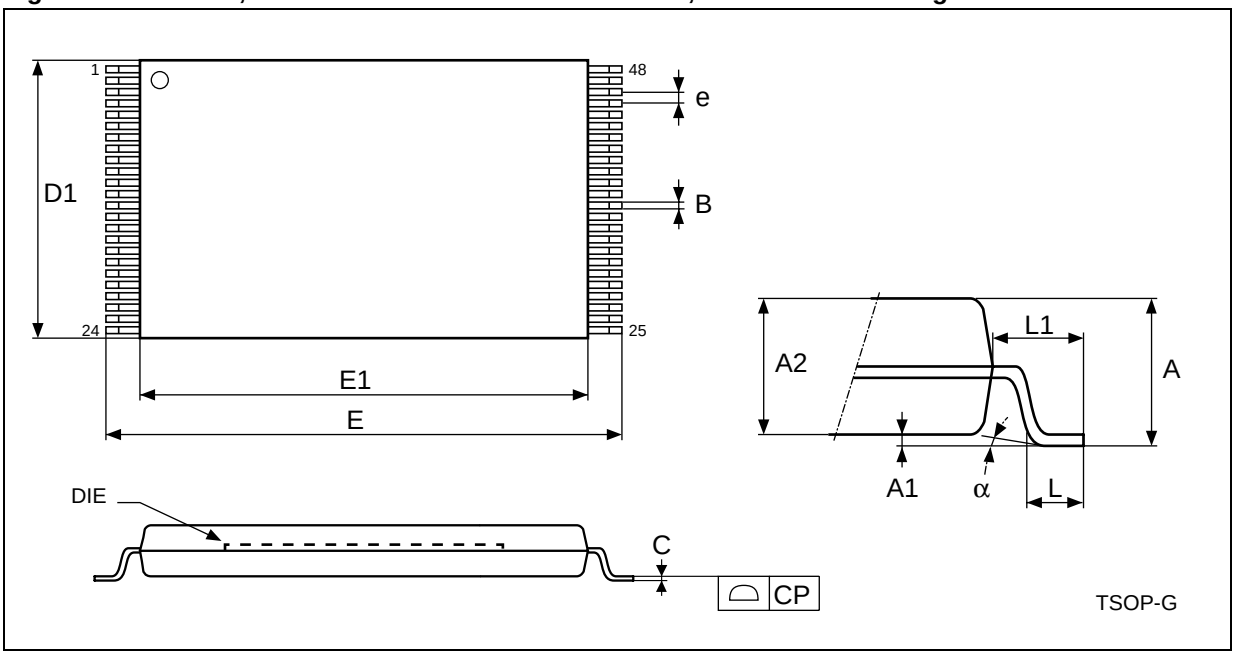


Table 24. TSOP48, 48 Lead Plastic Thin Small Outline, 12x20 mm - Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
a	3	0	5	3	0	5

Figure 19. TFBGA48, 6 x 8 Ball Array, 0.8mm Pitch - Bottom View Package Outline

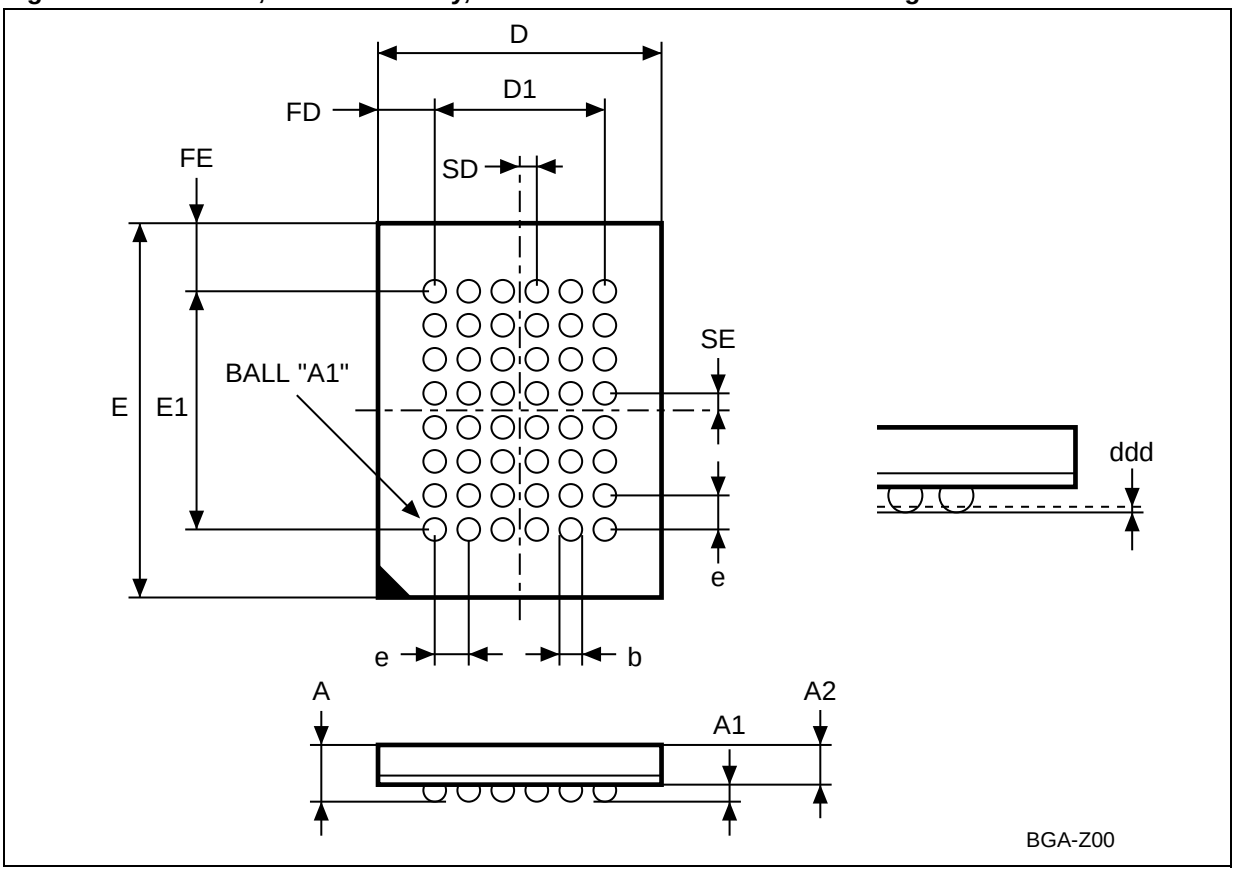


Table 25. TFBGA48, 6 x 8 Ball Array, 0.8mm Pitch - Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2			1.000			0.0394
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	4.000	–	–	0.1575	–	–
ddd			0.100			0.0039
E	9.000	8.900	9.100	0.3543	0.3504	0.3583
e	0.800	–	–	0.0315	–	–
E1	5.600	–	–	0.2205	–	–
FD	1.000	–	–	0.0394	–	–
FE	1.700	–	–	0.0669	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

Figure 20. TFBGA48 Daisy Chain Connections (Top view through package)

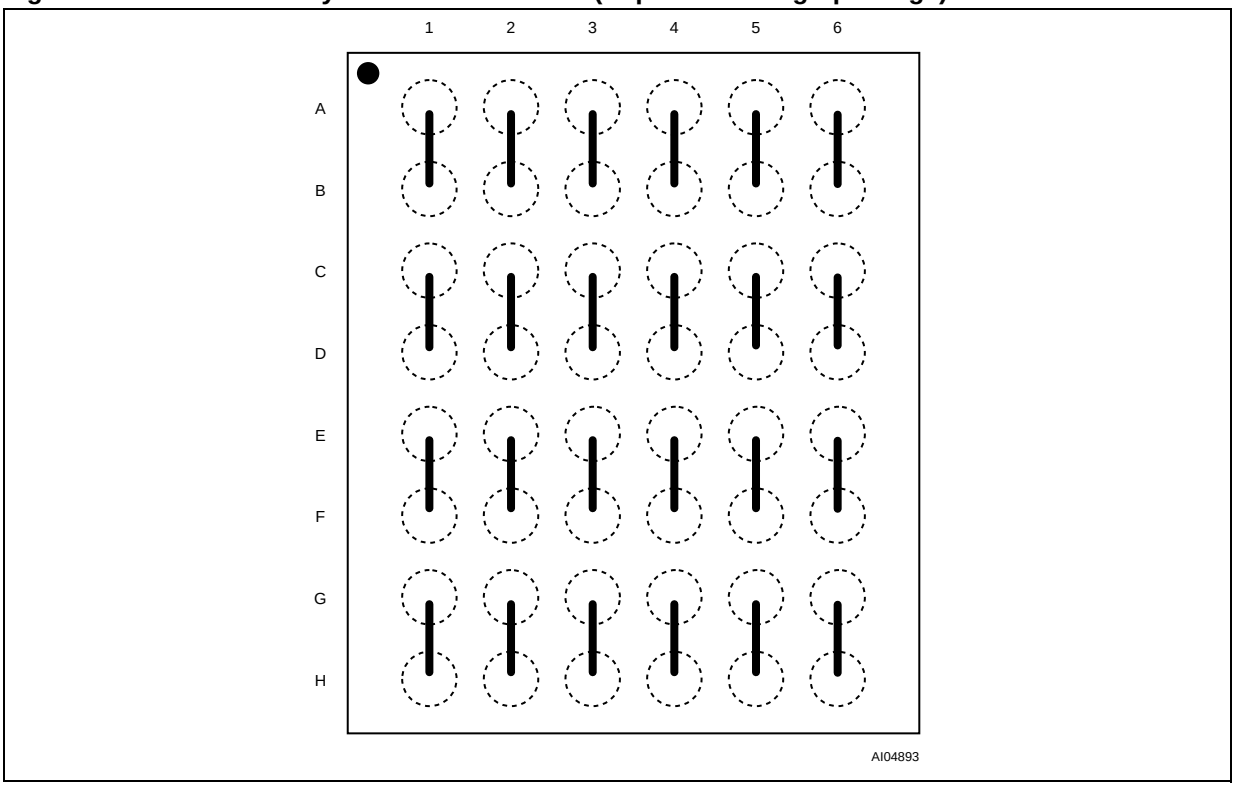


Figure 21. TFBGA48 Daisy Chain - PCB Connections (Top view through package)

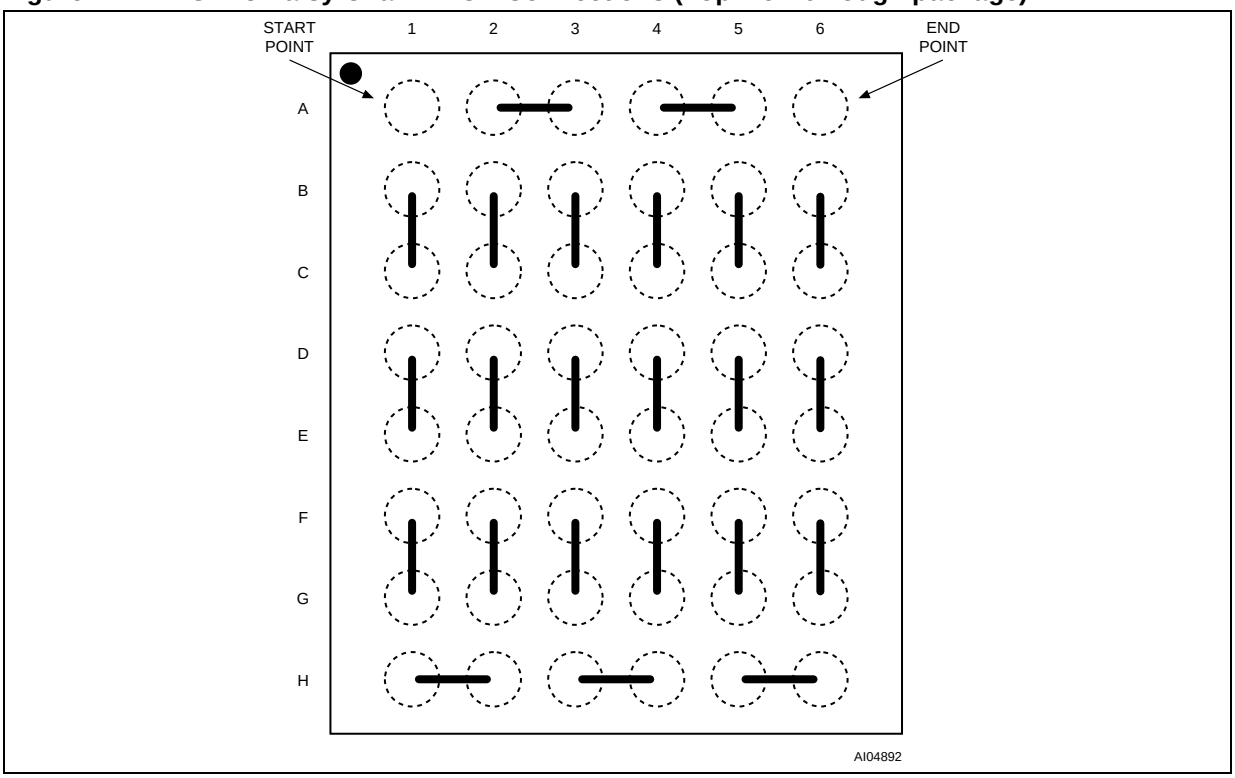


Figure 22. SO44 , Small Outline, 525mm Body Width - Package Outline

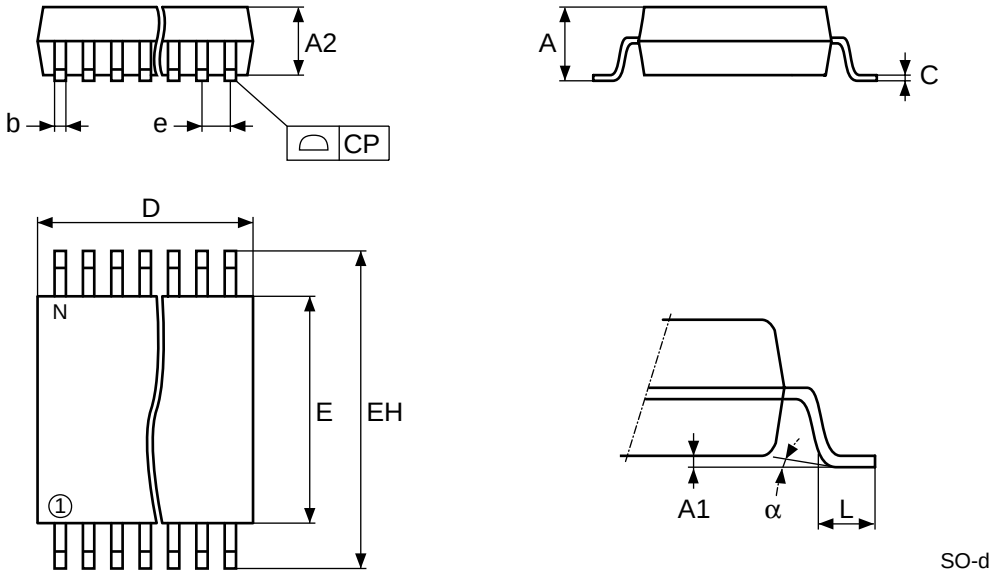


Table 26. SO44 , Small Outline, 525mm Body Width Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.80			0.1102
A1		0.10			0.0039	
A2	2.30	2.20	2.40	0.0906	0.0866	0.0945
b	0.40	0.35	0.50	0.0157	0.0138	0.0197
C	0.15	0.10	0.20	0.0059	0.0039	0.0079
CP			0.08			0.0030
D	28.20	28.00	28.40	1.1102	1.1024	1.1181
E	13.30	13.20	13.50	0.5236	0.5197	0.5315
EH	16.00	15.75	16.25	0.6299	0.6201	0.6398
e	1.27	–	–	0.0500	–	–
L	0.80			0.0315		
a			8			8
N	44			44		

PART NUMBERING

Table 27. Ordering Information Scheme

Example: M29W800AT 80 N 1 T

Device Type
M29

Operating Voltage
W = 2.7 to 3.6V

Device Function
800A = 8 Mbit (1Mb x8 or 512Kb x16), Boot Block

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
80 = 80 ns
90 = 90 ns
100 = 100 ns
120 = 120 ns

Package
N = TSOP48: 12 x 20 mm
M = SO44
ZA = TFBGA48: 0.8 mm pitch

Temperature Range
1 = 0 to 70 °C
5 = –20 to 85°C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Table 28. Daisy Chain Ordering Scheme

Example: M29 DCL1-8 T

Device Type
M29

Daisy Chain
DCL1-8 = Daisy Chain Level 1 for 8 Mbit parts

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 29. Revision History

Date	Version	Description
November 1998	-01	First issue
February 1999	-02	Removed TSOP48 Package Reverse Pinout
March 1999	-03	Program, Erase Times and Erase Endurance Cycles change
02/09/00	-04	New document template Document type: from Preliminary Data to Data Sheet Program, Erase Times and Endurance Cycles change (Table 22) TFBGA Package Mechanical Data change TFBGA Package Outline drawing change
03/06/00	-05	Program Erase Times change (Table 22)
6/21/01	-06	TFBGA48 package mechanical ouline and data changed Daisy Chain commercial code defined (Table 28) TFBGA48 Daisy Chain diagrams, Package and PCB Connections added (Figure 20 and 21)
24-Jan-2002	-07	-90 version changed to Vcc=2.7 to 3.6V; -120 version changed to CL=100pF
09-Mar-2004	8.0	INSTRUCTIONS AND COMMANDS section: description of Block Erase (BE) and Erase Suspend (ES) instructions updated.

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