PRELIMINARY

8XC196NU COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- **50 MHz Operation**†
- **1 Mbyte of Linear Address Space**
- **Optional 48 Kbytes of ROM**
- **1 Kbyte of Register RAM**
- **Register-register Architecture**
- **Footprint and Functionally Compatible Upgrade for the 8XC196NP**
- **32 I/O Port Pins**
- **16 Prioritized Interrupt Sources**
- **4 External Interrupt Pins and NMI Pin**
- **2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability**
- **3 Pulse-width Modulator (PWM) Outputs with High Drive Capability**
- **Full-duplex Serial Port with Dedicated Baud-rate Generator**
- **Peripheral Transaction Server**

† 40 MHz standard; 50 MHz is Speed Premium

- **Chip-select Unit**
  - **— 6 Chip-select Pins**
  - **— Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select**
  - **— Programmable Wait States (0–3) for Each Chip Select**
  - **— Programmable Bus Width (8- or 16-bit) for Each Chip Select**
  - **— Programmable Address Range for Each Chip Select**
- **Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels**
- **Multiply and Accumulate Executes in 640 ns Using the 32-bit Hardware Accumulator**
- **960 ns 32/16 Unsigned Division**
- **100-pin SQFP or 100-pin QFP Package**
- **Complete System Development Support**
- **High-speed CHMOS Technology**

The 8XC196NU is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation.

February 1997 **Order Number:** 272644-004

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641
or call 1-800-548-4725

8XC196NU Commercial
CHMOS 16-bit Microcontroller

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1.0 PRODUCT OVERVIEW

The 8XC196NU is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation.

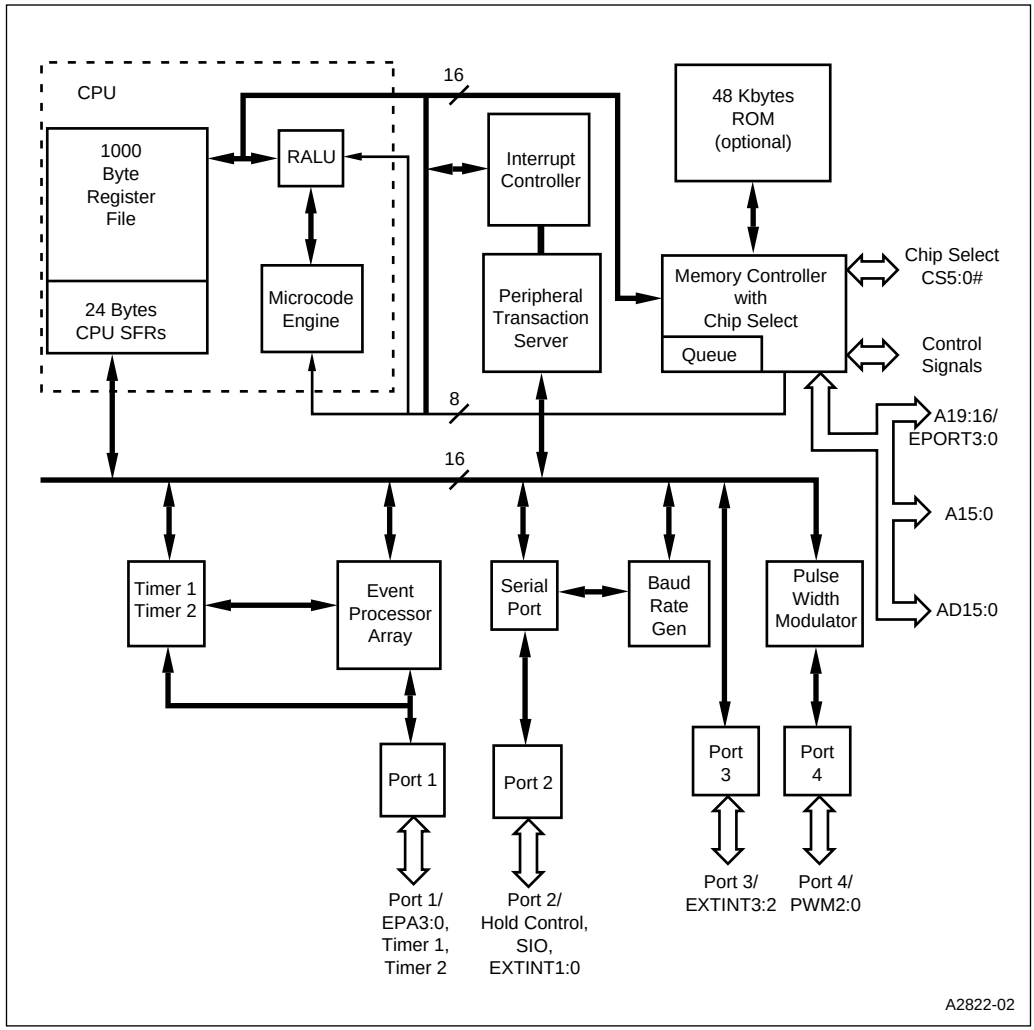


Figure 1. 8XC196NU Block Diagram

2.0 NOMENCLATURE OVERVIEW

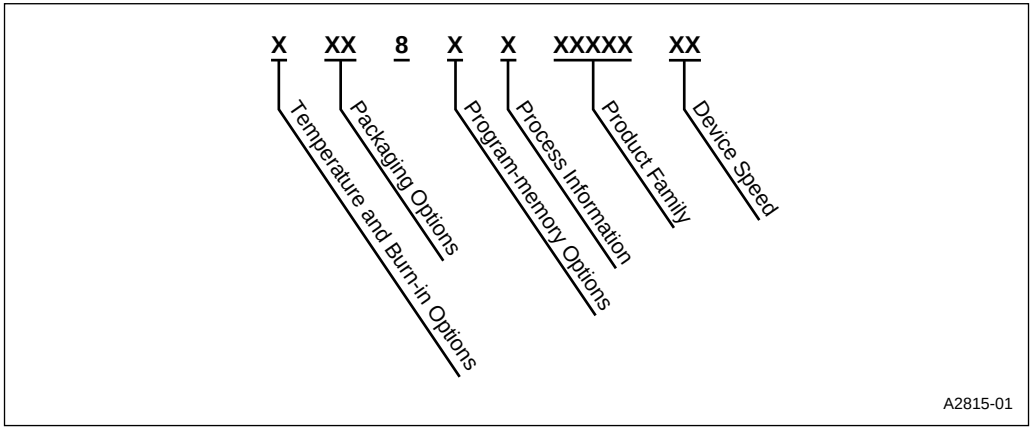


Figure 2. The 8XC196NU Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S	QFP
	SB	SQFP
Program–memory Options	0	Without ROM
	3	ROM
Process Information	C	CHMOS
Product Family	196NU	—
Device Speed	no mark	40 MHz
	50	50 MHz

3.0 PINOUT

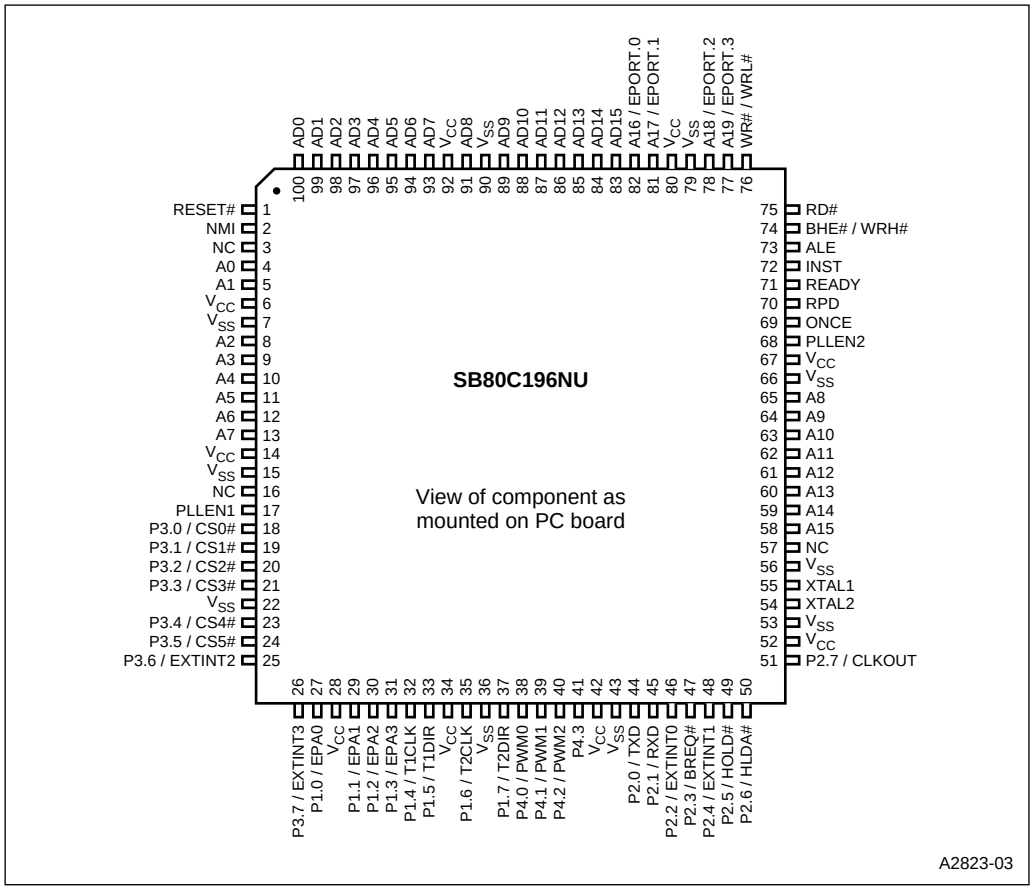


Figure 3. 80C196NU 100-pin SQFP Package

Table 2. 80C196NU 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	V_{CC}	77	EPORT.3/A19
3	NC	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC	41	P4.3	66	V_{SS}	91	AD8
17	PLLEN1	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	PLLEN2	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

NOTE: To be compatible with future products, tie the NC (no connection) pins as follows: Pin 57 = V_{SS}, Pin 16 = V_{CC}, and Pin 3 = NC.

Table 3. 80C196NU 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	4
A1	5
A2	8
A3	9
A4	10
A5	11
A6	12
A7	13
A8	65
A9	64
A10	63
A11	62
A12	61
A13	60
A14	59
A15	58
A16	82
A17	81
A18	78
A19	77
AD0	100
AD1	99
AD2	98
AD3	97
AD4	96
AD5	95
AD6	94
AD7	93
AD8	91
AD9	89
AD10	88
AD11	87

Address & Data (continued)	
Name	**Pin**
AD12	86
AD13	85
AD14	84
AD15	83

Bus Control & Status	
Name	**Pin**
ALE	73
BHE#/WRH#	74
BREQ#	47
HOLD#	49
HLDA#	50
INST	72
RD#	75
READY	71
WR#/WRL#	76

Processor Control	
Name	**Pin**
CLKOUT	51
EXTINT0	46
EXTINT1	48
EXTINT2	25
EXTINT3	26
NMI	2
ONCE	69
RESET#	1
RPD	70
XTAL1	55
XTAL2	54
PLLEN1	17
PLLEN2	68

Input/Output	
Name	**Pin**
CS0#/P3.0	18
CS1#/P3.1	19
CS2#/P3.2	20
CS3#/P3.3	21
CS4#/P3.4	23
CS5#/P3.5	24
EPA0/P1.0	27
EPA1/P1.1	29
EPA2/P1.2	30
EPA3/P1.3	31
EPORT.0	82
EPORT.1	81
EPORT.2	78
EPORT.3	77
P2.2	46
P2.3	47
P2.4	48
P2.5	49
P2.6	50
P2.7	51
P3.6	25
P3.7	26
P4.3	41
PWM0/P4.0	38
PWM1/P4.1	39
PWM2/P4.2	40
RXD/P2.1	45
T1CLK/P1.4	32
T1DIR/P1.5	33
T2CLK/P1.6	35
T2DIR/P1.7	37
TXD/P2.0	44

Power & Ground	
Name	**Pin**
V_{CC}	6
V_{CC}	14
V_{CC}	28
V_{CC}	34
V_{CC}	42
V_{CC}	52
V_{CC}	67
V_{CC}	80
V_{CC}	92
V_{SS}	7
V_{SS}	15
V_{SS}	22
V_{SS}	36
V_{SS}	43
V_{SS}	53
V_{SS}	56
V_{SS}	66
V_{SS}	79
V_{SS}	90

No Connection	
Name	**Pin**
NC	3
NC	16
NC	57

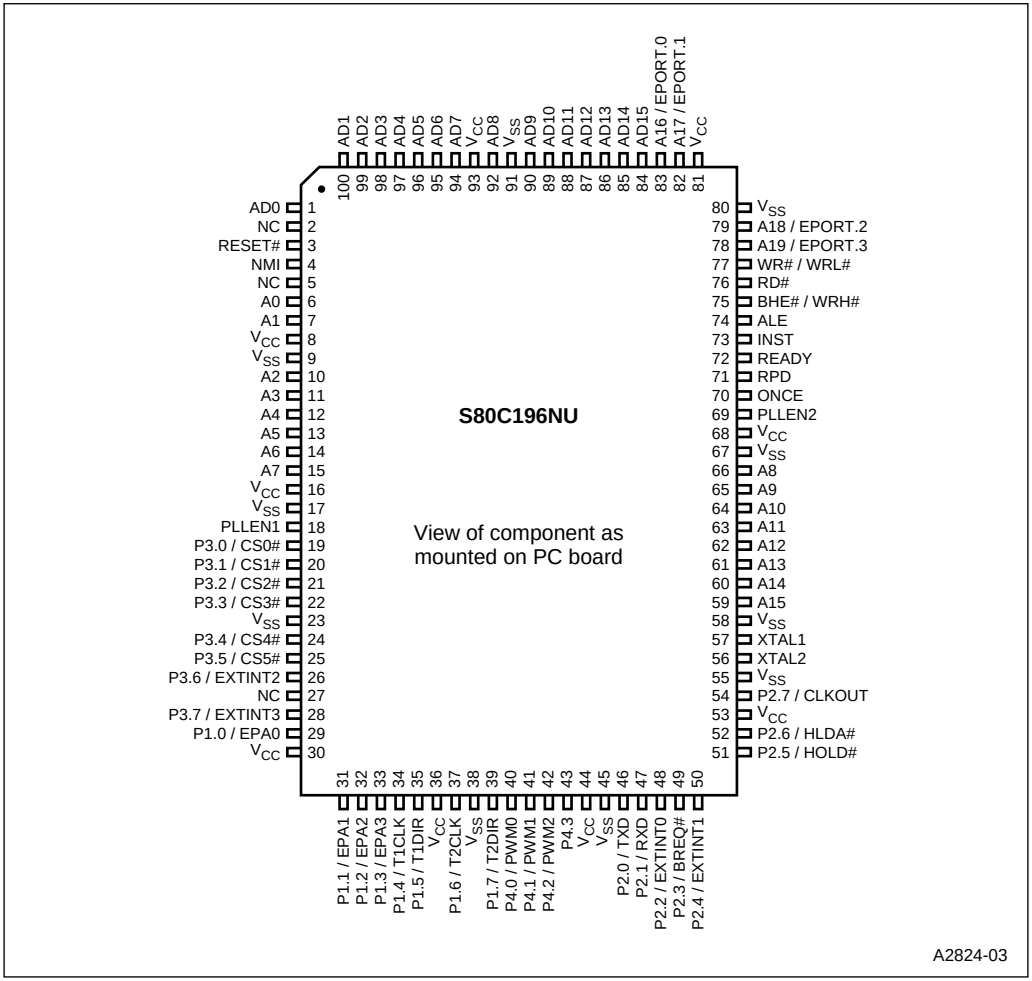


Figure 4. 80C196NU 100-pin QFP Package

Table 4. 80C196NU 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC	27	NC	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	NC	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

NOTE: To be compatible with future proliferations, tie the NC (no connect) pin as follows:

Pin 2 = V_{SS}
Pin 5 = EA# on products with internal memory (V_{CC} = internal memory, V_{SS} = external memory)
Pin 27 = V_{CC}

Table 5. 80C196NU 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	**Pin**
AD12	87
AD13	86
AD14	85
AD15	84

Bus Control & Status	
Name	**Pin**
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	**Pin**
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69

Input/Output	
Name	**Pin**
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	**Pin**
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	**Pin**
NC	2
NC	5
NC	27

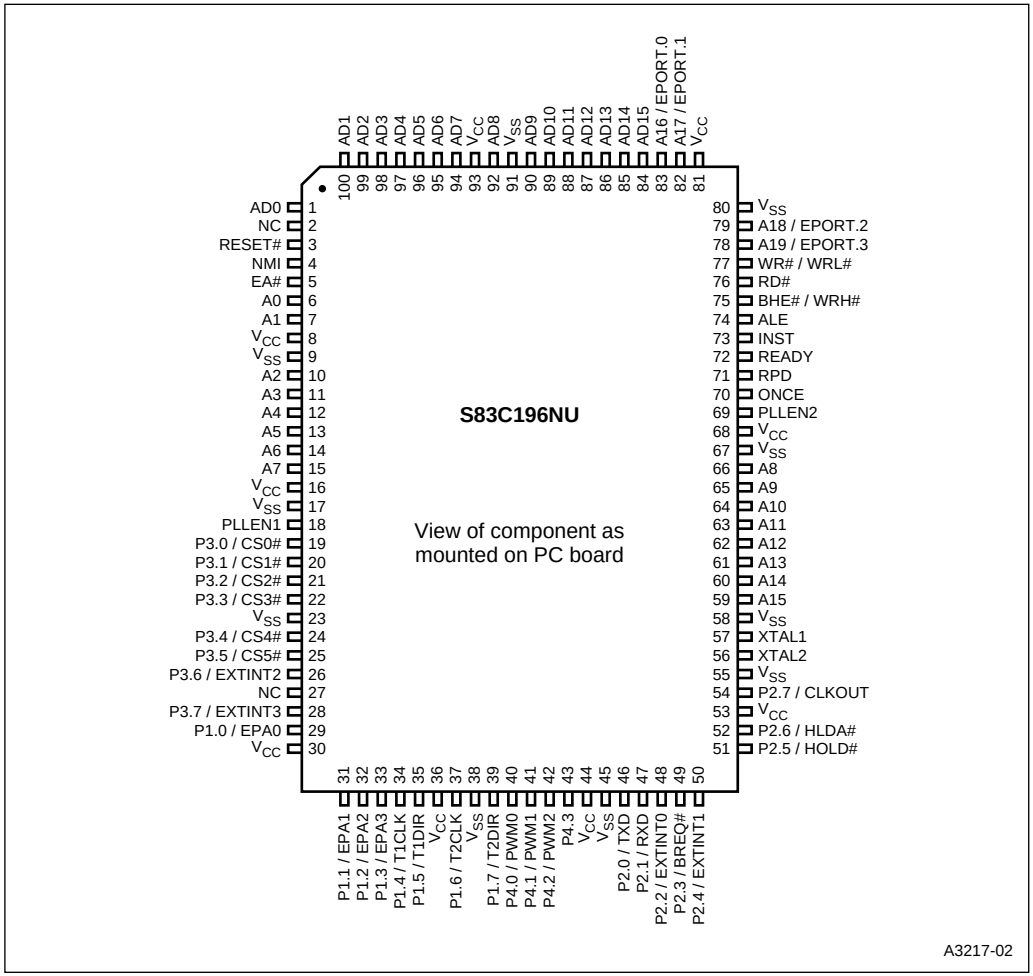


Figure 5. 83C196NU 100-pin QFP Package

Table 6. 83C196NU 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC	27	NC	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	EA#	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

NOTE: To be compatible with future proliferations, tie the NC (no connect) pins as follows:

Pin 2 = V_{SS}
Pin 27 = V_{CC}.

Table 7. 83C196NU 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	**Pin**
AD12	87
AD13	86
AD14	85
AD15	84
Bus Control & Status	
Name	**Pin**
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	**Pin**
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69
EA#	5

Input/Output	
Name	**Pin**
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	**Pin**
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	**Pin**
NC	2
NC	27

4.0 SIGNALS

Table 8. Signal Descriptions

Name	Type	Description
A15:0	I/O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A19:16	I/O	Address Lines 16–19 These address lines provide address bits 16–19 during the entire external memory cycle, supporting extended addressing of the 1 Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 20 external address pins (A19:0) are implemented. The internal address space is 16 Mbytes (000000–FFFFFFH) and the external address space is 1 Mbyte (00000–FFFFFH). The device resets to FF2080H in internal memory or F2080H in external memory. A19:16 are multiplexed with EPORT.3:0.
AD15:0	I/O	Address/Data Lines The functions of these pins depend on the bus size and mode. When a bus access is not occurring, these pins revert to their I/O port function. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). ALE differs from ADV# in that it does not remain active during the entire bus cycle. An external latch can use this signal to demultiplex the address bits 0–15 from the address/data bus in multiplexed mode.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
BHE#	O	Byte High Enable† During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only BHE# is multiplexed with WRH#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). BREQ# is multiplexed with P2.3.
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (f). CLKOUT has a 50% duty cycle. CLKOUT is multiplexed with P2.7.
CS5#:0	O	Chip-select Lines 0–5 The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x*. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external). CS5:0# is multiplexed with P3.5:0.
EA#	I	External Access This active-low input signal determines whether memory accesses to special purpose and program memory partitions (FF2000–FFDFFFH) are directed to internal or external memory. These memory accesses are directed to internal memory if EA# is deasserted and to external memory if EA# is asserted. For an access to any other memory location, the value of EA# is irrelevant. EA# is not latched and can be switched dynamically during normal operating mode. Be sure to thoroughly consider the issues, such as different access times for internal and external memory, before using this dynamic switching capability. Always connect EA# to V_{SS} when using a microcontroller that has no internal nonvolatile memory.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
EPA3:0	I/O	Event Processor Array (EPA) Input/Output pins These are the high-speed input/output pins for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin. EPA3:0 are multiplexed with P1.3:0.
EPORT.3:0	I/O	Extended Addressing Port This is a standard, 4-bit, bidirectional I/O port. EPORT.3:0 are multiplexed with A19:16.
EXTINT3:0	I	External Interrupts In normal operating mode, a rising edge on EXTINT*x* sets the EXTINT*x* interrupt pending bit. EXTINT*x* is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In standby and powerdown modes, asserting the EXTINT*x* signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT0 is multiplexed with P2.2, EXTINT1 is multiplexed with P2.4, EXTINT2 is multiplexed with P3.6, and EXTINT3 is multiplexed with P3.7.
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HLDA# is multiplexed with P2.6.
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HOLD# is multiplexed with P2.5.
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent accidental entry into ONCE mode, connect the ONCE pin to V_{SS}.
P1.7:0	I/O	Port 1 This is a standard bidirectional port that is multiplexed with individually selectable special-function signals. Port 1 is multiplexed as follows: P1.0/EPA0, P1.1/EPA1, P1.2/EPA2, P1.3/EPA3, P1.4/T1CLK, P1.5/T1DIR, P1.6/T2CLK, and P1.7/T2DIR.
P2.7:0	I/O	Port 2 This is a standard bidirectional port that is multiplexed with individually selectable special-function signals. Port 2 is multiplexed as follows: P2.0/TXD, P2.1/RXD, P2.2/EXTINT0, P2.3/BREQ#, P2.4/EXTINT1, P2.5/HOLD#, P2.6/HLDA#, and P2.7/CLKOUT.
P3.7:0	I/O	Port 3 This is an 8-bit, bidirectional, standard I/O port. Port 3 is multiplexed as follows: P3.0/CS0#, P3.1/CS1#, P3.2/CS2#, P3.3/CS3#, P3.4/CS4#, P3.5/CS5#, P3.6/EXTINT2, and P3.7/EXTINT3.
P4.3:0	I/O	Port 4 This is a 4-bit, bidirectional, standard I/O port with high-current drive capability. Port 4 is multiplexed as follows: P4.0/PWM0, P4.1/PWM1, and P4.2/PWM2. P4.3 is not multiplexed.
PLLEN2:1	I	Phase-locked Loop 1 and 2 Enable These input pins are used to enable the on-chip clock multiplier feature and select either the doubled or quadrupled clock speed as follows: **PLLEN2** **PLLEN1** **Mode** 0 0 Standard mode; clock multiplier circuitry disabled. Internal clock equals the XTAL1 input frequency. 1 0 Reserved† 0 1 Doubled mode; clock multiplier circuitry enabled. Internal clock is twice the XTAL1 input frequency. 1 1 Quadrupled mode; clock multiplier circuitry enabled. Internal clock is four times the XTAL1 input frequency. † This reserved combination causes the device to enter an unsupported test mode.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable. PWM2:0 are multiplexed with P4.2:0.
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers or the chip-select *x* bus control register. READY is ignored for all internal memory accesses.
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. If the phase-locked loop (PLL) clock circuitry is enabled, you must hold RESET# low for at least 2 ms to allow the PLL to stabilize before the internal CPU and peripheral clocks are enabled. After a device reset, the first instruction fetch is from FF2080H (or F2080H in external memory). The program and special-purpose memory locations (FF2000–FF2FFFH) reside in external memory.
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if **either** of the following conditions is true: • the internal oscillator is the clock source • the phase-locked loop (PLL) circuitry is enabled (see PLLEN2:1 signal description) The capacitor causes a delay that enables the oscillator and PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled. The capacitor is not required if your application uses powerdown mode and if **both** of the following conditions are true: • an external clock input is the clock source • the phase-locked loop circuitry is disabled If your application does not use powerdown mode, leave this pin unconnected.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD is multiplexed with P2.1.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. **and** External clock for the serial I/O baud-rate generator input (program selectable). T1CLK is multiplexed with P1.4.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. Also used in conjunction with T2DIR for quadrature counting mode. T2CLK is multiplexed with P1.6.
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode. T1DIR is multiplexed with P1.5.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. Also used in conjunction with T2CLK for quadrature counting mode. T2DIR is multiplexed with P1.7.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD is multiplexed with P2.0.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# is multiplexed with WRL#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High† During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# is multiplexed with BHE#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
WRL#	O	Write Low[†] During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# is multiplexed with WR#. [†] The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator, phase-locked loop circuitry, and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1 (see datasheet).
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses a external clock source instead of the on-chip oscillator.

5.0 ADDRESS MAP

Table 9. 8XC196NU Address Map

Hex Address	Description	Addressing Modes
FF FFFFH FF E000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF DFFFH FF 2080H	Program memory (Note 1)	Indirect, indexed, extended
FF 207FH FF 2000H	Special-purpose memory (Note 1)	Indirect, indexed, extended
FF 1FFFH FF 0100H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF 00FFH FF 0000H	Reserved for ICE (Note 2)	—
FE FFFFH 0F 0000H	Overlaid memory (reserved for future devices) (Note 2)	Indirect, indexed, extended
0E FFFFH 01 0000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 FFFFH 00 E000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 DFFFH 00 2000H	External device (memory or I/O) connected to address/data bus or remapped internal ROM (determined by EA# pin) (Note 3)	Indirect, indexed, extended
00 1FFFH 00 1F00H	Internal peripheral special-function registers (SFRs) (Note 4)	Indirect, indexed, extended, windowed direct
00 1EFFH 00 0400H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 03FFH 00 0100H	Upper register file (general-purpose register RAM)	Indirect, indexed, windowed direct
00 00FFH 00 001AH	Lower register file (general-purpose register RAM)	Direct, indirect, indexed, windowed direct
00 0019H 00 0018H	Lower register file (stack pointer)	Direct, indirect, indexed, windowed direct
00 0017H 00 0000H	Lower register file (CPU SFRs) (Note 4)	Direct, indirect, indexed, windowed direct

NOTES:
1. For the 80C196NU, the program and special-purpose memory locations (FF2000–FFDFFFH) reside in external memory. For the 83C196NU, these locations can reside either in external memory or in internal ROM.
2. Locations *x*F0000–*x*F00FFH are reserved, write 0FFH to these locations.
3. For the 80C196NU, this address range (FF2080–FFDFFFH) is always external memory. For the 83C196NU, this address range is mapped into internal ROM if the REMAP bit (CCB1.2) is set and EA# is at logic 1. Otherwise, they are mapped to external memory.
4. Unless otherwise noted, write 0 to reserved SFR bits.

6.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... –60°C to +150°C
Supply Voltage with Respect to V_{SS} ..... –0.5 V to +7.0 V
Power Dissipation ..... 1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
F_{XTAL1} (Input frequency for V_{CC} = 4.5 V – 5.5 V)
(Note 1, 2, 3) ..... 16 MHz to 50 MHz

NOTES:
1. This device is static and should operate below 1 Hz, but has been tested only down to 16 MHz.
2. The maximum crystal that can be used is 25 MHz.
3. The minimum XTAL1 frequency when using the PLL is 8 MHz.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 DC Characteristics

Table 10. DC Characteristics Over Specified Operating Conditions

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		90	120	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle Mode Current		45	60	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V
I_{PD}	Powerdown Mode Current		20	50	µA	V_{CC} = 5.5 V (Note 2)
I_{STDBY}	Standby Mode		8	15	mA	V_{CC} = 5.5 V
I_{LI}	Input Leakage Current (Standard Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	–0.5		0.8	V	
V_{IH}	Input High Voltage	0.2 V_{CC} + 1		V_{CC} + 0.5	V	
V_{IL1}	Input Low Voltage XTAL1	–0.5		0.3 V_{CC}	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (Reset pin) (Note 3)	0.2 V_{CC} + 1.4		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Note 4, 5)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 5)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. B-step only.
4. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
5. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

6. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
7. Pin capacitance is not tested. This value is based on design simulations.

Table 10. DC Characteristics Over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
V_{OL1}	Output Low Voltage on P4.*x* (output configured as complementary) (Note 5)			0.45 0.6	V V	I_{OL} = 10 mA I_{OL} = 15 mA
V_{OL2}	Output Low Voltage in RESET on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OH1}	Output High Voltage in RESET (Note 6)	V_{CC} – 0.7			V	I_{OH} = –3 µA
V_{OL3}	Output Low Voltage in RESET for ONCE pin			0.45	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{TH+} – $V_{TH–}$	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 7)			10	pF	
R_{RST}	RESET Pull-up Resistor	9		95	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. B-step only.
4. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
5. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

6. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
7. Pin capacitance is not tested. This value is based on design simulations.

6.2 AC Characteristics

6.2.1 RELATIONSHIP OF XTAL1 TO CLKOUT

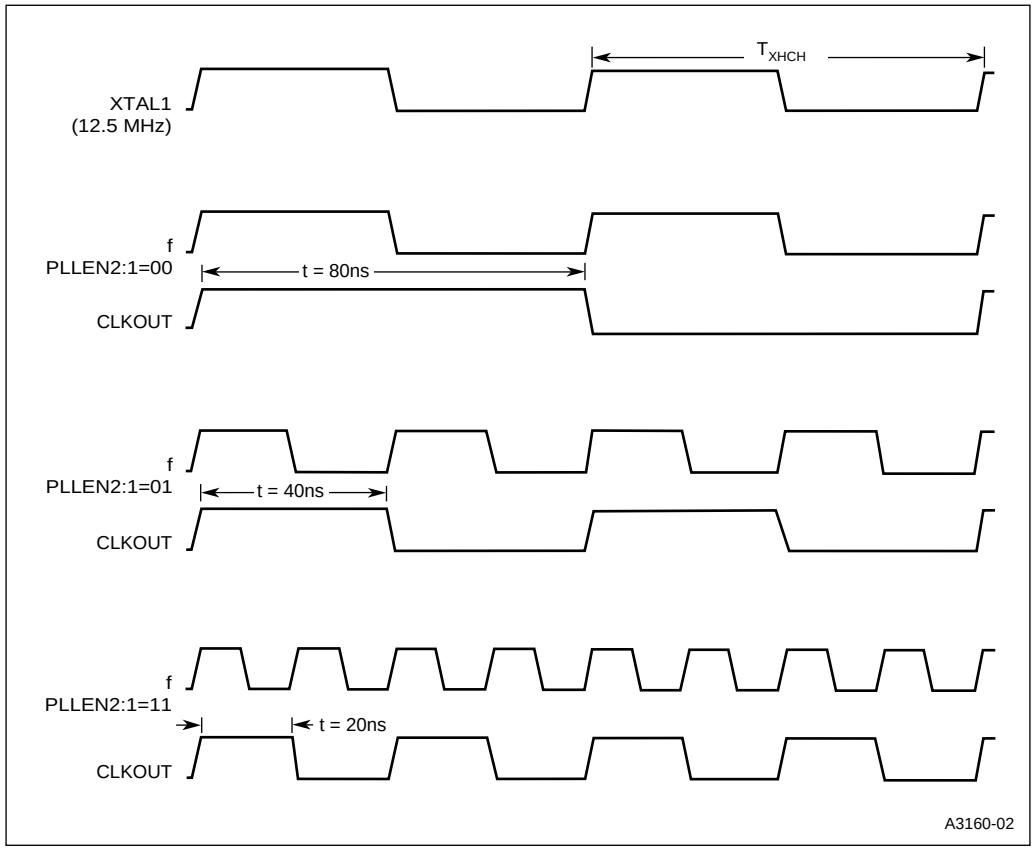


Figure 6. Effect of Clock Mode on CLKOUT

6.2.2 EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by “T” for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 11. AC Timing Symbol Definitions

Character	Signal(s)
A	AD15:0, A19:0
B	BHE#
C	CLKOUT
D	AD15:0, AD7:0
H	HOLD#
HA	HLDA#
L	ALE
Q	AD15:0, AD7:0
R	RD#
S	CS*x*#
W	WR#, WRL#
X	XTAL1,
Y	READY

Character	Condition
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating (low impedance)

6.2.3 AC CHARACTERISTICS — MULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics the 8XC196NU Will Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{AVWL}	Address Valid to WR# Falling Edge	2t – 25		ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	– 10	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	– 15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Valid to ALE Falling Edge	t – 14		ns
T_{LLAX}	Address Hold after ALE Falling Edge	t – 10		ns
T_{LLRL}	ALE Falling Edge to RD# Falling Edge	t – 15		ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	– 10	20	ns
T_{RLRH}	RD# Low Period	t – 10		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 5	t + 15	ns (4)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Falling Edge to WR# Falling Edge	t – 11		ns
T_{QVWH}	Data Stable to WR# Rising Edge	t – 14		ns (3)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 15	5	ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 12. AC Characteristics the 8XC196NU Will Meet, Multiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WLWH}	WR# Low Period	t – 10		ns (3)
T_{WHQX}	Data Hold after WR# Rising Edge	t – 7		ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 14	t + 20	ns
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge A-step B-step	 t – 4 0		ns
T_{WHAX}	AD15:8 Hold after WR# Rising Edge	t – 4		ns (5)
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge A-step B-step	 t 0		ns
T_{RHAX}	AD15:8 Hold after RD# Rising Edge	t		ns (5)
T_{WHSH}	A19:16, CS# Hold after WR# Rising Edge	0		ns
T_{RHSH}	A19:16, CS# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 13. AC Characteristics the External Memory System Must Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	AD15:0 Valid to Input Data Valid		3t – 32	ns (1)
T_{RLDV}	RD# Active to Input Data Valid		t – 22	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 32	ns (1)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t – 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	AD15:0 Valid to READY Setup		2t – 38	ns (2)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 36	ns (3)
T_{YLYH}	Non-READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add $2t \times n$, where n = number of wait states.
2. When forcing wait states using the BUSCON register, add $2t \times n$.
3. Exceeding the maximum specification causes additional wait states.

6.2.3.1 System Bus Timings, Multiplexed Bus

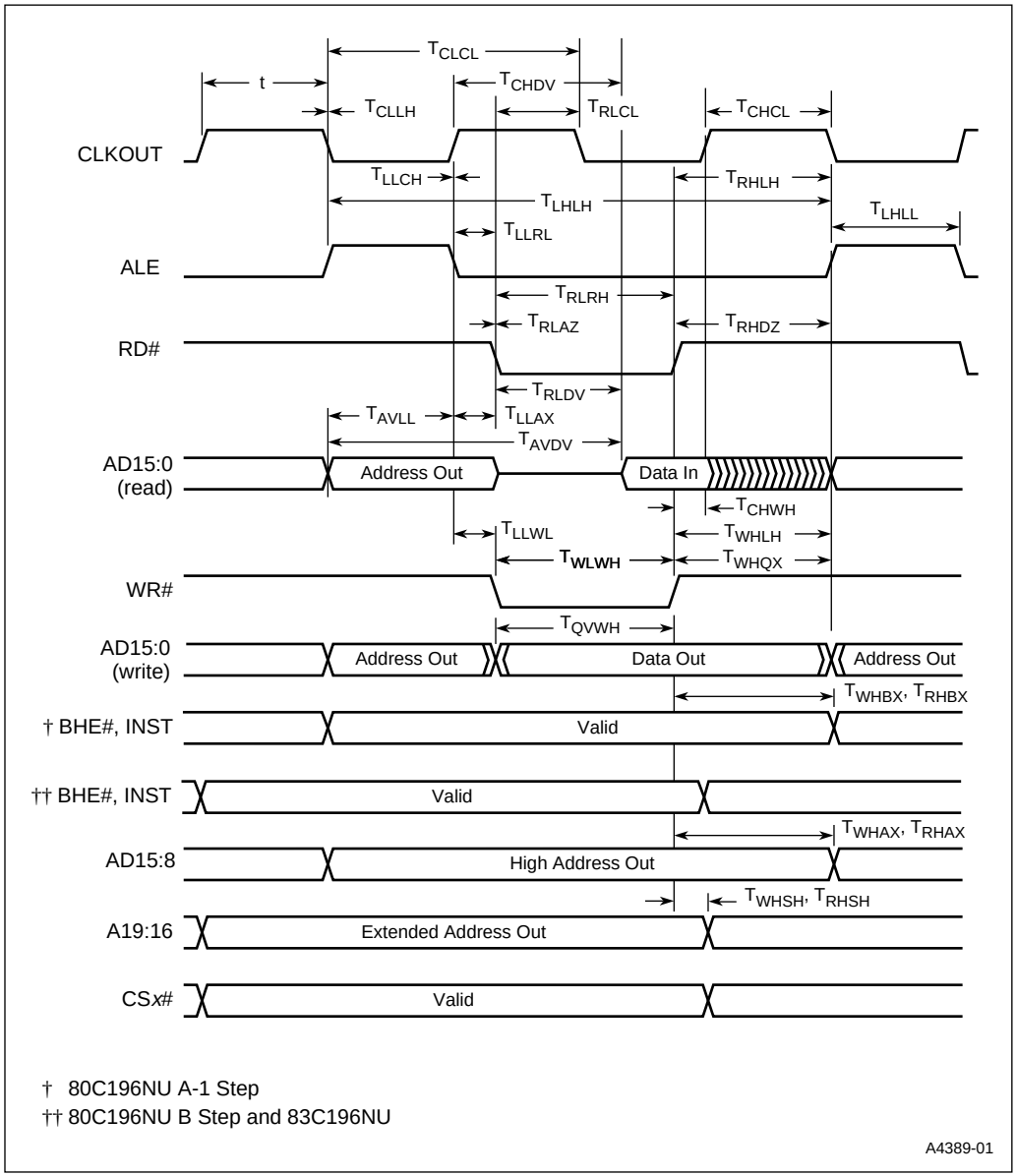


Figure 7. System Bus Timings, Multiplexed Bus Mode

6.2.3.2 READY Timing, Multiplexed Bus

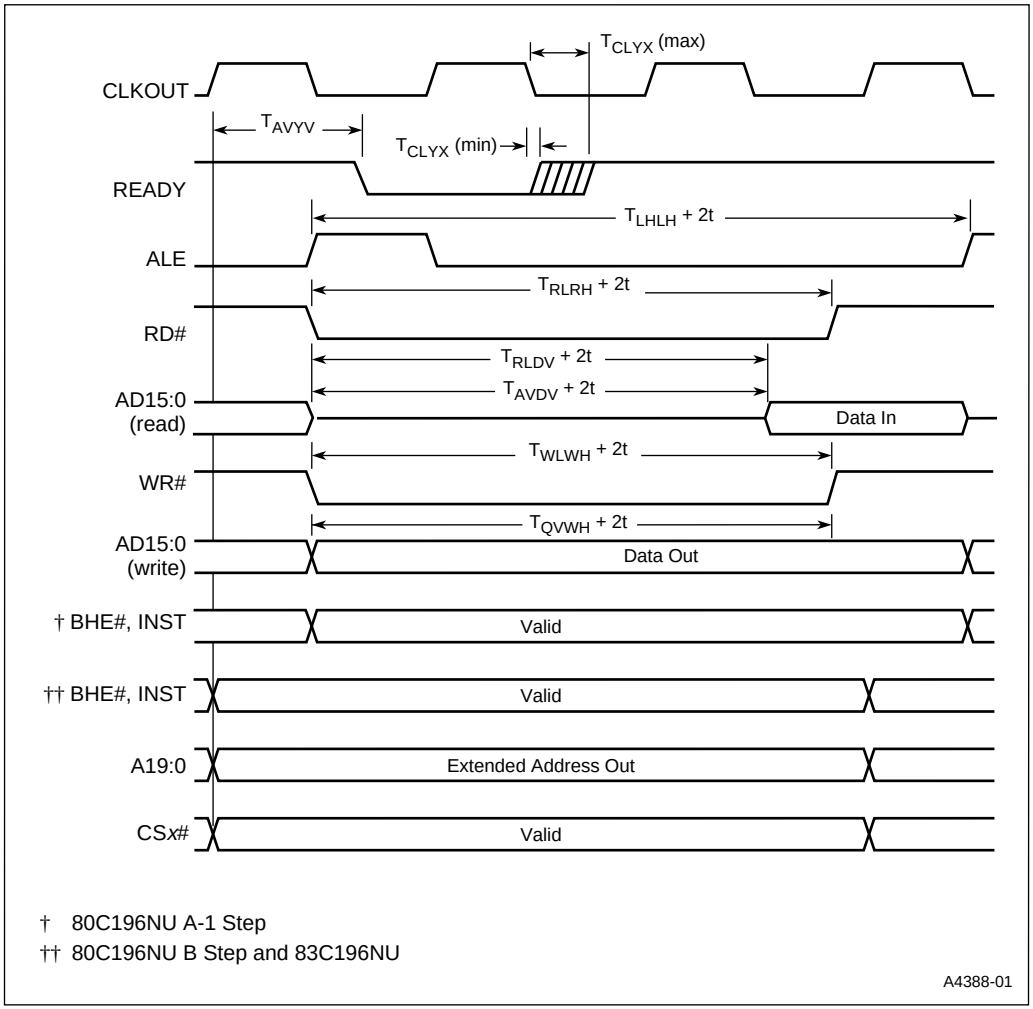


Figure 8. READY Timing, Multiplexed Bus Mode

6.2.4 AC CHARACTERISTICS — DEMULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 14. AC Characteristics the 8XC196NU Will Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{AVWL}	Address Valid to WR# Falling Edge	t – 8		ns(3)
T_{AVRL}	Address Valid to RD# Falling Edge	t – 8		ns(3)
T_{RHRL}	Read High to Next Read Low	t – 5		ns(3)
T_{XHCH}	XTAL1 High to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	– 10	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	– 15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3,4,5)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	– 5	11	ns
T_{RLRH}	RD# Low Period	3t – 18		ns (4)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 4	t + 15	ns (3)
T_{WLCL}	WR# Low to CLKOUT Falling Edge	– 8	5	ns
T_{QVWH}	Data Stable to WR# Rising Edge	3t – 25		ns (4)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 11	10	ns
T_{WLWH}	WR# Low Period	3t – 18		ns (4)
T_{WHQX}	Data Hold after WR# Rising Edge	t	t + 20	ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
4. If wait states are used, add 2t × *n*, where *n* = number of wait states.
5. Assuming back-to-back bus cycles.

Table 14. AC Characteristics the 8XC196NU Will Meet, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 5	t + 10	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge A-step B-step	 t – 5 0		ns
T_{WHAX}	A19:0, CS*x*# Hold after WR# Rising Edge	0		ns
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge A-step B-step	 t – 5 0		ns
T_{RHAX}	A19:0, CS*x*# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
4. If wait states are used, add 2t × *n*, where *n* = number of wait states.
5. Assuming back-to-back bus cycles.

Table 15. AC Characteristics the External Memory System Must Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	A19:0 Valid to Input Data Valid		4t – 25	ns (1,2)
T_{RLDV}	RD# Active to Input Data Valid		3t – 35	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 25	ns (1,2)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	A19:0 Valid to READY Setup		3t – 45	ns (3)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 26	ns (4)
T_{YLYH}	Non READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add 2t × *n*, where *n* = number of wait states.
2. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
3. When forcing wait states using the BUSCON register, add 2t × *n.*
4. Exceeding the maximum specification causes additional wait states.

6.2.4.1 System Bus Timings, Demultiplexed Bus

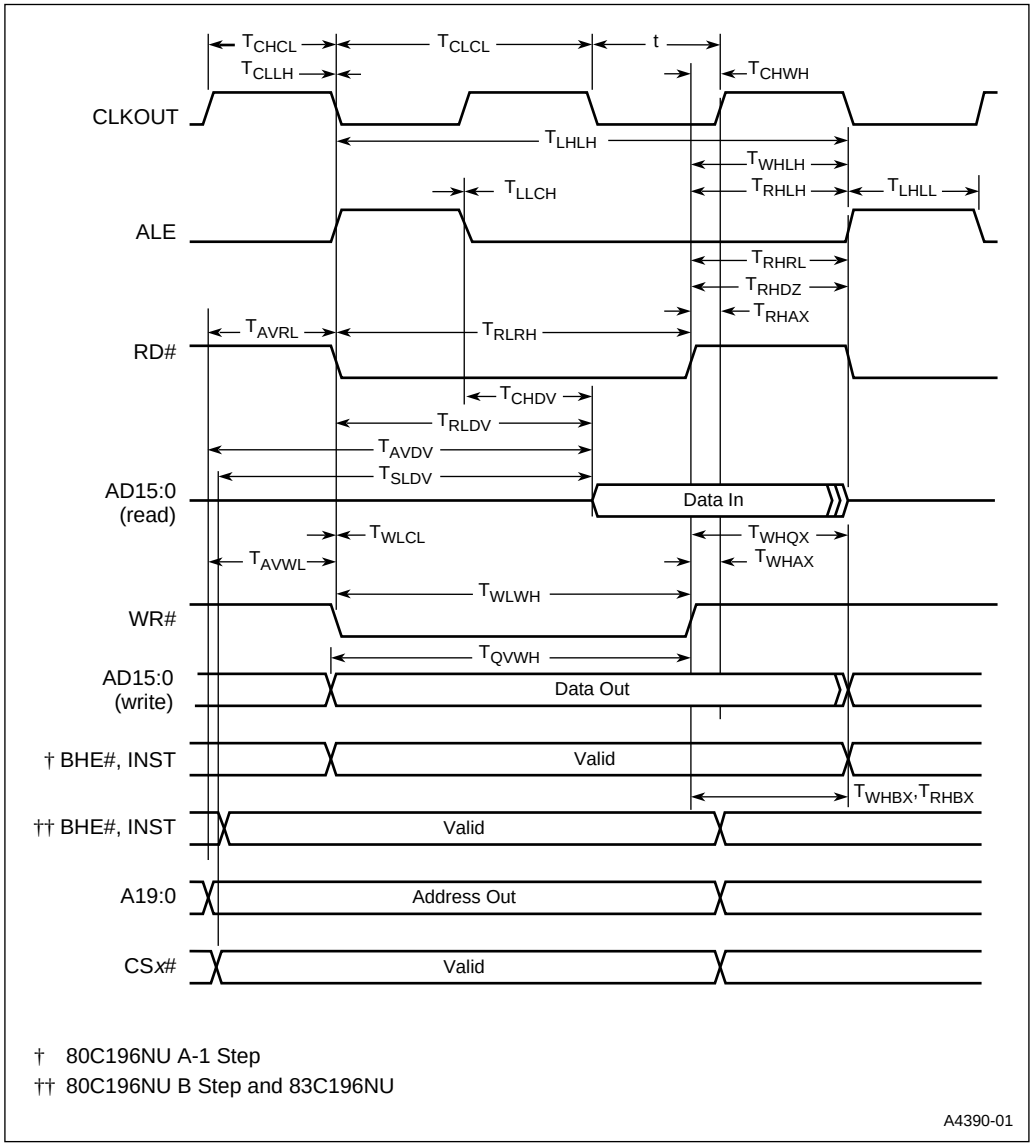


Figure 9. System Bus Timings, Demultiplexed Bus Mode

6.2.4.2 READY Timing, Demultiplexed Bus

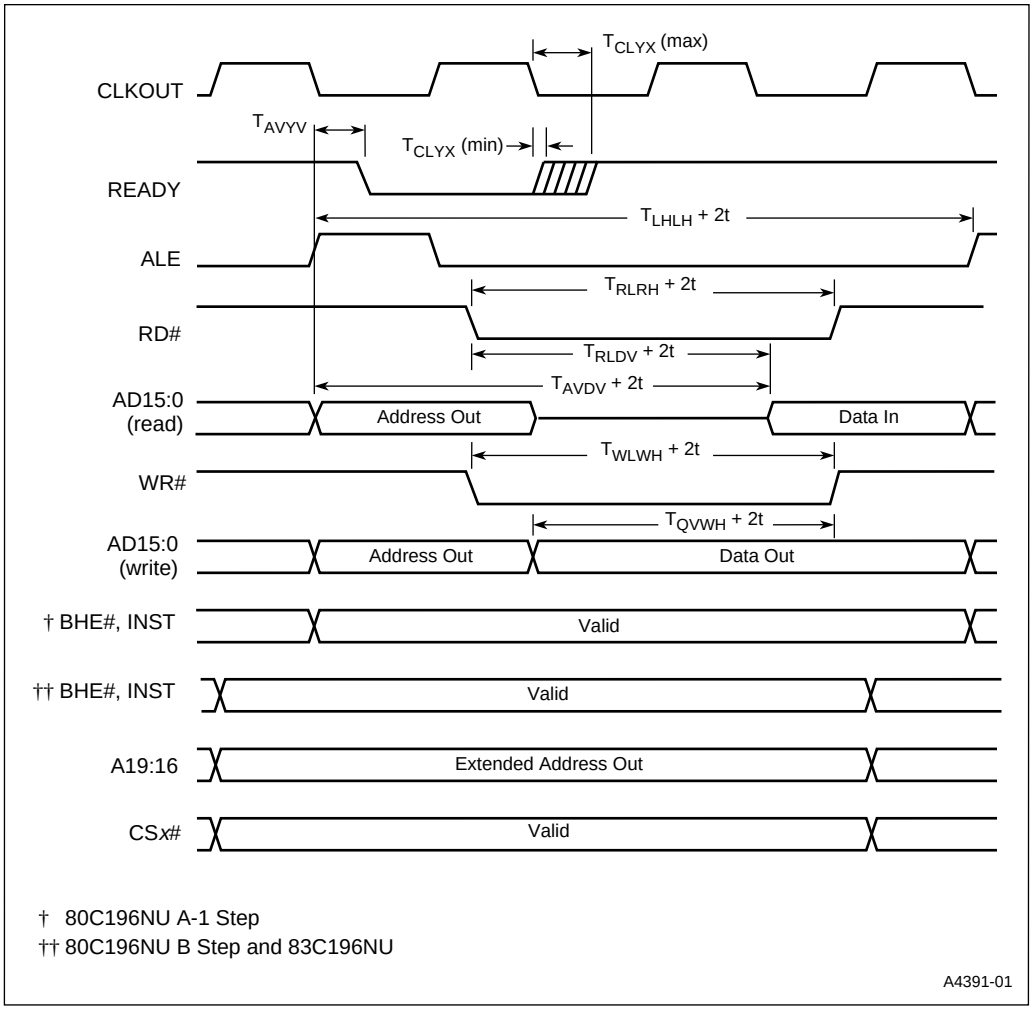


Figure 10. READY Timing, Demultiplexed Bus Mode

6.2.4.3 8XC196NU Deferred Bus Timing Mode

The deferred bus cycle mode (enabled by setting CCB1.5) is designed to reduce bus contention when using the 8XC196NU in demultiplexed mode with slow memories. When the deferred mode is enabled, a delay will occur (equal to 2t) in the first bus cycle following a chip-select change or the first write cycle following a read cycle. This mode will work in parallel with wait states. Refer to Figure 11 to determine which control signals are affected.

Cycle 1 is a normal 4t read cycle. Cycle 2 is a write cycle that follows a read cycle, so a 2t delay is inserted. Notice that the chip-select change at the beginning of cycle 2 did not cause a double delay (4t). The chip-select change in cycle 3, a read cycle, causes a 2t delay.

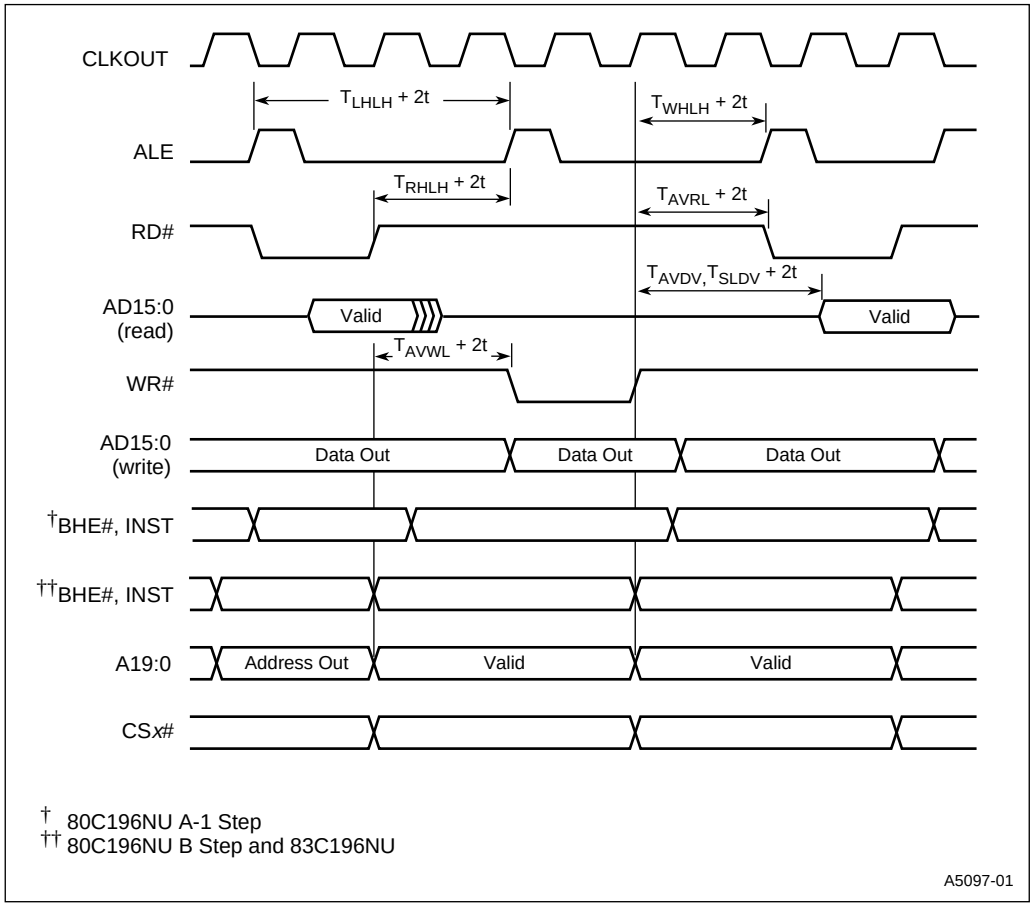


Figure 11. Deferred Bus Mode Timing Diagram

6.2.5 HOLD#, HLDA# TIMINGS

Table 16. HOLD#, HLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup Time (To guarantee recognition at next clock)	65		ns
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–20		ns

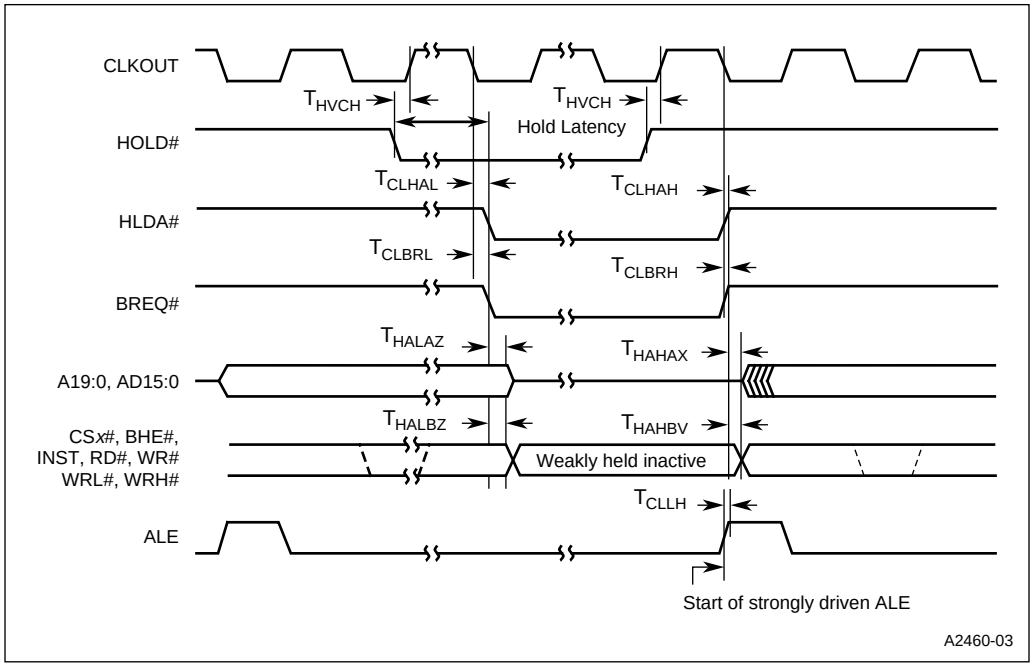


Figure 12. HOLD#, HLDA# Timing Diagram

6.2.6 AC CHARACTERISTICS — SERIAL PORT, SYNCHRONOUS MODE 0

Table 17. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period			
	SP_BAUD ≥ *x*002H	6t		ns
	SP_BAUD = *x*001H (Note 1)	4t		ns
T_{XLXH}	Serial Port Clock falling edge to rising edge			
	SP_BAUD ≥ *x*002H	4t – 27	4t + 27	ns
	SP_BAUD = *x*001H (Note 1)	2t – 27	2t + 27	ns
T_{QVXH}	Output data setup to clock high	4t – 30		ns
T_{XHQX}	Output data hold after clock high	2t – 30		ns
T_{XHQV}	Next output data valid after clock high		2t + 30	ns
T_{DVXH}	Input data setup to clock high	2t + 30		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		t + 30	ns

NOTE:
1. The minimum baud-rate (SP_BAUD) register value for receive is *x*002H and the minimum baud-rate (SP_BAUD) register value for transmit is *x*001H.

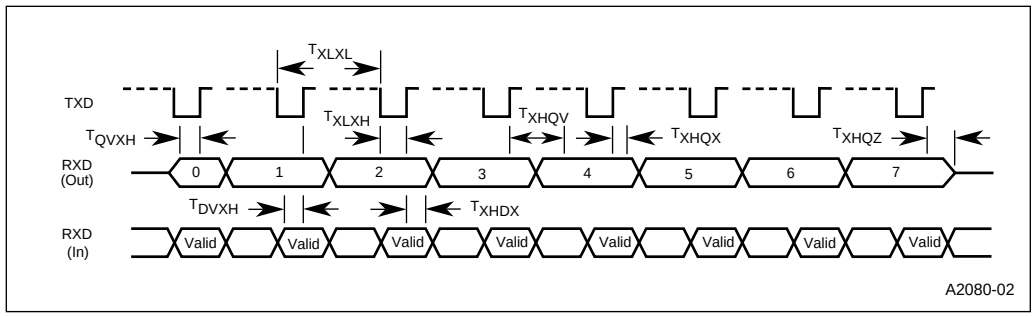


Figure 13. Serial Port Waveform — Synchronous Mode 0

6.2.7 EXTERNAL CLOCK DRIVE

Table 18. External Clock Drive

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	External Input Frequency ($1/T_{XLXL}$), PLL disabled	16	50†	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 2x mode	8	25	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 4x mode	8	12.5	MHz
T_{XTAL1}	Oscillator Period (T_{XLXL}), PLL disabled	20	62.5	ns
	Oscillator Period (T_{XLXL}), PLL in 2x mode	40	125	ns
	Oscillator Period (T_{XLXL}), PLL in 4x mode	80	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

† Assumes an external clock; the maximum input frequency for an external crystal oscillator is 25 MHz.

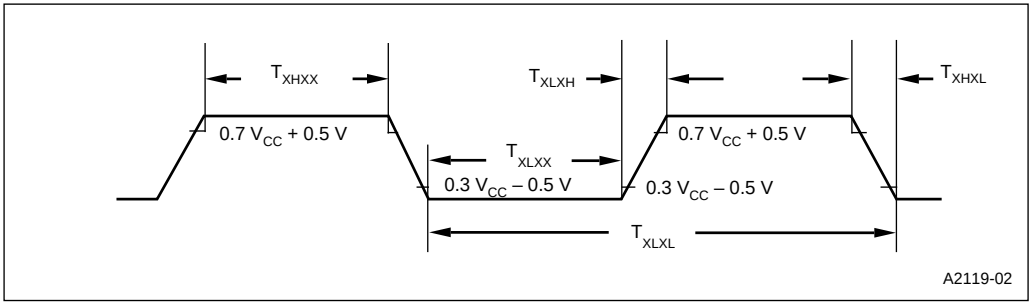


Figure 14. External Clock Drive Waveforms

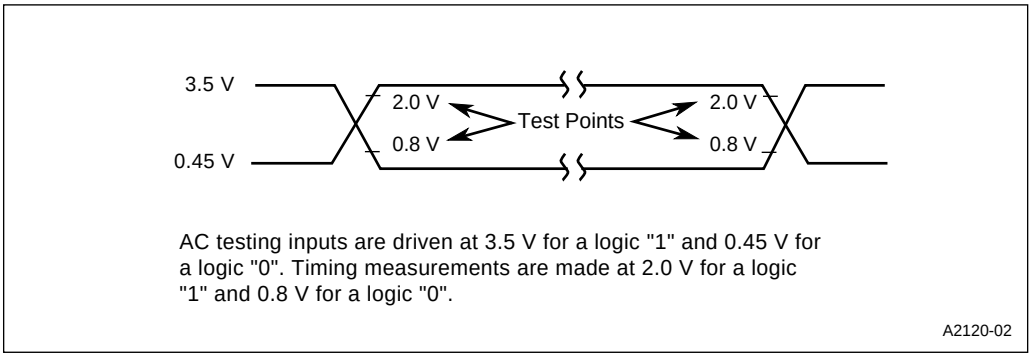
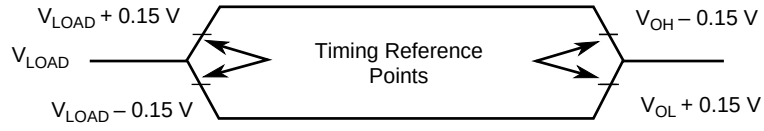


Figure 15. AC Testing Output Waveforms During 5.0 Volt Testing



For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-01

Figure 16. Float Waveforms During 5.0 Volt Testing

7.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 19. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin QFP 80C196NU	55°C/W	11°C/W
100-pin SQFP 80C196NU	66°C/W	16.5°C/W
100-pin QFP 83C196NU	55°C/W	11°C/W

8.0 8XC196NU ERRATA

The 8XC196NU may contain design defects or errors known as errata. Characterized errata that may cause the 8XC196NU's behavior to deviate from published specifications are documented in the *8XC196NU Specification Update* (272864-001). Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

9.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with a "B" or "C" designation at the end of the topside tracking number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the -004 version of the datasheet. The following changes were made in this version:

1. All references to "ADVANCE INFORMATION" have been changed to "PRELIMINARY".
2. Table note added to Tables 4 and 6.
3. Table 15, removed note (2) attachment from T_{RHDZ}.
4. Table 15, specification change made to the following timings: T_{AVDV}, T_{SLDV}, T_{CLYX}.

This is the -003 version of the datasheet. The following changes were made in this version:

1. A heading was added for Section 1.0, "Product Overview," and the remaining sections were renumbered.
2. List of features, the 8XC196NU has four options (0–3) for programmable wait states for each chip select, not sixteen (0–15) as previously stated.
3. The ROM SQFP (SB83C196NU) pinout and pin assignment tables have been deleted.
4. Figure 5, package designator in diagram changed to "S" from "SB" to correctly indicate the QFP package type.
5. Table 8, EA# signal description added.
6. Table 8, signal descriptions for BREQ#, HLDA#, HOLD#, PLLEN2:1, and RESET# have been modified.
7. Table 9, redesigned and footnotes reordered.
8. Table 10, V_{IH2} specification added with footnote.
9. Figure 6, corrected to state PLLEN2:1=01 (not PLLEN2:1=10).
10. Tables 12 and 14, B-step timing added for T_{WHBX} min and T_{RHBX} min.
11. Table 12, deleted notes 4 and 5, added note 2, and reordered remaining notes.
12. Table 13, deleted notes 1, 3, and 6 and reordered remaining notes.
13. Table 14, deleted notes 4, 5, and 6, added note 2, and reordered remaining notes.
14. Table 15, deleted notes 1, 3, and 6 and reordered remaining notes.
15. Tables 13 and 15, the minimum timing for T_{RXDX} improved from 2 ns to 0 ns.
16. Figures 7–11, updated to reflect both A- and B-step timings on the BHE#, INST signal.
17. Section 5.4.3, the second sentence of the first paragraph, the word "and" replaced by "or".
18. Table 19, thermal characteristics specifications have been changed and expanded.
19. The errata list was replaced with a reference to the specification update document.

The following changes were made in the -002 version of the datasheet:

1. The input frequency on XTAL1, formerly called F_{OSC}, is now called F_{XTAL1}. The internal operating frequency and operating period are denoted by (f) and (t), respectively.
2. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.

3. The minimum frequency input with PLL in 4x mode has changed from 4 MHz to 8MHz.
4. The AC characteristics tables have been divided into the following: the timing specifications met by the device, and the timing specifications that must be met by the external memory system.
5. Electrical characteristics notes #2 and #3 added to section 3.0.
6. Maximum I_{OL} and I_{OH} specifications added to the DC characteristics tables.
7. AC timings T_{AVWL} and T_{SLDV} added to the AC characteristics–multiplexed bus mode tables.
8. Figure 7 added, and figures 8–12 have been revised.
9. Thermal characteristics for the 100-pin SQFP package have been added in section 1.0.
10. Specifications for the 83C196NU have been added.
11. Several AC timing specifications have changed.