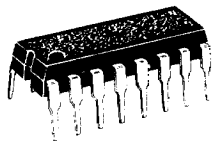
MN4510B / MN4510BS

BCD Up/Down Counters

■ Description

The MN4510B/S are BCD up/down counters composed of a gate circuit with the function of D-flip-flop 4-stage and T-flip-flop.
The counter is cleared when MR is "H". High speed operation is possible due to internal synchronization.
The MN4510B/S are suitable for up/down counters, frequency synthesizers which need low power dissipation and high noise immunity, and also for A/D and D/A converters.
They are equivalent to MOTOROLA MC14510B and RCA CD4510B.

P-3



16-Pin • Plastic DIL Package

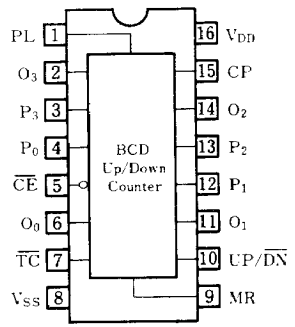
P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	Mode
L	H	×	×	×	load
L	L	×	H	×	no change
L	L	L	L	↓	count down
L	L	H	L	↓	count up
H	×	×	×	×	leset

Pin Configuration



■ Maximum Ratings (Ta=25℃)

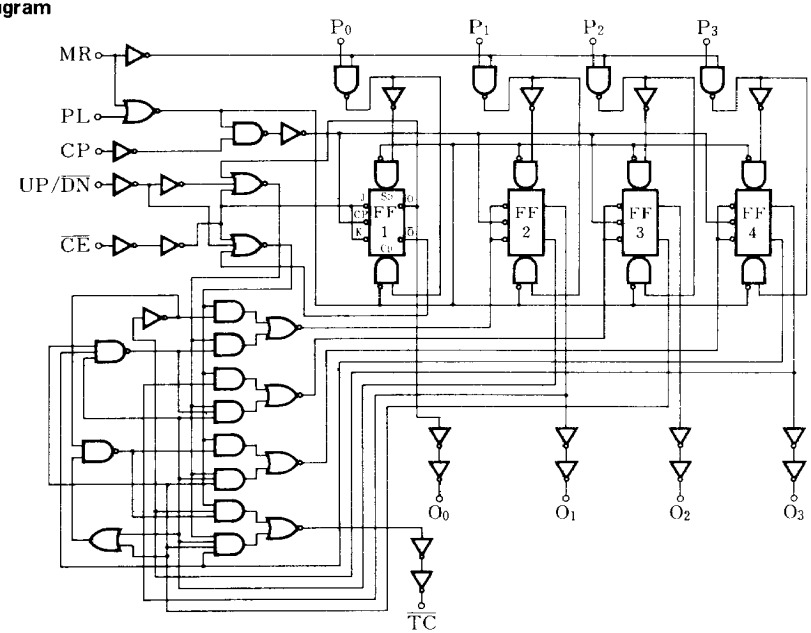
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/℃	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD} $\lvert I_O\rvert<1\mu A$		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD} $\lvert I_O\rvert<1\mu A$		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert<1\mu A$	$V_O=0.5V$ or $4.5V$	—	1.5	—	1.5	—	1.5	V
	10			$V_O=1V$ or $9V$	—	3	—	3	—	3	
	15			$V_O=1.5V$ or $13.5V$	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert<1\mu A$	$V_O=0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	—	V
	10			$V_O=1V$ or $9V$	7	—	7	—	7	—	
	15			$V_O=1.5V$ or $13.5V$	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O=0.4V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=0.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=1.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=4.6V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=9.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=13.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=2.5V$, $V_I=0$ or $5V$		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_I=0$ or $15V$		—	0.3	—	0.3	—	1	μA

■ Logic Diagram



■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$)

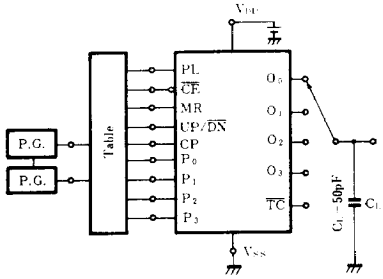
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	155	465	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time CP→$\overline{TC}$ (H→L)	5	t_{PHL}	—	260	780	ns
	10		—	105	315	
	15		—	75	225	
Propagation Delay Time CP→$\overline{TC}$ (L→H)	5	t_{PLH}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	125	375	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	170	510	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time PL→$\overline{TC}$ (H→L)	5	t_{PHL}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time PL→$\overline{TC}$ (L→H)	5	t_{PLH}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (H→L)	5	t_{PHL}	—	165	495	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time MR→On, $\overline{TC}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→$\overline{TC}$ (L→H)	5	t_{PLH}	—	225	675	ns
	10		—	75	225	
	15		—	50	150	
Minimum Clock Pulse Width	5	t_{WCPL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	

■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$) (continued)

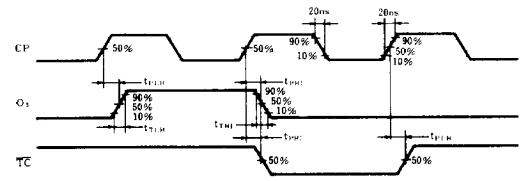
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Minimum PL Pulse Width	5	t_{WPLH}	—	55	165	ns
	10		—	25	75	
	15		—	15	45	
Minimum Reset Pulse Width	5	t_{WMRH}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Reset Recovery Time	5	t_{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
PL Recovery Time	5	t_{RPL}	—	75	225	ns
	10		—	25	75	
	15		—	15	45	
Set-up Time Pn→PL	5	t_{su}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time UP/$\overline{DN}$→CP	5	t_{su}	—	125	375	ns
	10		—	50	150	
	15		—	35	105	
Set-up Time $\overline{CE}$→CP	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Hold Time Pn→PL	5	t_{hold}	—	−40	10	ns
	10		—	−20	5	
	15		—	−20	0	
Hold Time UP/$\overline{DN}$→CP	5	t_{hold}	—	−90	35	ns
	10		—	−35	15	
	15		—	−25	15	
Hold Time $\overline{CE}$→CP	5	t_{hold}	—	−40	20	ns
	10		—	−15	5	
	15		—	−10	5	
Maximum Clock Frequency	5	f_{max}	5	10	—	MHz
	10		12	24	—	
	15		17	34	—	
Input Capacitance		C_I	—	—	7.5	pF

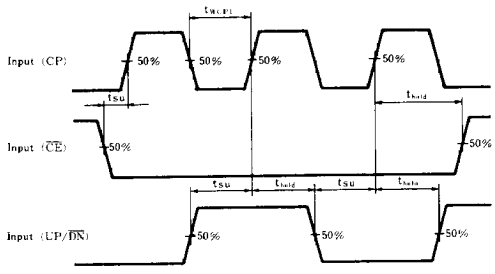
• Switching Time Test Circuit and Waveforms

1. Test Circuit

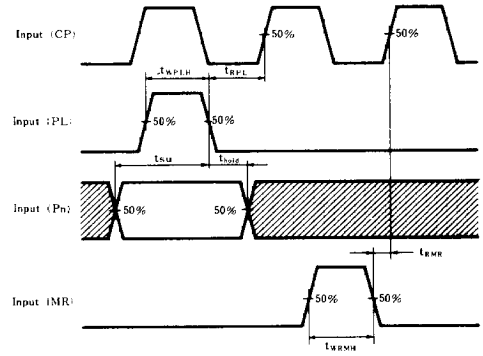


2. Waveforms





Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP



Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL

■ Timing Diagram