

## Wideband variable gain amplifier

NE/SA5219

## DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

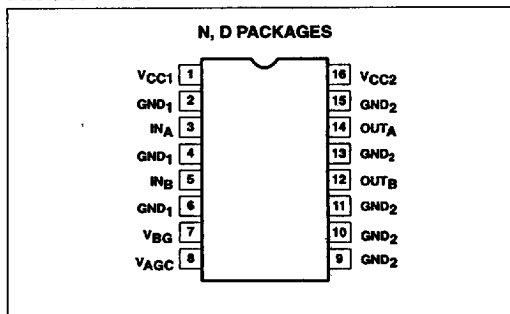
The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1k $\Omega$ ) differential inputs. The output is 50 $\Omega$  differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

## FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50 $\Omega$  differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional  $V_{\text{CONTROL}} / V_{\text{GAIN}}$  linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

## PIN CONFIGURATION



## APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

## ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	0 to +70°C	NE5219N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	0406C

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## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}$	Supply voltage	-0.5 to +8.0	V
$P_D$	Power dissipation, $T_A = 25^\circ\text{C}$ (still air) <sup>1</sup> 16-Pin Plastic DIP 16-Pin Plastic SO	1450 1100	mW mW
$T_{JMAX}$	Maximum operating junction temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage temperature range	-65 to +150	$^\circ\text{C}$

## NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,  $\theta_{JA}$ :16-Pin DIP:  $\theta_{JA} = 85^\circ\text{C/W}$ 16-Pin SO:  $\theta_{JA} = 110^\circ\text{C/W}$ 

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}$	Supply voltage	$V_{CC1} = V_{CC2} = 4.5 \text{ to } 7.0\text{V}$	V
$T_A$	Operating ambient temperature range NE Grade SA Grade	0 to +70 -40 to +85	$^\circ\text{C}$ $^\circ\text{C}$
$T_J$	Operating junction temperature range NE Grade SA Grade	0 to +90 -40 to +105	$^\circ\text{C}$ $^\circ\text{C}$

## DC ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = +5\text{V}$ ,  $V_{AGC} = 1.0\text{V}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$I_{CC}$	Supply current	DC tested	36	43	50	mA
$A_V$	Voltage gain (single-ended in/single-ended out)	DC tested, $R_L = 10\text{k}\Omega$	16	19	22	dB
$A_V$	Voltage gain (single-ended in/differential out)	DC tested, $R_L = 10\text{k}\Omega$	22	25	28	dB
$R_{IN}$	Input resistance (single-ended)	DC tested at $\pm 50\mu\text{A}$	0.8	1.2	1.6	k $\Omega$
$R_{OUT}$	Output resistance (single-ended)	DC tested at $\pm 1\text{mA}$	35	60	80	$\Omega$
$V_{OS}$	Output offset voltage (output referred)			$\pm 20$	$\pm 150$	mV
$V_{IN}$	DC level on inputs		1.6	2.0	2.4	V
$V_{OUT}$	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
$V_{BG}$	Bandgap reference voltage	$4.5\text{V} < V_{CC} < 7\text{V}$ $R_{BG} = 10\text{k}\Omega$	1.2	1.32	1.45	V
$R_{BG}$	Bandgap loading		2	10		k $\Omega$
$V_{AGC}$	AGC DC control voltage range			0-1.3		V
$I_{BAGC}$	AGC pin DC bias current	$0\text{V} < V_{AGC} < 1.3\text{V}$		-0.7	-6	$\mu\text{A}$

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## AC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C, V<sub>CC1</sub> = V<sub>CC2</sub> = +5.0V, V<sub>AGC</sub> = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V <sub>IMAX</sub>	Maximum input voltage swing (single-ended) for linear operation <sup>1</sup>			200		mV <sub>p-p</sub>
V <sub>OMAX</sub>	Maximum output voltage swing (single-ended) for linear operation <sup>1</sup>	R <sub>L</sub> = 50Ω		400		mV <sub>p-p</sub>
		R <sub>L</sub> = 1kΩ		1.9		V <sub>p-p</sub>
NF	Noise figure (unmatched configuration)	R <sub>S</sub> = 50Ω, f = 50MHz		9.3		dB
V <sub>IN-EQ</sub>	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		-60		dB
ΔG/ΔV <sub>CC</sub>	Gain supply sensitivity (single-ended)			0.3		dB/V
ΔG/ΔT	Gain temperature sensitivity	R <sub>L</sub> = 50Ω		0.013		dB/°C
C <sub>IN</sub>	Input capacitance (single-ended)			2		pF
BW <sub>AGC</sub>	-3dB bandwidth of gain control function			20		MHz
P <sub>O-1dB</sub>	1dB gain compression point at output	f = 100MHz		-3		dBm
P <sub>I-1dB</sub>	1dB gain compression point at input	f = 100MHz, V <sub>AGC</sub> = 0.1V		-10		dBm
IP3 <sub>OUT</sub>	Third-order intercept point at output	f = 100MHz, V <sub>AGC</sub> > 0.5V		+13		dBm
IP3 <sub>IN</sub>	Third-order intercept point at input	f = 100MHz, V <sub>AGC</sub> < 0.5V		+5		dBm
ΔG <sub>AB</sub>	Gain match output A to output B	f = 100MHz, V <sub>AGC</sub> = 1V		0.1		dB

## NOTE:

1. With R<sub>L</sub> > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R<sub>L</sub> = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

## NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V<sub>AGC</sub> input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function.

Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A

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maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes

BAT17 as shown. The diodes are biased by R1 and R2 to  $V_{CC}$  such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the  $V_{AGC}$  pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

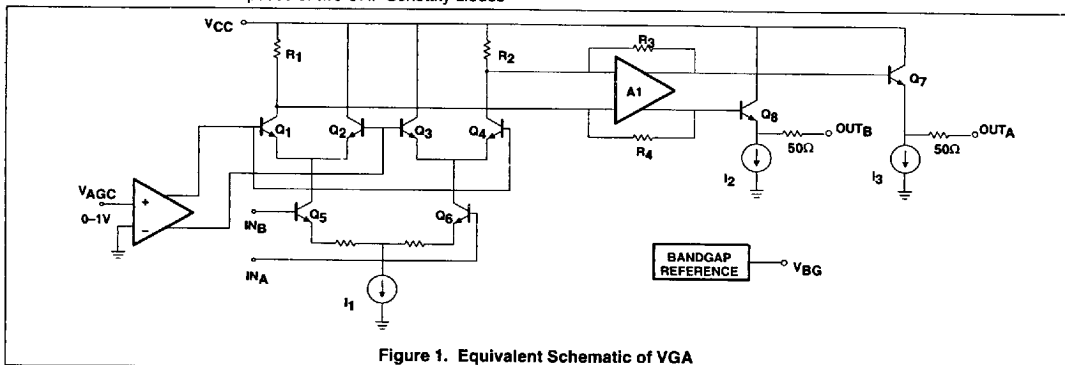


Figure 1. Equivalent Schematic of VGA

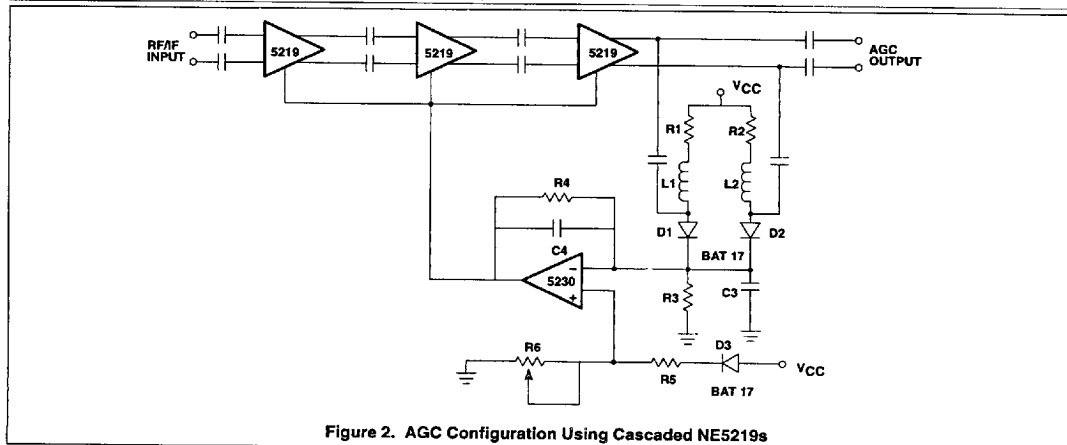


Figure 2. AGC Configuration Using Cascaded NE5219s

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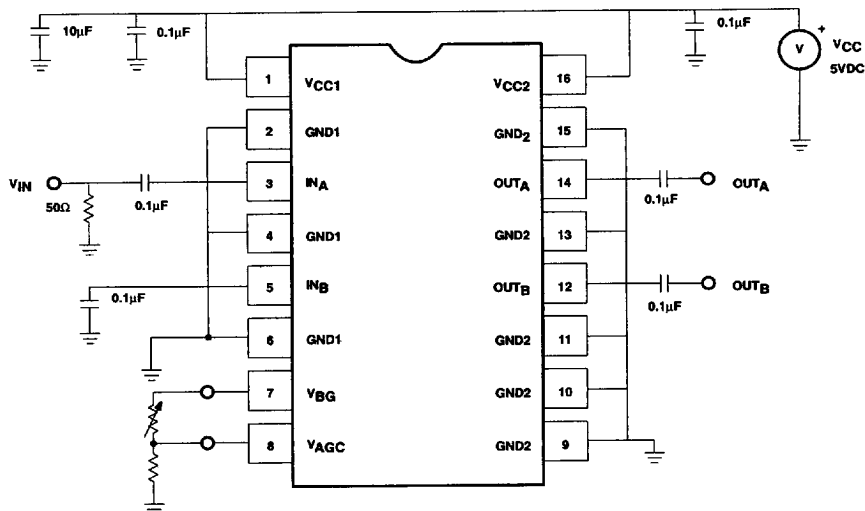
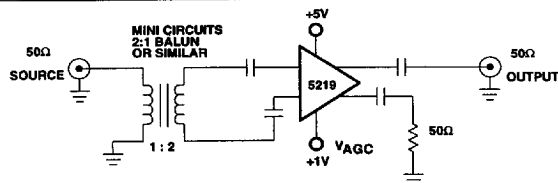
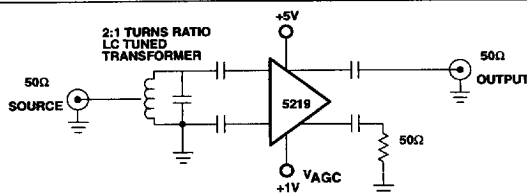


Figure 3. VGA AC Evaluation Board



This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization

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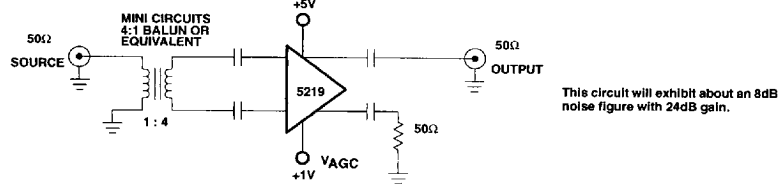


Figure 6. Broadband Gain Optimization

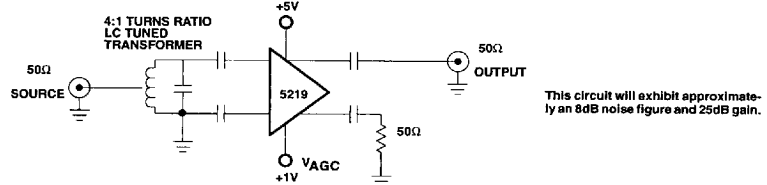


Figure 7. Narrowband Gain Optimization

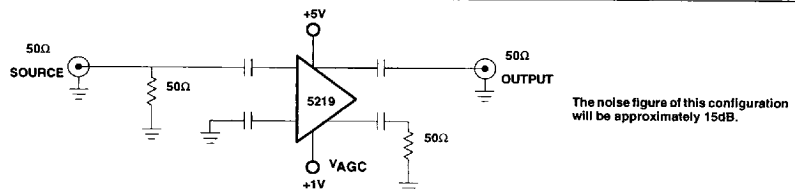


Figure 8. Simple Amplifier Configuration

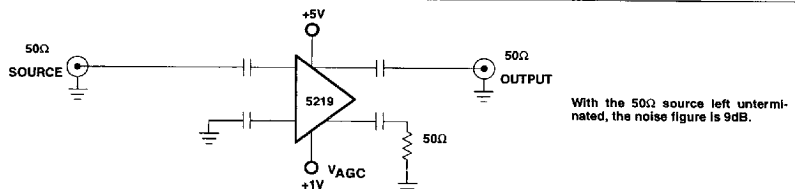


Figure 9. Underterminated Configuration

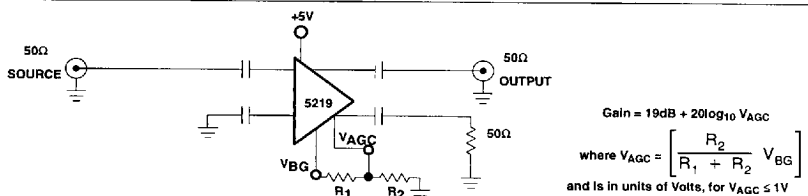
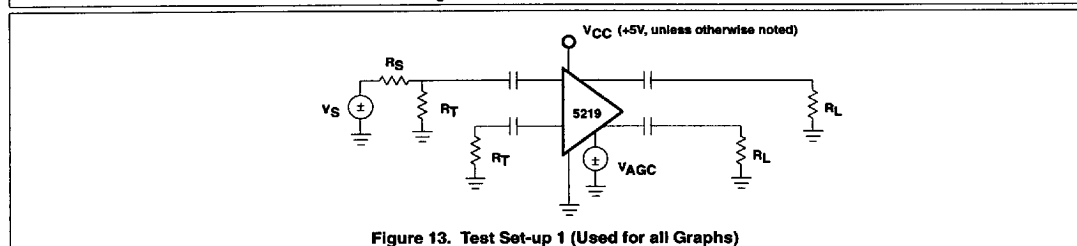
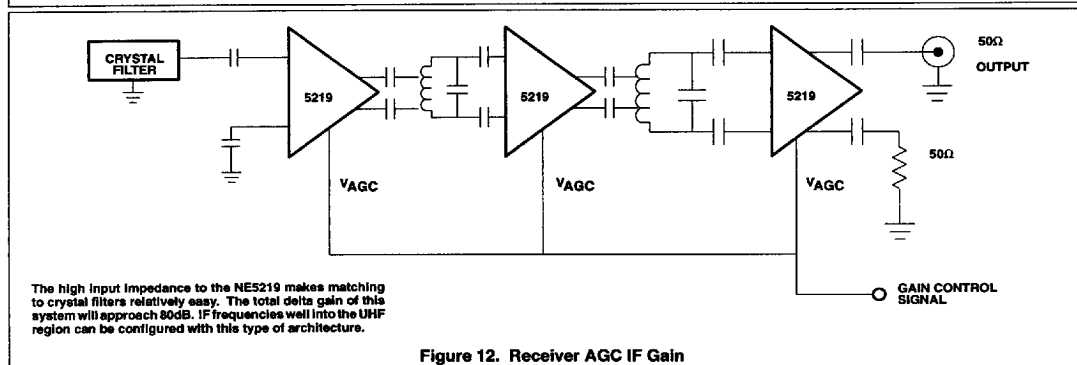
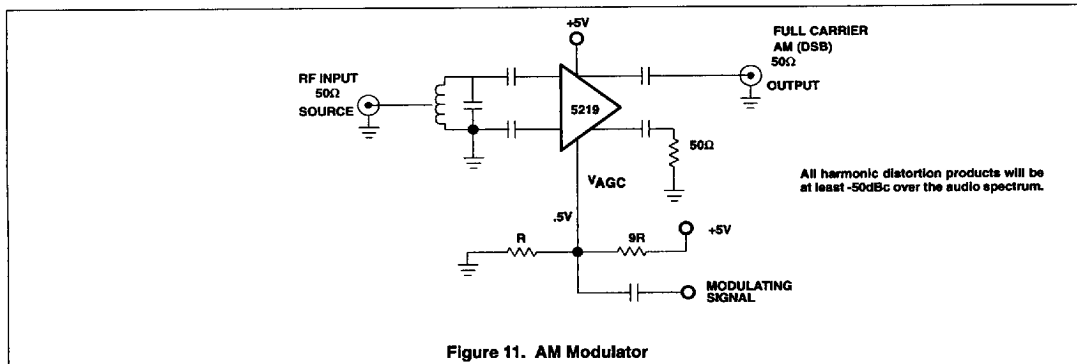


Figure 10. User-Programmable Fixed Gain Block

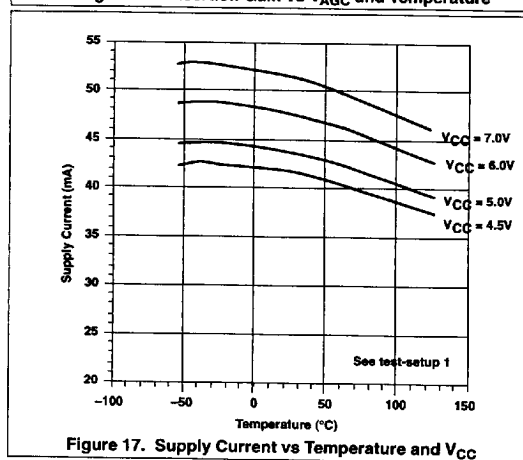
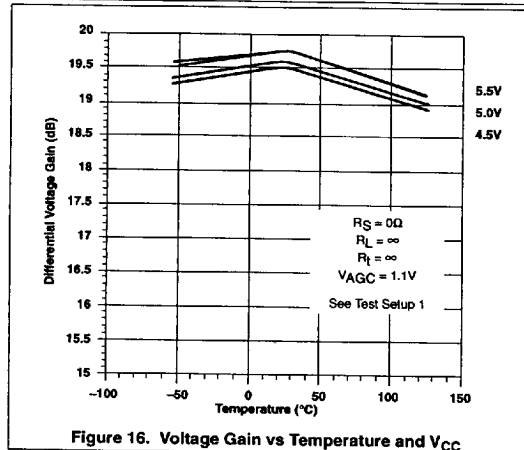
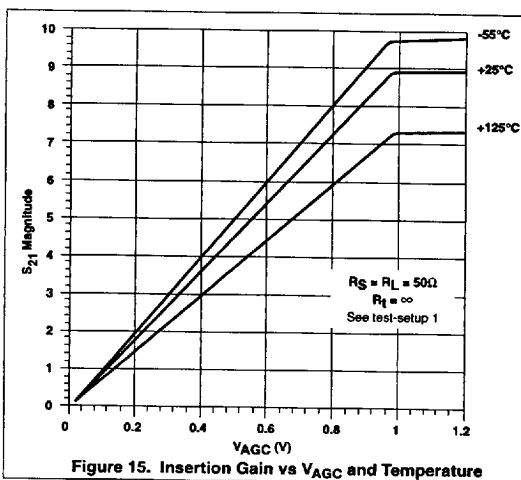
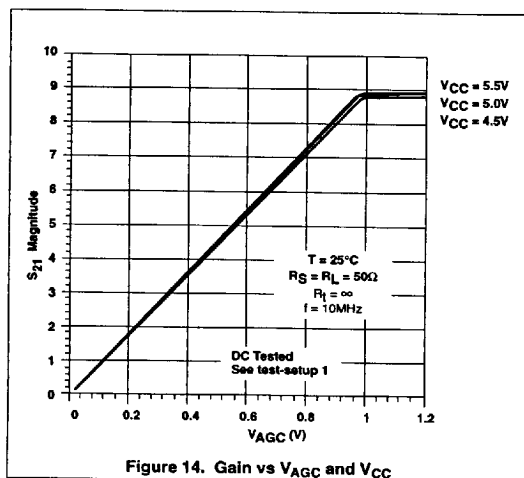
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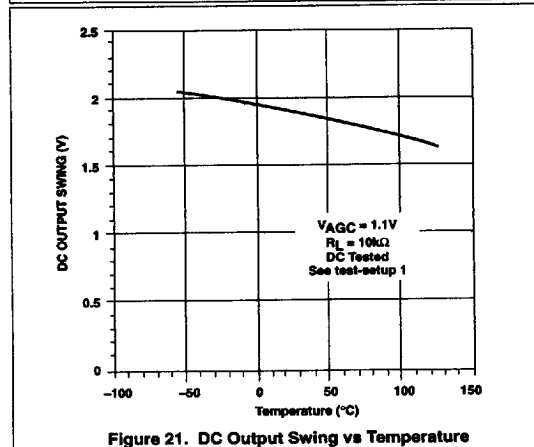
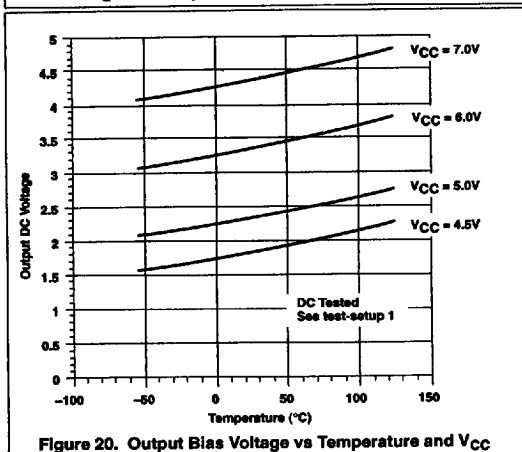
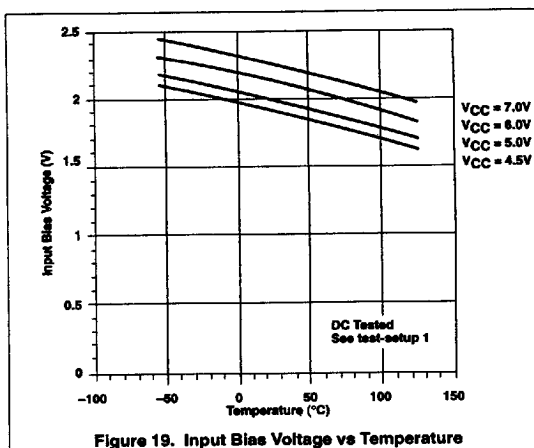
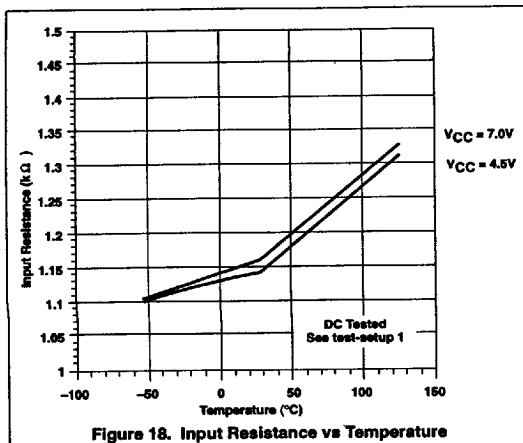
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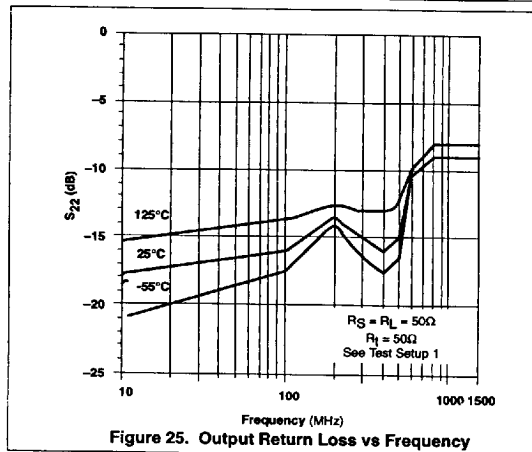
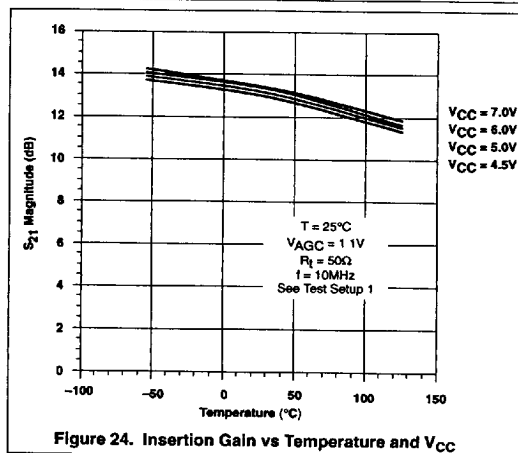
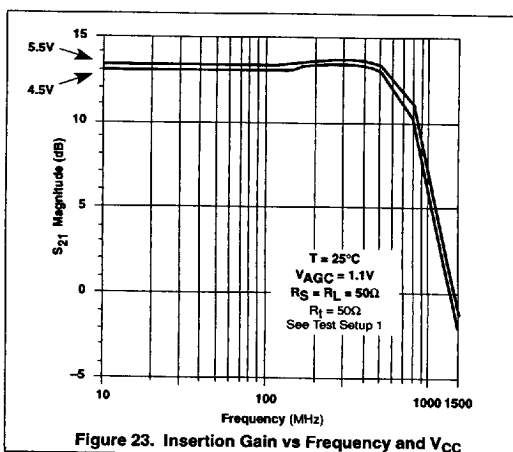
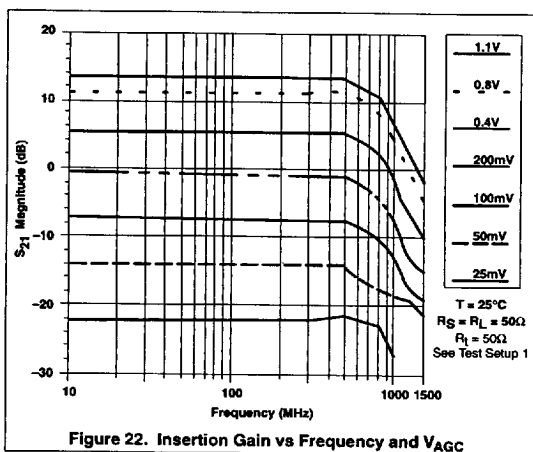
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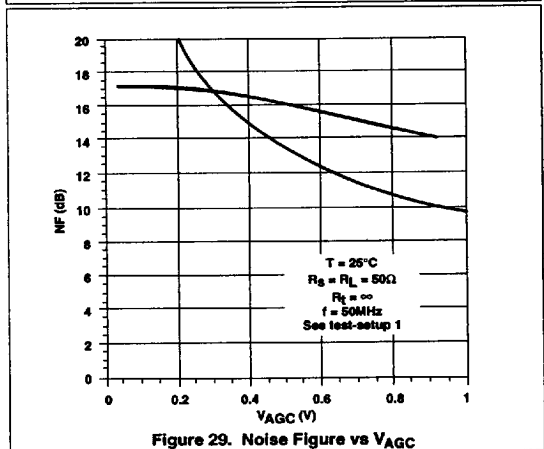
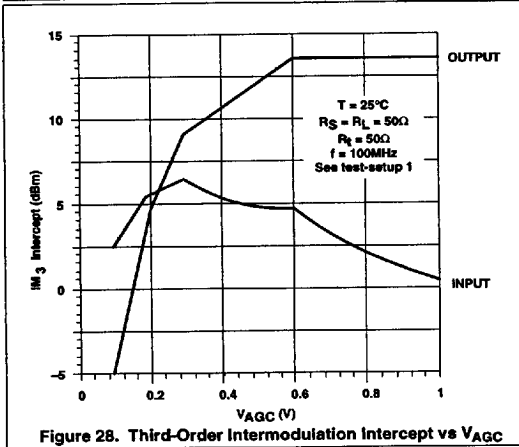
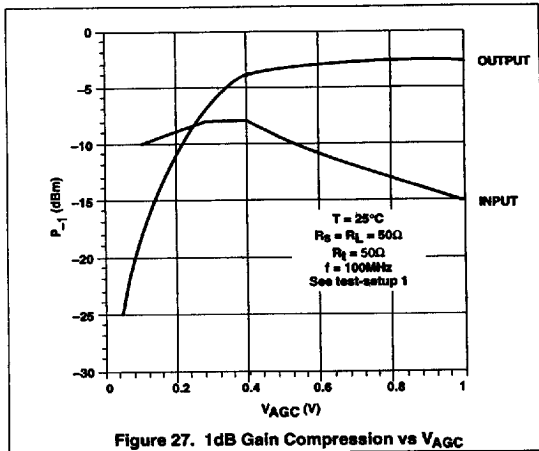
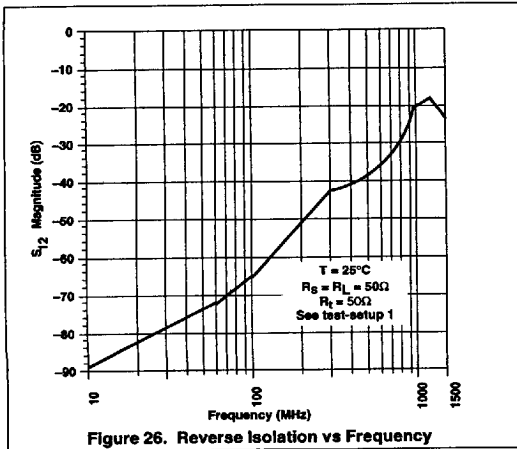
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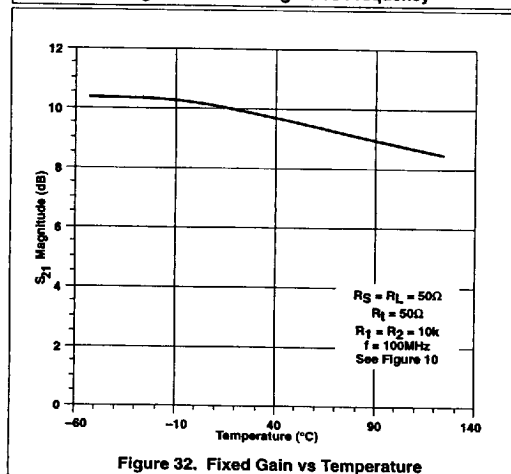
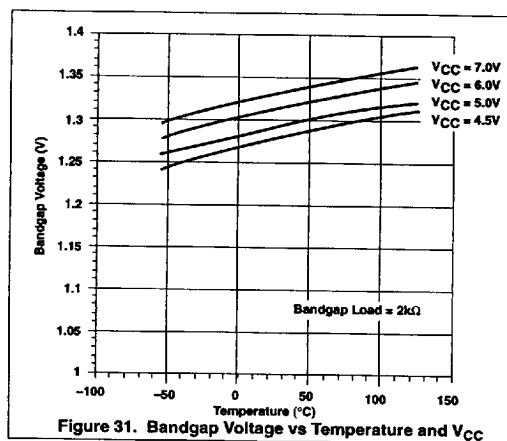
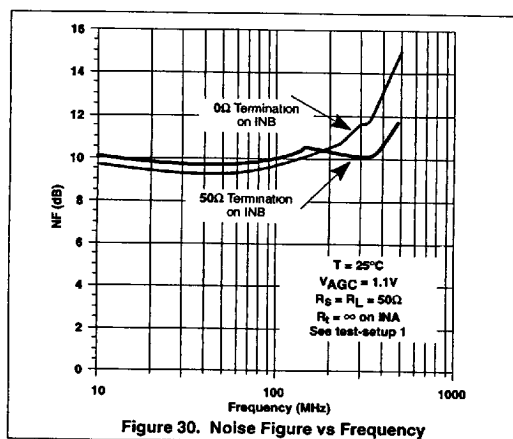
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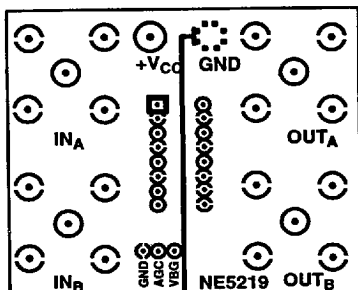
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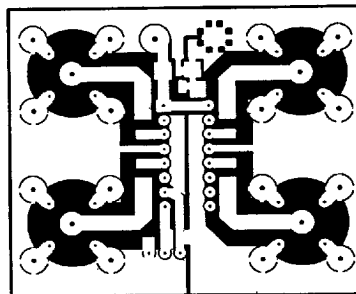


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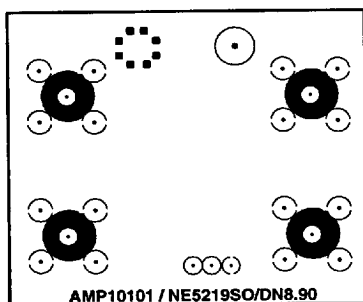


TOP VIEW - COMPONENT SIDE

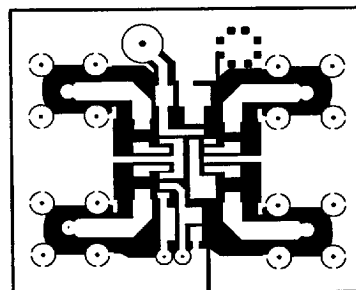


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package



TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)