ADC08831 /ADC08832 8-Bit Serial I/O CMOS A/D Converters with Multiplexer and Sample/Hold Function

Check for Samples: ADC08831, ADC08832

FEATURES

- **3-Wire Serial Digital Data Link Requires Few I/O Pins**
- **Analog Input Track/Hold Function**
- **2-Channel Input Multiplexer Option with Address Logic**
- **Analog Input Voltage Range from GND to V_{CC}**
- **No Zero or Full Scale Adjustment Required**
- **TTL/CMOS Input/Output Compatible**
- **Superior Pin Compatible Replacement for ADC0831/2**

APPLICATIONS

- **Digitizing Sensors and Waveforms**
- **Process Control Monitoring**
- **Remote Sensing in Noisy Environments**
- **Instrumentation**
- **Embedded Systems**

KEY SPECIFICATIONS

- **Resolution: 8 Bits**
- **Conversion Time (f_C = 2 MHz): 4µs (Max)**
- **Power Dissipation: 8.5mW (Typ)**
- **Low Power Mode: 3.0mW (Typ)**
- **Single Supply: $5V_{DC}$**
- **Total Unadjusted Error: ±1LSB**
- **No Missing Codes over Temperature**

DESCRIPTION

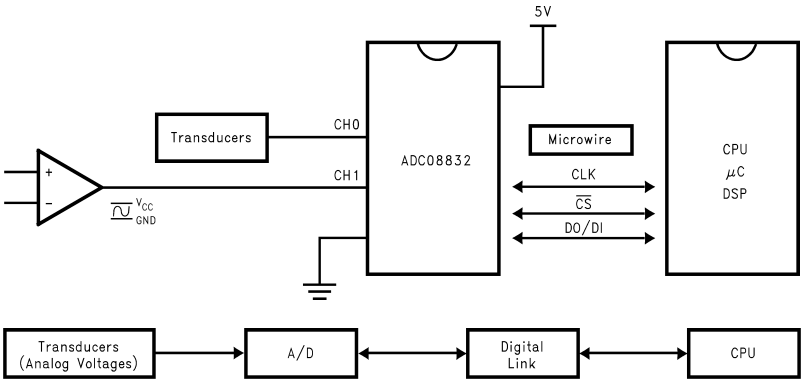
The ADC08831/ADC08832 are 8-bit successive approximation Analog to Digital converters with 3-wire serial interfaces and a configurable input multiplexer for 2 channels. The serial I/O will interface to COPSfamily of micro-controllers, PLD's, microprocessors, DSP's, or shift registers. The serial I/O is configured to comply with the MICROWIRE serial data exchange standard.

To minimize total power consumption, the ADC08831/ADC08832 automatically go into low power mode whenever they are not performing conversions.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. The voltage reference input can be adjusted to allow encoding of small analog voltage spans to the full 8-bits of resolution.

Typical Application



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Connection Diagram

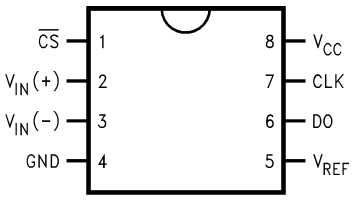


Figure 1. ADC08831
8-Lead SOIC or VSSOP
See D or DGK Packages

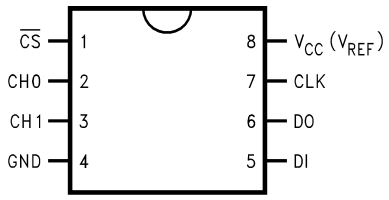


Figure 2. ADC08832
8-Lead SOIC or VSSOP
See D or DGK Packages

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage (V_{CC})		6.5V
Voltage at Inputs and Outputs		−0.3V to V_{CC} + 0.3V
Input Current at Any Pin(4)		±5 mA
Package Input Current(4)		±20 mA
ESD Susceptibility(5)	Human Body Model	2000V
	Machine Model	200V
Junction Temperature(6)		150°C
Storage Temperature Range		−65° C to 150°C
Mounting Temperature	Lead Temp. (soldering, 10 sec)	260°C
	Infrared (10 sec)	215°C

(1) All voltages are measured with respect to GND = 0 V_{DC}, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage V_{IN} at any pin exceeds the power supplies (V_{IN} < (GND) or V_{IN} > V_{CC},) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.
(5) Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor. The machine mode is a 200pF capacitor discharged directly into each pin.
(6) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Operating Ratings(1)(2)

Temperature Range		−40°C ≤ T_J ≤ +85°C
Supply Voltage		4.5 V to 6.0 V
Thermal Resistance (θ_{jA})	VSSOP, 8-pin Surface Mount	122°C/W
	SOIC Package, 8-pin Surface Mount	235°C/W
Clock Frequency		10kHz ≤ f_{CLK} ≤ 2MHz

(1) Operating Ratings indicate conditions for which the device is functional. These ratings do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V_{DC}, unless otherwise specified.

Electrical Characteristics

The following specifications apply for $V_{CC} = V_{REF} = +5V_{DC}$, and $f_{CLK} = 2$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical[1]	Limits[2]	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
TUE	Total Unadjusted Error	See[3]	±0.3	**±1**	LSB (max)
	Offset Error		±0.2		LSB
DNL	Differential NonLinearity		±0.2		LSB
INL	Integral NonLinearity		±0.2		LSB
FS	Full Scale Error		±0.3		LSB
R_{REF}	Reference Input Resistance	See[4]	3.5	**2.8** **5.9**	kΩ (min) kΩ (max)
V_{IN}	Analog Input Voltage	See[5]		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	DC Common-Mode Error			**±¼**	LSB (max)
	Power Supply Sensitivity	V_{CC} = 5V ±10%, V_{CC} = 5V ±5%		±¼ **±¼**	LSB (max) LSB (max)
	On Channel Leakage Current[6]	On Channel = 5V, Off Channel = 0V		0.2 **1**	µA (max)
		On Channel = 0V Off Channel = 5V		−0.2 **−1**	µA (min)
	Off Channel Leakage Current[7]	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	µA (min)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	µA (max)
DC CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage			**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 5.0V	0.05	**+1**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	0.05	**−1**	µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	V_{CC} = 4.75V:			
		I_{OUT} = −360 µA		**2.4**	V (min)
		I_{OUT} = −10 µA		**4.5**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**	V (max)

(1) Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.
(2) Specified to TI's AOQL (Average Outgoing Quality Level).
(3) Total Unadjusted Error (TUE) includes offset, full-scale, linearity, multiplexer errors.
(4) It is not tested for the ADC08832.
(5) For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see ADC08832 Functional Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.
(6) Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining off channel tied low (0 V_{DC}), total current flow through the off channel is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channel is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.
(7) Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining off channel tied low (0 V_{DC}), total current flow through the off channel is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channel is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

Electrical Characteristics (continued)

The following specifications apply for $V_{CC} = V_{REF} = +5V_{DC}$, and $f_{CLK} = 2$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limits)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$		**−3.0** **3.0**	µA (max) µA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		**−6.5**	mA (max)
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		**8.0**	mA (min)
I_{CC}	Supply Current ADC08831 CLK = V_{CC}	$\overline{CS} = V_{CC}$	0.6	**1.0**	mA (max)
		$\overline{CS}$ = LOW	1.7	**2.4**	mA (max)
I_{CC}	Supply Current ADC08832 CLK = V_{CC}(8)	$\overline{CS} = V_{CC}$	1.3	**1.8**	mA (max)
		$\overline{CS}$ = LOW	2.4	**3.5**	mA (max)

(8) For the ADC08832 V_{ref} is internally tied to V_{CC}, therefore, for the ADC08832 reference current is included in the supply current.

Electrical Characteristics

The following specifications apply for $V_{CC} = V_{REF} = +5\ V_{DC}$, and $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limits)
f_{CLK}	Clock Frequency			**2**	MHz (max)
	Clock Duty Cycle(3)			**40** **60**	% (min) % (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 2MHz		**8** **4**	$1/f_{CLK}$ (max) µs (max)
t_{CA}	Acquisition Time			**½**	$1/f_{CLK}$ (max)
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid(4)	C_L = 100 pF: Data MSB First Data LSB First		 **250** **200**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10 pF, R_L = 10 kΩ (see TRI-STATE Test Circuits and Waveforms)	50		ns
		C_L = 100 pF, R_L = 2 kΩ		**180**	ns (max)
C_{IN}	Capacitance of Analog Input(5)		13		pF
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

(1) Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.
(2) Specified to TI's AOQL (Average Outgoing Quality Level).
(3) A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 250 ns. The maximum time the clock can be high or low is 60 µs.
(4) Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in to allow for comparator response time.
(5) Analog inputs are typically 300 ohms input resistance to a 13pF sample and hold capacitor.

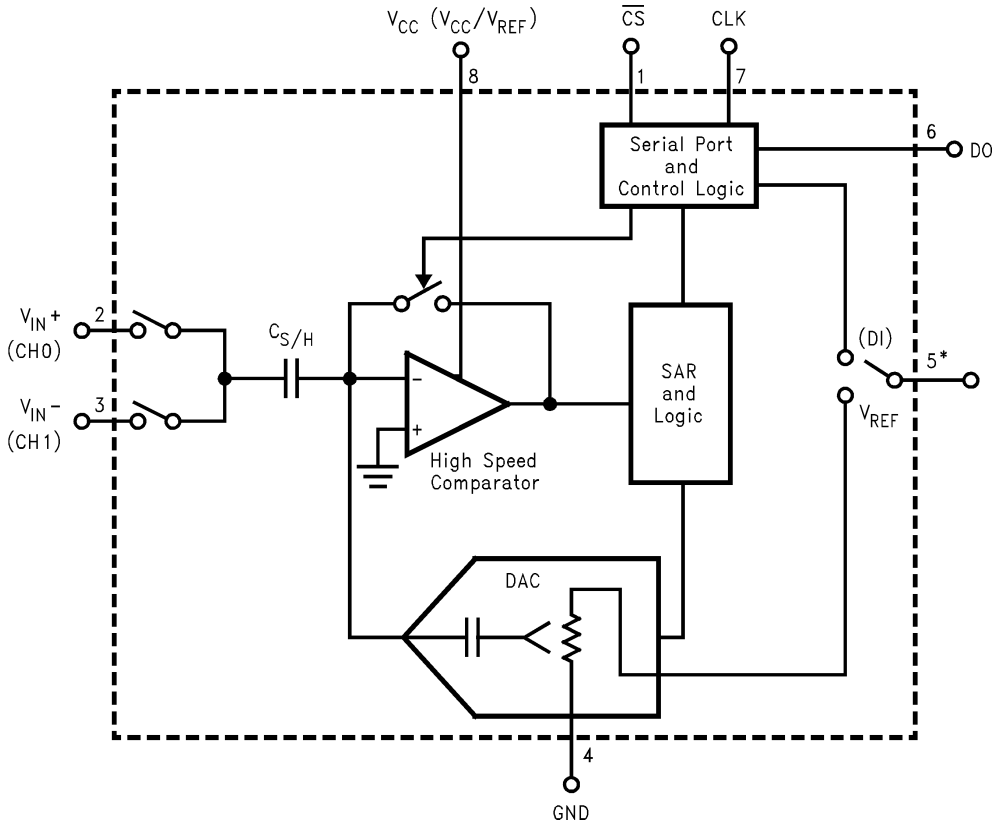
Dynamic Characteristics

The following specifications apply for V_{CC} = 5V, f_{CLK} = 2MHz, T_A= 25°C, R_{SOURCE} = 50Ω, f_{IN} = 45kHz, V_{IN} = $5V_P$, V_{REF} = 5V, non-coherent 2048 samples with windowing.

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limits)
f_S	Sampling Rate ADC08831 ADC08832	f_{CLK}/11 f_{CLK}/13 (3)		181 153	ksps ksps
SNR	Signal-to -Noise Ratio (4)		48.5		dB
THD	Total Harmonic Distortion (5)		−59.5		dB
SINAD	Signal-to -Noise and Distortion		48.0		dB
ENOB	Effective Number Of Bits (6)		7.7		Bits
SFDR	Spurious Free Dynamic Range		62.5		dB

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Specified to TI's AOQL (Average Outgoing Quality Level).
(3) The maximum sampling rate is slightly less than f_{CLK}/11 if $\overline{CS}$ is reset in less than one clock period.
(4) The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in it's calculation.
(5) The contributions from the first 6 harmonics are used in the calculation of the THD.
(6) Effective Number Of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation ENOB = (SINAD-1.76)/6.02.

Block Diagram



*For ADC08831 V_{REF} pin is available, for ADC08832 DI pin is available, and V_{REF} is tied to V_{CC}
Pin names in parentheses refer to ADC08832

Typical Performance Characteristics

The following specifications apply for T_A = 25°C, V_{CC} = V_{REF} = 5V, unless otherwise specified.

Linearity Error (TUE) vs Reference Voltage

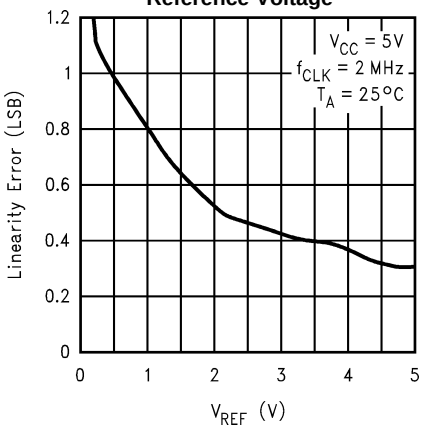


Figure 3.

Linearity Error (TUE) vs Temperature

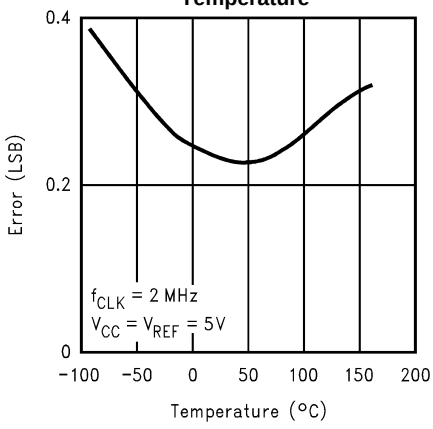


Figure 4.

Linearity Error (TUE) vs Clock Frequency

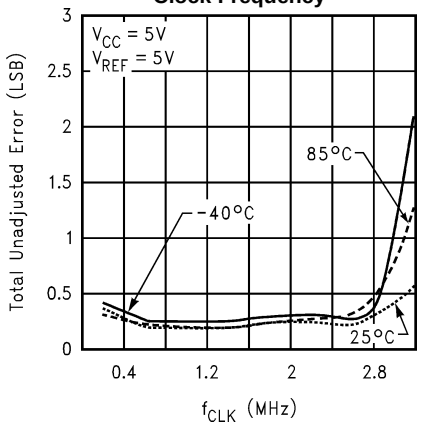


Figure 5.

Power Supply Current vs Temperature (ADC08831)

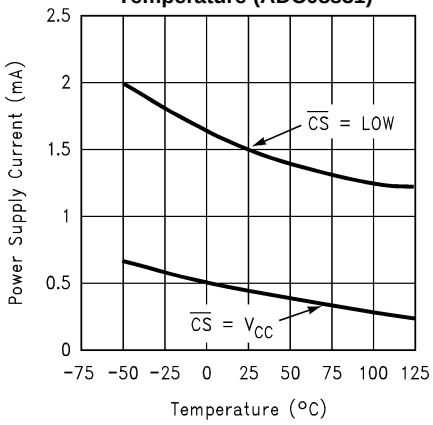


Figure 6.

Power Supply Current vs Temperature (ADC08832)

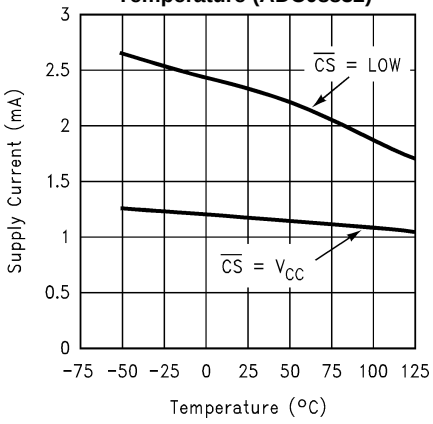


Figure 7.

Power Supply Current vs Clock Frequency, CS = Low, ADC08831

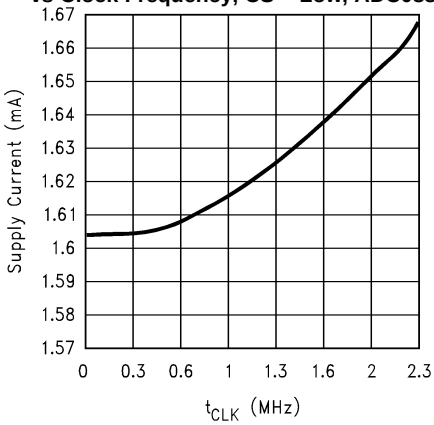


Figure 8.

Typical Performance Characteristics (continued)

The following specifications apply for T_A = 25°C, V_{CC} = V_{REF} = 5V, unless otherwise specified.

Output Current vs Temperature

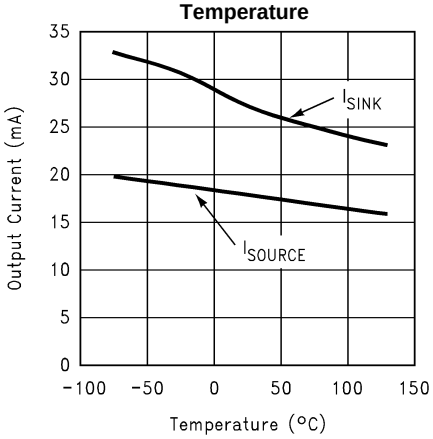


Figure 9.

Spectral Response with 10KHz Sine Wave Input

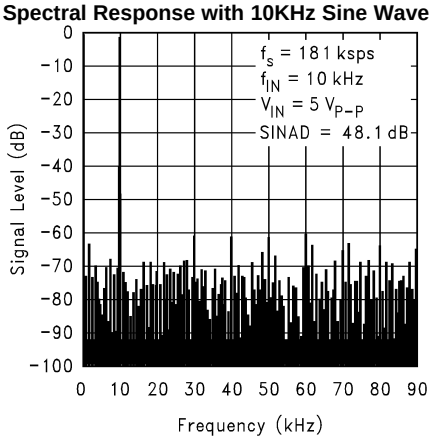


Figure 10.

Spectral Response with 55 KHz Sine Wave Input

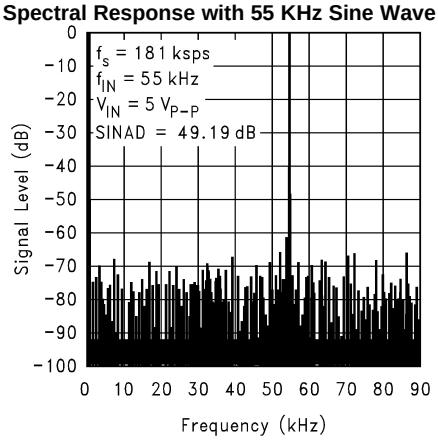


Figure 11.

Spectral Response with 90 KHz Sine Wave Input

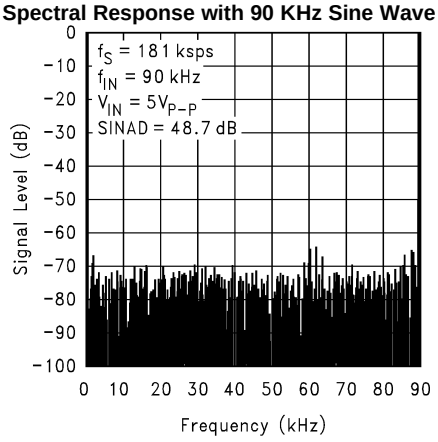


Figure 12.

Total Unadjuster Error Plot

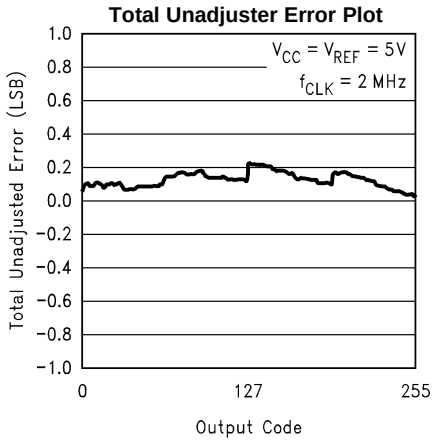


Figure 13.

Leakage Current Test Circuit

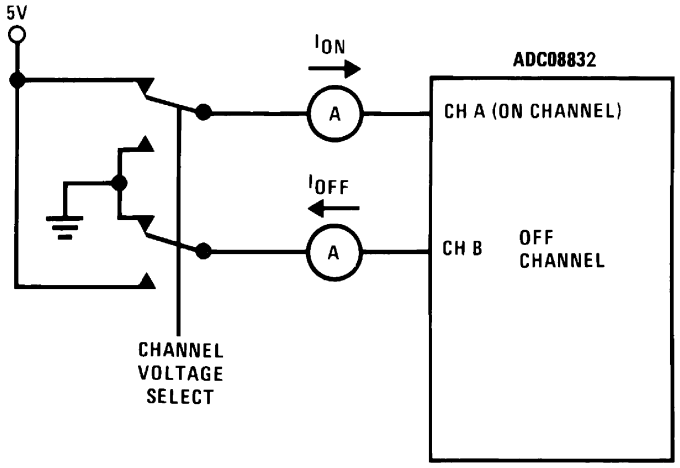
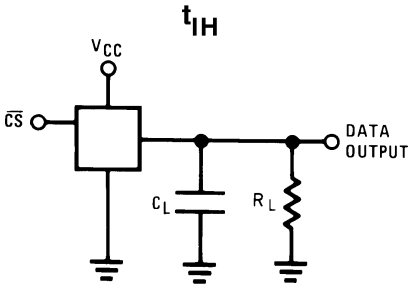
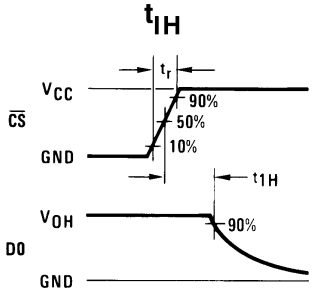


Figure 14.

TRI-STATE Test Circuits and Waveforms





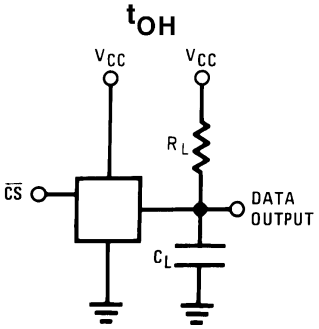


Figure 15.

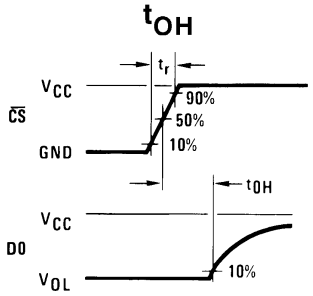


Figure 16.

Timing Diagrams

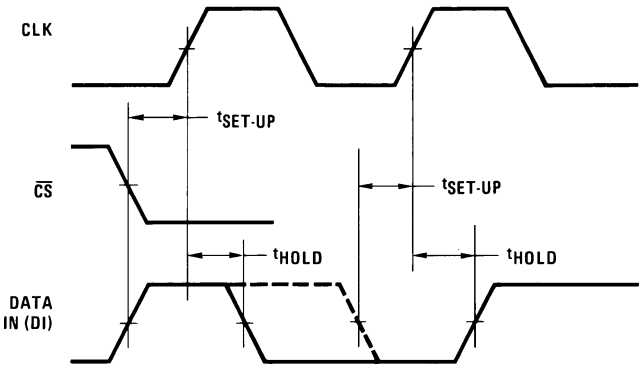


Figure 17. Data Input Timing

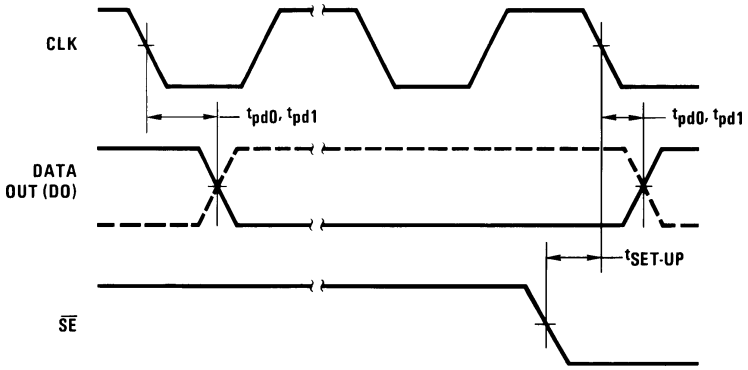


Figure 18. Data Output Timing

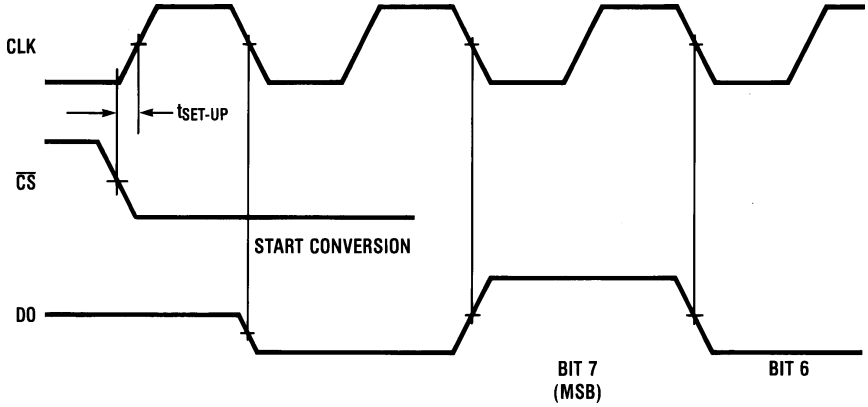
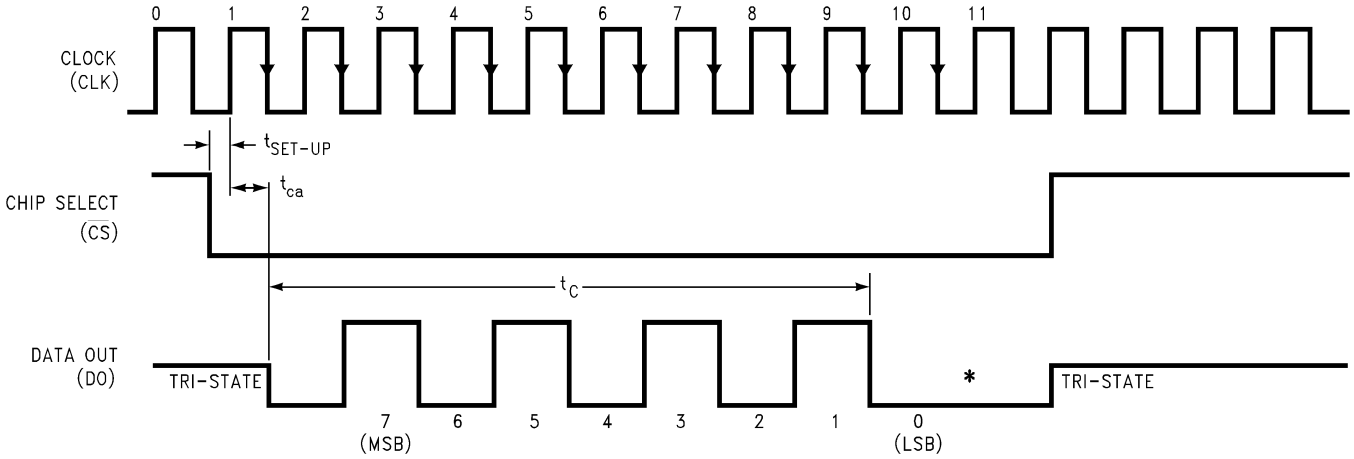


Figure 19. ADC08831 Start Conversion Timing



*LSB first output not available on ADC08831.

Figure 20. ADC08831 Timing

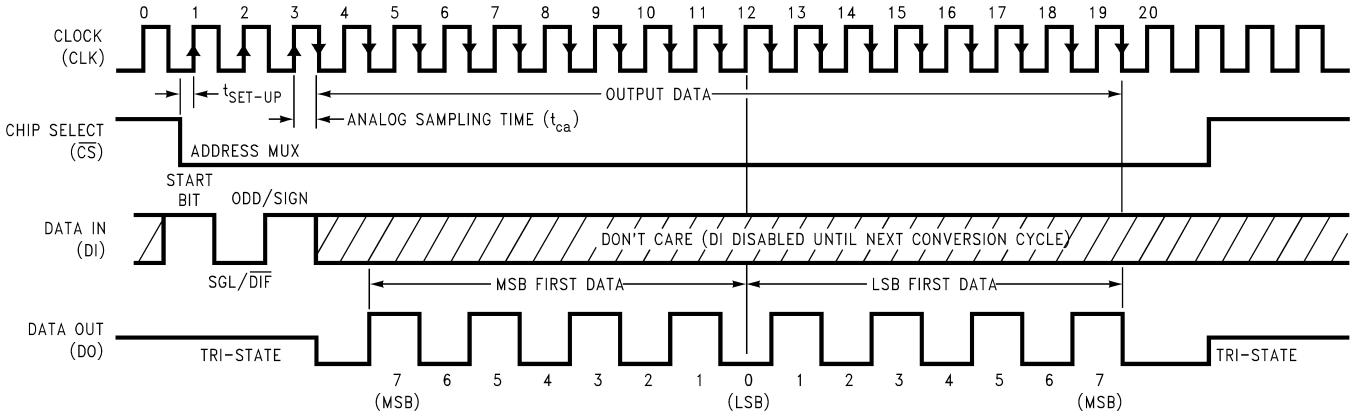
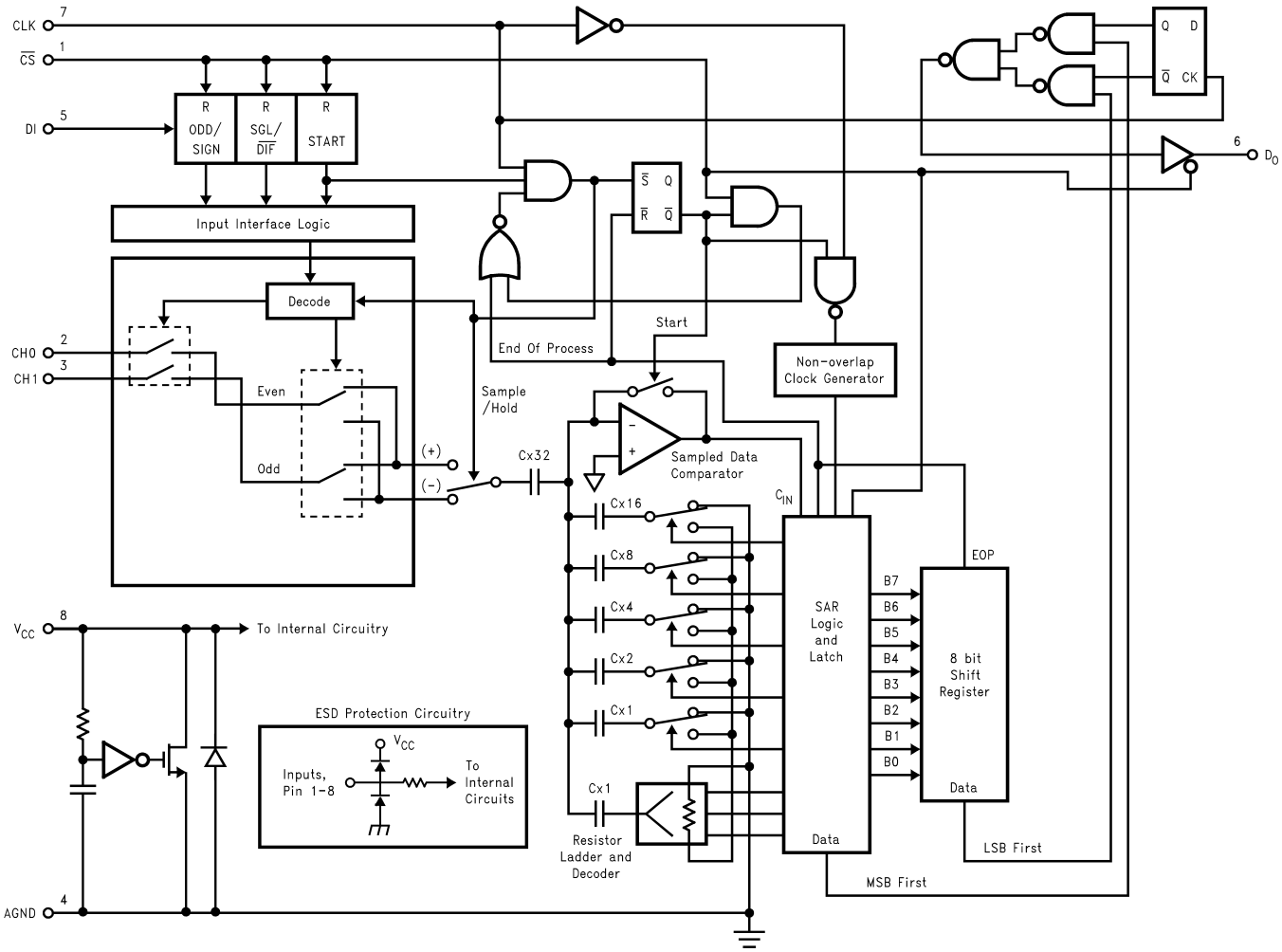


Figure 21. ADC08832 Timing

ADC08832 Functional Block Diagram



*Some of these functions/pins are not available with other options.

FUNCTIONAL DESCRIPTION

MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, or differential operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs, differential inputs, as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes for the ADC08832.

The MUX address is shifted into the converter via the DI line. Because the ADC08831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

Table 1. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08831	1	1	8 or 14
ADC08832	2	1	8 or 14

Table 2. MUX Addressing: ADC08832

Single-Ended MUX Mode				
MUX Address			Channel #	
Start Bit	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	1	0	+	
1	1	1		+

Differential MUX Mode				
MUX Address			Channel #	
Start Bit	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	0	+	−
1	0	1	−	+

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion.

The analog input voltages for each channel can range from 50mV below ground to 50mV above V_{CC} (typically 5V) without degrading conversion accuracy.

THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements. It allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to Timing Diagrams and ADC08832 Functional Block Diagram and to follow a complete conversion sequence. For clarity, a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word, if applicable.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 bits to be the MUX assignment word.
3. When the start bit has been shifted into the start location of the MUX register, and the input channel has been assigned, a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle to a final analog input value. The DI line is disabled at this time. It no longer accepts data.
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed.
7. The stored data in the successive approximation register is loaded into an internal shift register. The data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. The ADC08831 is an exception in that its data is only output in MSB first format.
8. The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

Reducing Power Consumption

The ADC08831 operate up to a 2MHz clock frequency, or about 181 ksps. At 5V supply, it consumes about 1.7 mA or 8.5 mW when $\overline{CS}$ is logic low. The ADC08831 has a low power mode to minimize total power consumption.

When the chip select is asserted with a logic high, some analog circuitry and digital logic are pulled to a static, low power condition. Also, DOUT, the output driver is taken into TRI-STATE mode.

To optimize static power consumption, special attention is needed to the digital input logic signals: CLK, $\overline{CS}$, DI. Each digital input has a large CMOS buffer between V_{CC} and GND. A traditional TTL level high (2.4V) will be sufficient for each input to read a logical "1". However, there could be a large V_{IH} to V_{CC} voltage difference at each input. Such a voltage difference would cause static power dissipation, even when chip select pin is high and the part is in low power mode.

Therefore, to minimize static power dissipation, it is recommended that all digital input logic levels should equal the converter's supply. Various CMOS logic is particularly well suited for this application.

The reference pin on the ADC08831 is not affected by the power-down mode. To reduce static reference current during non-conversion time, there are a couple options. First, a low voltage external reference (ie, 2.5V could be used). A shunt reference, such as the LM385-2.5, could be powered by a logic gate that is the inverse of the signal on $\overline{CS}$. When $\overline{CS}$ is high, the reference is off. As a second option, an external, low on-resistance switch could be used.

The ADC08832 is similar to the ADC08831, except its reference is derived from V_{CC}. The ADC08832 does enter a low-power mode when $\overline{CS}$ is logic high, as the analog and digital logic enter static current modes. However power dissipation from the reference ladder occurs, regardless of the signal on $\overline{CS}$

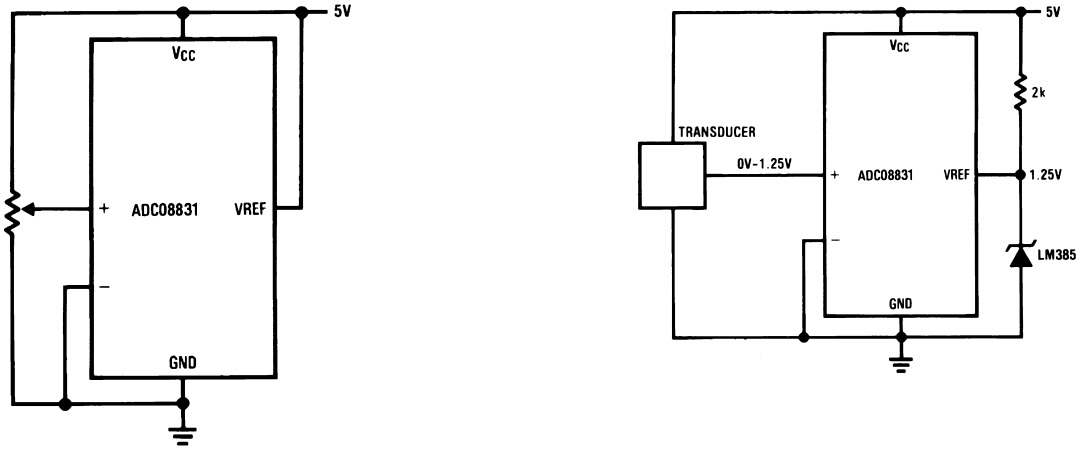
REFERENCE CONSIDERATIONS

The voltage applied to the reference input on these converters, V_{REF}, defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply. The devices can be used either in ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance which can be as low as 2.8kΩ. This pin is the top of a resistor divider string and capacitor array used for the successive approximation conversion.

In a ratiometric system the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC08832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385, LM336 and LM4040 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



Left) Ratiometric

Right) Absolute with a Reduced Span

Figure 22. Reference Examples

THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}}\right) \quad (1)$$

where

- where f_{CM} is the frequency of the common-mode signal
- V_{PEAK} is its peak voltage value
- f_{CLK} is the A/D clock frequency

For a 60Hz common-mode signal to generate a ¼ LSB error (≅5mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. Bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1µA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

Sample and Hold

The ADC08831/2 provide a built-in sample-and-hold to acquire the input signal. The sample and hold can sample input signals in either single-ended or pseudo differential mode.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time. To achieve the full sampling rate, the analog input should be driven with a low impedance source (100Ω) or a high-speed op amp such as the LM6142. Higher impedance sources or slower op amps can easily be accommodated by allowing more time for the analog input to settle.

Source Resistance

The analog inputs of the ADC08831/2 look like a 13pF capacitor (C_{IN}) in series with 300Ω resistor (Ron). C_{IN} gets switched between the selected "+" and "−" inputs during each conversion cycle. Large external source resistors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog input to completely settle.

Board Layout Consideration, Grounding and Bypassing:

The ADC08831/2 are easy to use with some board layout consideration. They should be used with an analog ground plane and single-point grounding techniques. The GND pin should be tied directly to the ground plane.

The supply pin should be bypassed to the ground plane with a surface mount or ceramic capacitor with leads as short as possible. All analog inputs should be referenced directly to the single-point ground. Digital inputs and outputs should be shielded from and routed away from the reference and analog circuitry.

OPTIONAL ADJUSTMENTS

Zero Error

The offset of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for V_{REF} = 5.000V_{DC}).

Full Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input (or V_{CC} for the ADC08832) for a digital output code which is just changing from 1111 1110 to 1111 1111.

Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}\,(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right] \quad (2)$$

where

- V_{MAX} = the high end of the analog input range
- V_{MIN} = the low end (the offset zero) of the analog range
- (Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

DYNAMIC PERFORMANCE

Dynamic performance specifications are often useful in applications requiring waveform sampling and digitization. Typically, a memory buffer is used to capture a stream of consecutive digital outputs for post processing. Capturing a number of samples that is a power of 2 (ie, 1024, 2048, 4096) allows the Fast Fourier Transform (FFT) to be used to digitally analyze the frequency components of the signal. Depending on the application, further digital filtering, windowing, or processing can be applied.

Sampling Rate

The Sampling Rate, sometimes referred to as the Throughput Rate, is the time between repetitive samples by an Analog-to-Digital Converter. The sampling rate includes the conversion time, as well as other factors such a MUX setup time, acquisition time, and interfacing time delays. Typically, the sampling rate is specified in the number of samples taken per second, at the maximum Analog-to-Digital Converter clock frequency.

Signals with frequencies exceeding the Nyquist frequency (1/2 the sampling rate), will be aliased into frequencies below the Nyquist frequency. To prevent signal degradation, sample at twice (or more) than the input signal and/or use of a low pass (anti-aliasing) filter on the front-end. Sampling at a much higher rate than the input signal will reduce the requirements of the anti-aliasing filter.

Some applications require under-sampling the input signal. In this case, one expects the fundamental to be aliased into the frequency range below the Nyquist frequency. In order to be assured the frequency response accurately represents a harmonic of the fundamental, a band-pass filter should be used over the input range of interest.

Signal-to-Noise Ratio

Signal-to-Noise Ratio (SNR) is the ratio of RMS magnitude of the fundamental to the RMS sum of all the non-fundamental signal, excluding the harmonics, up to 1/2 of the sampling frequency (Nyquist).

Total Harmonic Distortion

Total Harmonic distortion is the ratio of the RMS sum of the amplitude of the harmonics to the fundamental input frequency.

$$THD = 20 \log [(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)^{1/2} / V_1] \quad (3)$$

where

- V_1 is the RMS amplitude of the fundamental
- V_2,V_3, V_4, V_5, V_6 are the RMS amplitudes of the individual harmonics.

In theory, all harmonics are included in THD calculations, but in practice only about the first 6 make significant contributions and require measurement.

For under-sampling applications, the input signal should be band pass filtered (BPF) to prevent out of band signals, or their harmonics, to appear in the spectral response.

The DC Linearity transfer function of an Analog-to-Digital Converter tends to influence the dominant harmonics. A parabolic Linearity curve would tend to create 2nd (and even) order harmonics, while an S-curve would tend to create 3rd (or odd) order harmonics. The magnitude of an DC linearity error correlates to the magnitude of the harmonics.

Signal-to-Noise and Distortion

Signal-to-Noise And Distortion ratio (SINAD) is the ratio of RMS magnitude of the fundamental to the RMS sum of all the non-fundamental signals, including the noise and harmonics, up to 1/2 of the sampling frequency (Nyquist), excluding DC.

SINAD is also dependent on the number of quantization levels in the A/D Converter used in the waveform sampling process. The more quantization levels, the smaller the quantization noise and theoretical noise performance. The theoretical SINAD for a N-Bit Analog-to-Digital Converter is given by:

$$SINAD = (6.02\ N + 1.76)\ dB$$

Thus, for an 8-bit converter, the ideal SINAD = 49.92 dB

Effective Number of Bits

Effective Number Of Bits (ENOB) is another specification to quantify dynamic performance. The equation for ENOB is given by:

$$ENOB = [(SINAD - 1.76)] / 6.02]$$

The Effective Number Of Bits portrays the cumulative effect of several errors, including quantization, non-linearities, noise, and distortion.

Spurious Free Dynamic Range

Spurious Free Dynamic Range (SFDR) is the ratio of the signal amplitude to the amplitude of the highest harmonic or spurious noise component. If the amplitude is at full scale, the specification is simply the reciprocal of the peak harmonic or spurious noise.

Applications

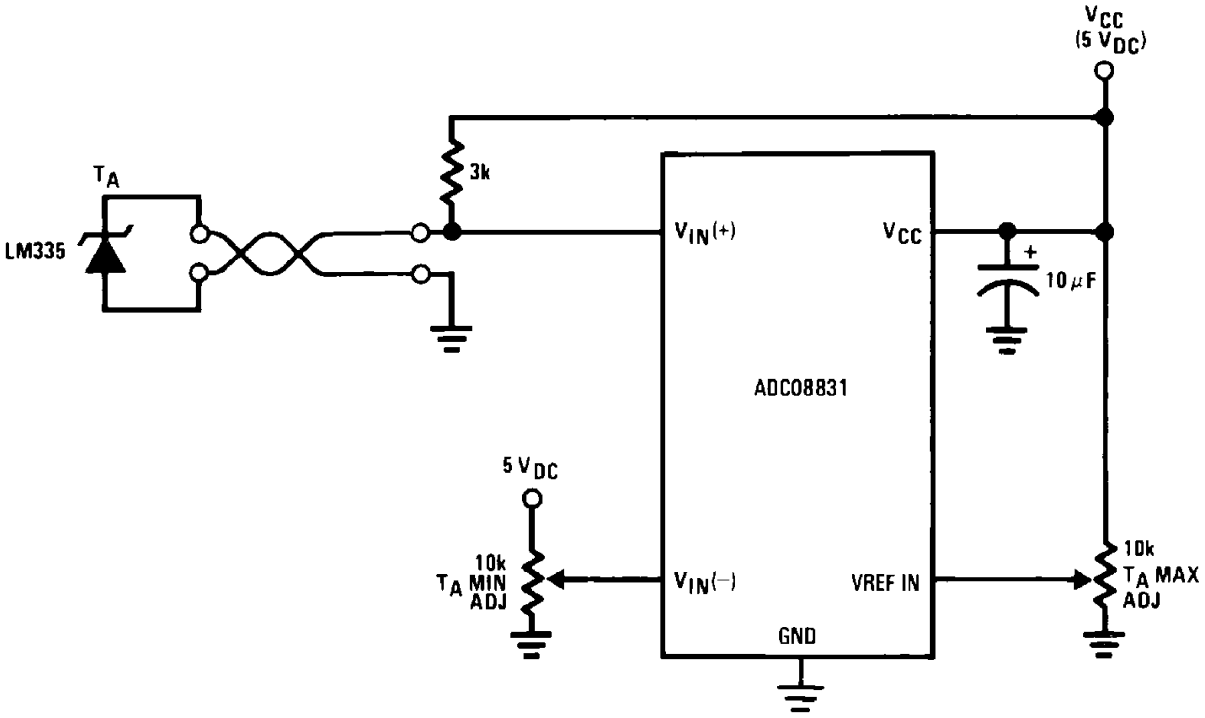
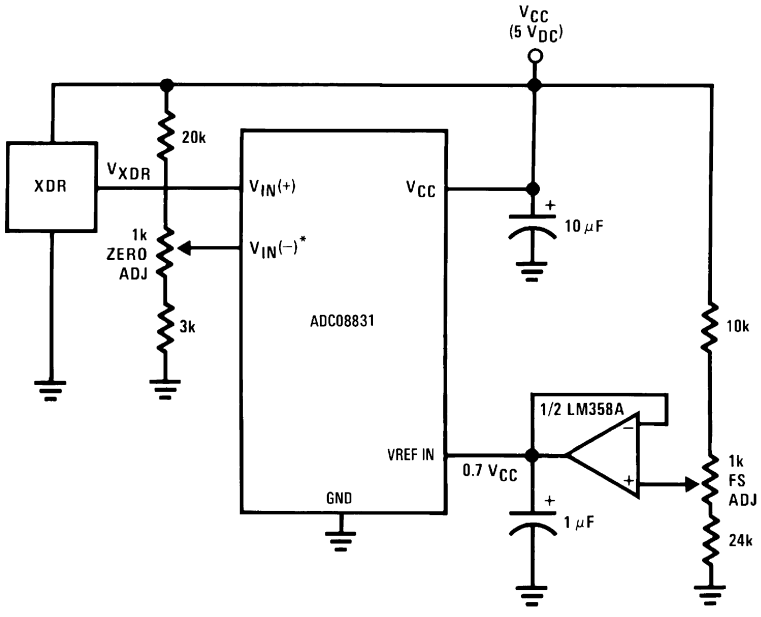


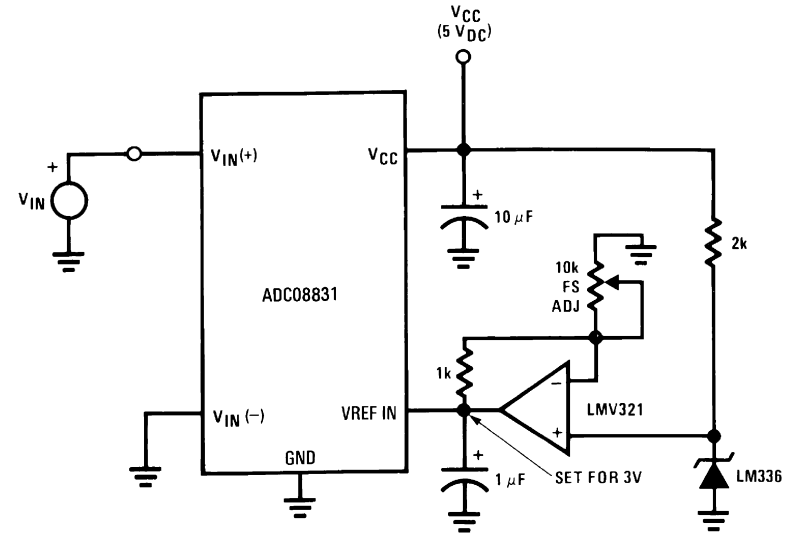
Figure 23. Low-Cost Remote Temperature Sensor



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

Figure 24. Operating with Ratiometric Transducers

Span Adjust; 0V ≤ V_{IN} ≤ 3V



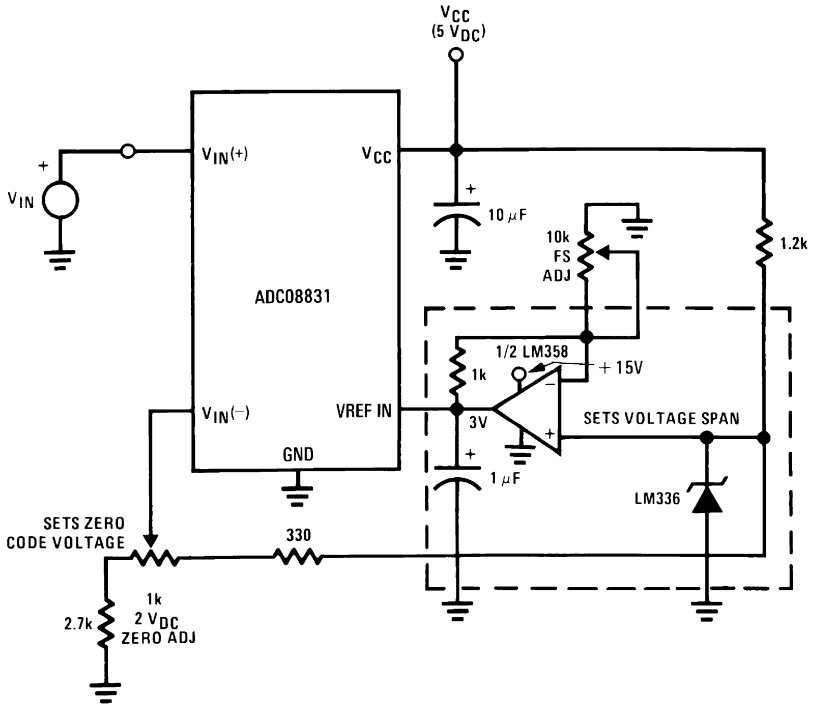
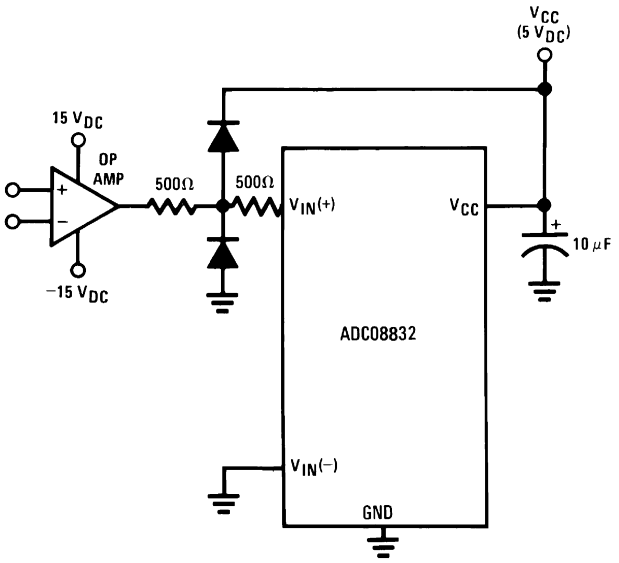
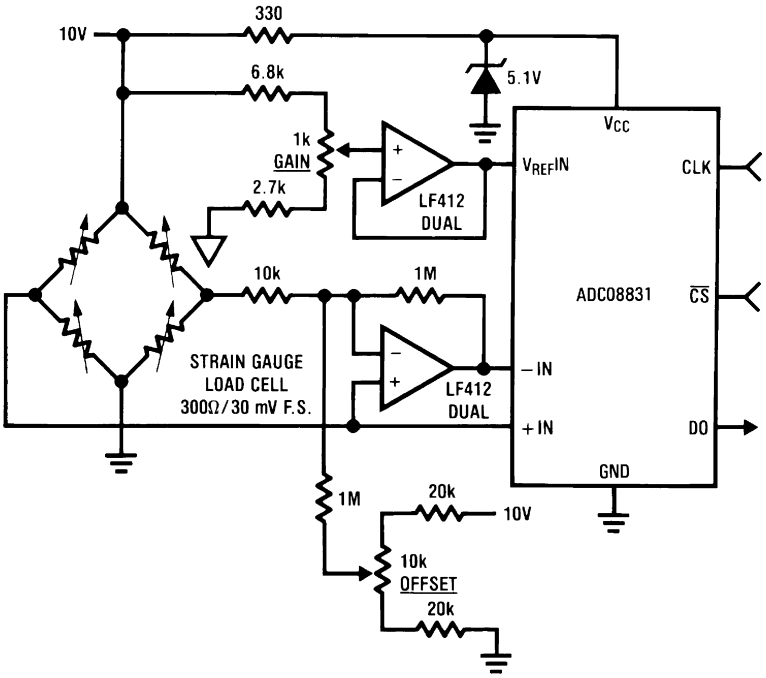


Figure 25. Zero-Shift and Span Adjust: 2V≤V_{IN} ≤ 5V



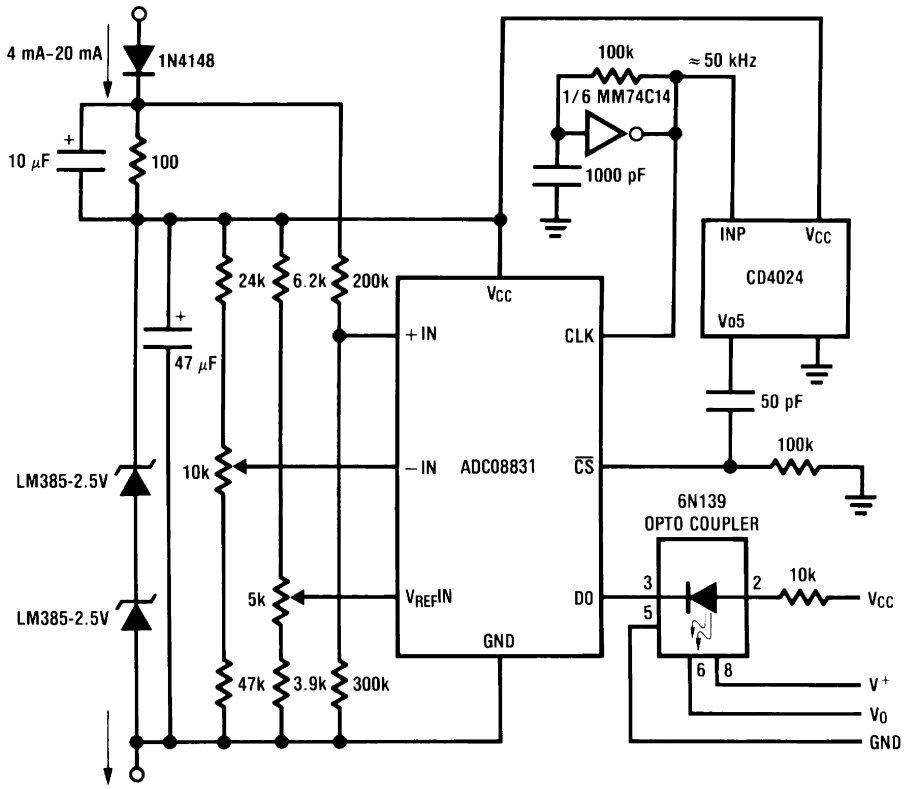
Diodes are 1N914

Figure 26. Protecting the Input



Uses one more wire than load cell itself
Two mini-DIPs could be mounted inside load cell for digital output transducer
Electronic offset and gain trims relax mechanical specs for gauge factor and offset
Low level cell output is converted immediately for high noise immunity

Figure 27. Digital Load Cell



All power supplied by loop
1500V isolation at output

Figure 28. 4 mA-20 mA Current Loop Converter

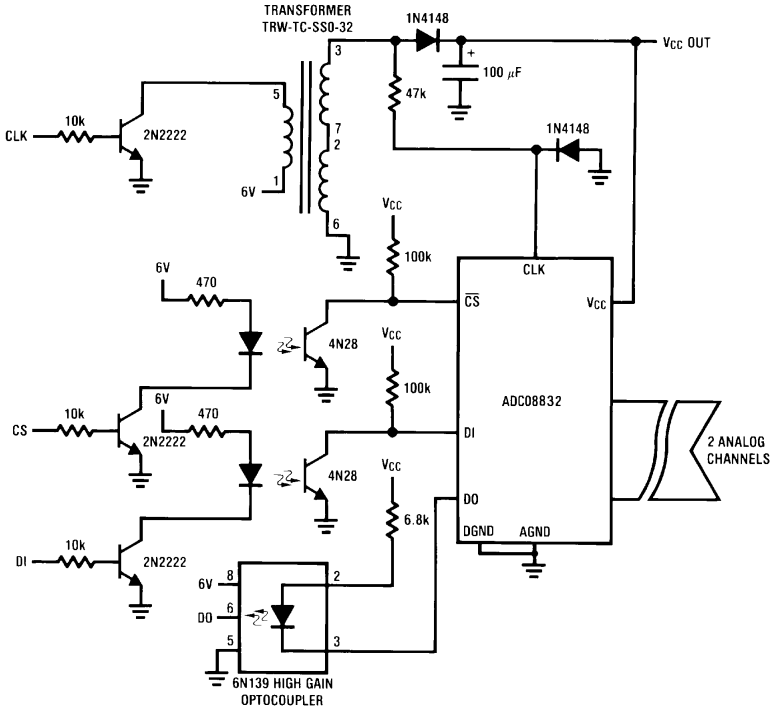


Figure 29. Isolated Data Converter

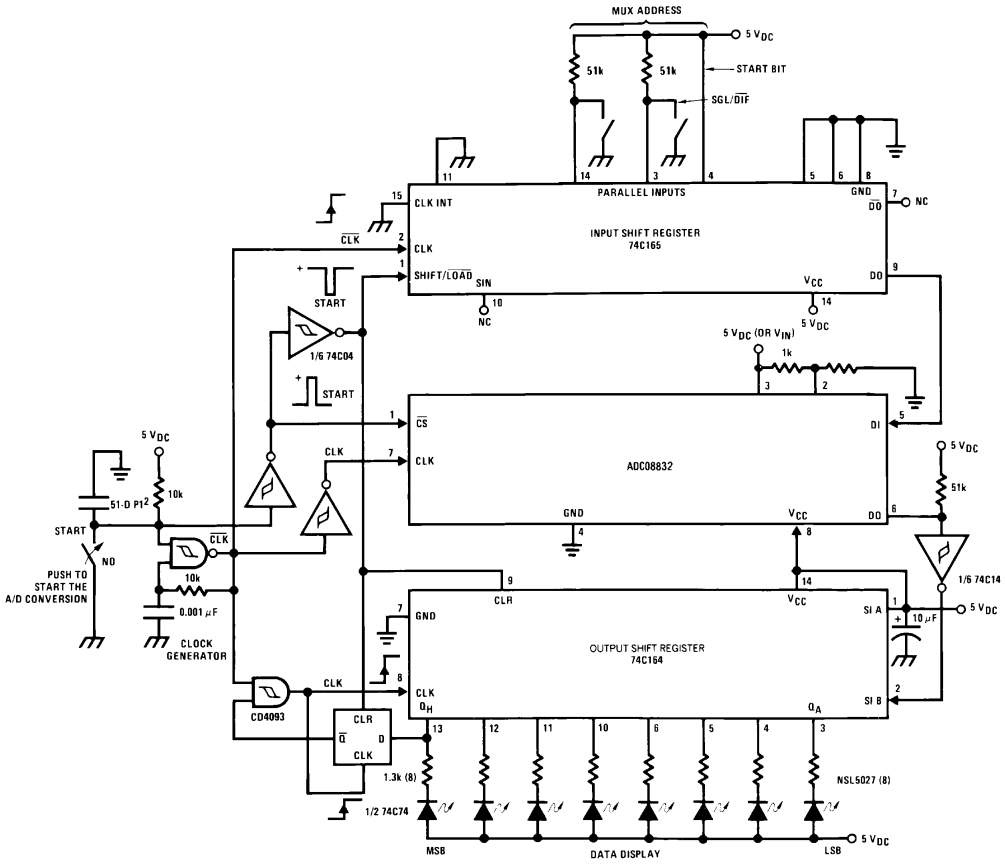


Figure 30. A "Stand-Alone" Hook-Up for ADC08832 Evaluation

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08831IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	08831 IM	
ADC08831IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	08831 IM	Samples
ADC08831IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	08831 IM	Samples
ADC08832IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	08832 IM	Samples
ADC08832IMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	8832	
ADC08832IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	8832	Samples
ADC08832IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	8832	Samples
ADC08832IMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	08832 IM	
ADC08832IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	08832 IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

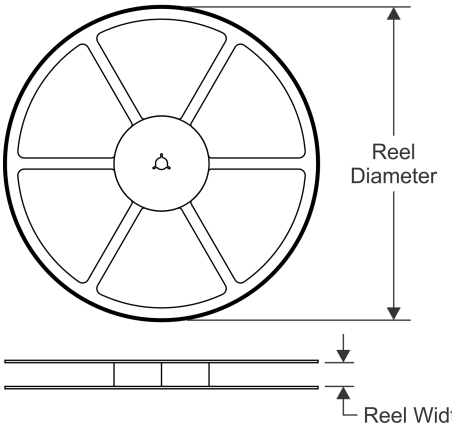
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

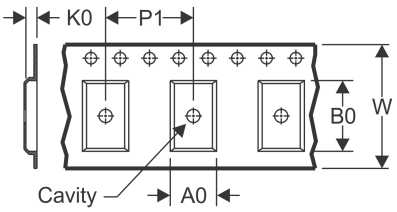
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

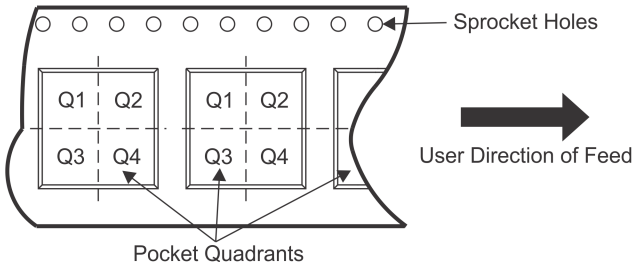


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

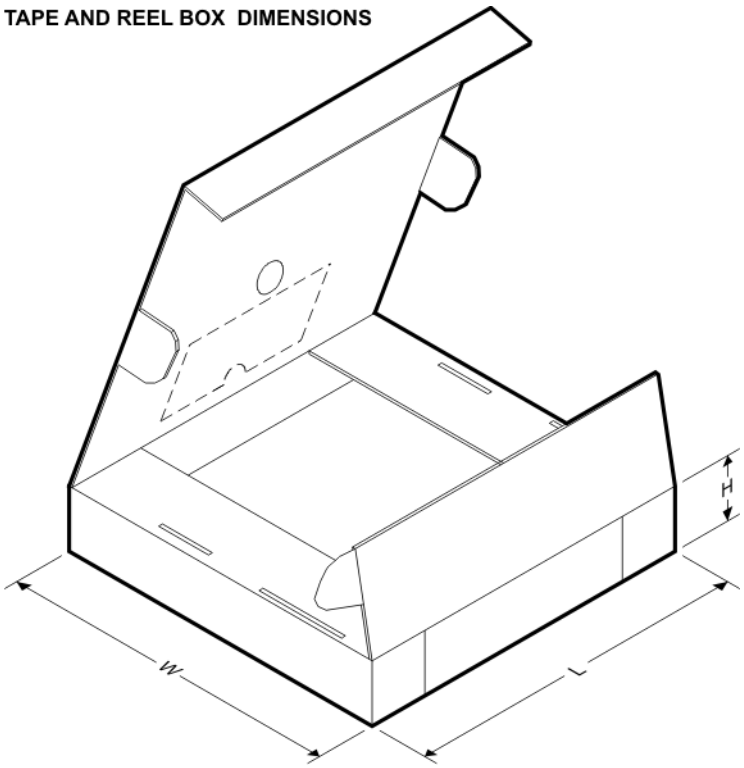
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC08831IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
ADC08832IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC08832IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC08832IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC08832IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
ADC08832IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

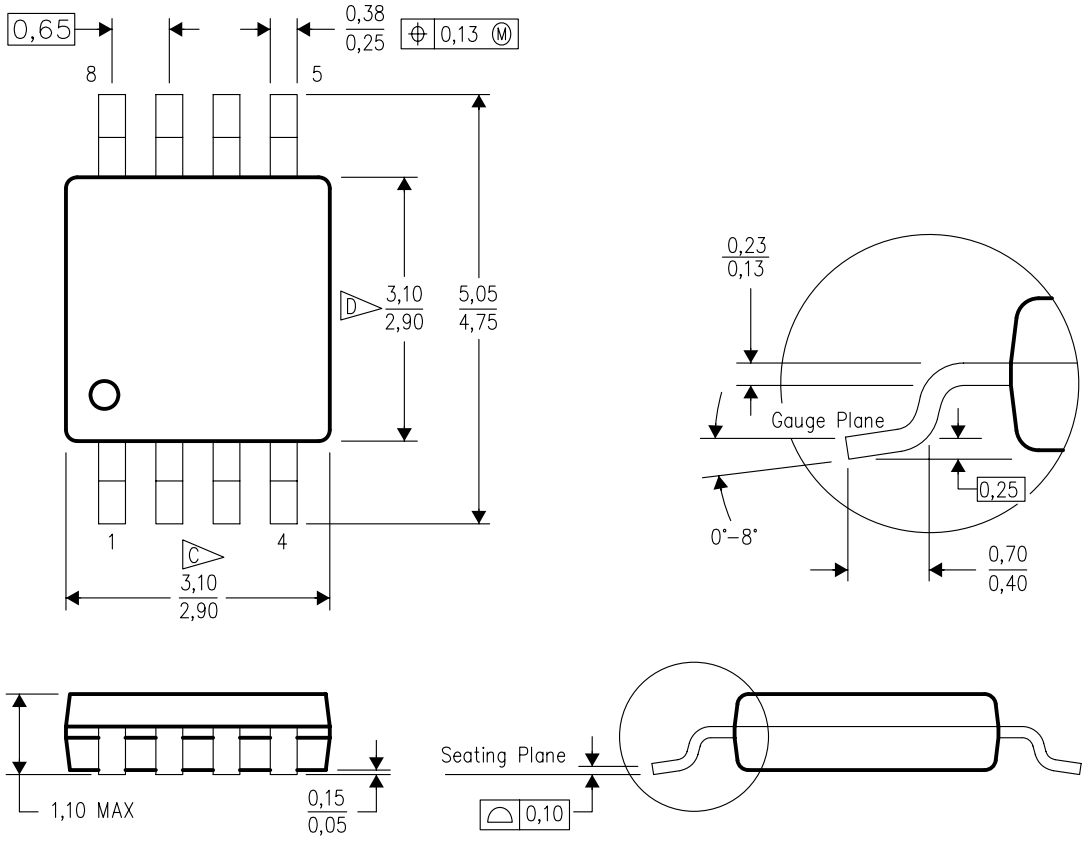
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC08831IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
ADC08832IMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
ADC08832IMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
ADC08832IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
ADC08832IMX	SOIC	D	8	2500	367.0	367.0	35.0
ADC08832IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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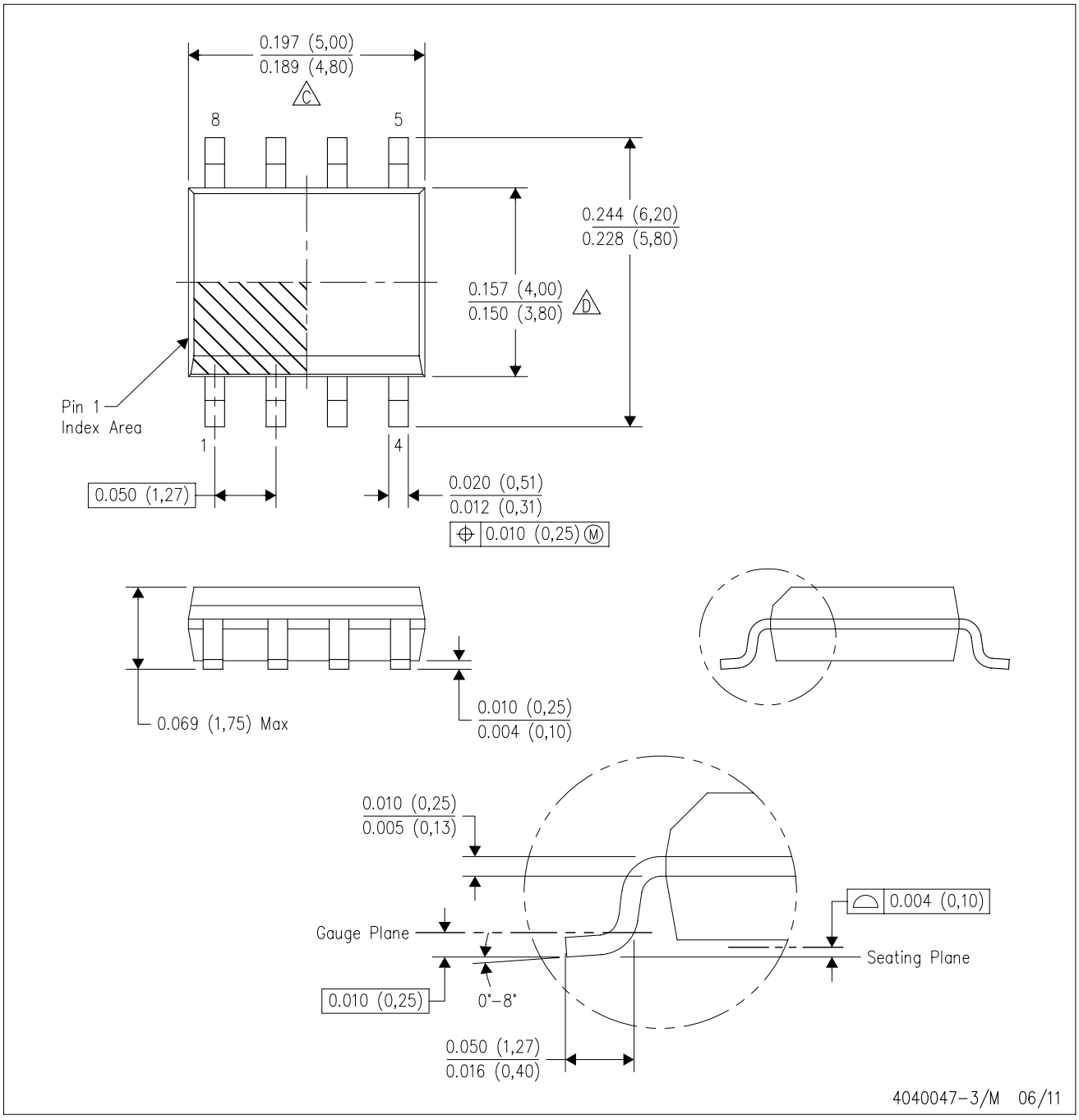
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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