

TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope available in TO220AB and SOT404. Using 'trench' technology which features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

QUICK REFERENCE DATA

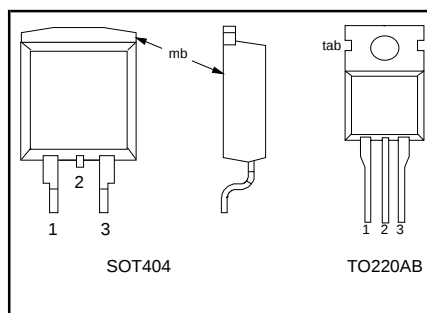
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	13	A
P_{tot}	Total power dissipation	53	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	150	mΩ
	$V_{GS} = 5\text{ V}$	137	mΩ
	$V_{GS} = 10\text{ V}$		

PINNING

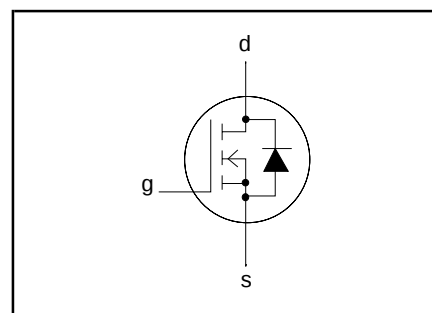
TO220AB & SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab/mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50\mu\text{S}$	-	15	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	13	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	9	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	53	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	53	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	2.8	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient(TO220AB)	in free air	60	-	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient(SOT404)	Minimum footprint, FR4 board	50	-	K/W

TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A

STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.5 -	1.5 - -	2.0 - 2.3	V V V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	- -	0.05 -	10 500	μA μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 13\text{ A}$ $T_j = 175^\circ\text{C}$	- -	125 -	150 300	m Ω m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 13\text{ A}$	-	116	137	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 13\text{ A}$	-	124	161	m Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	254	339	pF
C_{oss}	Output capacitance		-	54	65	pF
C_{rss}	Feedback capacitance		-	42	58	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}$; $R_{load} = 1.2\Omega$; $V_{GS} = 5\text{ V}$; $R_G = 10\Omega$	-	6	6	ns
t_r	Turn-on rise time		-	285	428	ns
t_{doff}	Turn-off delay time		-	1	1.4	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die(TO220AB)	-	3.5	-	nH
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die(SOT404)	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

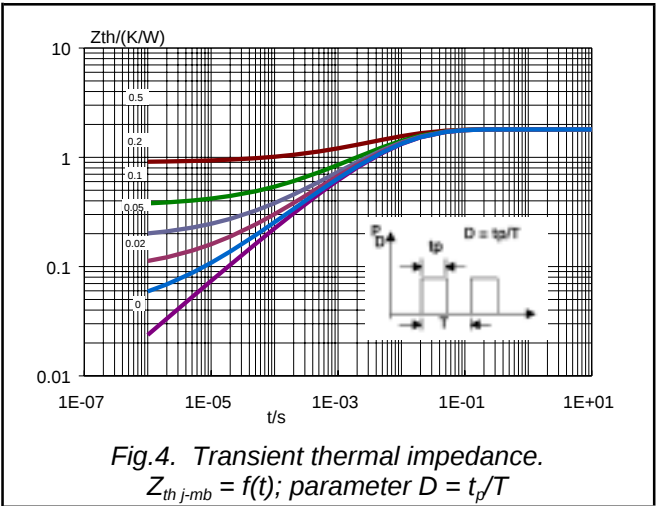
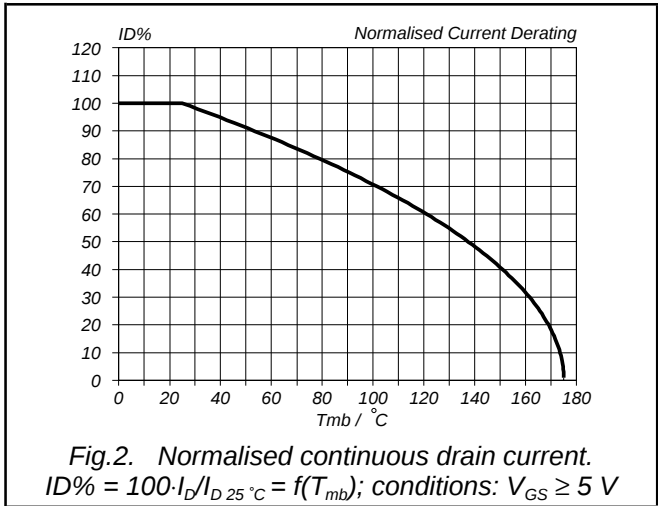
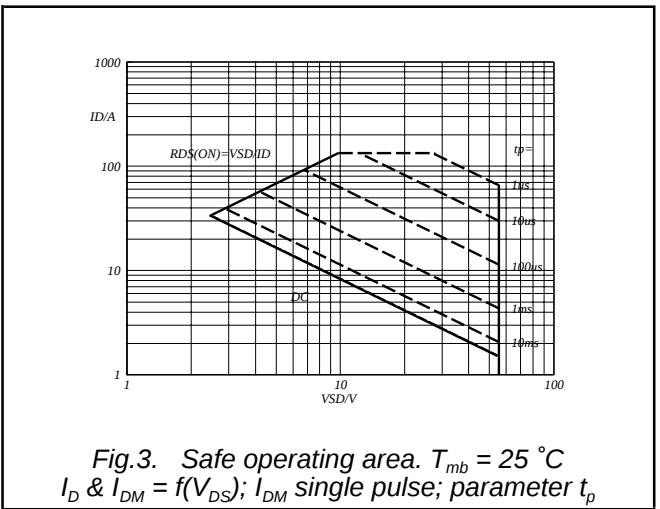
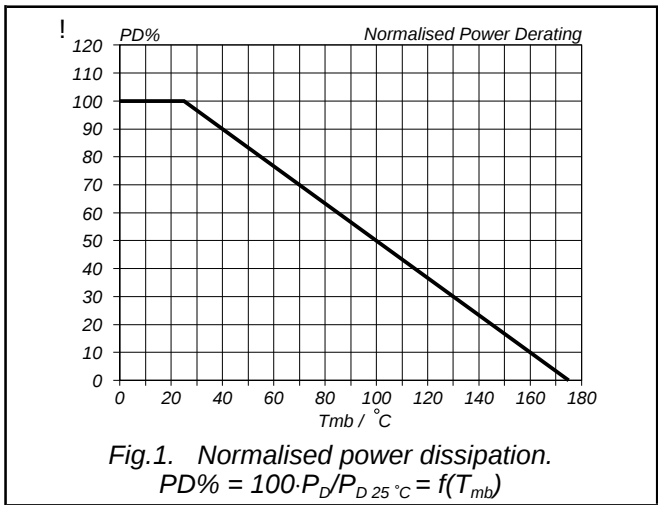
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	13	A
I_{DRM}	Pulsed reverse drain current		-	-	53	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}$; $V_{GS} = 0\text{ V}$ $I_F = 53\text{ A}$; $V_{GS} = 0\text{ V}$	- -	0.85 1.1	1.2 -	V V
t_{rr}	Reverse recovery time	$I_F = 53\text{ A}$; $-dI_F/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = -10\text{ V}$; $V_R = 30\text{ V}$	-	24	-	ns
Q_{rr}	Reverse recovery charge		-	0.026	-	μC

TrenchMOS™ transistor
Logic level FET

BUK95150-55A
BUK96150-55A

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}^1	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 8\text{ A}$; $V_{DD} \leq 25\text{ V}$; $V_{GS} = 5\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $T_{mb} = 25\text{ }^\circ\text{C}$	-	-	25	mJ

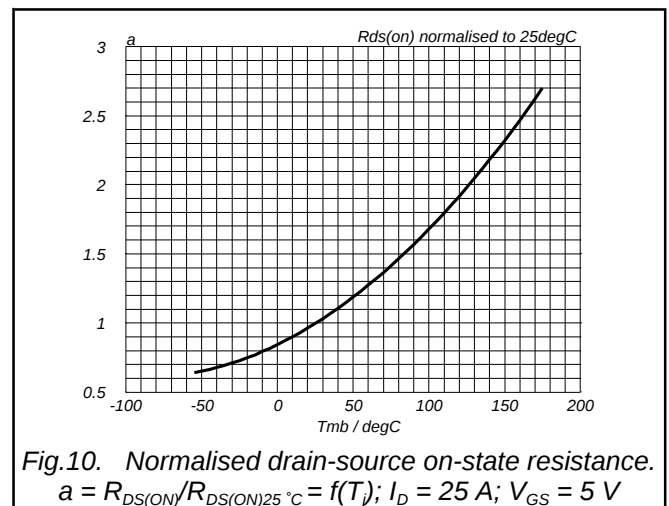
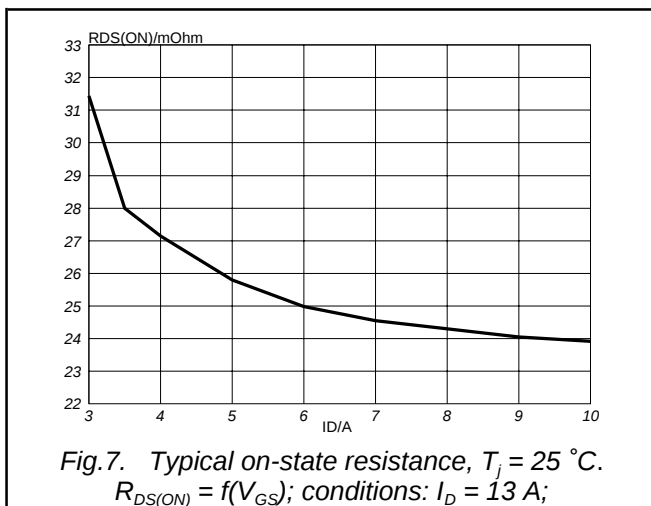
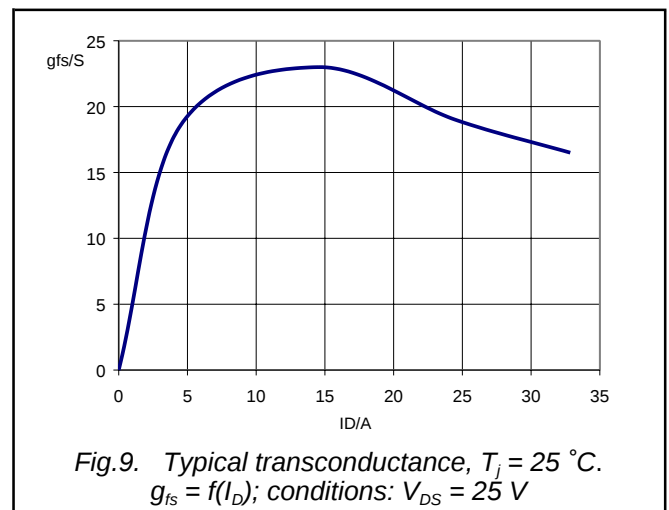
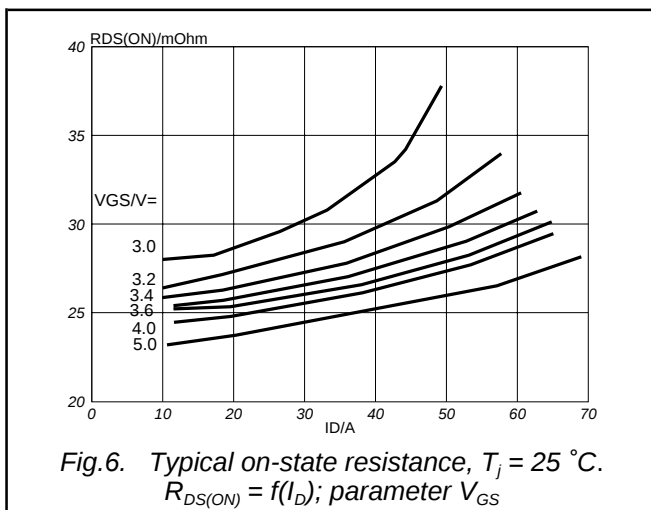
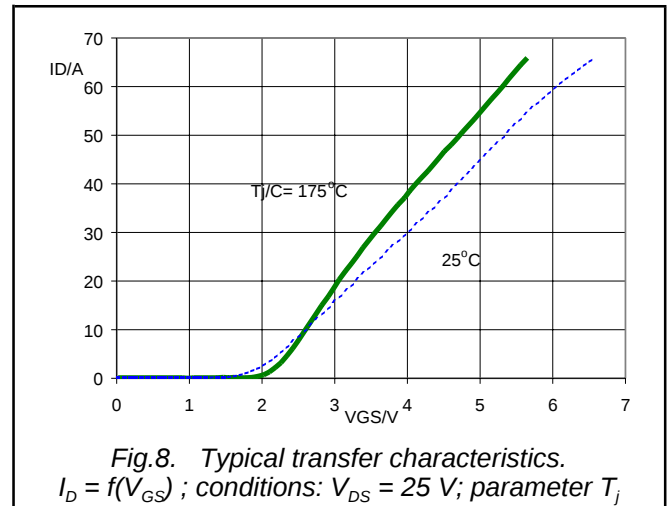
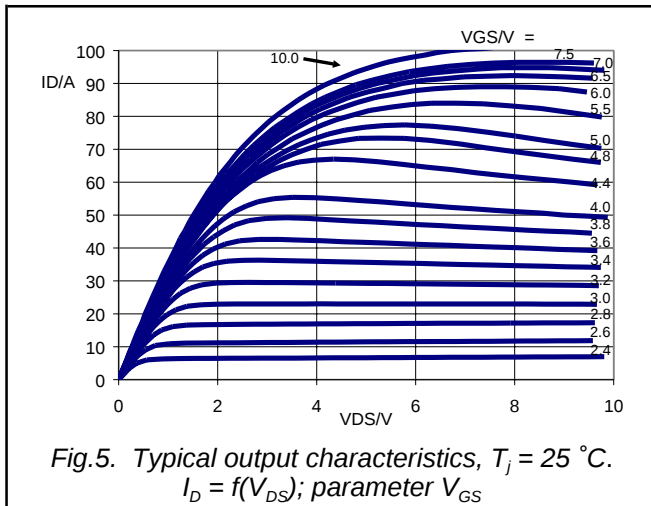


1 For maximum permissible repetitive avalanche current see fig.18.

TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A



TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A

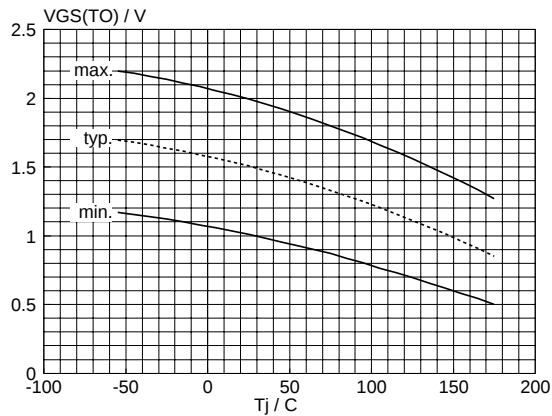


Fig.11. Gate threshold voltage.
 $V_{GS(TO)} = f(T_J)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

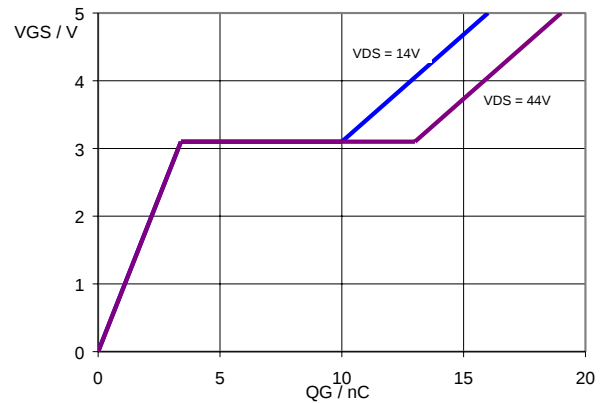


Fig.14. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 25 \text{ A}$; parameter V_{DS}

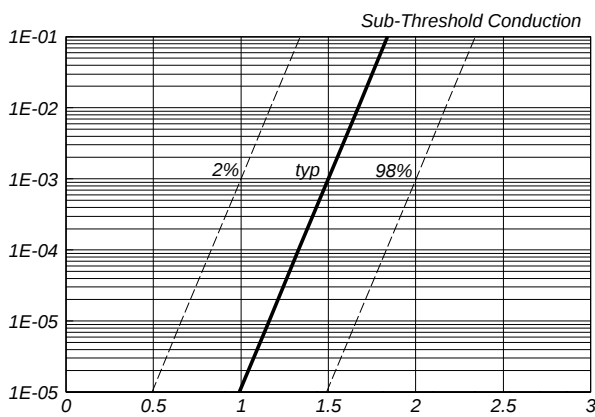


Fig.12. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

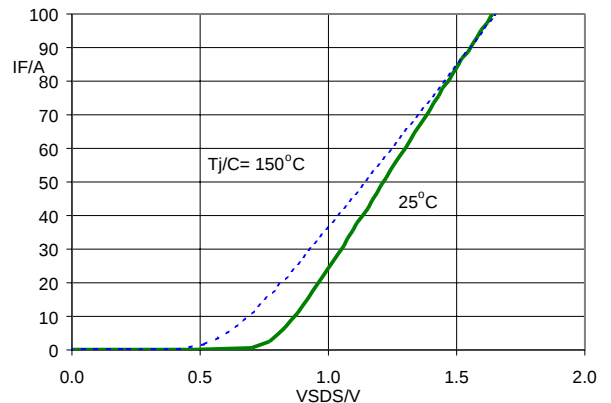


Fig.15. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0 \text{ V}$; parameter T_J

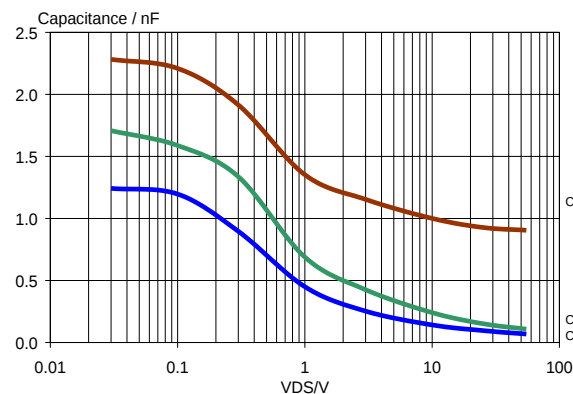


Fig.13. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

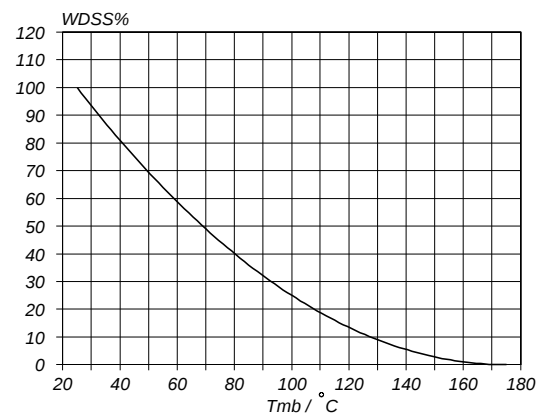
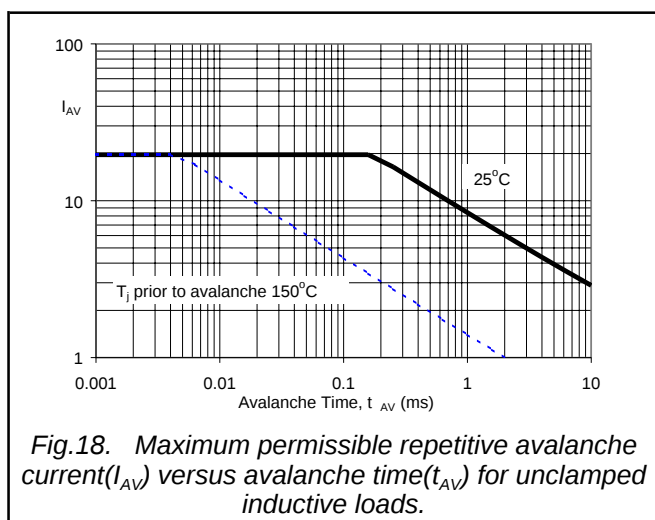
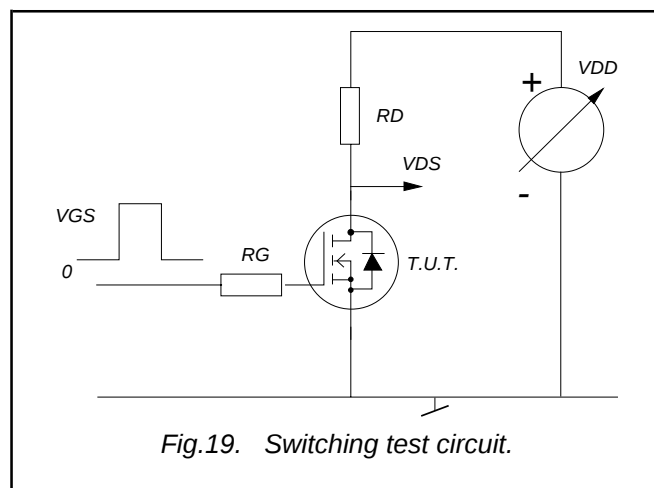
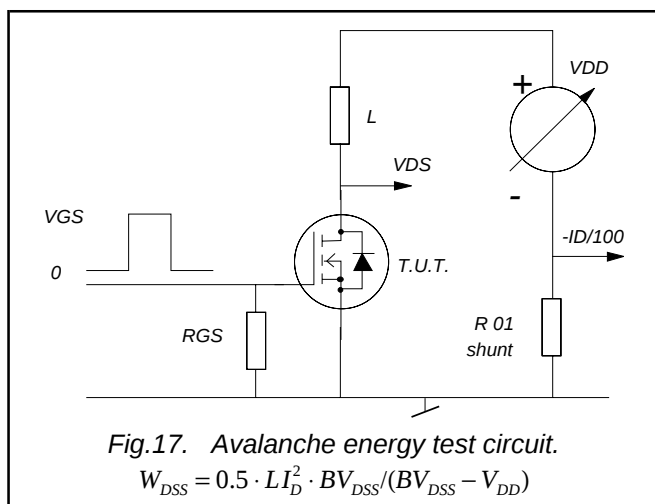


Fig.16. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75 \text{ A}$

TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A



TrenchMOS™ transistor
Logic level FET

BUK95150-55A
BUK96150-55A

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

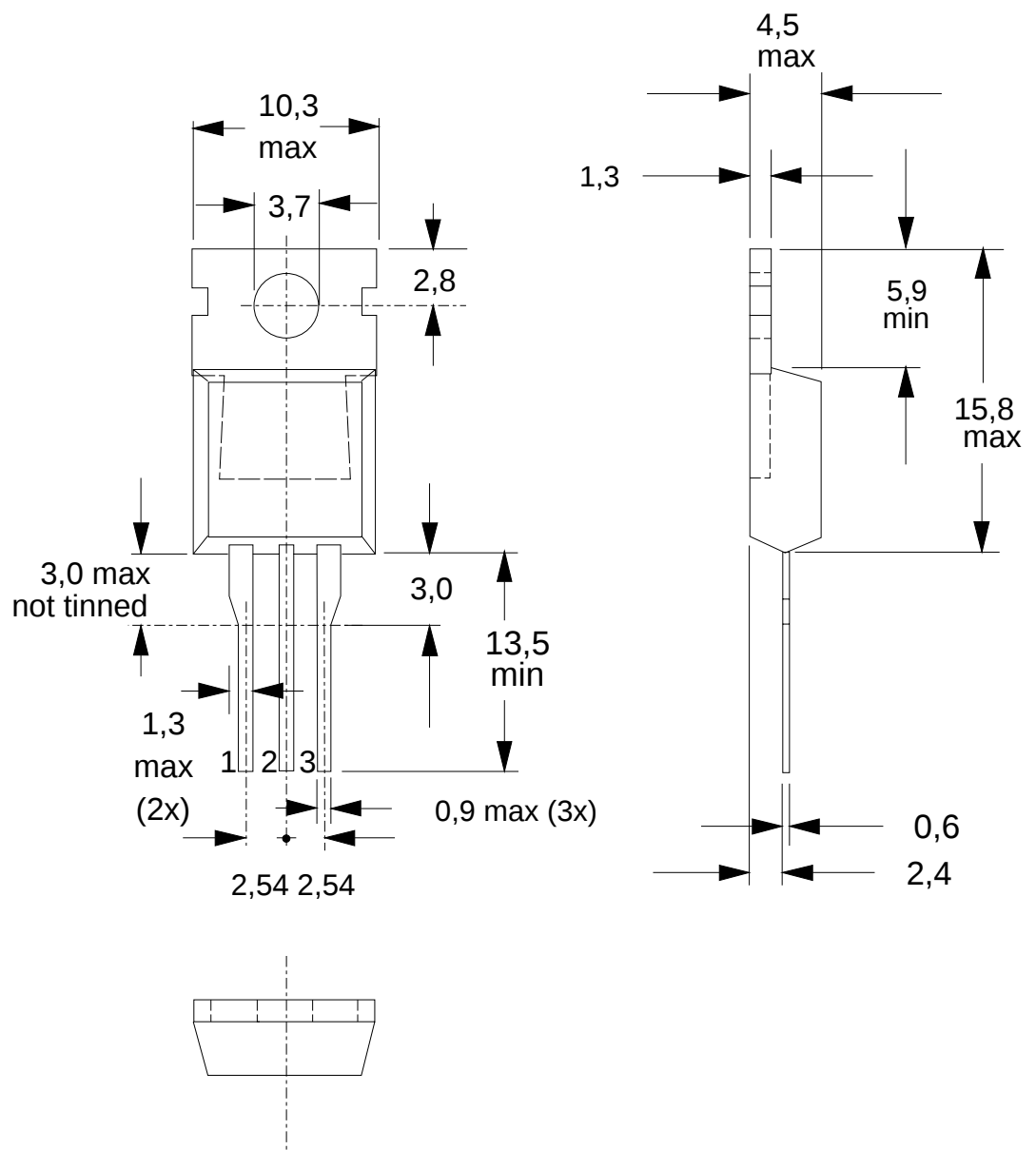


Fig.20. SOT78 (TO220AB); pin 2 connected to mounting base.

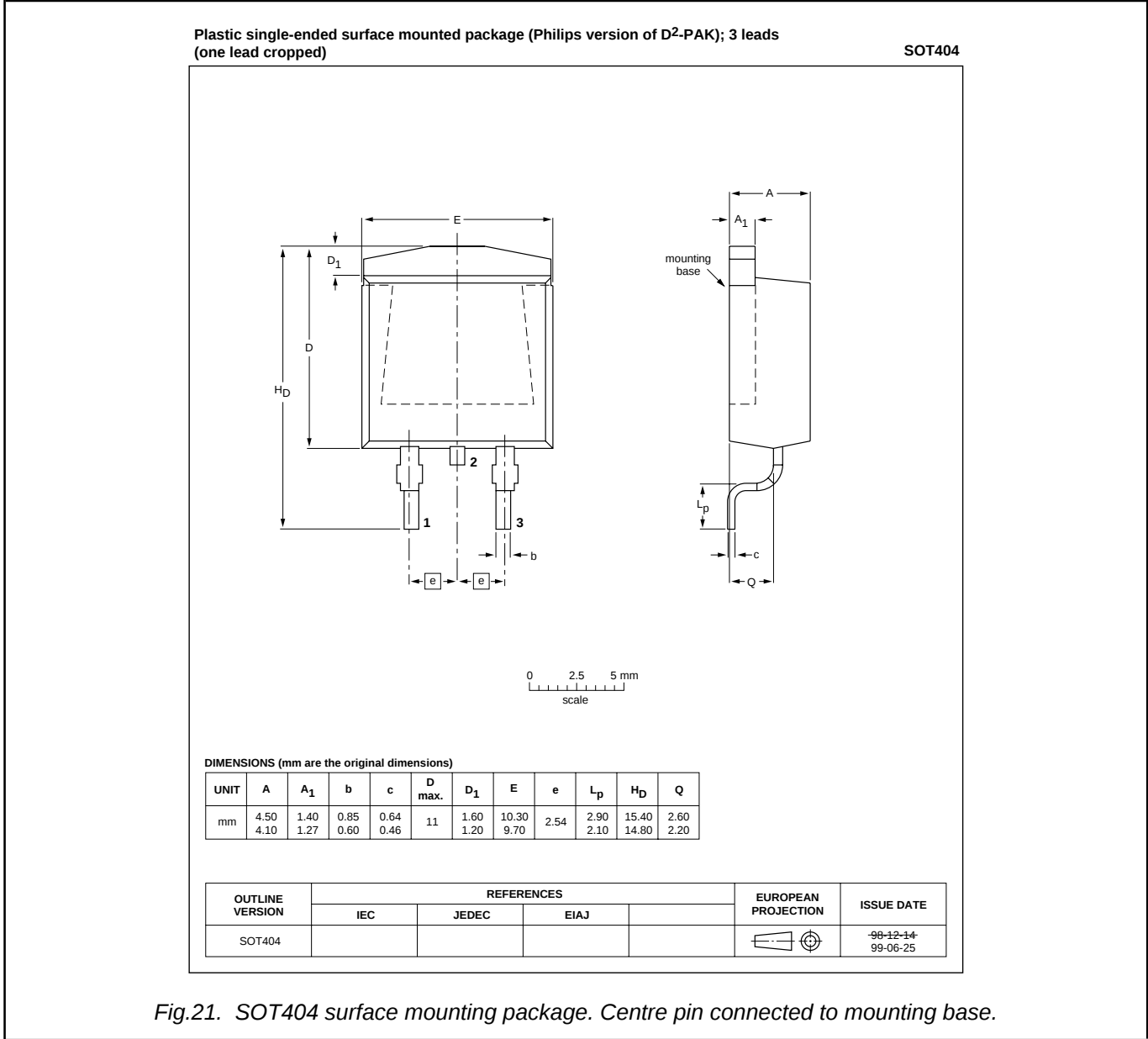
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor
Logic level FET

BUK95150-55A
BUK96150-55A

MECHANICAL DATA



Notes

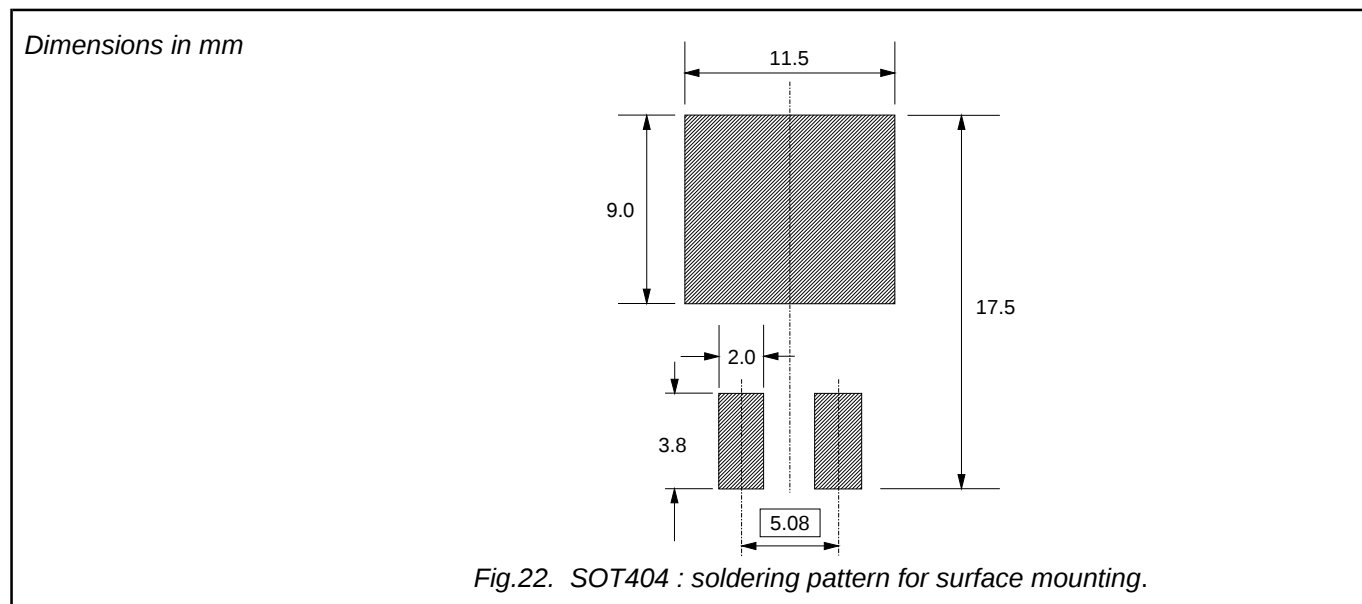
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

Logic level FET

BUK95150-55A
BUK96150-55A

MOUNTING INSTRUCTIONS



DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 2000	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.