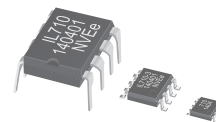
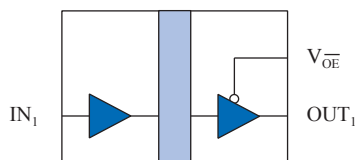


## High Speed Digital Isolators



### Functional Diagram



**IL710**

**Truth Table**

$V_I$	$V_{OE}$	$V_O$
L	L	L
H	L	H
L	H	Z
H	H	Z

### Features

- High Speed: 150 Mbps typical (IL710S)
- 2500  $V_{RMS}$  isolation voltage
- 600  $V_{RMS}$  working voltage per VDE V 0884-10
- 50 kV/ $\mu$ s typ.; 30 kV/ $\mu$ s min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- 1.2 mA/channel typical quiescent current
- 300 ps typical pulse width distortion (IL710S)
- 100 ps pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- 44000 year barrier life
- Excellent magnetic immunity
- VDE V 0884-10 certified; UL 1577 recognized
- 8-pin MSOP, SOIC, and PDIP packages

### Applications

- Digital Fieldbus
- RS-485 and RS-422
- Ground loop elimination
- Peripheral interfaces
- Serial communication
- Logic level shifting
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV $_{RMS}$  rated IEC 60601-1 medical applications

### Description

NVE's IL700 family of high-speed digital isolators are CMOS devices manufactured with NVE's patented\* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion as low as 300 ps (0.3 ns), achieving the best specifications of any isolator. Typical transient immunity of 50 kV/ $\mu$ s is unsurpassed. The IL710 is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The IL710 is available in 8-pin MSOP, SOIC, and PDIP packages.

The IL710S is the world's fastest isolator of its type, with a 150 Mbps typical data rate. Standard and S-Grade parts are specified over a temperature range of -40°C to +100°C. T-Grade parts are specified over a temperature range of -40°C to +125°C. The MSOP V-Series version offers full 2500  $V_{RMS}$  isolation in an ultraminiature package.

### Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Junction Temperature	$T_J$	-55		150	°C	
Ambient Operating Temperature <sup>(1)</sup> IL710T	$T_A$	-40		100 125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD1}+0.5$	V	
Input Voltage	$V_{OE}$	-0.5		$V_{DD2}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD2}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

### Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL710 and IL710S	$T_A$	-40		100	°C	
IL710T		-40		125	°C	
Junction Temperature IL710 and IL710S	$T_J$	-40		110	°C	
IL710T		-40		125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	3.0		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD1}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	µs	

### Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)						
MSOP		3.01			mm	
SOIC		4.04			mm	
PDIP		7.04			mm	
Total Barrier Thickness (internal)		0.012	0.013		mm	
Leakage Current <sup>(5)</sup>			0.2		µA	240 $V_{RMS}$ , 60 Hz
Barrier Resistance <sup>(5)</sup>	$R_{IO}$		$>10^{14}$		Ω	500 V
Barrier Capacitance <sup>(5)</sup>	$C_{IO}$		1.1		pF	f = 1 MHz
Comparative Tracking Index	CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	1000 1500			$V_{RMS}$ $V_{DC}$	At maximum operating temperature
Barrier Life			44000		Years	100°C, 1000 $V_{RMS}$ , 60% CL activation energy

### Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	MSOP SOIC PDIP	$\theta_{JA}$		80 60 60		°C/W	Soldered to double- sided board; free air
Junction–Case (Top) Thermal Resistance	MSOP SOIC PDIP	$\Psi_{JT}$		40 10 20		°C/W	
Power Dissipation	MSOP SOIC PDIP	$P_D$			500 675 800	mW	

## Safety and Approvals

**VDE V 0884-10** (VDE V 0884-11 pending; Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600  $V_{RMS}$  (848  $V_{PK}$ ); basic insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 2500  $V_{RMS}$
- Transient overvoltage ( $V_{IOTM}$ ) 4000  $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	$T_S$	180	°C
Safety rating power (180°C)	$P_S$	270	mW
Supply current safety rating (total of supplies)	$I_S$	54	mA

**IEC 61010-1** (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	MSOP (standard)	150 $V_{RMS}$
V-1	MSOP (high isolation voltage)	300 $V_{RMS}$
-2	PDIP	300 $V_{RMS}$
-3	SOIC	150 $V_{RMS}$

**UL 1577** (Component Recognition Program File Number E207481)

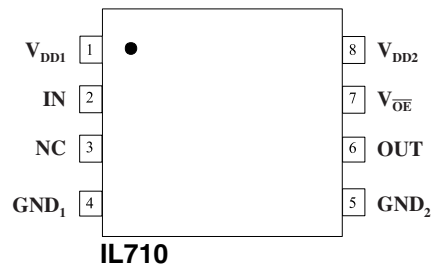
- Each part other than standard MSOP tested at 3000  $V_{RMS}$  (4240  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3530  $V_{PK}$ ) for 1 minute
- Standard MSOPs tested at 1200  $V_{RMS}$  (1768  $V_{PK}$ ) for 1 second; each lot sample tested at 1200  $V_{RMS}$  (1768  $V_{PK}$ ) for 1 minute

## Soldering Profile

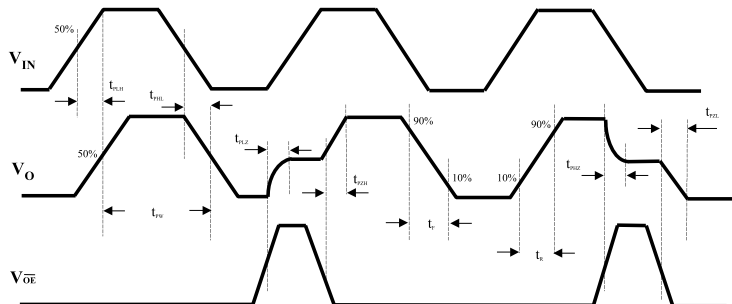
Per JEDEC J-STD-020C, MSL 1

## IL710 Pin Connections

1	$V_{DD1}$	Supply voltage
2	IN	Data In
3	NC	No internal connection
4	$GND_1$	Ground return for $V_{DD1}$
5	$GND_2$	Ground return for $V_{DD2}$
6	OUT	Data Out
7	$V_{OE}$	Output enable. Internally held low with 100 k $\Omega$
8	$V_{DD2}$	Supply voltage



## Timing Diagram



## Legend

$t_{PLH}$	Propagation Delay, Low to High
$t_{PHL}$	Propagation Delay, High to Low
$t_{PW}$	Minimum Pulse Width
$t_{PLZ}$	Propagation Delay, Low to High Impedance
$t_{PHZ}$	Propagation Delay, High Impedance to High
$t_{PHL}$	Propagation Delay, High to High Impedance
$t_{PZL}$	Propagation Delay, High Impedance to Low
$t_R$	Rise Time
$t_F$	Fall Time

3.3 Volt Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current	I <sub>DD1</sub>		8	10	μA	
Output Quiescent Supply Current	I <sub>DD2</sub>		1.2	1.75	mA	
Logic Input Current	I <sub>I</sub>	-10		10	μA	
Logic High Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> -0.1	V <sub>DD</sub>		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		0.8 x V <sub>DD</sub>	0.9 x V <sub>DD</sub>			I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>

Switching Specifications (V <sub>DD</sub> = 3.3 V)						
Maximum Data Rate IL710, IL710T, and IL710V IL710S		100 130	110 140		Mbps Mbps	C <sub>L</sub> = 15 pF C <sub>L</sub> = 15 pF
Pulse Width <sup>(7)</sup>	PW	10	7.5		ns	50% Points, V <sub>O</sub>
Propagation Delay Input to Output (High to Low)	t <sub>PHL</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)	t <sub>PLH</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t <sub>PHZ</sub>		3	5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t <sub>PLZ</sub>		3	5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t <sub>PZH</sub>		3	5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t <sub>PZL</sub>		3	5	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion <sup>(2)</sup> IL710, IL710T, and IL710V IL710S	PWD		2 1	3 3	ns	C <sub>L</sub> = 15 pF
Pulse Jitter <sup>(10)</sup>	t <sub>J</sub>		100		ps	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>	t <sub>PSK</sub>		4	6	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%–90%)	t <sub>R</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%–90%)	t <sub>F</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	CM <sub>H</sub>  ,  CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
Dynamic Power Consumption <sup>(6)</sup>			140	240	μA/Mbps	

Magnetic Field Immunity <sup>(8)</sup> (V <sub>DD2</sub> = 3V, 3V < V <sub>DD1</sub> < 5.5V)						
Power Frequency Magnetic Immunity	H <sub>PF</sub>	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>	1800	2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	K <sub>X</sub>		2.5			

5 Volt Electrical Specifications ( $T_{min}$ to $T_{max}$ unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Supply Current	$I_{DD1}$		10	15	$\mu A$	
Output Quiescent Supply Current	$I_{DD2}$		1.8	2.5	mA	
Logic Input Current	$I_I$	-10		10	$\mu A$	
Logic High Output Voltage	$V_{OH}$	$V_{DD}-0.1$	$V_{DD}$		V	$I_O = -20 \mu A, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{ mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu A, V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{ mA}, V_I = V_{IL}$

Switching Specifications ( $V_{DD} = 5 \text{ V}$ )						
Maximum Data Rate IL710, IL710T, and IL710V IL710S		100 130	110 150		Mbps Mbps	$C_L = 15 \text{ pF}$ $C_L = 15 \text{ pF}$
Pulse Width <sup>(7)</sup>	PW	10	7.5		ns	50% Points, $V_O$
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	$t_{PHZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	$t_{PLZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	$t_{PZH}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	$t_{PZL}$		3	5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion <sup>(2)</sup> IL710, IL710T, and IL710V IL710S	PWD		2 0.3	3 3	ns	$C_L = 15 \text{ pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10%–90%)	$t_R$		1	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10%–90%)	$t_F$		1	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	30	50		kV/ $\mu s$	$V_{CM} = 1500 \text{ V}_{DC}$ $t_{TRANSIENT} = 25 \text{ ns}$
Dynamic Power Consumption <sup>(6)</sup>			200	340	$\mu A/Mbps$	

Magnetic Field Immunity <sup>(8)</sup> ( $V_{DD2} = 5 \text{ V}, 3 \text{ V} < V_{DD1} < 5.5 \text{ V}$ )						
Power Frequency Magnetic Immunity	$H_{PF}$	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	$H_{PM}$	4000	4500		A/m	$t_b = 8 \mu s$
Damped Oscillatory Magnetic Field	$H_{OSC}$	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	$K_X$		2.5			

## Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD is equal to PWD divided by pulse width.
3.  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at 25°C.
4.  $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_O < 0.8 \text{ V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
9. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 7).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

## Application Information

### Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial

Methods EN55022, EN55014

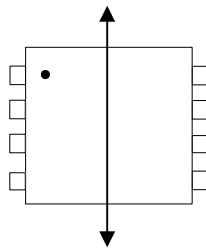
EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

### Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND<sub>1</sub> and GND<sub>2</sub> are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V<sub>DD</sub> pins.

### Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

### Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

$$\text{PWD\%} = \frac{3 \text{ ns}}{80 \text{ ns}} \times 100\% = 3.75\%$$

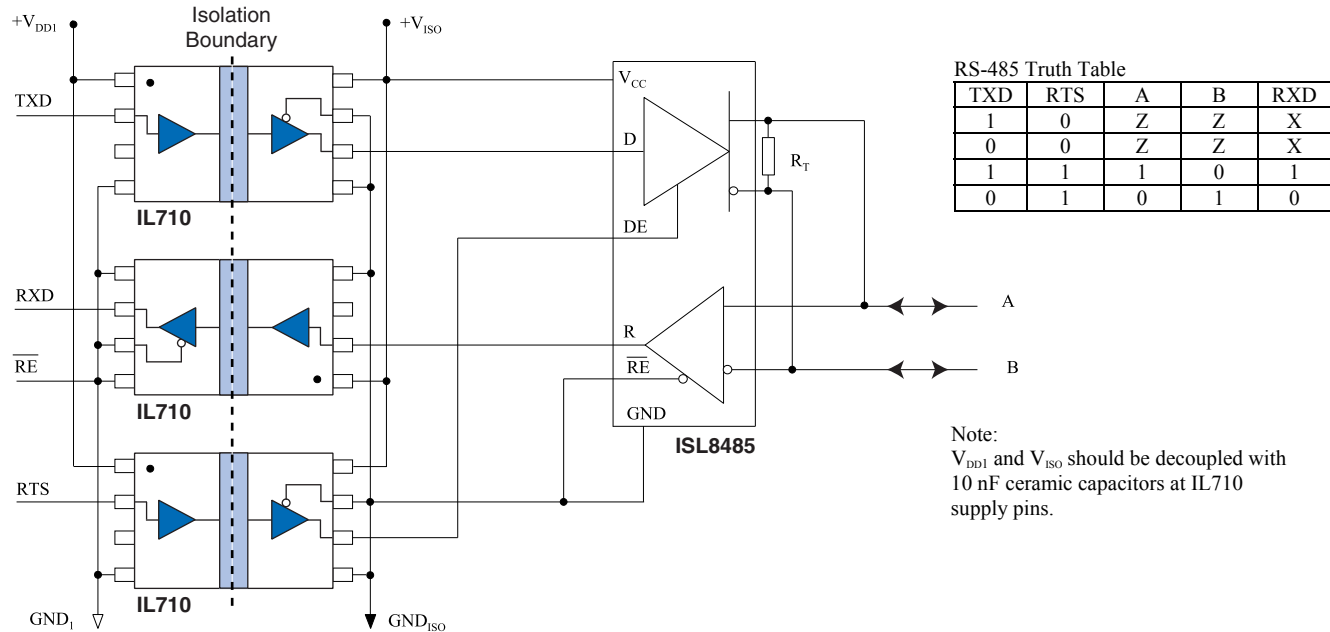
This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is only 3 ns, which is **ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

## Application Diagrams

### Isolated PROFIBUS / RS-485

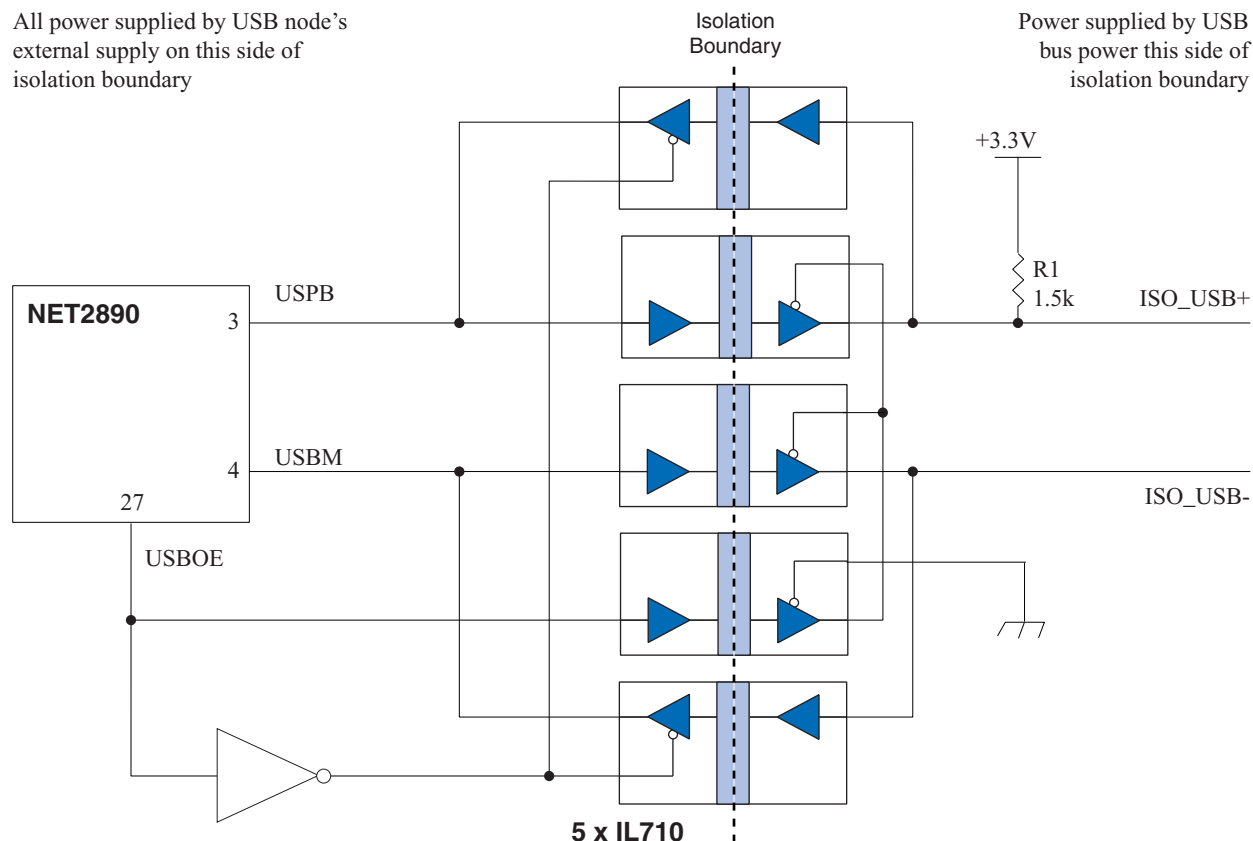
NVE offers a unique line of single-chip isolated PROFIBUS/RS-485 transceivers, but as this circuit illustrates, IL710 isolators can also be used as part of multi-chip designs using non-isolated PROFIBUS transceivers:



## Isolated USB

In this circuit, power is supplied by USB bus power on one side of the isolation barrier, and the USB node's external supply on the other side of the barrier. IL700 Isolators are specified with just 3 ns worst-case pulse width distortion:

All power supplied by USB node's external supply on this side of isolation boundary



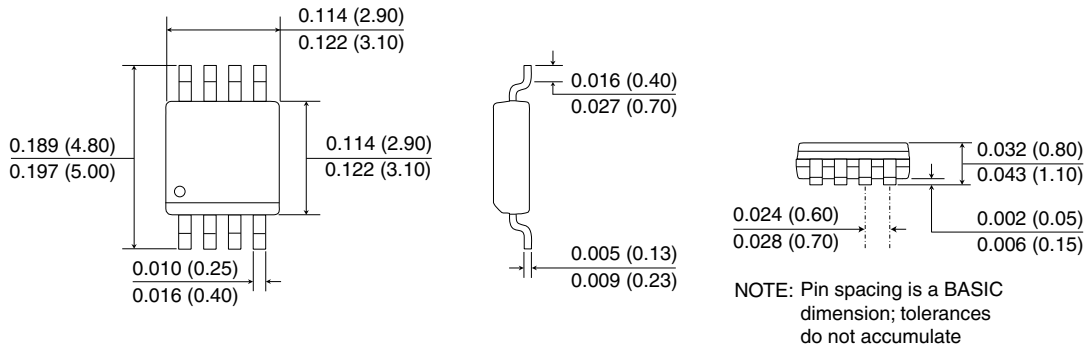
Power supplied by USB bus power this side of isolation boundary



**Package Drawings**

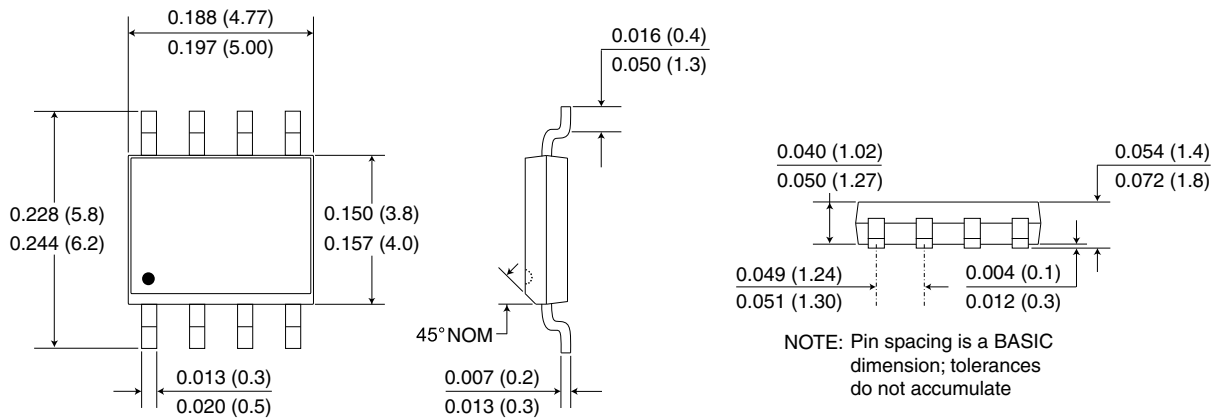
**8-pin MSOP (-1 suffix)**

Dimensions in inches (mm); scale = approx. 5X



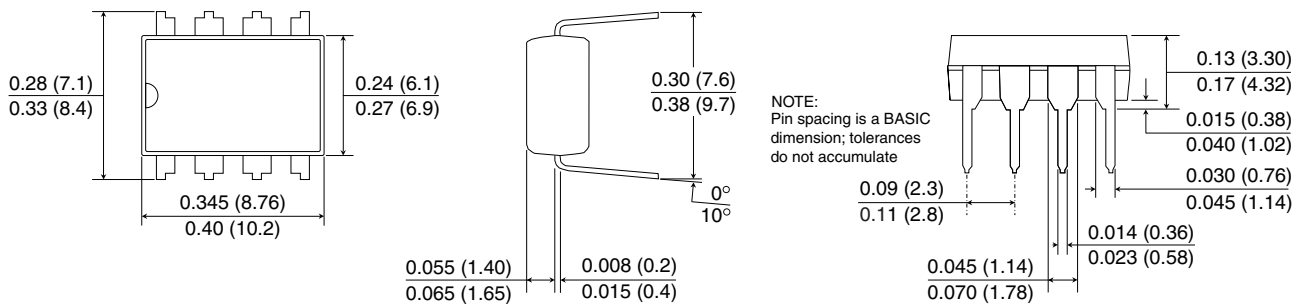
**8-pin SOIC Package (-3 suffix)**

Dimensions in inches (mm); scale = approx. 5X



**8-pin PDIP (-2 suffix)**

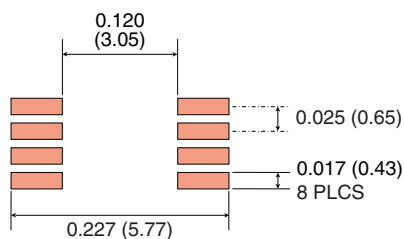
Dimensions in inches (mm); scale = approx. 2.5X



## Recommended Pad Layouts

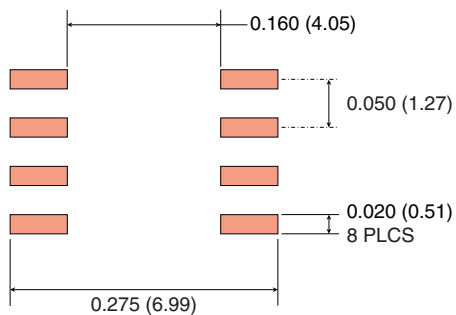
### 8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



### 8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



## Ordering Information and Valid Part Numbers

IL 710 T - 3 E TR13

- ➔ **Bulk Packaging**  
Blank = Tube  
TR7 = 7" Tape and Reel  
TR13 = 13" Tape and Reel
- ➔ **Package**  
Blank = 80/20 Tin/Lead Plating  
E = RoHS Compliant
- ➔ **Package Type**  
-1 = MSOP  
-2 = PDIP  
-3 = 0.15" 8-pin SOIC
- ➔ **Grade**  
Blank = Standard  
S = High Speed  
T = High Temperature  
V = High Isolation MSOP
- ➔ **Base Part Number**  
710 = Single Channel
- ➔ **Product Family**  
IL = Isolators

### Valid Part Numbers

IL710-1E  
IL710S-1E  
IL710T-1E  
IL710V-1E

IL710-2  
IL710T-2  
IL710-2E  
IL710T-2E

IL710-3  
IL710S-3  
IL710T-3  
IL710-3E  
IL710S-3E  
IL710T-3E

All MSOP and SOIC  
parts are available on  
tape and reel.

## ISB-DS-001-IL710-AE November 2016

### Change

- Updated VDE approvals to VDE V 0884-10

## ISB-DS-001-IL710-AD

### Change

- Added MSOP V-Series version (2500 VRMS isolation).

## ISB-DS-001-IL710-AC

### Changes

- Added product illustrations to first page.
- Revised and added details to thermal specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).

## ISB-DS-001-IL710-AB

### Change

- IEC 60747-5-5 (VDE 0884) certification.

## ISB-DS-001-IL710-AA

### Changes

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

## ISB-DS-001-IL710-Z

### Changes

- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added high voltage endurance specification.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

## ISB-DS-001-IL710-Y

### Changes

- Detailed isolation and barrier specifications.
- Cosmetic changes.

## ISB-DS-001-IL710-X

### Changes

- Tightened typ. output quiescent supply spec. from 1.7 mA to 1.5 mA.
- T-Series quiescent supply specs. tightened to be the same as other grades.

## ISB-DS-001-IL710-W

### Changes

- Update terms and conditions.

## ISB-DS-001-IL710-V

### Change

- Additional changes to MSOP pin spacing on package drawing.

## ISB-DS-001-IL710-U

### Change

- Changed MSOP pin spacing on package drawing.

## ISB-DS-001-IL710-T

### Change

- Added typical jitter specification at 5V.

## ISB-DS-001-IL710-S

### Change

- Added EMC details.

## ISB-DS-001-IL710-R

### Change

- IEC 61010 approval for MSOP version.

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