SLUS419C − AUGUST 1999 − REVISED NOVEMBER 2001

BiCMOS PFC/PWM COMBINATION CONTROLLER

FEATURES

- **Combines PFC and Downstream Converter Controls**
- **Controls Boost Preregulator to Near-Unity Power Factor**
- **Accurate Power Limiting**
- **Improved Feedforward Line Regulation**
- **Peak Current-Mode Control in Second Stage**
- **Programmable Oscillator**
- **Leading-Edge/Trailing-Edge Modulation for Reduced Output Ripple**
- **Low Start-up Supply Current**
- **Synchronized Second Stage Start-Up, with Programmable Soft-start**
- **Programmable Second Stage Shutdown**

DESCRIPTION

The UCC2850x family provides all of the control functions necessary for an active power-factor-corrected preregulator and a second-stage dc-to- dc converter. The controller achieves near-unity power factor by shaping the ac input line current waveform to correspond to the ac input-line voltage using average current-mode control. The dc-to-dc converter uses peak current-mode control to perform the step-down power conversion.

The PFC stage is leading-edge modulated while the second stage is trailing-edge synchronized to allow for minimum overlap between the boost and PWM switches. This reduces ripple current in the bulk-output capacitor.In order to operate with over three-to-one range of input-line voltages, a line feedforward (V_{FF}) is used to keep input power constant with varying input voltage. Generation of V_{FF} is accomplished using I_{AC} in conjunction with an external single-pole filter. This not only reduces external parts count, but also avoids the use of high-voltage components, offering a lower-cost solution. The multiplier then divides the line current by the square of V_{FF}.

The UCC2850x PFC section incorporates a low offset-voltage amplifier with 7.5-V reference, a highly-linear multiplier capable of a wide current range, a high-bandwidth, low offset-current amplifier, with a novel noise-attenuation configuration, PWM comparator and latch, and a high-current output driver. Additional PFC features include over-voltage protection, zero-power detection to turn off the output when VAOUT is below 0.33 V and peak current and power limiting.

The dc-to-dc section relies on an error signal generated on the secondary-side and processes it by performing peak current mode control. The dc-to-dc section also features current limiting, a controlled soft-start, preset operating range with selectable options, and 50% maximum duty cycle.

The UCC28500 and UCC28502 have a wide UVLO threshold (16.5 V/10 V) for bootstrap bias supply operation. The UCC28501 and UCC28503 are designed with a narrow UVLO range (10.5 V/10 V) more suitable for fixed bias operation. The UCC28500 and UCC28501 have a narrow UVLO threshold for PWM stage (to allow operation down to 75% of nominal bulk voltage), while the UCC28502 and UCC38503 are configured for a much wider operation range for the PWM stage (down to 50% of bulk nominal voltage).

Available in 20-pin N and DW packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply Voltage VCC . . . . . 18 V
Gate Drive Current
  Continuous . . . . . 0.2 A
  Pulsed . . . . . 1.2 A
Input Voltage
  ISENSE1, ISENSE2, MOUT, VSENSE, OVP/ENBL . . . . . 10 V
  CAI, MOUT, CT . . . . . 8 V
  PKLMT, VERR . . . . . 5 V
Input Current
  RSET, RT, IAC, PKLMT, ENA . . . . . 10 mA
  VCC (no switching) . . . . . 20 mA
Maximum Negative Voltage GT1, GT2, PKLMT, MOUT . . . . . –0.5 V
Power Dissipation . . . . . 1 W
Storage temperature T_{stg} . . . . . −65°C to 150°C
Junction temperature T_J . . . . . −55°C to 125°C
Lead temperature (soldering, 10 sec) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

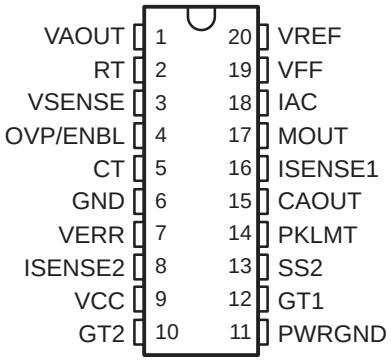
‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

AVAILABLE OPTIONS

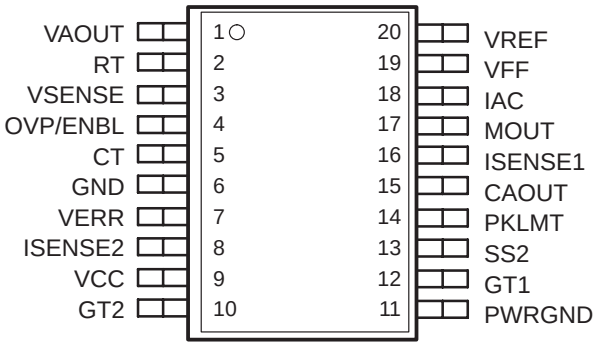
T_J	PFC THRESHOLD		PACKAGED DEVICES	
	UVLO TURN−ON THRESHOLD (V)	UVLO2 HYSTERESIS (V)	PLASTIC DIP (N)	SMALL OUTLINE (DW)
–40°C to 85°C	16	1.2	UCC28500N	UCC28500DW
	10.5	1.2	UCC28501N	UCC28501DW
	16	3.0	UCC28502N	UCC28502DW
	10.5	3.0	UCC28503N	UCC28503DW
0°C to 70°C	16	1.2	UCC38500N	UCC38500DW
	10.5	1.2	UCC38501N	UCC38501DW
	16	3.0	UCC38502N	UCC38502DW
	10.5	3.0	UCC38503N	UCC38503DW

The DW package is available taped and reeled. Add TR suffix to device type (e.g. UCC38500DWTR) to order quantities of 2000 devices per reel.

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



electrical characteristics T_A = 0°C to 70°C for the UCC3850X, –40°C to 85°C for the UCC2850X, $T_A = T_J$, VCC = 12 V, RT = 22 kΩ, CT = 330 pF (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current, off	VCC turn-on threshold –300 mV		150	300	µA
Supply current, on	VCC = 12 V (no load on GT1 or GT2)		4	6	mA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC turn-on threshold (UCCx8500/502)		15.4	16	16.6	V
UVLO hysteresis (UCCx8500/502)		5.8	6.3		V
Shunt voltage (UCCx8500/502)	I_{VCC} = 10 mA	15.4	16.2	17.0	V
VCC turn-on threshold (UCCx8501/503)		9.7	10.2	10.8	V
VCC turn-off threshold		9.4	9.7		V
UVLO hysteresis (UCCx8501/503)		0.3	0.5		V

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage	0°C ≤ T_A ≤ 70°C	7.387	7.500	7.613	V
	–40°C ≤ T_A ≤ 85°C	7.35	7.50	7.65	V
V_{SENSE} bias current			50	200	nA
Open loop gain	VAOUT = 2 V to 5 V	50	90		dB
High-level output voltage	I_{LOAD} = –150 µA	5.3	5.5	5.6	V
Low-level output voltage	I_{LOAD} = 150 µA	0.00	0.05	0.15	V

PFC overvoltage protection and enable

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over voltage reference		VREF + 0.480	VREF + 0.500	VREF + 0.520	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2	0.3	V

current amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input offset voltage	V_{CM} = 0 V, V_{CAOUT} = 3 V	–6	0	6	mV
Input bias current	V_{CM} = 0 V, V_{CAOUT} = 3 V		−50	−100	nA
Input offset current	V_{CM} = 0 V, V_{CAOUT} = 3 V		25	100	nA
Open loop gain	V_{CM} = 0 V, V_{CAOUT} = 2 V to 5 V	90			dB
Common−mode rejection ratio	V_{CM} = 0 V to 1.5 V, V_{CAOUT} = 3 V	90			dB
High-level output voltage	I_{LOAD} = –120 µA	5.6	7.0	7.5	V
Low-level output voltage	I_{LOAD} = 1 mA	0.1	0.2	0.5	V
Gain bandwidth product	See Note 1		2.5		MHz

NOTES: 1. Ensured by design. Not production tested.
2. See Figure 6 for reference variation.
3. See Figure 5 for reference variation for VCC < 10.8 V.

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voltage reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage	T_A = 0°C to 70°C	7.387	7.500	7.613	V
	T_A = –40°C to 85°C	7.35	7.50	7.65	V
Load regulation	I_{REF} = −1 mA to −2 mA, See Note 2	0		10	mV
Line regulation	VCC = 10.8 V to 15 V, See Note 3	0		10	mV
Short circuit current	VREF = 0V	−20	–25	−50	mA

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency, initial accuracy	T_A = 25°C	85	100	115	kHz
Frequency, voltage stability	VCC = 10.8 V to 15 V	−1%		1%	
Frequency, total variation	Line, Temp	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V

peak current limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PKLMT reference voltage		–15	0	15	mV
PKLMT propagation delay		150	300	500	ns

multiplier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{MOUT}, high-line low-power output current	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 1.25 V, 0°C ≤ T_A ≤ 85°C	0	–6	−20	µA
I_{MOUT}, high-line low-power output current	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 1.25 V, –40°C ≤ T_A ≤ 85°C	0	–6	−23	
I_{MOUT}, high-line high-power output current	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 5 V	−70	–90	−105	
I_{MOUT}, low-line low-power output current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 1.25 V	−10	–19	−50	
I_{MOUT}, low-line high-power output current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 5 V	−268	–300	−345	
I_{MOUT}, IAC-limited output current	I_{AC} = 150 µA, VFF = 1.3 V, VAOUT = 5 V	−250	–300	−400	
Gain constant (K)	I_{AC} = 300 µA, VFF = 2.8 V, VAOUT = 2.5 V	0.5	1	1.5	1/V
I_{MOUT}, zero current	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 0.25 V		0	–2	
	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 0.25 V		0	–2	µA
	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 0.5 V, 0°C ≤ T_A ≤ 85°C		0	–3	µA
	I_{AC} = 500 µA, VFF = 4.7 V, VAOUT = 0.5 V, −40°C ≤ T_A ≤ 85°C		0	–3.5	µA
Power limit ($I_{MOUT} \times V_{FF}$)	I_{AC} = 150 µA, VFF = 1.4 V, VAOUT = 5 V	−375	–420	−485	µW

zero power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero power comparator threshold	Measured on VAOUT	0.175	0.330	0.500	V

NOTES: 1. Ensured by design. Not production tested.
2. See Figure 6 for reference variation.
3. See Figure 5 for reference variation for VCC < 10.8 V .

electrical characteristics T_A = 0°C to 70°C for the UCC3850X, –40°C to 85°C for the UCC2850X, $T_A = T_J$, VCC = 12 V, RT = 22 kΩ, CT = 330 pF (unless otherwise noted)

PFC gate driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GT1 pull up resistance	I_{OUT} from −100 mA to –200 mA		5	12	Ω
GT1 pull down resistance	I_{OUT} = 100 mA		2	10	Ω
GT1 output rise time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω V_{GT1} from 0.7 V to 9.0 V		25	50	ns
GT1 output fall time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω V_{GT1} from 9.0 V to 0.7 V		10	50	ns
Maximum duty cycle		93%	95%	100%	
Minimum controlled duty cycle	f = 100 kHZ			2%	

second stage undervoltage lockout (UVLO2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM turn-on reference (UCCx8500/501)		6.30	6.75	7.30	V
Hysteresis (UCCx8500/501)		0.96	1.20	1.44	V
PWM turn−on reference (UCCx8502/503)		6.30	6.75	7.30	V
Hysteresis (UCCx8502/503)		2.4	3	3.6	V

second stage soft-start

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SS2 charge current		–7.3	–10	–12.5	µA
Input voltage (VERR)	I_{VERR} = 2 mA,UVLO = Low			300	mV
SS2 discharge current	ENBL = High, UVLO = Low, SS2 = 2.5 V	3		10	mA

second stage duty cycle clamp

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum duty cycle		44%		50%	

second stage pulse-by-pulse current sense

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current sense comparator threshold	VERR = 2.5 V measured on ISENSE2	0.94	1.05	1.15	V

second stage overcurrent limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak current comparator threshold		1.15	1.30	1.45	V
Input bias current			50		nA

second stage gate driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GT2 pull up resistance	I_{OUT} from −100 mA to –200 mA		5	12	Ω
GT2 pull down resistance	I_{OUT} = 100 mA		3	10	Ω
GT2 output rise time	C_{LOAD} = 1 nF,R_{LOAD} = 10 Ω V_{GT2} from 0.7 V to 9.0 V		25	50	ns
GT2 output fall time	C_{LOAD} = 1 nF,R_{LOAD} = 10 Ω V_{GT2} from 9.0 V to 0.7 V		25	50	ns

NOTES: 1. Ensured by design. Not production tested.
2. See Figure 6 for reference variation.
3. See Figure 5 for reference variation for VCC < 10.8 V .

pin assignments

CAOUT: (current amplifier output) This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse width modulator (PWM) to force the correct duty cycle. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary.

CT: (oscillator timing capacitor) A capacitor from CT to GND sets the oscillator frequency according to:

$$f = \frac{0.725}{\left(R_T \times C_T\right)}$$

GND: (ground) All voltages measured with respect to ground. VCC and VREF should be bypassed directly to GND with a 0.1-μF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND should be as short and direct as possible.

GT1: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on GT1. Use a series gate resistor of at least 10.5 Ω to prevent interaction between the gate impedance and the GT1 output driver that might cause the GT1 to overshoot excessively. Some overshoot of the GT1 output is always expected when driving a capacitive load. Refer to Figure 4 for gate drive resistor selections.

GT2: (gate drive) Same as output GT1 for the second stage output drive. Limited to 50% maximum duty cycle.

IAC: (input ac current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to MOUT, so this is the only multiplier input which should be used for sensing instantaneous line voltage. Recommended maximum I_{AC} is 500 μA.

ISENSE1: (current sense) This is the non-inverting input to the current amplifier. This input and the inverting input MOUT remain functional down to and below GND.

ISENSE2: (current sense) A resistor from the source of the lower FET to ground generates the input signal for the peak limit control of the second stage. The oscillator ramp can also be summed into this pin, for slope compensation.

MOUT: (multiplier output and current sense amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier to reject ground noise. Multiplier output current is given by:

$$I_{MOUT} = \frac{\left(V_{VAOUT} - 1.0\right) \times I_{IAC}}{K \times \left(V_{VFF}\right)^2}$$

Connect current loop compensation components between MOUT and CAOUT.

OVP/ENBL: (over-voltage/enable) A window comparator input which disables the PFC output driver if the boost output is 6.67% above nominal or disables both the PFC and second stage output drivers and reset SS2 if pulled below 1.9 V. This input is also used to determine the active range of the second stage PWM.

PKLMT: (PFC peak current limit) The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level-shift this signal to a voltage corresponding to the desired overcurrent threshold across the current sense resistor.

PWRGND: Ground for totem pole output drivers.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended. Nominal voltage on this pin is 3 V.

pin assignments (continued)

SS2: (soft-start for PWM) SS2 is at ground for either enable low or OVP/ENBL below the UVLO2 threshold conditions. When enabled, SS2 charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a disable command or a UVLO2 dropout, SS2 quickly discharges to disable the PWM.

VAOUT: (voltage amplifier output) This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20 mA between 12 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

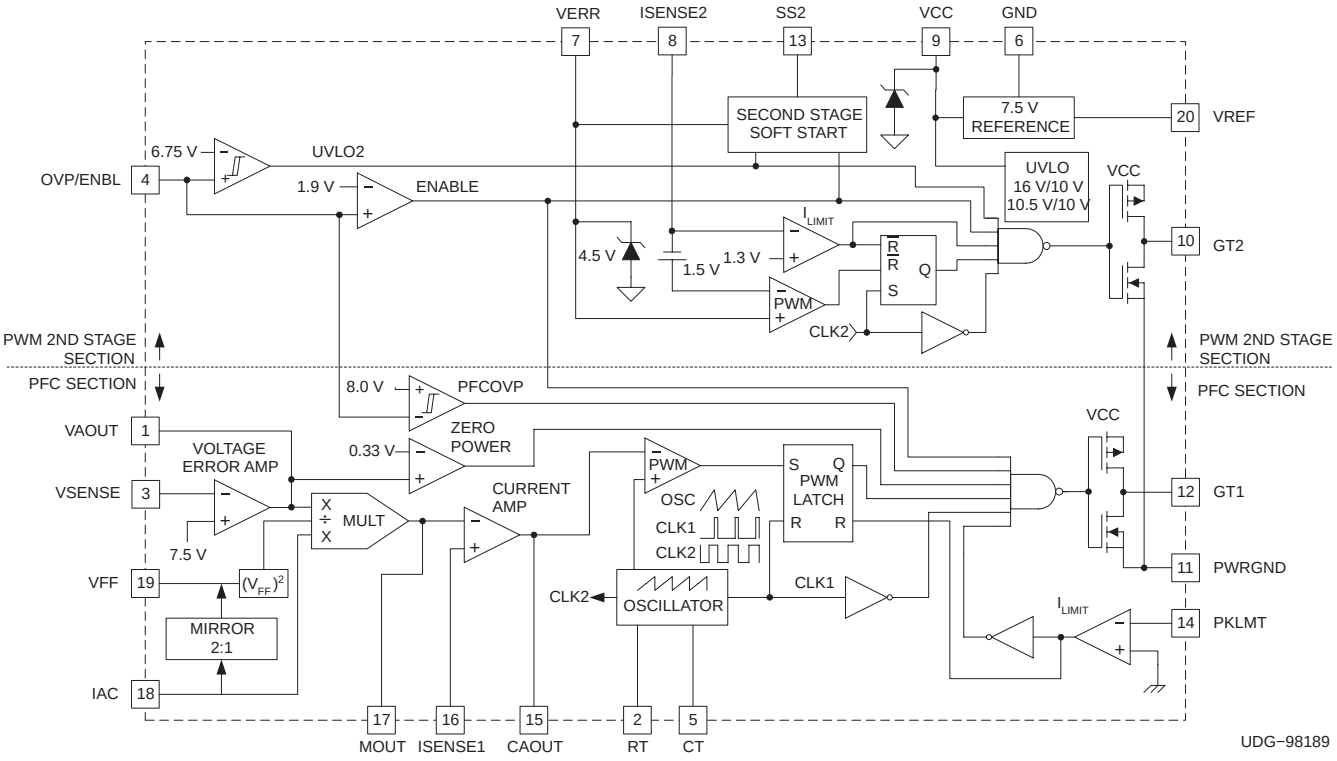
VERR: (voltage amp error signal for the second stage) The error signal is generated by an external amplifier which drives this pin. This pin has an internal 4.5-V voltage clamp that limits GT2 to less than 50% duty cycle to ensure transformer reset in the typical application.

VFF: (RMS feed forward signal) VFF signal is generated at this pin by mirroring one-half of I_{AC} into a single pole external filter. At low line, the VFF voltage should be 1.4 V.

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 10 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when VCC is below the UVLO threshold. Bypass VREF to GND with a 0.1-µF or larger ceramic capacitor for best stability.

block diagram



TYPICAL CHARACTERISTICS

MULTIPLIER OUTPUT CURRENT vs. VOLTAGE ERROR AMPLIFIER OUTPUT

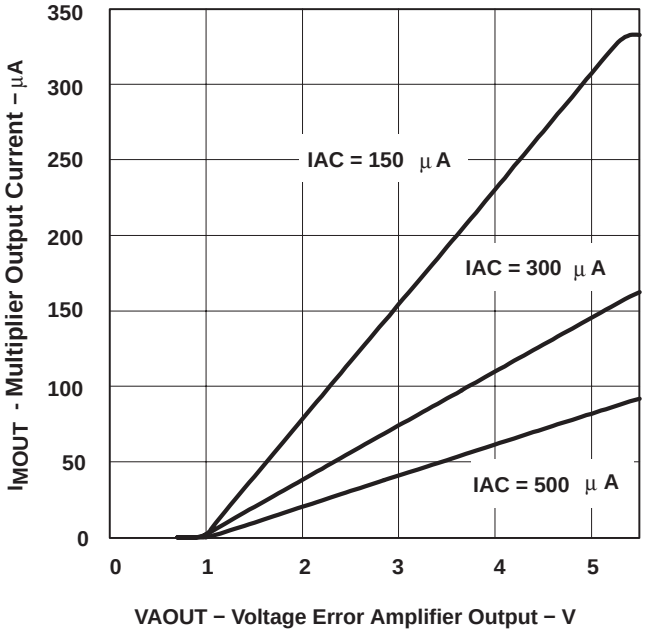


Figure 1

MULTIPLIER GAIN vs. VOLTAGE ERROR AMPLIFIER OUTPUT

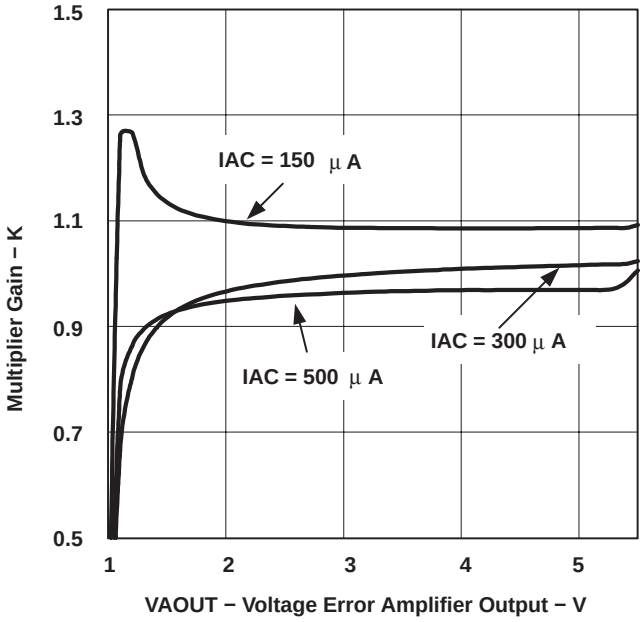


Figure 2

MULTIPLIER CONSTANT POWER PERFORMANCE

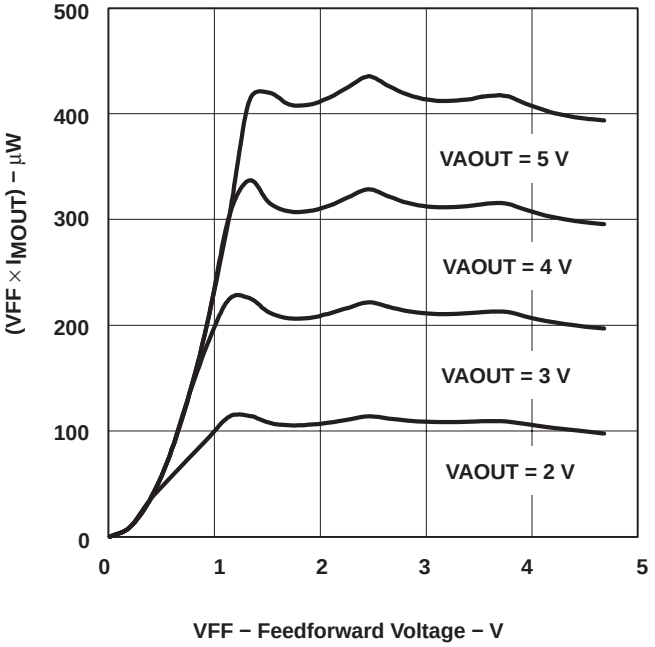


Figure 3

RECOMMENDED MINIMUM GATE RESISTANCE vs. SUPPLY VOLTAGE

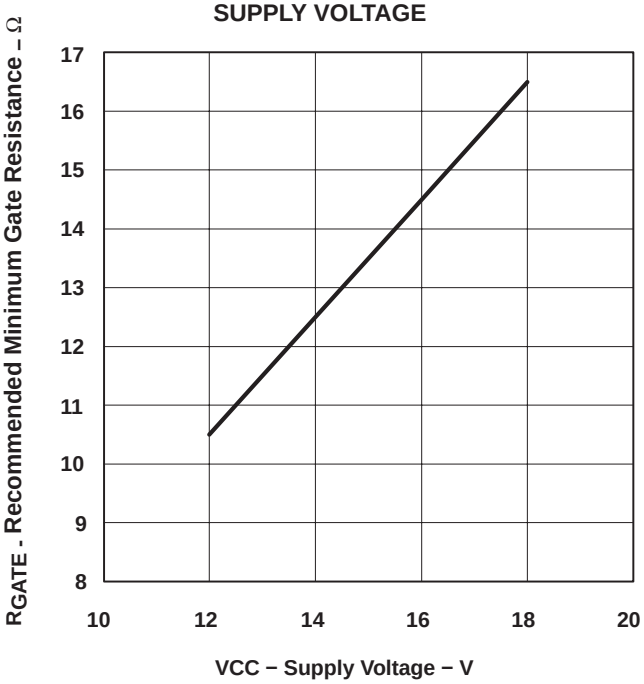


Figure 4

REFERENCE VOLTAGE vs. SUPPLY VOLTAGE

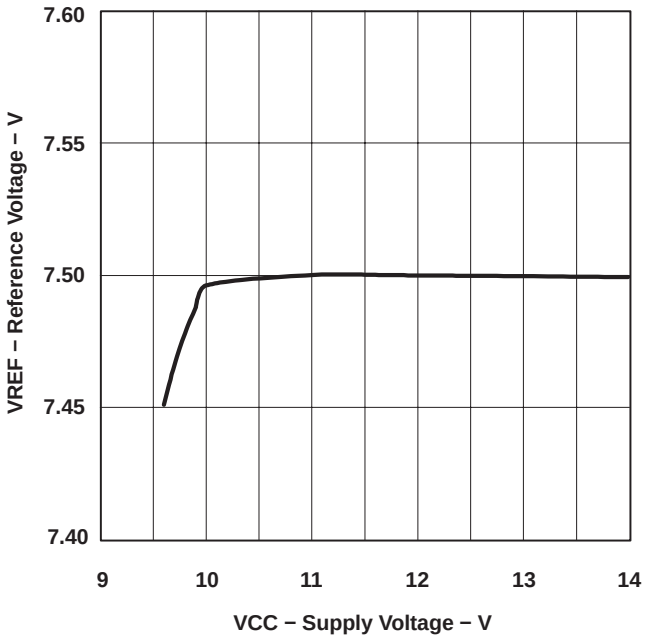


Figure 5

REFERENCE VOLTAGE vs. REFERENCE CURRENT

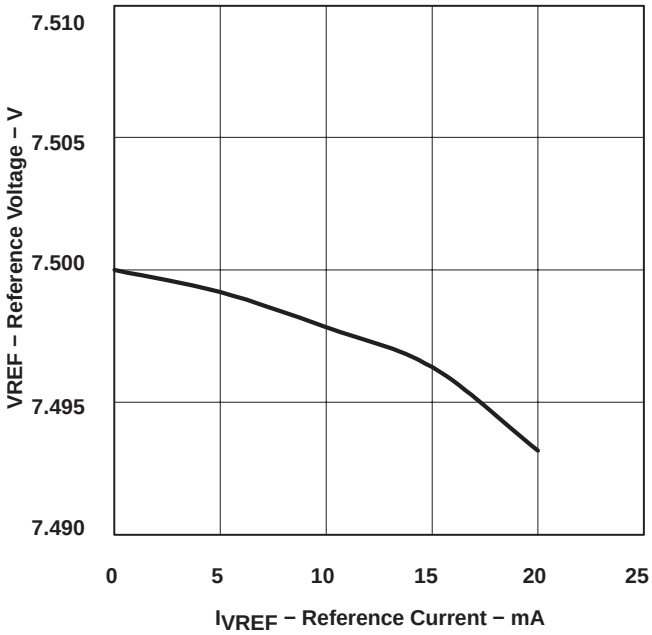


Figure 6

TYPICAL APPLICATION

The UCC38500 series is designed to incorporate all the control functions required for a power factor correction circuit and a second stage dc-to-dc converter. The PFC function is implemented as a full-feature, average-current-mode controller integrated circuit. In addition, the input voltage feedforward function is implemented in a simplified manner. Current from IAC input is mirrored over to the VFF pin. By simply adding a resistor and capacitor (to attenuate 120-Hz ripple) a voltage is developed which is proportional to RMS line voltage, eliminating the need for several components normally connected to the line.

The UCC3850x uses leading-edge modulation for the PFC stage and trailing-edge modulation for the dc-to-dc stage. This reduces ripple current in the output capacitor by reducing the overlap in conduction time of the PFC and dc-to-dc switches. Figures 7 and 8 depict the ripple current reduction in the boost switch. In addition to the reduced ripple current, noise immunity is improved through the current error amplifier implementation. Please refer to the UCC3817 datasheet (TI Literature No. SLUS395) for a detailed explanation of current error amplifier implementation.

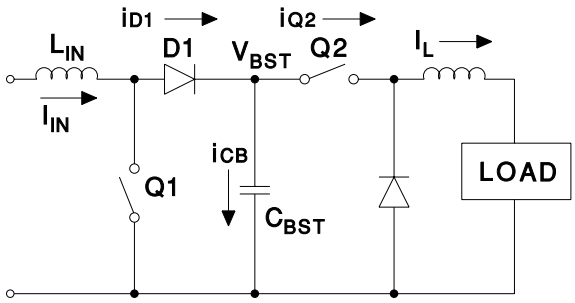


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Figure 7. Simplified Representation of a 2−Stage PFC Power Supply

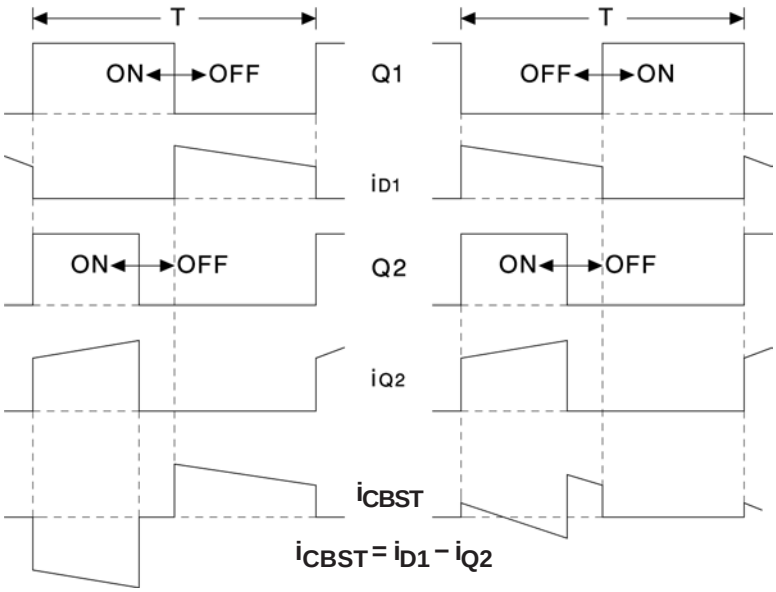

Figure 8. Timing Waveforms for Synchronization Scheme

TYPICAL APPLICATION

The UCC3850x is optimized to control a boost PFC stage operating in continuous conduction mode, followed by a dc-to-dc converter (typically a forward topology). The dc-to-dc converter is transformer isolated and therefore its error amplifier is located on the secondary side. For this reason the UCC3850x is configured without an internal error amplifier for the second power stage. The externally generated error signal is fed into the VERR pin typically through an opto coupler.

The UCC3850x can be configured for voltage-mode control or current-mode control of the second stage. The application figure shows a typical current-mode configuration. For voltage-mode control, the ramp generated by CT can be fed back into the ISENSE2 pin through a voltage divider.

One of the main system challenges in designing systems with a PFC front end is coordinating the turn-on and turn-off on the dc-to-dc converter. If the dc-to-dc converter is allowed to turn on before the boost converter is operational, it must operate at a much-reduced voltage and therefore represents a large current draw to the boost converter. This start-up sequencing is handled internally by the UCC3850x. The UCC3850x monitors the output voltage of the PFC converter and holds the dc-to-dc converter off until the output is within 10% of its regulation point. Once the trip point is reached the dc-to-dc section goes through a soft start sequence for a controlled, low stress start-up. Similarly, if the output voltage drops too low (two voltage options are available) the dc-to-dc converter shuts down thereby preventing overstress of the converter. For the UCC38500 and UCC38501, the dc-to-dc converter shuts down when the PFC output falls below 74% of its nominal value, while for the UCC38502 and UCC38503, the threshold is lowered to 50%.

design example: an off-line, 100-W, power converter

The following design example shows how to implement the UCC38500 in an off-line 100-W power converter. The system requires the converter to operate from a universal input of 85 V_{RMS} to 265 V_{RMS} with a 12-V, 100-W, dc output. This design example is divided into two parts. The first part is the PFC stage design and the second section is the dc-to-dc power stage design. The design goal of the system is to achieve an efficiency of approximately 80%. This is accomplished by requiring the boost regulator to be designed for an efficiency of 95% and the dc-to-dc power stage to be designed for 85% efficiency. The efficiency of the boost converter is designated by variable $\eta 1$ and the efficiency of the dc-to-dc converter is designated by variable $\eta 2$. Figure 9 shows the schematic of the typical application upon which this design example is based. The UCC38500 control device is chosen for this design because of it's self-biasing scheme and minimum input voltage requirements of the dc-to-dc power stage.

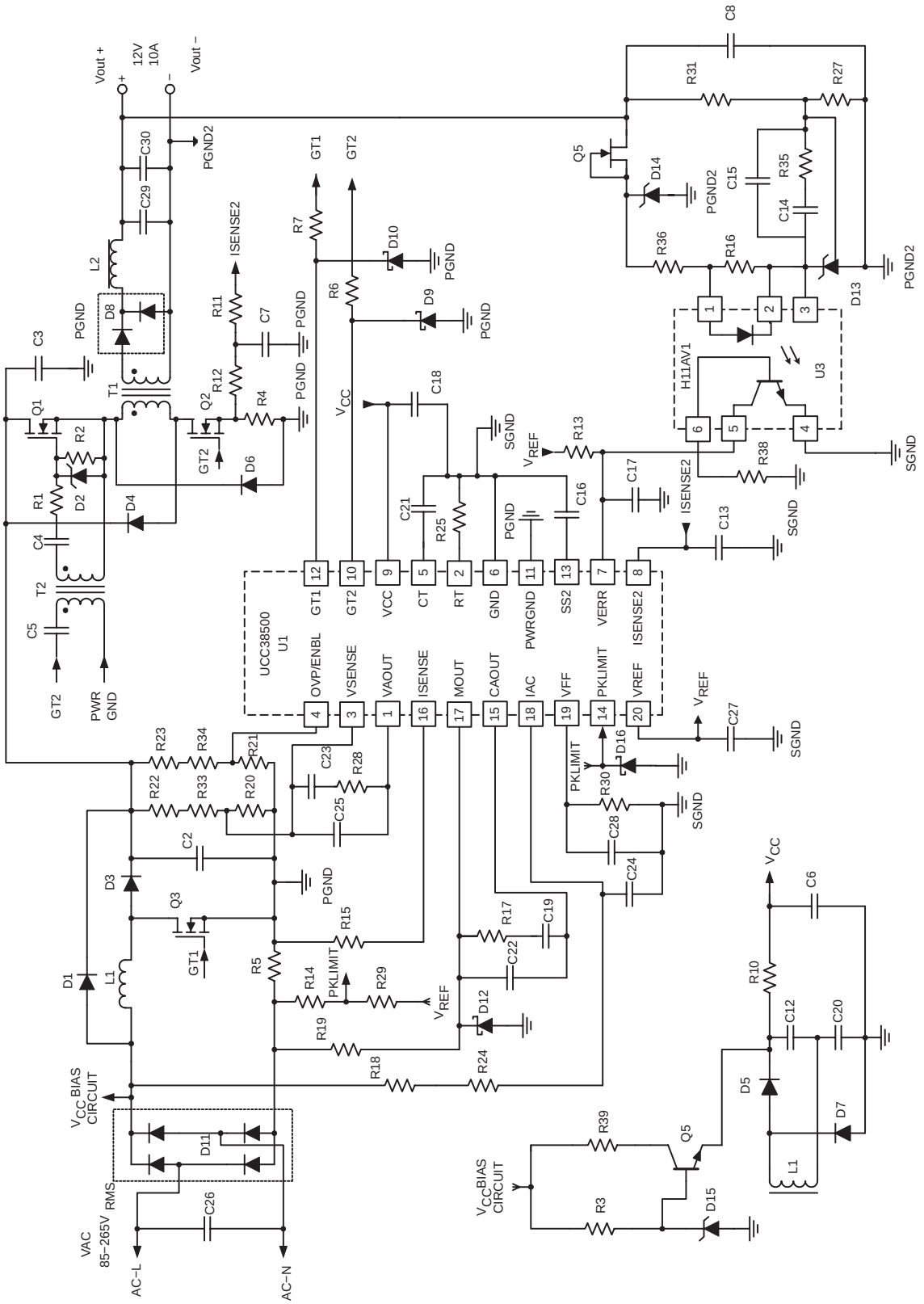

Figure 9. Typical Application Circuit

TYPICAL APPLICATION

I. PFC Boost Power Stage

LBOOST (L1 in Figure 9)

The boost inductor value is determined by the following equations:

$$\Delta I = \frac{\frac{P_{OUT} \times (0.25) \times \sqrt{2}}{\eta 1 \times \eta 2}}{V_{IN\ (min)}}, \quad (1)$$

$$D = 1 - \frac{V_{IN\ (min)} \times \sqrt{2}}{V_{BOOST}}, \quad (2)$$

$$L_{BOOST} = \frac{V_{IN\ (min)} \times \sqrt{2} \times D}{\Delta I \times f_S} \quad (3)$$

where ΔI, the inductor current ripple was set to approximately 25% of the peak inductor current.

In this design example ΔI is approximately 505 mA. D represents the duty cycle at the peak of low line voltage, $V_{IN(min)}$ is the minimum RMS input voltage, and V_{BOOST} is the controlled output voltage of the PFC stage. V_{BOOST} for this design is selected to be 385 V to ensure the PFC stage regulates for the full input voltage range. Variable f_S represent the switching frequency. The switching frequency was selected to be 100 kHz for this design. The calculated boost inductor required for this design is approximately 1.7 mH.

CBOOST (C2 in Figure 9)

Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the holdup time required for supporting the load after the input ac voltage is removed. Holdup is the amount of time that the output stays in regulation after the input has been removed. For this circuit, the desired holdup time is approximately 16 ms. Expressing the capacitor value in terms of output power, output voltage, and holdup time is described in equation (4):

$$C_{BOOST} = \frac{2 \times P_{OUT} \times \Delta t}{\left(V_{BOOST}\right)^2 - \left(V_{BOOST\ (min)}\right)^2} \quad (4)$$

In practice, the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed is determined by dividing the maximum specified output ripple voltage by the capacitor ripple current. In this design, holdup time is the dominant determining factor and a 100 μF, 450 V aluminum electrolytic capacitor from Panasonic, part number ECOS2TB101BA, is used. The voltage rating and the low ESR of 0.663 Ω make it an ideal choice for this design.

TYPICAL APPLICATION

power switch selection (Q3 in Figure 9)

As in any power supply design, tradeoffs between performance, cost and size are necessary. When selecting a power switch, it is useful to calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, drain source capacitance of the MOSFET loss and turnon and turnoff losses:

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times f_S \quad (5)$$

$$P_{COSS} = \frac{1}{2} C_{OSS} \left(V_{OFF}\right)^2 \times f_S \quad (6)$$

$$P_{SW} = \frac{1}{2} V_{OFF} \times I_L \times \left(t_{ON} + t_{OFF}\right) \times f_S \quad (7)$$

Where Q_{GATE} is the total gate charge, V_{GATE} is the gate drive voltage, f_s is the switching frequency, C_{OSS} is the drain source capacitance of the MOSFET, t_{ON} and t_{OFF} are the switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH}) and V_{OFF} is the voltage across the switch during the off time, in this case $V_{OFF} = V_{BOOST}$.

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \times K \times \left(I_{RMS}\right)^2 \quad (8)$$

where K is the temperature factor found in the manufacturer's $R_{DS(on)}$ vs junction temperature curves.

Calculating these losses and plotting against frequency gives a curve that enables the designer to determine either which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. For this design example an IRFP450 HEXFET from International Rectifier is chosen because of its low $R_{DS(on)}$ and its V_{DSS} rating. The IRFP450's $R_{DS(on)}$ of 400 mΩ and the maximum V_{DSS} of 500 V makes it an ideal choice. A comprehensive review of this procedure can be found in the Unitrode Power Supply Design Seminar SEM−1200, Topic 6, TI Literature No. SLUP117.

More recently, faster switching insulated gate bipolar transistors (IGBTs) have become widely available. Depending on the system power level (and the switching frequency), use of IGBTs may make sense for the power switch.

boost diode selection (D3 in Figure 9)

In order to keep the switching losses to a minimum and meet the voltage and current requirements, a HFA08TB60 fast recovery diode from International Rectifier is selected for the design. This diode is rated for a maximum reverse voltage of 600 V and a maximum forward current of 8 A. The typical reverse recovery of 18 ns made this diode ideal for this design.

TYPICAL APPLICATION

peak current limit

Resistor divider R14 and R29 along with current sense resistor R5, devise the peak-limit comparator of the UCC38500 and are used to protect the boost switch Q3 from excessive currents. Proper preparation of this comparator requires that it not interfere with the boost converter's power limit or the forward converter's pulse-by-pulse current limiting. For this design example the forward converter is selected to go into pulse-by-pulse current limiting at approximately 130% of maximum output power. The power limit of the boost converter is set at 140% of the maximum output power. The peak current limit for the boost stage was selected to engage at 150% of the maximum output power to ensure circuit stability.

The following equation is used to select the current-sense resistor R5, where the current-sense resistor is selected to operate over a 1-V dynamic range ($V_{DYNAMIC}$). The current-sense resistor required for the design needed to be approximately 0.43 Ω.

$$R5 = R_{SENSE} = \frac{V_{DYNAMIC}}{I_{PK} + (0.5) \times \Delta I} \cong 0.43\ \Omega \tag{9}$$

The following equation is used to size resistor R14 properly by first selecting R29 to be a standard resistance value. For this design resistor R29 was selected to be 10 kΩ. With a typical reference voltage (V_{REF}) of 7.5 V gives a calculated value of approximately 1.91 kΩ for resistor R14.

$$R14 = \frac{\left(\frac{P_{OUT} \times 1.5 \times \sqrt{2}}{V_{IN\ (min)} \times \eta 1 \times \eta 2} + \Delta I\right) \times R5 \times R29}{V_{REF}} \tag{10}$$

multiplier

The output of the multiplier of the UCC38500 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power-factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are V_{VAOUT}, the voltage amplifier output, I_{IAC}, a representation of the input rectified ac line voltage, and an input voltage feed forward signal, V_{VFF}. The output of the multiplier, I_{MOUT}, can be expressed:

$$I_{MOUT} = \frac{I_{IAC} \times \left(V_{VAOUT} - 1\right)}{K \times \left(V_{VFF}\right)^2} \tag{11}$$

Where K is a constant typically equal to 1 / V.

The I_{IAC} signal is obtained through a high-value resistor connected between the rectified ac line and the IAC pin of the UCC3850X. This resistor (R_{IAC}) is sized to provide the maximum I_{IAC} current at high line. For the UCC3850X the maximum I_{IAC} current is about 500 μA, and a higher current can drive the multiplier out of its linear range. A smaller current level is functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 V_{RMS} to 265 V_{RMS} gives a R_{IAC} value of 750 kΩ. Because of voltage rating constraints of the standard 1/4-W resistor, this application requires a combination of lower value resistors connected in series to give the required resistance and distribute the high voltage amongst the resistors. For this design example two 383 kΩ resistors are used in series.

TYPICAL APPLICATION

The current into the IAC pin is mirrored internally to the VFF pin where it is filtered to produce a voltage feed forward signal proportional to line voltage. The VFF voltage is used to keep the power stage gain constant and to providing input power limiting. Please refer to Texas instruments Application Note on *Power Limiting with Sinusoidal Input* TI Literature No. SLUA196, for detailed explanation on how the VFF pin provides power limiting. The following equation is used to determine the VFF resistor size (R_{VFF}) to provide power limiting where $V_{IN(min)}$ is the minimum RMS input voltage and R_{IAC} is the total resistance connected between the IAC pin and the rectified line voltage.

$$R_{VFF} = \frac{1.4\ V}{\left(\frac{V_{IN\ (min)} \times 0.9}{2 \times R_{IAC}}\right)} \cong 28.7\ k\Omega \tag{12}$$

Because the VFF voltage is generated from line voltage it needs to be adequately filtered to reduce total harmonic distortion caused by the 120-Hz rectified line voltage. Refer to Unitrode Power Supply Design Seminar, SEM−700 Topic 7, *Optimizing a High Power Factor Switching Preregulator*, TI Literature No. SLUP093. A single pole filter is adequate for this design. Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is:

$$\frac{1.5\%}{66\%} = 0.022 \tag{13}$$

With a ripple frequency (f_R) of 120-Hz and an attenuation of 0.022 requires that the pole of the filter (f_P) be placed at:

$$f_P = 120\ Hz \times 0.022 \cong 2.6\ Hz \tag{14}$$

The following equation is used to select the filter capacitor (C_{VFF}) required to produce the desired low pass filter.

$$C_{VFF} = \frac{1}{2\pi \times R_{VFF} \times f_P} \cong 2.2\ \mu F \tag{15}$$

This results in a single-pole filter, which adequately attenuates the harmonic distortion and provides power limiting.

The R_{MOUT} resistor is sized to provide power limiting for the circuit. The power limit is set to 140% of the maximum output power. This is done so that the power limit of the PFC stage does not interfere with power limiting of the dc-to-dc converter, which is set to 130% of the maximum output power. The following equations are used to size the R_{MOUT} resistor, R19. In these equations P_{LIMIT} is the power limit level, P_{OUT} is the maximum output power. $I_{MOUT(max)}$ is the maximum multiplier output current, $I_{IAC}@V_{IN(min)}$ is the minimum current into the IAC pin at low line and $V_{VAOUT(max)}$ is the maximum voltage amplifier output voltage. For this design R19 and R15 need to be approximately 3.57 kΩ.

$$P_{LIMIT} = \frac{P_{OUT} \times 1.4}{\eta 1 \times \eta 2} \tag{16}$$

$$I_{MOUT(max)} = \frac{I_{IAC}\ @\ V_{IN(min)} \times \left(V_{VAOUT(max)} - 1\ V\right)}{K \times \left(V_{FF}\right)^2} \tag{17}$$

TYPICAL APPLICATION

$$R_{MOUT} = \frac{\frac{P_{LIMIT} \times \sqrt{2} \times R_{SENSE}}{V_{IN\ (min)}}}{I_{MOUT(max)}} \quad (18)$$

current loop

The UCC38500 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous Texas Instruments PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC38500 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Please refer to Figure 10 for the typical configuration of the current amplifier.

The following equation defines the gain of the power stage, where V_P is the voltage swing of the oscillator ramp, 4 V for the UCC38500.

$$G_{ID}(s) = \frac{V_{BOOST} \times R_{SENSE}}{s \times L_{BOOST} \times V_P} \quad (19)$$

In order to have a good dynamic response the crossover frequency of the current loop was set to 10% of the switching frequency. This can be achieved by setting the gain of the current amplifier (G_{CA}) to the inverse of the current loop power stage gain at the crossover frequency. This design requires that the current amplifier have a gain of 2.581 at 10 kHz.

$$G_{CA} = \frac{1}{G_{ID}(s)} = 2.581 \quad (20)$$

R_I is the R_{MOUT} resistor, previously calculated to be 3.57 kΩ (refer to Figure 10). The gain of the current amplifier is R_F/R_I, so multiplying R_I by G_{EA} gives the value of R_F, in this case approximately 9.09 kΩ. Setting a zero at the crossover frequency and a pole at half the switching frequency to roll off the high-frequency gain completes the current loop compensation.

$$C_Z = \frac{1}{2\pi \times R_F \times f_C} \quad (21)$$

$$C_P = \frac{1}{2\pi \times R_F \times \left(\frac{f_S}{2}\right)} \quad (22)$$

TYPICAL APPLICATION

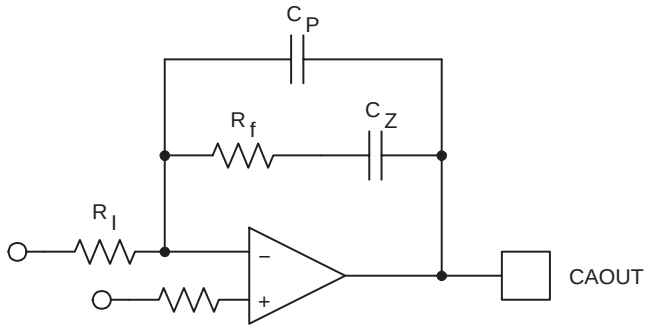

Figure 10. Current Loop Compensation

voltage loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a 3rd harmonic ripple at the input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system (refer to Figure 11).

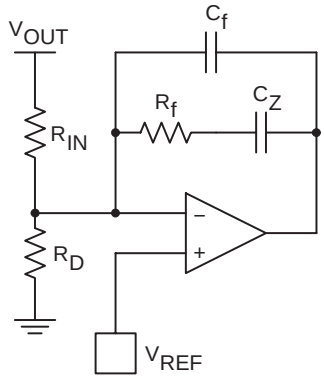

Figure 11. Voltage Amplifier Configuration

The gain of the voltage amplifier, G_{VA}, can be determined by first calculating the amount of peak ripple present on the output capacitor V_{OPK}. The peak value of the second harmonic voltage is given by equation (23), where f_R is the frequency of the rectified line voltage. For this design f_R is equal to 120 Hz.

$$V_{OPK} = \frac{P_{IN}}{\left(2\pi \times f_R \times C_{BOOST} \times V_{BOOST}\right)} \quad (23)$$

TYPICAL APPLICATION

In this example V_{OPK} is equal to 4 V. Assuming an allowable contribution of 0.75% (1.5% peak-to-peak) from the voltage loop to the total harmonic distortion budget sets the gain equal to:

$$G_{VA} = \frac{\left(\Delta V_{VAOUT}\right)(0.015)}{2 \times V_{OPK}} \tag{24}$$

Where ΔV_{VAOUT} is the effective output voltage range of the error amplifier (5 V for the UCC38500). The network needed to realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_F, C_Z, and R_F. The value of R_{IN} is already determined because of its function as one-half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case the value is 1.12 MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 560-kΩ resistors in series because of the voltage rating constraints of most standard 1/4 W resistors. The value of C_F is determined by the equation:

$$C_F = \frac{1}{\left(2\pi \times f_R \times G_{VA} \times R_{IN}\right)} \tag{25}$$

In this example C_F equals 150 nF. Resistor R_F and C_F generate a pole in the voltage amplifier feedback to reduce total harmonic distortion (THD). The location of the pole is found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, is calculated by the equation:

$$f_{VI} = \frac{\sqrt{P_{IN}}}{2\pi\sqrt{\Delta V_{VAOUT} \times V_{OUT} \times R_{IN} \times C_{BOOST} \times C_F}} \tag{26}$$

f_{VI} for this converter is 10 Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM−1000, Topic 1, *Power Factor Correction Circuit,* TI Literature No. SLUP106.

Solving for R_F becomes:

$$R_F = \frac{1}{\left(2\pi \times f_{VI} \times C_F\right)} \tag{27}$$

Or R_F equals approximately 118 kΩ.

Due to the low output impedance of the voltage amplifier, capacitor C_Z is added to improve dc regulation. To maintain good phase margin, the zero from C_Z is set to 10% of f_{VI}. For this design, C_Z is a 2.2-µF capacitor. The following equation is used to calculate C_Z.

$$C_Z = \frac{1}{2\pi \times \left(\frac{f_{VI}}{10}\right) \times R_F} \tag{28}$$

TYPICAL APPLICATION

II. Two Switch Forward DC−to−DC Power Stage

A two-switch forward converter topology was selected for the second stage of this design. The two-switch forward power converter has two major advantages over a traditional forward converter, making it ideal for this application. First, the FETs used in the two-switch forward required only one-half the maximum V_{DS} as compared to the traditional forward converter. Second, the transformer's reset energy is returned to the input through clamping diodes for higher efficiency.

transformer turns ratio

Equation (29) calculates the transformer turns ratio required for the two-switch forward power converter of this design example. It can be derived from the dc transfer function of a forward converter. V_{OUT} is the output voltage of the forward converter and is 12-V for this design. V_F is the forward voltage drop of the secondary rectifier diode and is set to 1V. $V_{BOOST(min)}$ is the minimum input voltage to the forward converter. The level of this voltage is determined by where the control device forces the dc-to-dc converter into undervoltage lockout (UVLO). The UCC38500 control device is configured to drive the dc-to-dc power stage into UVLO at approximately 74% of the nominal boost converters output voltage. $V_{BOOST(min)}$ for this design is approximately 285 V. D_{MAX} is 0.44 and is the guaranteed maximum duty cycle of the forward converter. For this design example the calculated turns ratio is approximately 0.101.

$$\text{Transformer Turns} = \frac{V_{OUT} + V_F}{V_{BOOST(min)} \times D_{MAX}} = \frac{N_S}{N_P} \tag{29}$$

output inductor

The following equations can be used to calculate the inductor required for this design example. First, the minimum duty cycle D_{MIN}, which occurs at the maximum boost voltage, needs to be calculated. The maximum boost voltage is limited by the OVP trip point, which is set to approximately 425 V. For this design D_{MIN} is approximately 31%. The output inductor ripple current (ΔI_L) for this design is given at 30% of the maximum load current. Next calculate the output inductor (L), where the switching frequency (f_S) is 100 kHz. The calculated output inductor for this design is approximately 38 μH.

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{BOOST(max)}} \times \frac{N_P}{N_S} \tag{30}$$

$$\Delta I_L = \frac{P_{OUT} \times 0.3}{V_{OUT}} \tag{31}$$

$$L = \frac{\left(V_{OUT} + V_F\right) \times \left(1 - D_{MIN}\right)}{\Delta I_L \times f_S} \tag{32}$$

TYPICAL APPLICATION

output capacitor

The following equations can be used to estimate the minimum output capacitance and the capacitor's maximum allowable equivalent series resistance (ESR), where C_{OUT} is the minimum output capacitance and t_S is the period of the switching frequency. ΔV_{OUT} is the maximum allowable output ripple voltage, selected as approximately 1% of the output voltage. For this design, the minimum calculated output capacitance is 170 µF and the maximum allowable ESR is 96 mΩ. A Panasonic HFQ 1800-µF electrolytic capacitor with an ESR of 0.048 Ω is used.

$$C_{OUT} = \frac{1}{8} \times \frac{\left(V_{OUT} + V_F\right) \times \left(D_{MAX} \times \left(t_S\right)^2\right)}{L \times \Delta V_{OUT}} \quad (33)$$

$$ESR = \frac{\Delta V_{OUT}}{\Delta I_L} \quad (34)$$

R_{SENSE2}

The dc-to-dc power converter is designed for peak current mode control. R_{SENSE2} is the resistor that senses the current in the forward converter. The sense resistor in Figure 9 is referred to as R4. The following equations can be used to calculate R_{SENSE2}. Where I_M is the magnetizing current of the transformer used in the step-down converter and V_{BOOST} is the output voltage of the boost stage. D is the typical duty ratio of the forward converter. $V_{ISENSE2\_peak}$ is the peak current sense comparator voltage that is typically 1.15 V. For this design example L_M is approximately 8 mH and the R_{SENSE2} is approximately 1 Ω.

$$I_M = \frac{V_{BOOST}}{L_M} \times \frac{D}{f_S} \quad (35)$$

$$R_{SENSE2} = \frac{V_{ISENSE2\_peak}}{I_M + \frac{N_S}{N_P}\left(\frac{\Delta I_L}{2} + I_{OUT(max)} \times 1.3\right)} \quad (36)$$

soft-start

The UCC38500 has soft-start circuitry to allow for a controlled ramp of the second stage's duty cycle during start-up. This is accomplished through the SS2 circuitry described earlier in this data sheet. Equation (37) calculates the approximate capacitance needed based on the designer's soft-start requirements. Where I_{SS2} is the soft-start charging current, which is typically 10 µA. Δt is the desired soft start time, which was selected to be approximately 5 ms for this example. The calculated soft-start capacitor (C_{SS}) for this example is approximately 10 nF.

$$C_{SS} = \frac{I_{ISS2} \times \Delta t}{4.5} \quad (37)$$

slope compensation

When designing with peak current-mode control, slope compensation may be necessary to prevent instability. In this design, the magnetizing current provided more than enough slope compensation. If slope compensation is needed with external components, please refer to Unitrode/Texas Instruments Application Note, *Practical Considerations in Current Mode Power Supplies*, TI Literature No. SLUA110.

TYPICAL APPLICATION

control loop

Figure 12 shows the control block diagram for the typical application shown in Figure 9. $G_C(s)$ is the compensation network's transfer function (TF), $G_{OPTO}(s)$ is the opto-isolator TF, $G_{CO}(s)$ is the control-to-output TF, and H(s) is the divider TF. The following equations can be used to estimate the frequency response of each gain block, where f_{OPTO_pole} is the frequency, where the optoisolator is −3 dB from its dc operating point, and V_{REF_TL431} is the reference voltage of the TL431 shunt regulator. R_{LOAD} represents the typical load impedance for the design.

$$G_{OPTO}(s) = \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi \times f_{OPTO\_pole}}} \tag{38}$$

$$G_C(s) = \frac{s \times R35 \times C14 + 1}{s \times C14 \times R31 \times (1 + (s \times R35 \times C15))} \times \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi \times f_{OPTO\_pole}}} \tag{39}$$

$$H(s) = \frac{R27}{R27 + R31} = \frac{V_{VREF\_TL431}}{V_{OUT}} \tag{40}$$

$$G_{CO}(s) = \frac{V_{OUT}}{V_C} = \frac{R_{LOAD}}{R_{SENSE2}} \times \frac{N_P}{N_S} \times \frac{\left(1 + \left(s \times C_{OUT} \times ESR\right)\right)}{\left(1 + \left(s \times C_{OUT} \times R_{LOAD}\right)\right)} \tag{41}$$

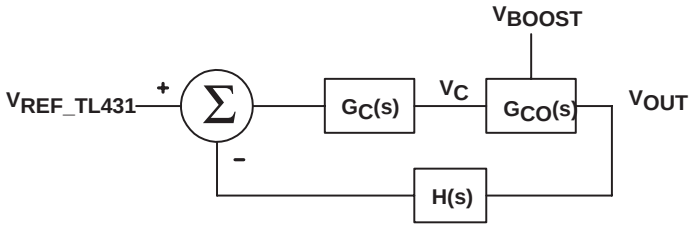

Figure 12. UCC38500 Control Block

TYPICAL APPLICATION

Figure 13 shows the circuitry for the voltage feedback loop. D13 is a TL431 shunt regulator that functions as an operational amplifier, providing feedback control.

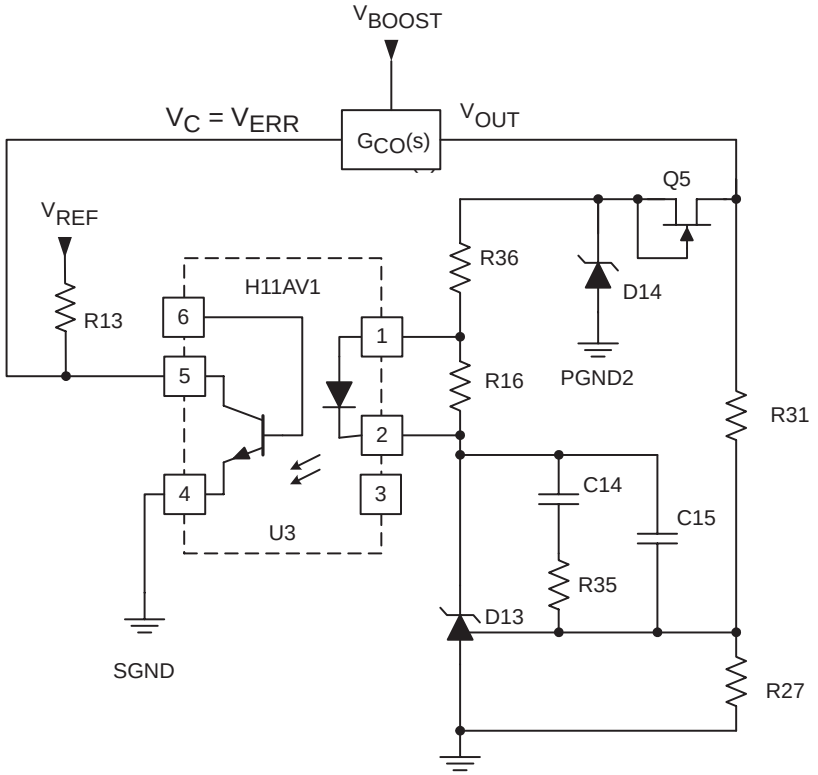

Figure 13. UCC38500 Feedback Loop

Initially the designer must select the resistor values for the divider gain H(s). Equation (42) is used to determine resistor size. Selecting R27 to be a standard value of 10-kΩ requires R31 to be approximately 38.3 kΩ.

$$R31 = \frac{R27\left(V_{OUT} - V_{REF}\right)}{V_{REF}} \tag{42}$$

It is important to correctly bias the TL431 and the optoisolator for proper operation. Zener diode D14 and a depletion mode J-FET, Q5, supply the bias voltage for the TL431. Resistors R16 and R13 provide the minimum bias currents for the TL431 and the optoisolator respectively and can be calculated with the following equations. Where $I_{OP(min)}$ is the minimum optoisolation current, and $V_{VERR(max)}$ is the maximum voltage seen at the VERR pin of the UCC38500. VERR has an internal clamp that limits this pin to 4.5 V. V_F is the typical forward voltage of the diode in the opto isolator, and $I_{TL431(min)}$ is the minimum cathode current of the TL431. For the components used in this design example R13 is calculated to be approximately 2.0 kΩ and R16 was calculated to be approximately 680 Ω. The optoisolator is configured to have dc gain of approximately 20 dB and the optoisolator −3 dB point is approximately 8 kHz. Figure 14 shows the frequency response of the optoisolator.

TYPICAL APPLICATION

$$R16 = \frac{V_F}{I_{TL431\ (min)}} \tag{43}$$

$$R13 = \frac{V_{REF} - V_{VERR\ (max)}}{I_{OP\ (min)}} \tag{44}$$

To compensate the loop, it is necessary to estimate or measure the control-to-output gain's frequency response $G_{CO}(s)$. The frequency response for $G_{CO}(s)$ was measured with a network analyzer and the measured frequency response is shown in Figure 15.

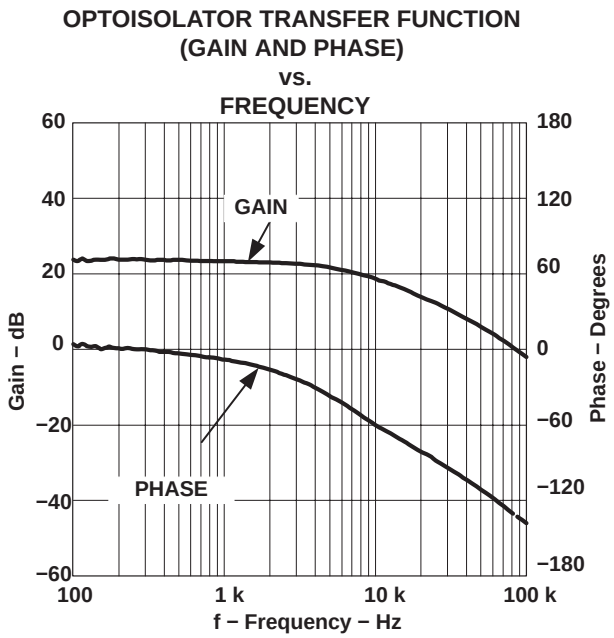

Figure 14

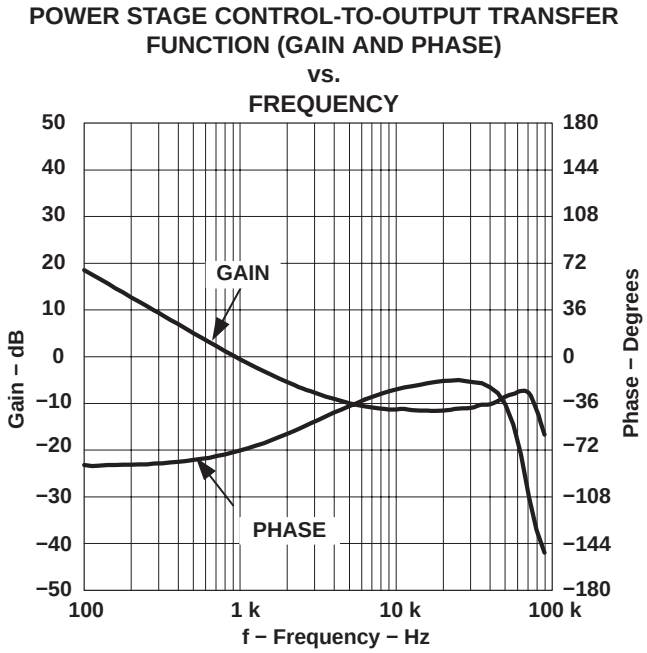

Figure 15

After determining the frequency response of $G_{CO}(s)$ it is necessary to define some closed loop frequency response design goals. The following equation describes the frequency response of the loop gain ($T(s)_{dB}$) of the system in decibels. Typically, the loop is designed to crossover at a frequency below one-sixth of the switching frequency. In order for this design example to have good transient response, the design goal is to have the loop gain crossover at approximately 1 kHz, which is less than one-sixth of the switching frequency. The gain crossover frequency for this design example is referenced as f_C.

$$T(s)\ dB = G_C(s) + G_{CO}(s) + H(s) \tag{45}$$

The compensation network that is used ($G_C(s)$) has three poles and one zero. One pole occurs at the origin, and a second pole is caused by the limitations of the opto-isolator. The third pole is set to attenuate the high-frequency gain and needs to be set to one-half of the switching frequency. The zero is set at the desired crossover frequency.

The following equations can be used to select R35, C14 and C15, where $G_{CO}(s)$, $G_{OPTO}(s)$, and H(s) are the gains in decibels (dB) of each control block at the desired f_C. From the graphs in Figures 14 and 15 it can be observed at the desired crossover frequency $G_{CO}(s)$ is approximately 0 dB and $G_{OPTO}(s)$ is approximately

23 dB. Therefore the compensation circuitry needs to have a gain of −23 dB at the desired crossover frequency. For this example R35 is calculated at approximately 18.2 kΩ. Capacitor C14 is estimated to be approximately 10 nF and C15 is calculated at approximately 180 pF.

$$H(s) = 20\log\left[\frac{V_{REF}}{V_{OUT}}\right] \quad (46)$$

$$R35 = R31 \times 10^{\left(-G_{CO}(s)\ dB + G_{OPTO}(s)\ dB + H(s)\ dB\right)} \quad (47)$$

$$C14 = \frac{1}{\left(2\pi \times R35 \times f_C\right)} \quad (48)$$

$$C15 = \frac{1}{\left(2\pi \times R35 \times \frac{f_{SW}}{2}\right)} \quad (49)$$

Figure 16 shows the frequency response of the compensation network $G_C(s)$ and Figure 17 shows the measured frequency response of the loop gain T(s). The frequency response characteristics in Figure 17 show that f_C is approximately 1.5 kHz with a phase margin of about 55 degrees. The gain margin is approximately 50 dB.

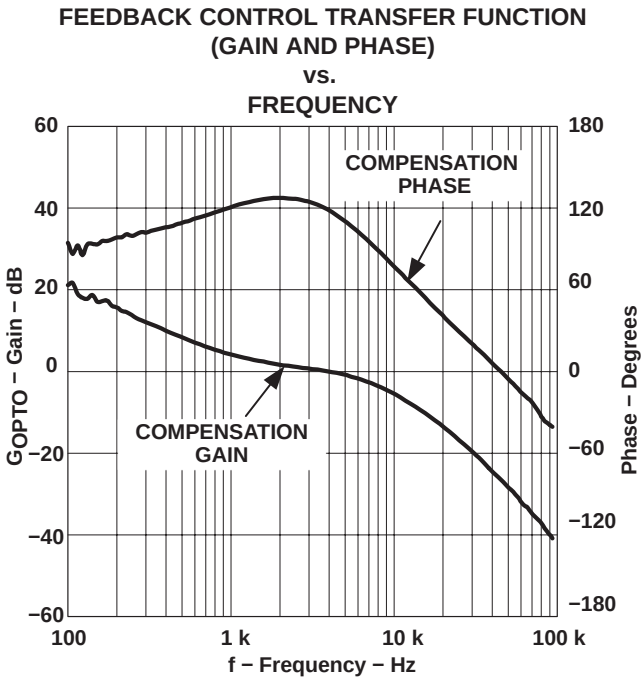

Figure 16

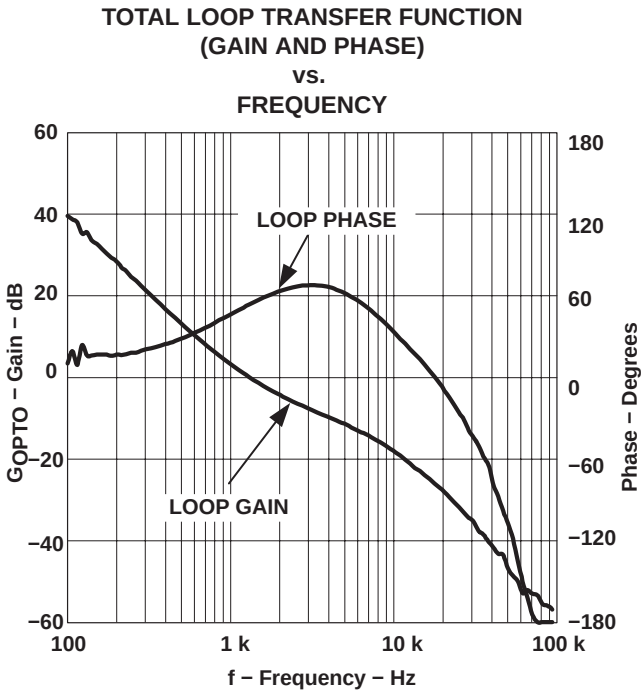

Figure 17

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28500DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28500DW
UCC28500DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28500DW
UCC28500DWTR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28500DW
UCC28500DWTR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28500DW
UCC28501DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	UCC28501DW
UCC28501DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	UCC28501DW
UCC28503DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28503DW
UCC28503DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC28503DW
UCC38500DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38500DW
UCC38500DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38500DW
UCC38500N	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38500N
UCC38500N.A	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38500N
UCC38501DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38501DW
UCC38501DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38501DW
UCC38501N	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38501N
UCC38501N.A	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38501N
UCC38502DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38502DW
UCC38502DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38502DW
UCC38502DWTR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38502DW
UCC38502DWTR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38502DW
UCC38502N	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38502N
UCC38502N.A	Active	Production	PDIP (N) | 20	18 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC38502N
UCC38503DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38503DW
UCC38503DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38503DW
UCC38503DWTR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38503DW
UCC38503DWTR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC38503DW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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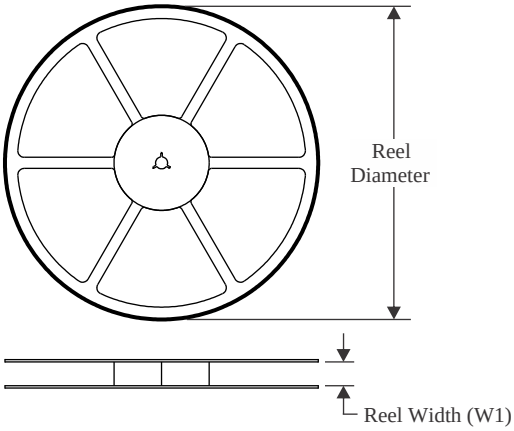
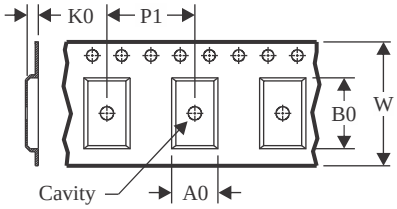
TAPE AND REEL INFORMATION

REEL DIMENSIONS

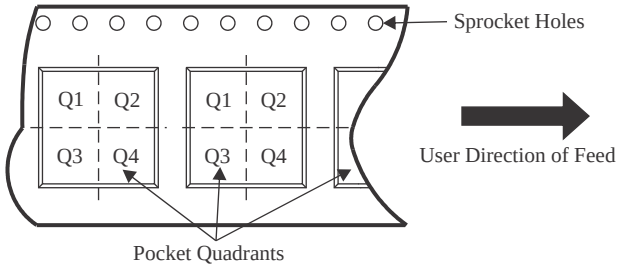


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

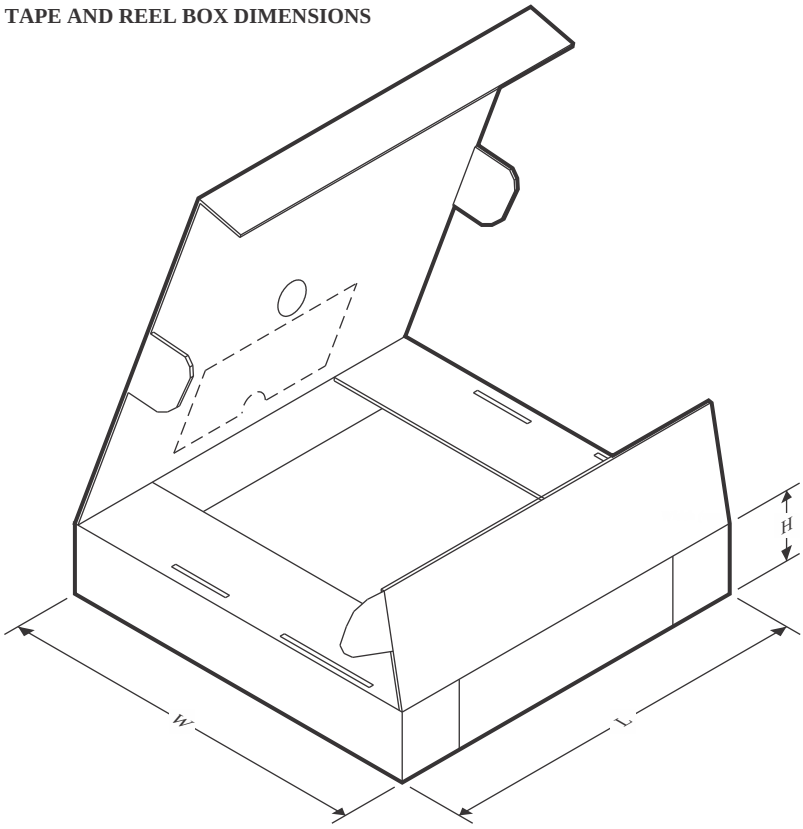
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28500DWTR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

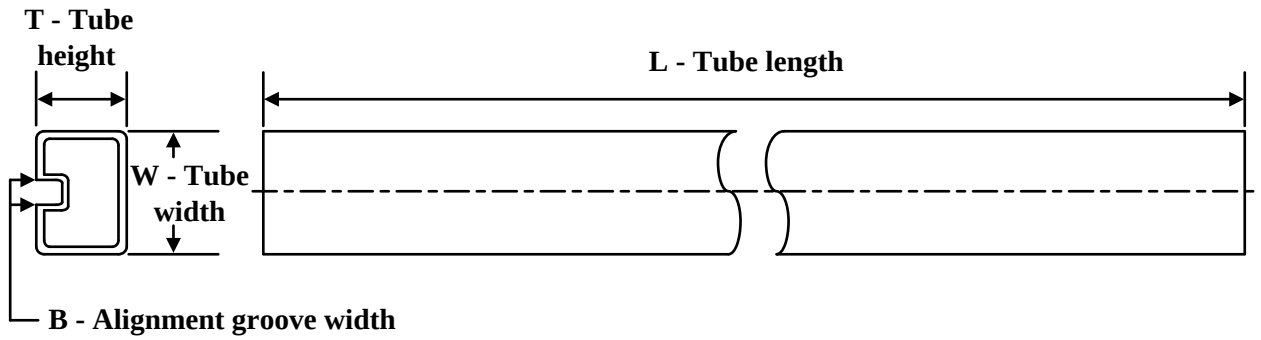
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28500DWTR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



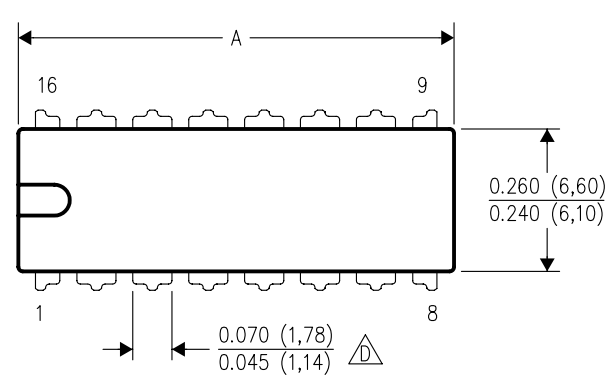
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28500DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28500DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28501DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28501DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28503DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC28503DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38500DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38500DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38500N	N	PDIP	20	18	506	13.97	11230	4.32
UCC38500N.A	N	PDIP	20	18	506	13.97	11230	4.32
UCC38501DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38501DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38501N	N	PDIP	20	18	506	13.97	11230	4.32
UCC38501N.A	N	PDIP	20	18	506	13.97	11230	4.32
UCC38502DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38502DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38502N	N	PDIP	20	18	506	13.97	11230	4.32
UCC38502N.A	N	PDIP	20	18	506	13.97	11230	4.32
UCC38503DW	DW	SOIC	20	25	507	12.83	5080	6.6
UCC38503DW.A	DW	SOIC	20	25	507	12.83	5080	6.6

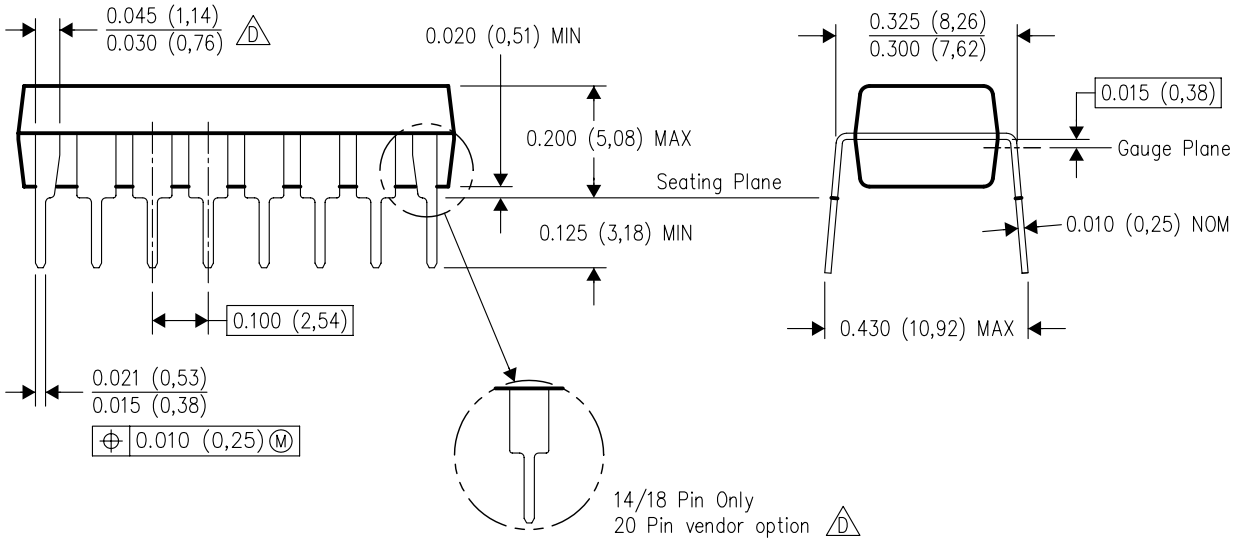
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

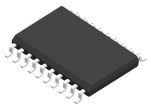


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

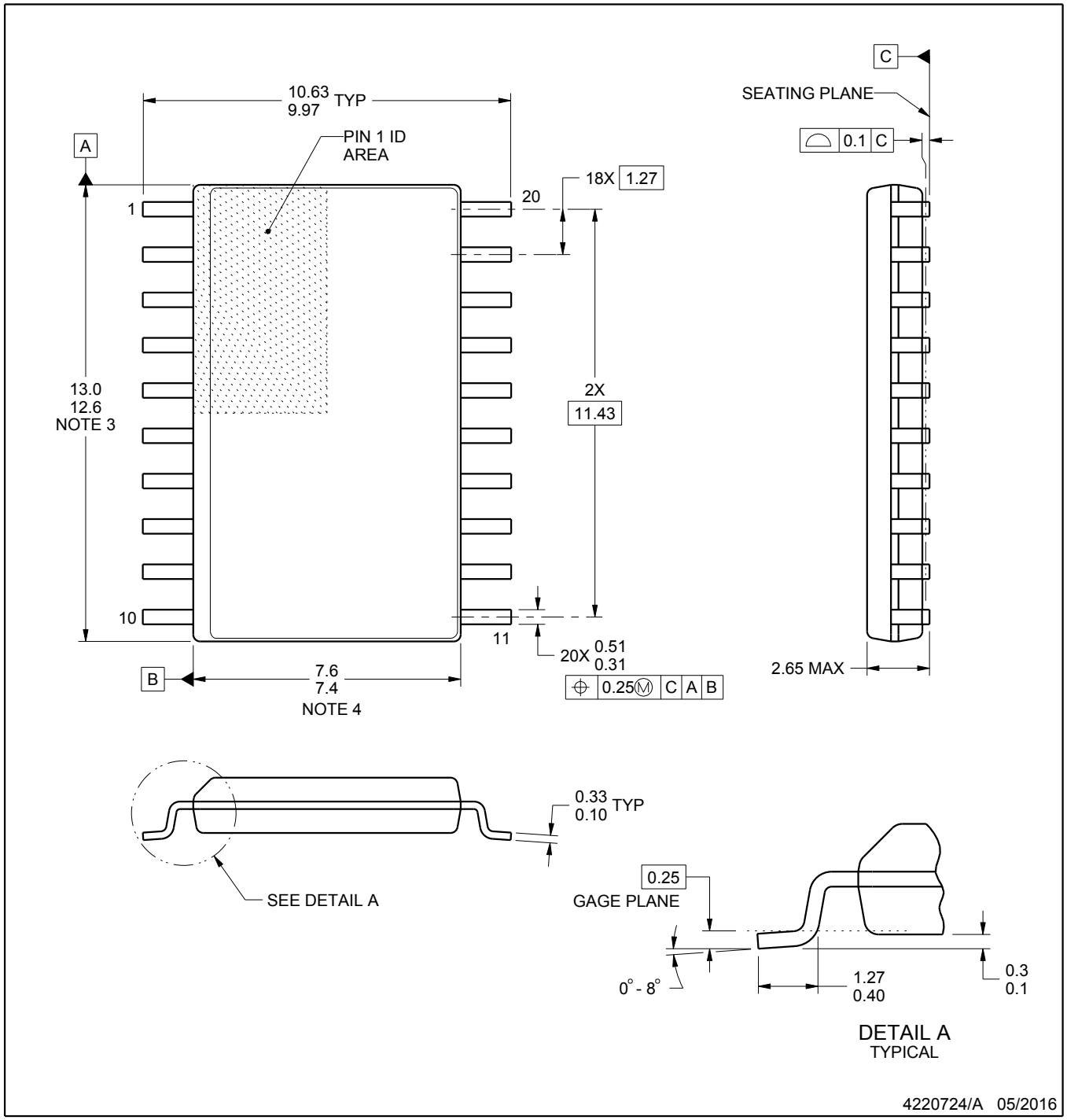


PACKAGE OUTLINE

DW0020A

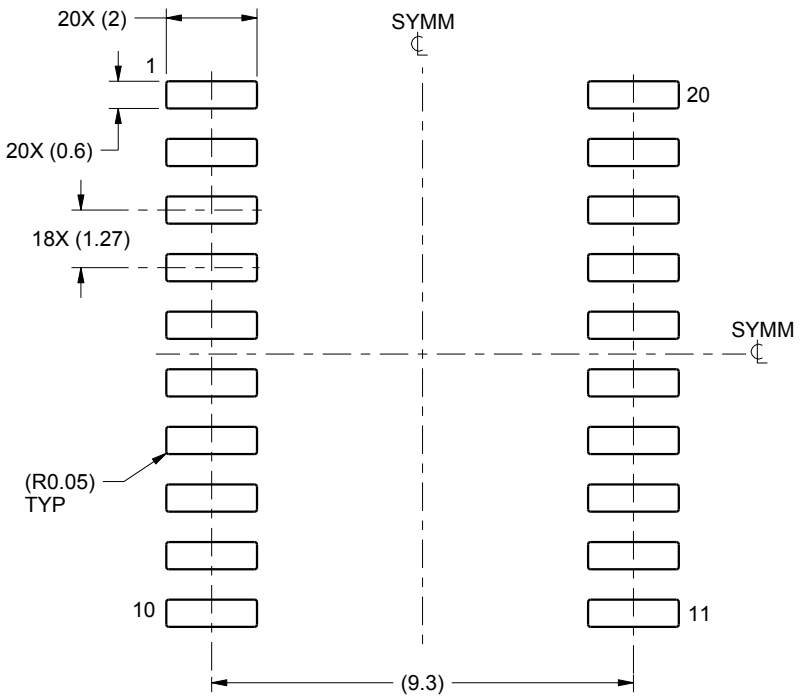
SOIC - 2.65 mm max height

SOIC

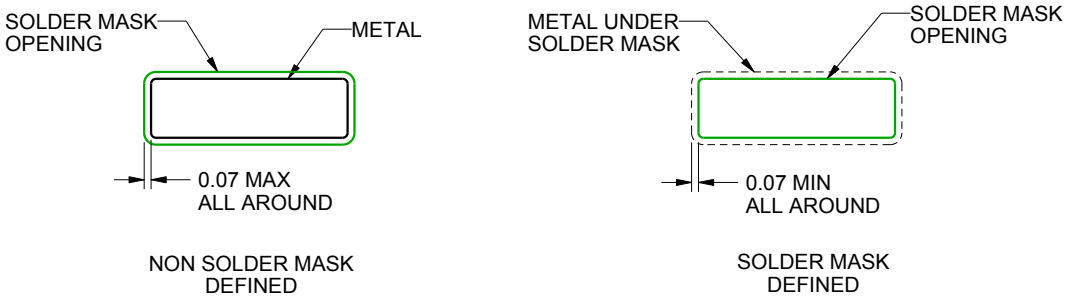


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

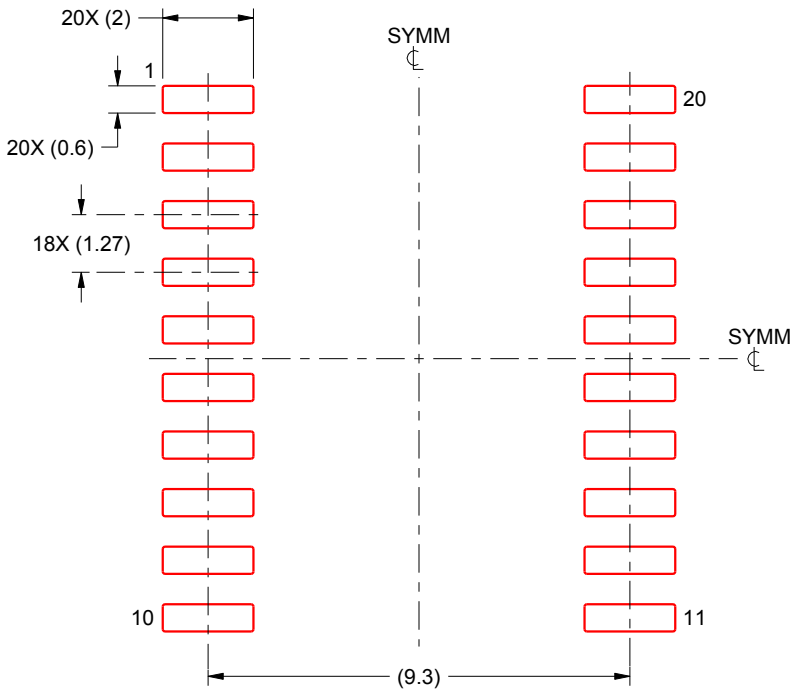


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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