Document Number: MC33287
Rev. 5.0, 2/2007

Contact Monitoring and Dual Low-Side Protected Driver

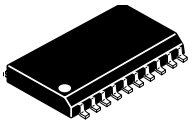
33287

AUTOMOTIVE CONTACT MONITORING AND DUAL LOW-SIDE PROTECTED DRIVER

The 33287 interfaces between switch contacts and a microcontroller. Eight switch-to-battery (or switch-to-ground) sense monitor switch status. Additionally, two internal low-side switches are available to control inductive or capacitive loads.

The 33287 has eight sense inputs (rated at 40 V) with thresholds ratiometric to V_{BAT}. One sense input has a dedicated output for direct interfacing to the MCU and the remaining seven inputs are multiplexed interfaced to the MCU.

The two low-side switch outputs are current limited to 535 mA and internally clamped to 50 V. Outputs also have independent overtemperature shutdown and diagnostic reporting.



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42343B
20-PIN SOICW

Features

- Eight High-Voltage Sense Inputs
- Direct Interfacing to Microcontroller
- Two Current Limited Low-Side Drivers
- Drivers Internally Overvoltage Clamped and Thermally Protected
- 55 µA Standby Current
- Pb-Free Packaging Designated by Suffix Code EG

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33287DW/R2	-40 to 125°C	20 SOICW
MCZ33287EG/R2		

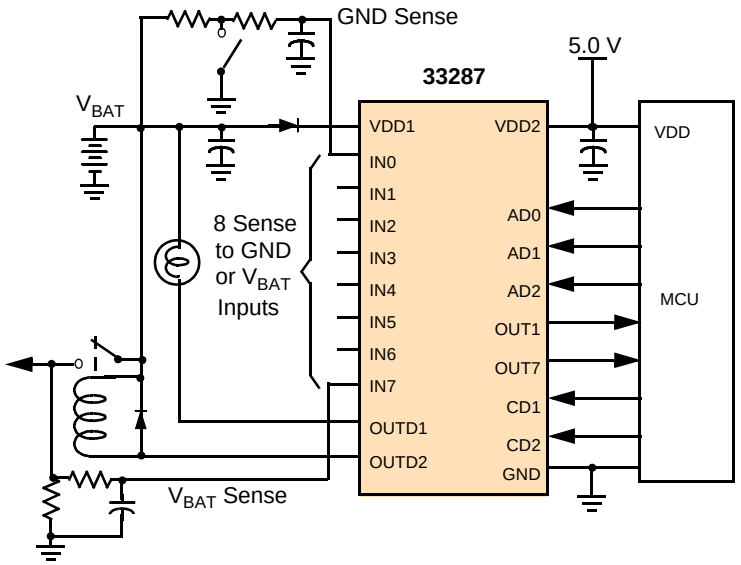


Figure 1. Simplified Application Design

INTERNAL BLOCK DIAGRAM

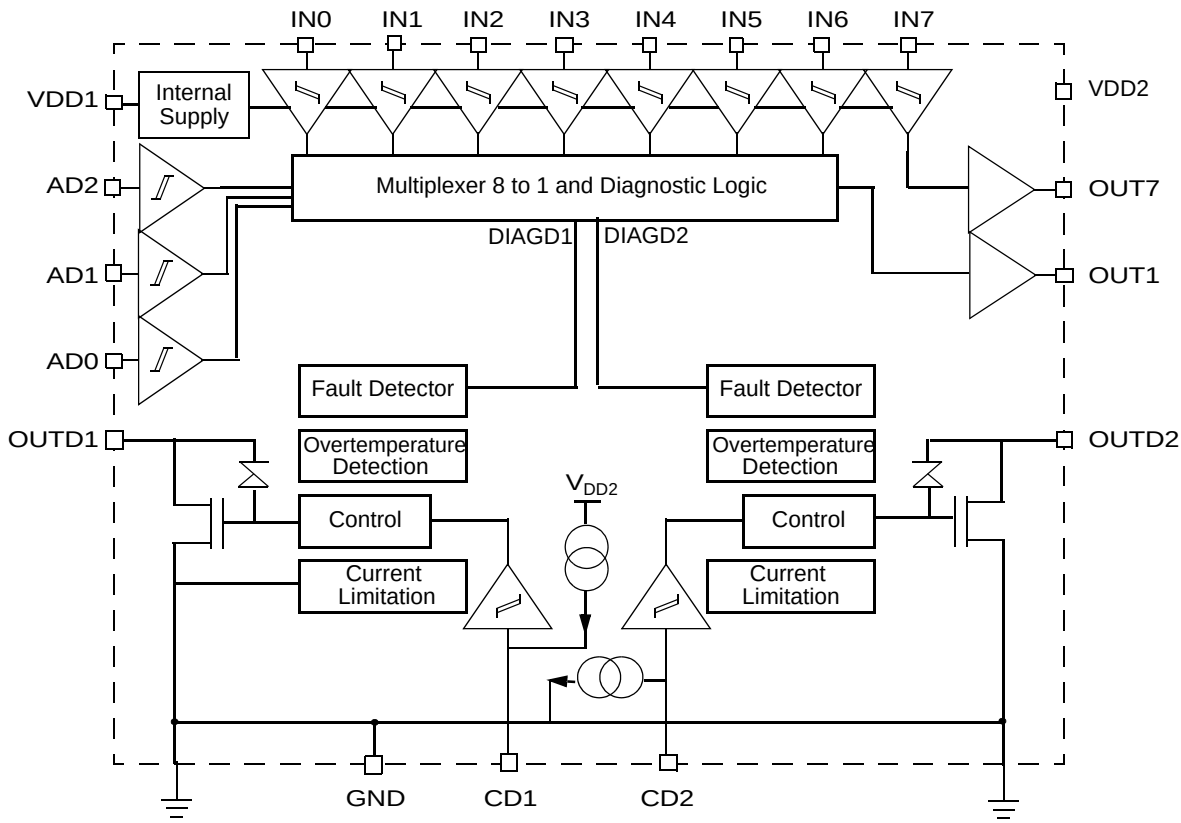


Figure 2. 33287 Simplified Internal Block Diagram

PIN CONNECTIONS

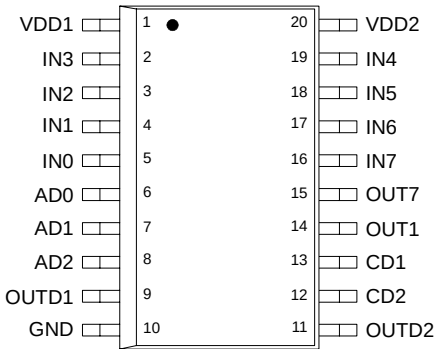


Figure 3. 33287 Pin Connections

Table 1. 33287 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1, 20	V_{DD1}, V_{DD2}	Voltage Power	These are high-voltage power supply 5.0 V pins (V_{BAT}).
5, 4, 3, 2, 19, 18, 17, 16	IN0 – IN7	Input 0 – 7	These are high-voltage input pins.
6, 7, 8	AD0 – AD2	Address	These pins are the addresses for mode and input selection.
9, 11	OUTD1, OUTD2	Output Drain	These two are output driver pins (drain).
10	GND	Ground	This pin in the ground for the logic and analog circuitry of the device.
12, 13	CD1, CD2	Command Driver	These are the two driver command pins.
14	OUT1	Output 1	This is the output (multiplexed Output 1 = 0 to 6.0 V for IN0 to IN6 and DIAGD1 or DIAGD2) and DIAGD2 pins.
15	OUT7	Output 7	This is the direct output from IN7 pin.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Power Supply Voltage Normal Operation (Steady-State) Load Dump Conditions	V_{DD1}	 24 40	V
Logic Supply Voltage (Continuous)	V_{DD2}	7.0	V
Input Pin Voltage (1)	V_{IN}	40	V
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Operating Ambient Temperature	T_A	-40 to 125°C	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation (T_A = 85°C)	P_D	0.7	W
Peak Package Reflow Temperature During Reflow (3), (4)	T_{PPRT}	Note 4.	°C
Thermal Resistance Junction-to-Ambient	$R\theta_{J-A}$	100	°C/W

Notes

1 With Serial Resistor ≥ 25 kΩ

2 ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).

3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 7.0 V ≤ V_{DD1} ≤ 18 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Extended limit is 5.0 V ≤ V_{DD1} ≤ 7.0 V and other parameters are full specification in this mode. Inputs IN1–IN7 and low-side drivers are still functional with down-graded characteristics.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE (V_{DD1} AND V_{DD2} PINS)					
Operational Supply Voltage	VDD1				V
Full Specification		7.0	12	18	
Extend Limit		5.0	—	7.0	
Operational Supply Voltage (Full Specification)	VDD2	4.75	—	—	V
Supply Current Standby Mode[5]					µA
V_{DD1} ≤ 14 V	IVDD1-0	—	55	110	
V_{CD1} = V_{DD2}, V_{CD2} = 0 V	I_{VDD2-0}	—	—	10	
Supply Current in Drivers on Configuration (Full Specification)[5]					µA
V_{CD1} = 0 V	IVDD1-1	—	250	1500	
V_{CD2} = V_{DD2}	I_{VDD2-1}	—	650	1500	
OUTPUT DRIVERS CHARACTERISTICS (OUTD1 AND OUTD2 PINS)					
Output Resistance (Full Specification and T_J ≤ 130°C)	$R_{DS(ON)}$	—	1.40	3.20	Ω
Output Resistance (Extent Limit and T_J ≤ 130°C)	$R_{DS(ON)}$	—	—	5.0	Ω
Leakage Current (Internal Current Source)	I_{LEAK}	1.0	—	13	µs
PROTECTION AND LEVEL DETECTION (OUTD1 AND OUTD2 PINS)					
Positive Output Clamp	V_{CLAMP}	40	50	60	V
Output Current Limitation (130°C ≥ T_J)	I_{LIM}	300	535	750	mA
Output Fault Detector Level	V_{FAULT}	2.0	2.75	3.5	V
Overtemperature Detection (at 25°C by Function Simulation)	T_{DETEC}	145	160	175	°C
INPUTS (CD1 AND CD2 PINS)					
Input Voltage Low	V_{IL}	—	—	4.0 x V_{DD2}	V
Input Voltage High	V_{IH}	8.0 x V_{DD2}	—	—	V
Hysteresis	V_{HST}	500	800	—	mV
Input Current on Pin CD1 (Internal Pull-Up and CD1 Connected to Ground)	I_{CD1}	-100	-30	-10	µA
Leakage Current on Pin CD1 (Internal Pull-Up Connected to V_{DD2})	I_{LEAK}	-5.0	—	5.0	µA
Input Current on Pin CD2 (Internal Pull Down CD2 Connected to V_{DD2})	I_{CD2}	10	30	100	µA
Leakage Current on Pin CD2 (Internal Pull-Up CD1 Connected to Ground)	I_{LEAK}	-5.0	—	5.0	µA

Notes

5 All INn and ADn inputs are connected to ground.

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 7.0 V ≤ V_{DD1} ≤ 18 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Extended limit is 5.0 V ≤ V_{DD1} ≤ 7.0 V and other parameters are full specification in this mode. Inputs IN1–IN7 and low-side drivers are still functional with down-graded characteristics.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUTS (IN0 TO IN7 PINS)					
Input Voltage Low (Full Specification)	V_{IL}	—	—	4.0 x V_{DD1}	V
Input Voltage Low (Extended Limit)	V_{IL}	—	—	3.0 x V_{DD1}	V
Input Voltage High (Full Specification and Extended Limit)	V_{IH}	7.0 x V_{DD1}	—	—	V
Hysteresis (5.0 V < V_{DD1} < 16 V)	V_{HYS}	5.0	1.0	—	V
Input Current (V_{IN} < 16 V)	I_{LEAK}	5.0	—	5.0	µA
Input Voltage Clamp (I = 100 µA)	$V_{INCLAMP}$	17	20	23	V
INPUTS (AD0, AD1, AND AD2 PINS)					
Input Voltage Low	V_{IL}	—	—	4.0 x V_{DD2}	V
Input Voltage High	V_{IH}	8.0 x V_{DD2}	—	—	V
Hysteresis	V_{HYS}	500	750	—	mV
Input Current	I_{LEAK}	-5.0	—	5.0	µA
OUTPUTS (OUT1 AND OUT7 PINS)					
Output Voltage Low (I_{LOAD} = 2.0 mA)	V_{OL}	—	—	2.0 x V_{DD2}	V
Output Voltage High (I_{LOAD} = -2.0 mA)	V_{OH}	8.0 x V_{DD2}	—	—	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVERS CHARACTERISTICS (OUTD1 AND OUTD2 PINS)					
Turn ON Delay Time	t_{ON}	—	1.3	10	µs
Turn OFF Delay Time	t_{OFF}	—	2.1	10	µs
Output Rising Edge	t_{RISE}	—	2.8	10	µs
Output Falling Edge	t_{FALL}	—	1.0	10	µs
Difference Between Command Duration and Bit Duration	Δ_{BIT}	-5.0	—	5.0	µs

TIMING DIAGRAMS

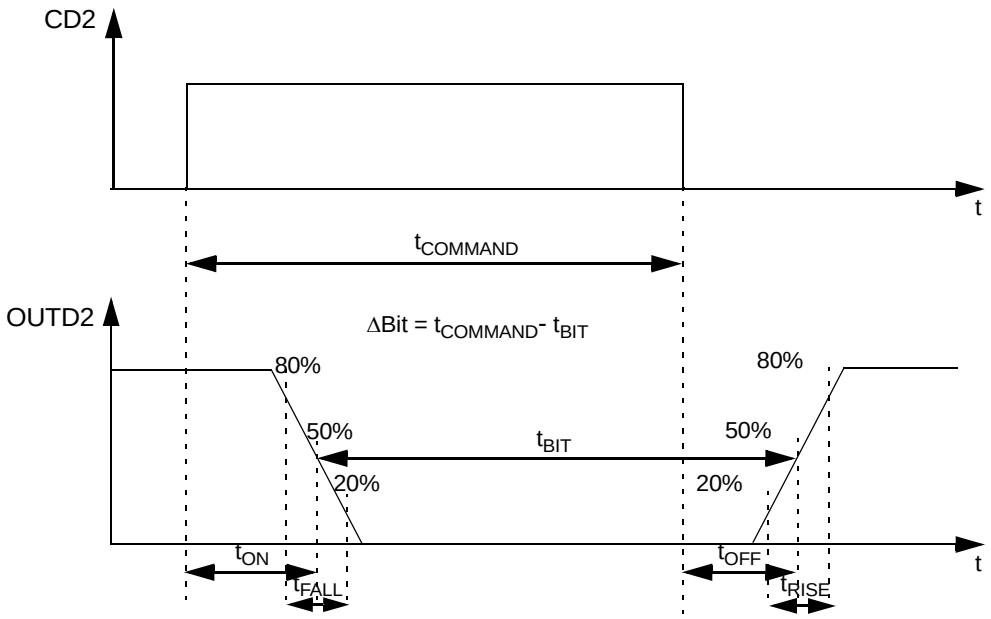


Figure 4. Timing Characteristics

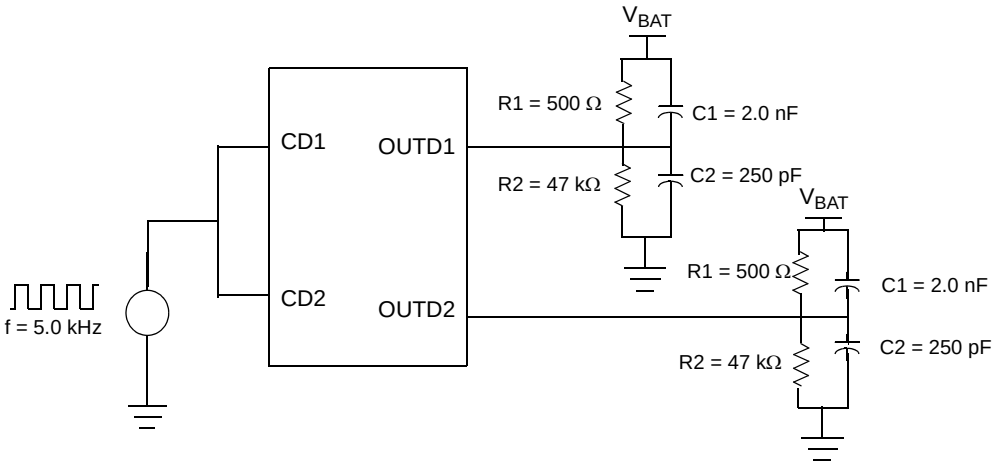


Figure 5. Timing Test Configuration

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

Table 5. Drivers Function Table

CD1 (6)	OUTD1	DIAGD1 (8)	Status
High Level for Logic Signals	High Level for Drivers Outputs	High Level for Logic Signals	Driver 1 Normally OFF
Low Level for Logic Signals	Low Level for Drivers Outputs	High Level for Logic Signals	Driver 1 Normally ON
High Level for Logic Signals	Low Level for Drivers Outputs	Low Level for Logic Signals	Driver 1 Shorted to GND or Open Load
Low Level for Logic Signals	High Level for Drivers Outputs	Low Level for Logic Signals	Driver 1 Overloaded
CD2 (7)	**OUTD2**	**DIAGD2**	**Status**
Low Level for Logic Signals	High Level for Drivers Outputs	High Level for Logic Signals	Driver 2 Normally OFF
High Level for Logic Signals	Low Level for Drivers Outputs	High Level for Logic Signals	Driver 2 Normally ON
Low Level for Logic Signals	Low Level for Drivers Outputs	Low Level for Logic Signals	Driver 2 Shorted to GND or Open Load
High Level for Logic Signals	High Level for Drivers Outputs	Low Level for Logic Signals	Driver 2 Overloaded

Notes
6 CD1 is active on low level (driver 1 is on when CD1 is low).
7 CD2 is active on high level (driver 2 is on when CD2 is high.
8 DIAGD1 output is neither latched nor filtered.

Table 6. Eight-to-One Data Multiplexer Function

Inputs			**OUT1**
AD2	**AD1**	**AD0**	
High Impedance	High Impedance	High Impedance	Unknown
Low Level	Low Level	Low Level	IN0(9)
Low Level	Low Level	High Level	IN1
Low Level	High Level	Low Level	IN2
Low Level	High Level	High Level	IN3
High Level	Low Level	Low Level	IN4
High Level	Low Level	High Level	IN5
High Level	High Level	Low Level	IN6
High Level	High Level	High Level	DIAGD1 or DIAGD2(10)

Notes
9 IN0 to IN6 are the normalized values.
10 DIAGD1 or DIAGD2 are the values of the selected internal fault detector. See **Table 7**.

Table 7. Fault Detector Selection

Inputs			OUT1
AD2	**AD1**	**AD0**	
Unknown	Unknown	Unknown	Unknown
Unknown	Low Level	High Level	Unknown
High Level	High Level	High Level	DIAGD1
Unknown	Unknown	Unknown	Unknown
Unknown	High Level	Low Level	Unknown
High Level	High Level	High Level	DIAGD2

TYPICAL APPLICATIONS

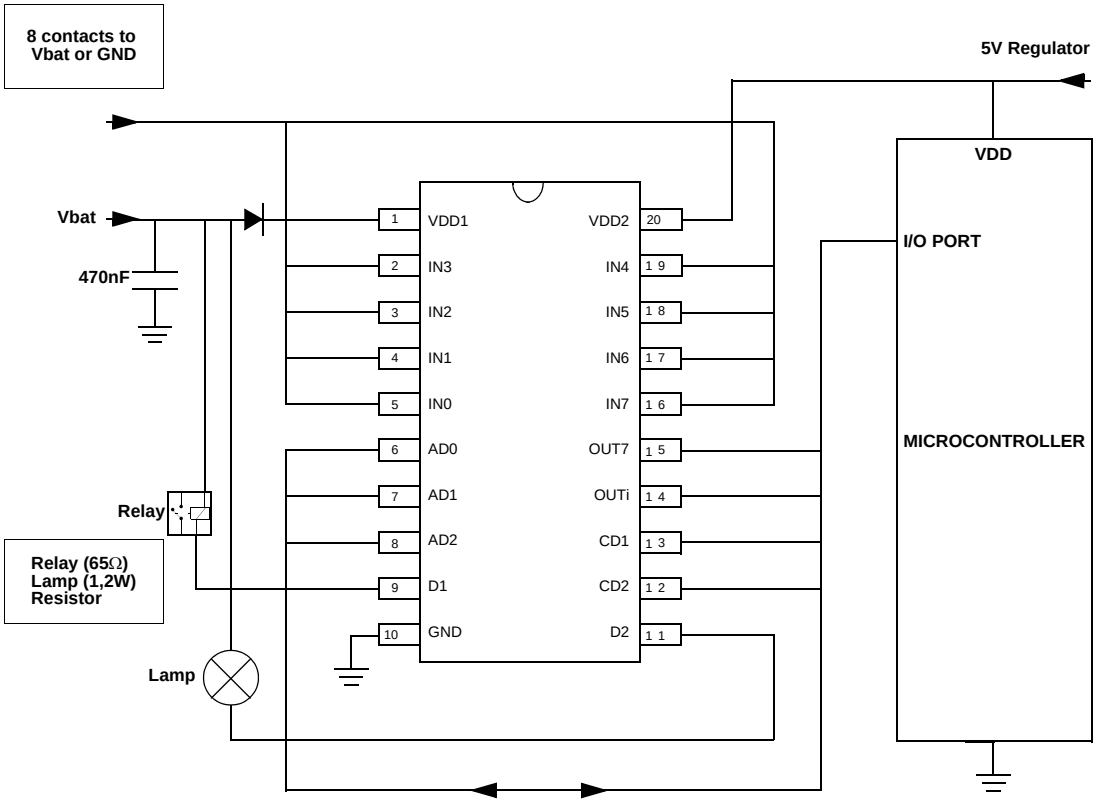


Figure 6. Typical Application Configuration

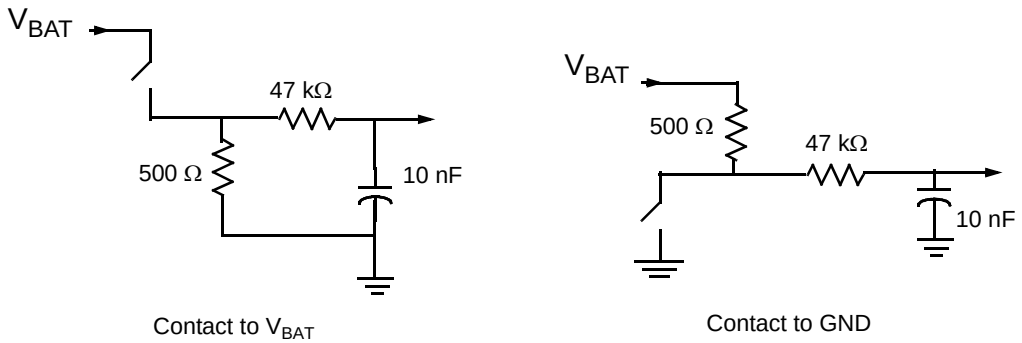
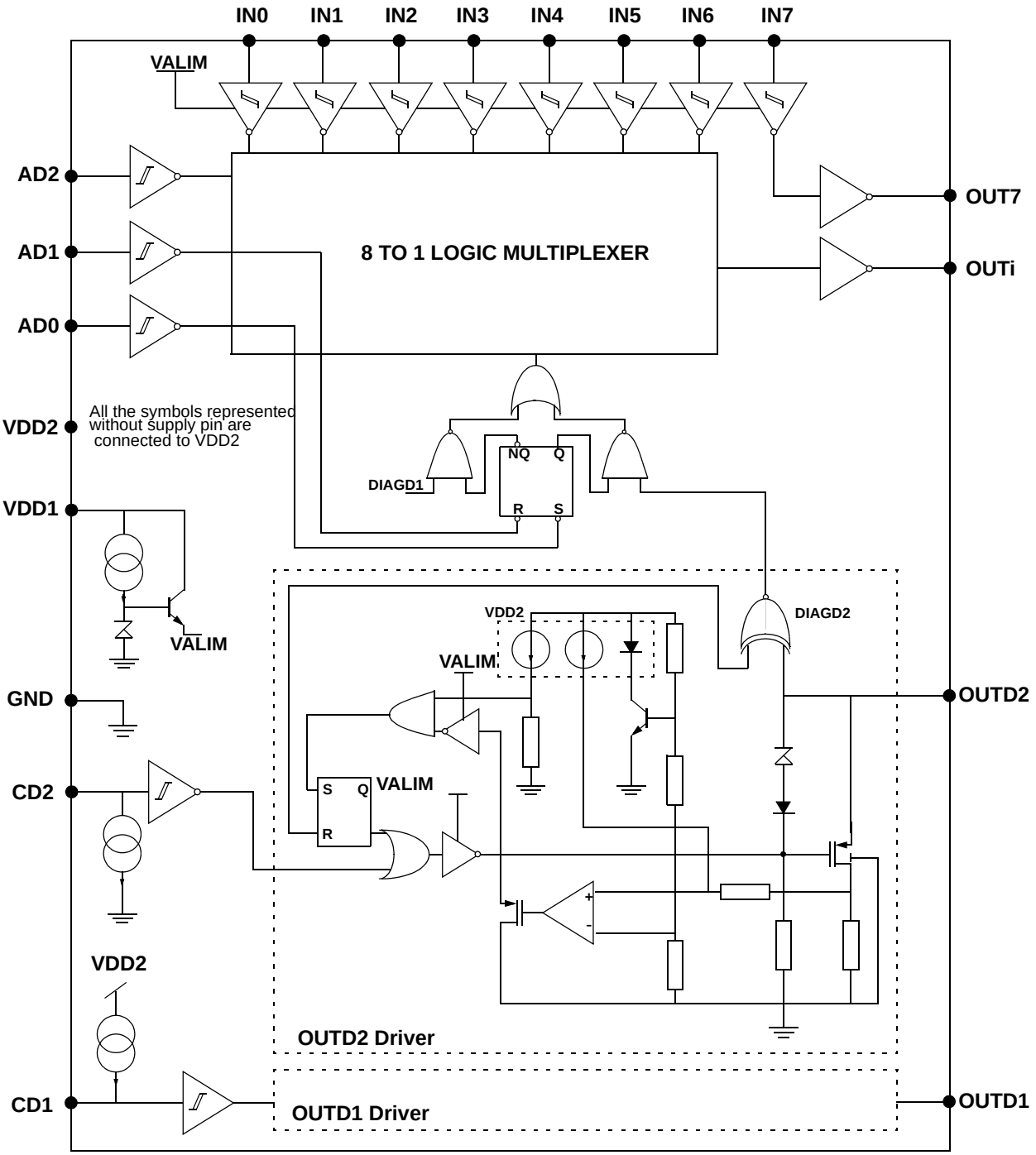


Figure 7. Contact Configuration



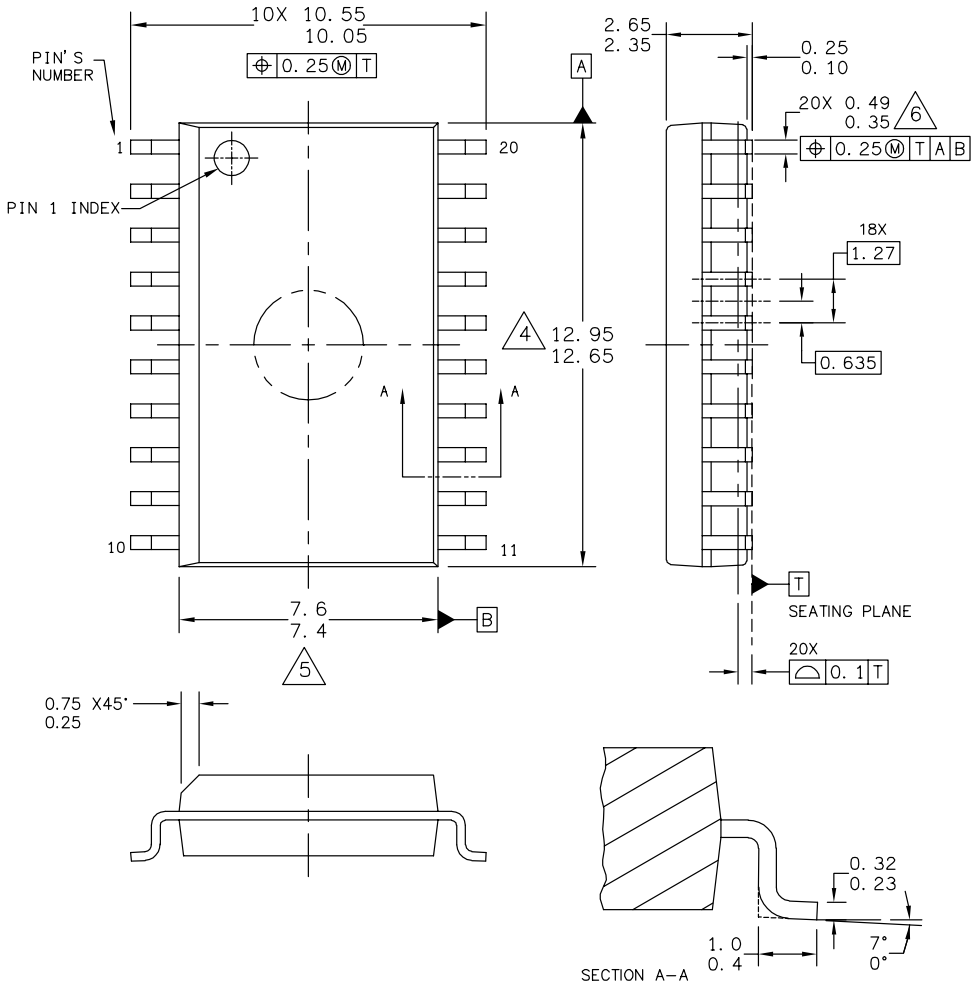
NOTE: The only difference between the low side driver 1 and 2 is the polarity of the command. Also, there is an integral pull-up at pin CD1, and an internal pull-down at pin CD2.

Figure 8. Electrical Schematic

PACKAGE

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

DW SUFFIX
EG SUFFIX (PB-FREE)
20-PIN
PLASTIC PACKAGE
98ASB42343B
REV. J

33287

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	11/2006	• Converted to Freescale format with the current form and style • Implemented Revision History page • Updated Package Drawing 98ASB42343B to Rev. J • Added EG Pb-FREE suffix • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions to obtain this information from www.freescale.com.
5.0	2/2007	• Corrected Internal Block Diagram on page 2 • Restated Definition for OUT1 in 33287 Pin Definitions on page 3 • Corrected value for Storage Temperature on page 4 • Corrected unit for Output Resistance (Extent Limit and $T_J \leq 130°C$) on page 5 • Corrected Electrical Schematic on page 12 • Restated note 4 in Maximum Ratings on page 4.

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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
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Europe, Middle East, and Africa:
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Technical Information Center
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+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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