



April 2000
Revised May 2003

NC7SZ57 • NC7SZ58

TinyLogic® UHS Universal Configurable 2-Input Logic Gates

General Description

The NC7SZ57 and the NC7SZ58 are Universal Configurable 2-Input Logic Gates. Each device is capable of being configured for 1 of 5 unique 2-input logic functions. Any possible 2-input combinatorial logic function can be implemented as shown in the Function Selection Table. Device functionality is selected by how the device is wired at the board level. Figure 1 through Figure 10 illustrate how to connect the NC7SZ57 and NC7SZ58 respectively for the desired logic function. All inputs have been implemented with hysteresis.

The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The input and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 5.5V independent of V_{CC} operating range.

Features

- Space saving SC70-6 lead surface mount package
- Ultra small MicroPak™ leadless package
- Ultra High Speed
- Capable of implementing any 2-input logic function
- Typical usage replaces 2 TinyLogic® gate devices
- Reduces part counts in inventory
- Broad V_{CC} operating range: 1.65V to 5.5V
- Power down high impedance input/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

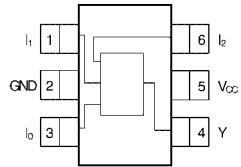
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ57P6X	MAA06A	Z57	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ58P6X	MAA06A	Z58	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ57L6X	MAC06A	KK	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel
NC7SZ58L6X	MAC06A	LL	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

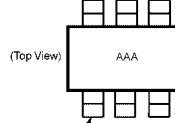
Pin Descriptions

Pin Name	Description
I_0, I_1, I_2	Data Inputs
Y	Output

Connection Diagrams**Pin Assignments for SC70**

(Top View)

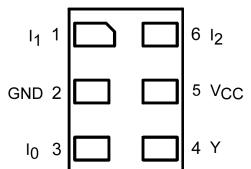
NC7SZ57 and NC7SZ58

Pin One Orientation Diagram

Pin One

AAA = Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right. Pin One is the lower left pin (see diagram).

Pad Assignment for MicroPak

(Top Thru View)

H = HIGH Logic Level

L = LOW Logic Level

Function Selection Table

2-Input Logic Function	Device Selection	Connection Configuration
2-Input AND	NC7SZ57	Figure 1
2-Input AND with inverted input	NC7SZ58	Figures 7, 8
2-Input AND with both inputs inverted	NC7SZ57	Figure 4
2-Input NAND	NC7SZ58	Figure 6
2-Input NAND with inverted input	NC7SZ57	Figures 2, 3
2-Input NAND with both inputs inverted	NC7SZ58	Figure 9
2-Input OR	NC7SZ58	Figure 9
2-Input OR with inverted input	NC7SZ57	Figures 2, 3
2-Input OR with both inputs inverted	NC7SZ58	Figure 6
2-Input NOR	NC7SZ57	Figure 4
2-Input NOR with inverted input	NC7SZ58	Figures 7, 8
2-Input NOR with both inputs inverted	NC7SZ57	Figure 1
2-Input XOR	NC7SZ58	Figure 10
2-Input XNOR	NC7SZ57	Figure 5

Logic Configurations NC7SZ57

Figure 1 through Figure 5 show the logical functions that can be implemented using the NC7SZ57. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

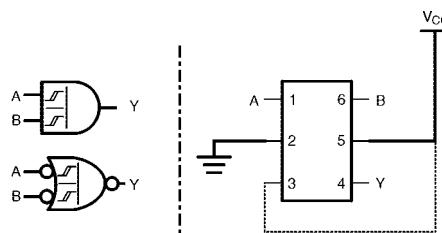


FIGURE 1. 2-Input AND Gate

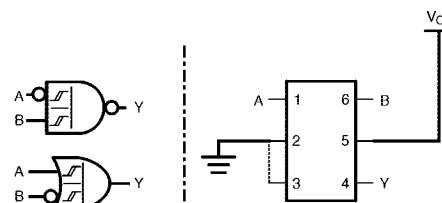


FIGURE 2. 2-Input NAND with Inverted A Input

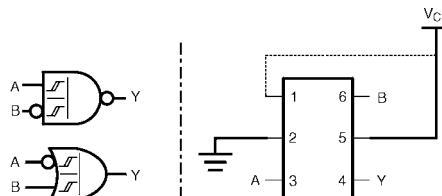


FIGURE 3. 2-Input NAND with Inverted B Input

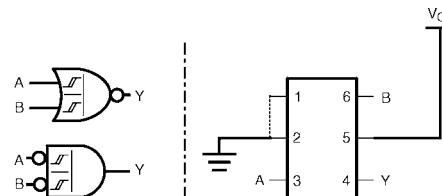


FIGURE 4. 2-Input NOR Gate

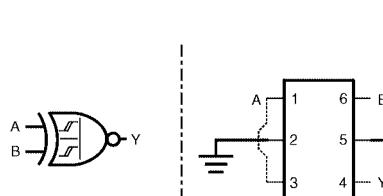


FIGURE 5. 2-Input XNOR Gate

Logic Configurations NC7SZ58

Figure 6 through Figure 10 show the logical functions that can be implemented using the NC7SZ58. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

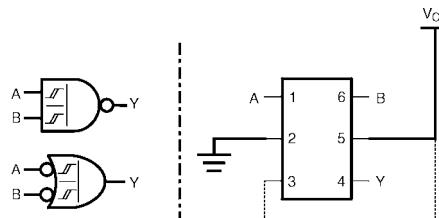


FIGURE 6. 2-Input NAND Gate

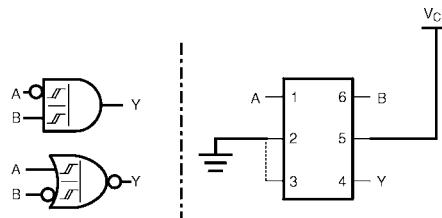


FIGURE 7. 2-Input AND with Inverted A Input

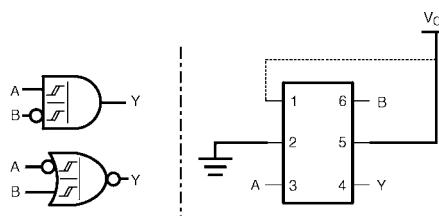


FIGURE 8. 2-Input AND with Inverted B Input

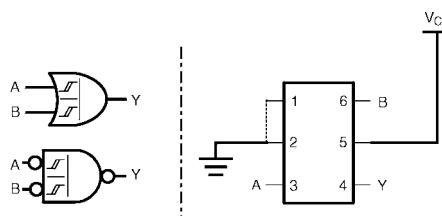


FIGURE 9. 2-Input OR Gate

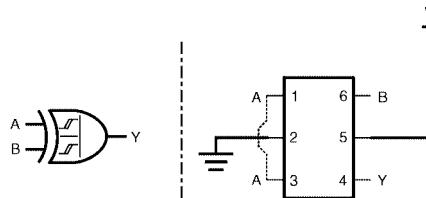


FIGURE 10. 2-Input XOR Gate

Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions												
Supply Voltage (V_{CC})	-0.5V to +7.0V		Supply Voltage Operating (V_{CC})	1.65V to 5.5V											
DC Input Voltage (V_{IN})	-0.5V to +7.0V		Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V											
DC Output Voltage (V_{OUT})	-0.5V to +7.0V		Input Voltage (V_{IN})	0V to 5.5V											
DC Input Diode Current (I_{IK}) @ $V_{IN} \leq 0.5V$	-50 mA		Output Voltage (V_{OUT})	0V to V_{CC}											
DC Output Diode Current (I_{OK}) @ $V_{IN} \leq -0.5V$	-50 mA		Operating Temperature (T_A)	-40°C to +85°C											
DC Output Source/Sink Current (I_{OUT})	±50 mA		Thermal Resistance (θ_{JA})												
DC V_{CC} or Ground Current (I_{CC} / I_{GND})	±50 mA		SC70-6	350°C/W											
Storage Temperature Range (T_{STG})	-65°C to +150°C		Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.												
Max Junction Temperature under Bias (T_J)	150°C														
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C														
Power Dissipation (P_D) @ +85°C	180 mW														
SC70-6															
DC Electrical Characteristics															
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units	Conditions								
			Min	Typ	Max			Min	Max						
V_P	Positive Threshold Voltage	1.65 2.3 3.0 4.5 5.5	0.6 1.0 1.3 1.9 2.2	0.99 1.39 1.77 2.49 2.95	1.4 1.8 2.2 3.1 3.6	V									
	V_N	Negative Threshold Voltage	1.65 2.3 3.0 4.5 5.5	0.2 0.4 0.6 1.0 1.2	0.50 0.75 0.99 1.43 1.70			0.9 1.15 1.5 2.0 2.3							
		V_H	Hysteresis Voltage	1.65 2.3 3.0 4.5 5.5	0.15 0.25 0.4 0.6 0.7			0.48 0.64 0.78 1.06 1.25	0.9 1.1 1.2 1.5 1.7	V					
			V_{OH}	HIGH Level Output Voltage	1.65 2.3 3.0 4.5			1.55 2.2 2.9 4.4	1.65 2.3 3.0 4.5			1.55 2.2 2.9 4.4	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$
					1.65 2.3 3.0 3.0 4.5			1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 3.68 4.20			1.29 1.9 2.4 2.3 3.8			
1.65 2.3 3.0 3.0 4.5					0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -4 mA$ $I_{OH} = -8 mA$ $I_{OH} = -16 mA$ $I_{OH} = -24 mA$ $I_{OH} = -32 mA$						
1.65 2.3 3.0 4.5	0.0 0.0 0.0 0.0				0.10 0.10 0.10 0.10	0.10 0.10 0.10 0.10									
1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55			0.24 0.3 0.4 0.55 0.55										
V_{OL}	LOW Level Output Voltage	1.65 2.3 3.0 4.5	0.0 0.0 0.0 0.0	0.10 0.10 0.10 0.10	0.10 0.10 0.10 0.10	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$							
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55										
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55										
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55										
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55										
	Input Leakage Current	0-5.5	±0.1	±1	μA	$V_{IN} = 5.5V, GND$									

DC Electrical Characteristics (Continued)

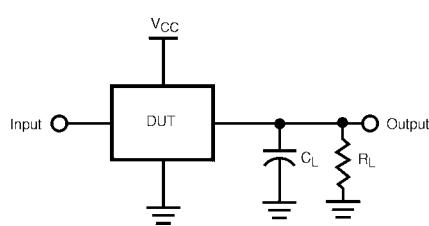
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C			Units	Conditions
			Min	Typ	Max	Min	Max			
I _{OFF}	Power Off Leakage Current	0.0		1		10		μA	V _{IN} or V _{OUT} = 5.5V	
I _{CC}	Quiescent Supply Current	1.65–5.5		1		10		μA	V _{IN} = 5.5V, GND	

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C			Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max				
t _{PLH}	Propagation Delay I _n to Y	1.8 ± 0.15	3.0	8	14.0	3.0	14.5	ns	C _L = 15 pF R _L = 1 MΩ	Figures 11, 13	
		2.5 ± 0.2	1.5	4.9	8.0	1.5	8.5				
		3.3 ± 0.3	1.2	3.7	5.3	1.2	5.7				
		5.0 ± 0.5	0.8	2.8	4.3	0.8	4.6				
t _{PLH}	Propagation Delay I _n to Y	3.3 ± 0.3	1.5	4.2	6.0	1.5	6.5	ns	C _L = 50 pF R _L = 500 Ω	Figures 11, 13	
		5.0 ± 0.5	1.0	3.4	4.9	1.0	5.3				
C _{IN}	Input Capacitance	0		2				pF			
C _{PD}	Power Dissipation Capacitance	3.3		14				pF	(Note 2)	Figure 12	
		5.0		17							

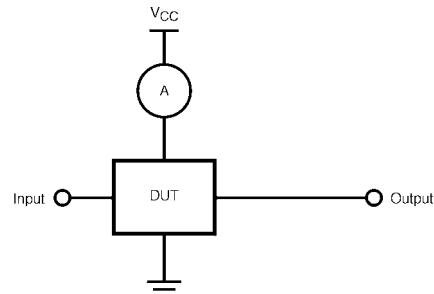
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 12) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$$I_{CCD} = (C_{PD})(V_{CC})(f_{in}) + (I_{CC\text{static}})$$

AC Loading and Waveforms

C_L includes load and stray Capacitance
Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 11. AC Test Circuit



Input = AC Waveforms
PRR = Variable; Duty Cycle = 50%

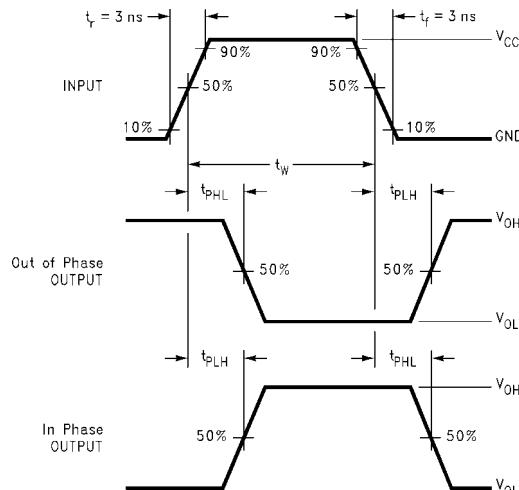
FIGURE 12. I_{CCD} Test Circuit

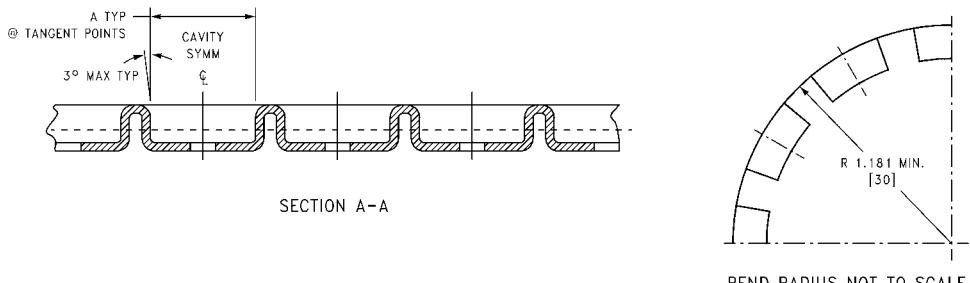
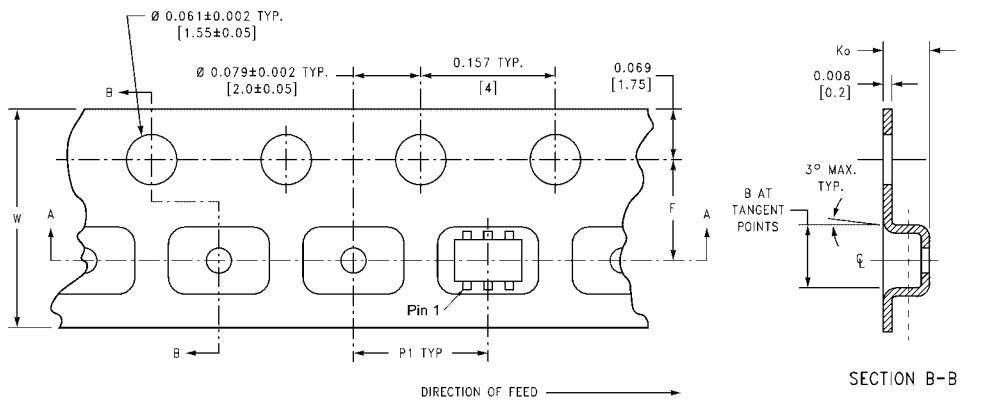
FIGURE 13. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

Tape and Reel Specification (Continued)
TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

SECTION B-B
SCALE:10X

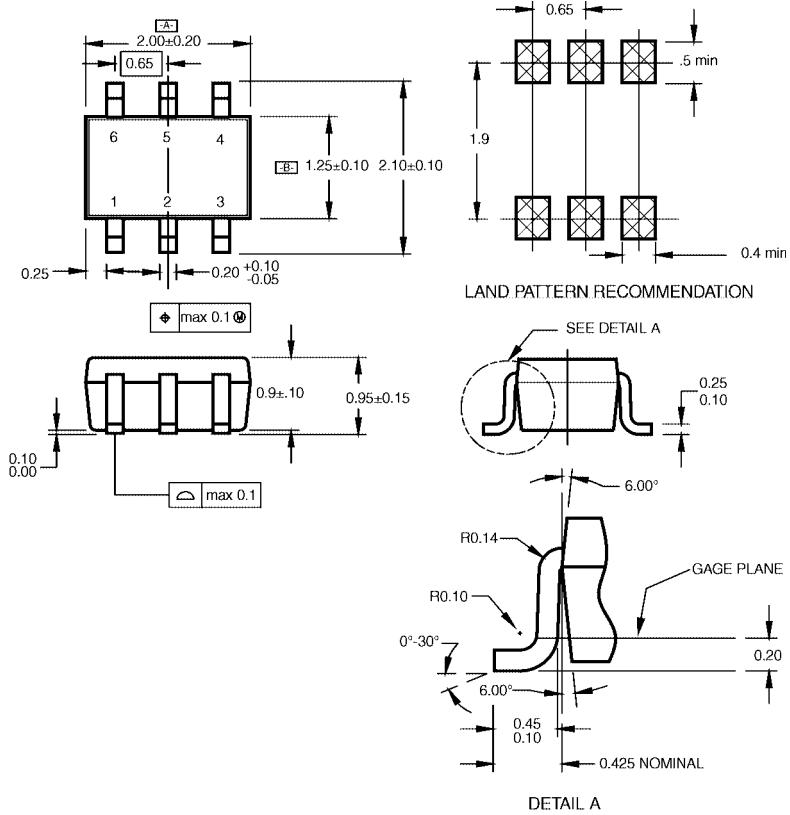
SECTION A-A
SCALE:10X

REEL DIMENSIONS inches (millimeters)

DETAIL X

DETAIL X
SCALE: 3X

Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

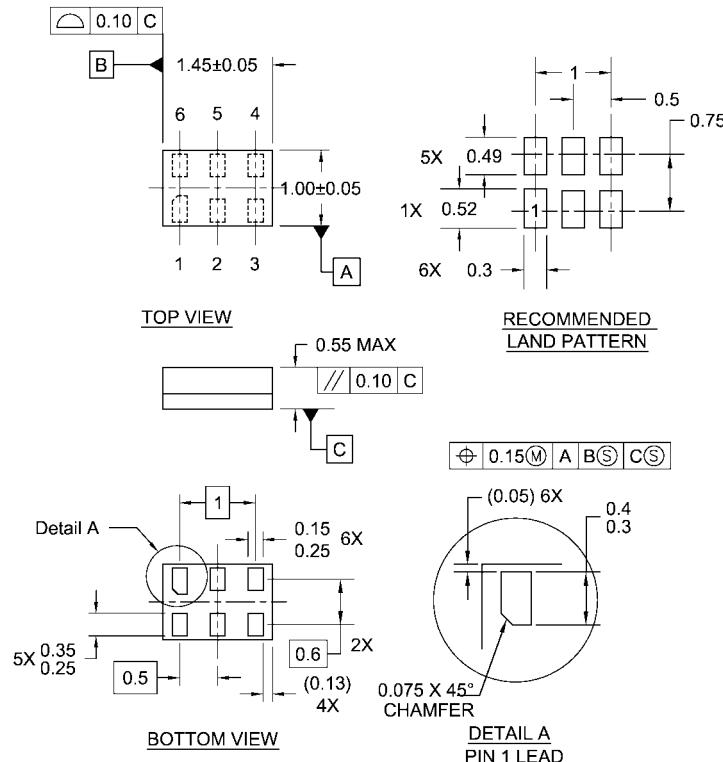
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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