Product Flyer

June 2000

MB86060

Version 1.2

16-Bit Interpolating Digital to Analog Converter

FME/MS/SFDAC1/FL_1/4270

The Fujitsu MB86060 is a high performance 12-bit, 400MSa/s Digital to Analog Converter (DAC) enhanced with a 16-bit interpolation filtering front-end. Use of novel techniques for the converter architecture delivers high speed operation consistent with BiCMOS or bipolar devices but at the low power of CMOS. Fujitsu's proprietary architecture is the subject of several patent applications. Additional versatility is provided by selectable input interpolation filters, programmable dither and noise shaping facilities. Excellent SFDR performance coupled with high speed conversion rate and low power make this device particularly suitable for high performance communication systems, in particular direct IF synthesis applications.

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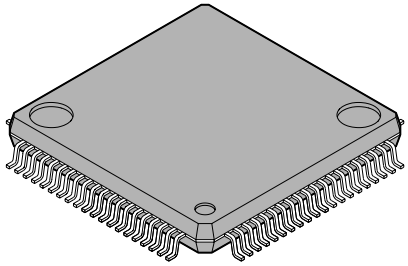
LQFP-80



(FPT-80P-M05)

Features

- 16-bit Interpolating Digital to Analog conversion
- x1, x2 or x4 interpolation filtering
- 100MSa/s input, with x4 interpolation enabled
- Programmable highpass filtered dither
- Selectable 2nd order noise shaping
- Versatile CMOS digital interface
- Internal programmable clock multiplier
- Low power, 3.3V operation (343mW @32MSa/s input, x4)
- Performance enhanced pinout with on-chip decoupling
- 0.35µm CMOS technology with Triple Well
- Industrial temperature range (-40°C to +85°C)

Applications

- Direct IF Synthesis
- Cellular basestations
- Wide-band communications systems

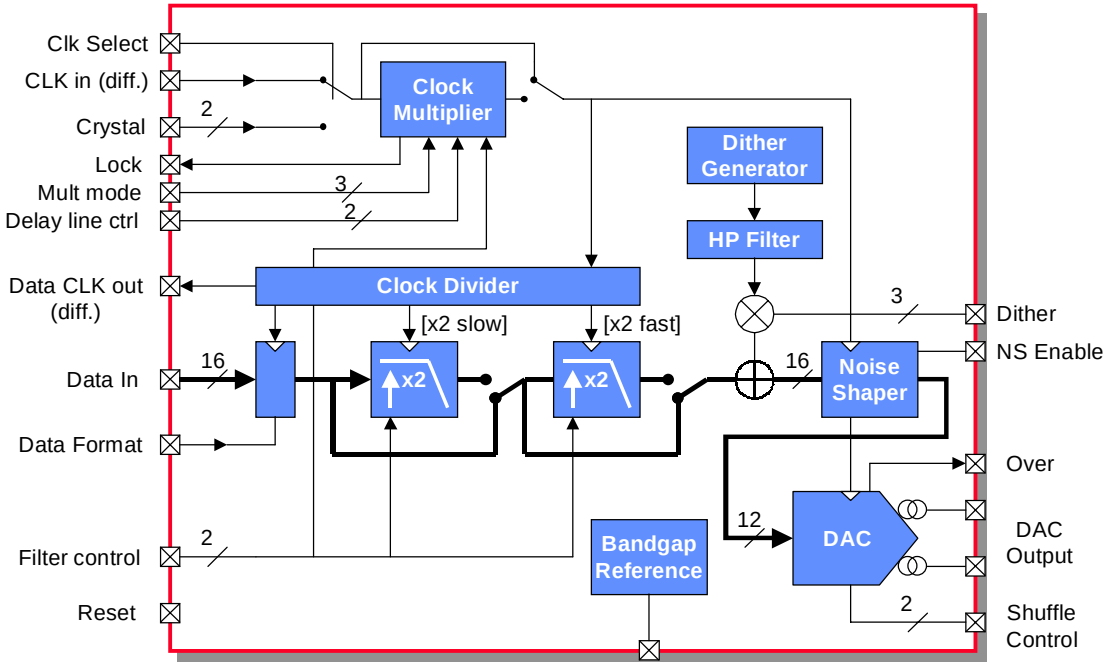
Ordering Information

Part	Order Number
MB86060 Datasheet	Contact Sales
MB86060 DAC	MB86060PFV
MB86060 Development Kit	DK86060-3
MB86060 Development Kit User Manual	Contact Sales

Functional Description

The MB86060 integrates a 12-bit 400MSa/s DAC with selectable front end processing to provide input interpolation filtering, dither and noise shaping. Versatile interfacing via the 16-bit parallel CMOS data input allows different system requirements to be accommodated, with either offset binary or 2's complement data formats selected by an input format control.

The device is manufactured in a 0.35µm advanced CMOS process with Triple Well extension giving improved isolation between analog blocks and digital-analog.



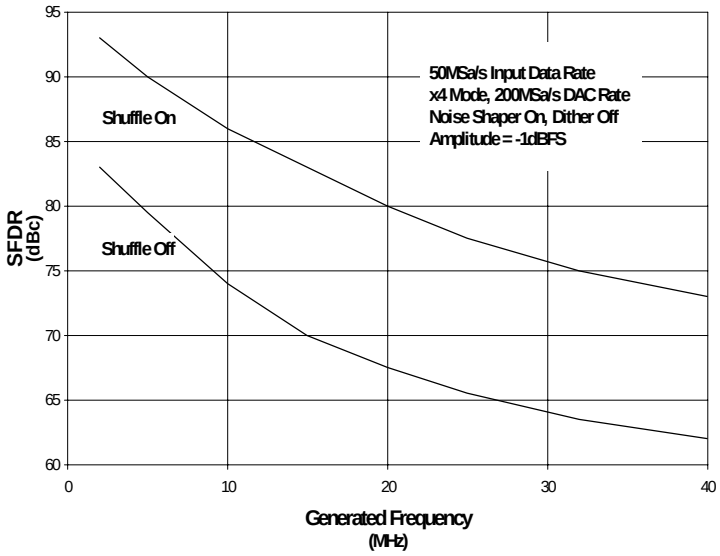
MB86060 Functional Block Diagram

Converter Architecture

The MB86060 Interpolating DAC incorporates a number of novel design aspects that are subject to patent applications. Key to its operation are the current sources where segmented, common centroid, interleaved techniques for the most significant bits, as well as load matching ensure good linearity and low distortion to at least the 12-bit level. In the switch elements tracking capacitance is minimised to improve settling, while controlled rise and fall times improve SFDR performance. Finally the digital decoding uses a 3-dimensional addressing approach to minimise propagation delays from latch to element.

Segment Shuffling

The DAC core incorporates a proprietary segment shuffling capability which is provided to further improve linearity, and hence improve SFDR. This feature reduces any signal level dependent effects on linearity as the same code can be generated by the same number of MSB cells but taken from any quarter of the MSB segments. Segment shuffling can be selected to operate every 4, 8 or 16 updates of the DAC output using a random shuffle sequence between the four segments. Most performance improvement will be observed when the device is used in one of the interpolating modes. The effect of segment shuffling is to produce a spread noise spectrum, raising the overall noise floor, but reducing the distortion. For minimum distortion when generating low frequency signals, it is recommended that the shuffling clock rate is no more than 25MHz (DAC Rate / Segment Shuffling setting). However, low shuffle clock rates give reduced spreading out of distortion components.



Single Tone SFDR Performance

Noise Shaping

Second order noise shaping can be applied to interpolated data prior to being passed to the DAC core. When enabled this provides an additional reduction in quantisation noise to that gained through the use of interpolation filtering. For the x4 interpolation mode this improvement will be 16dB, equivalent to 2.7 bits.

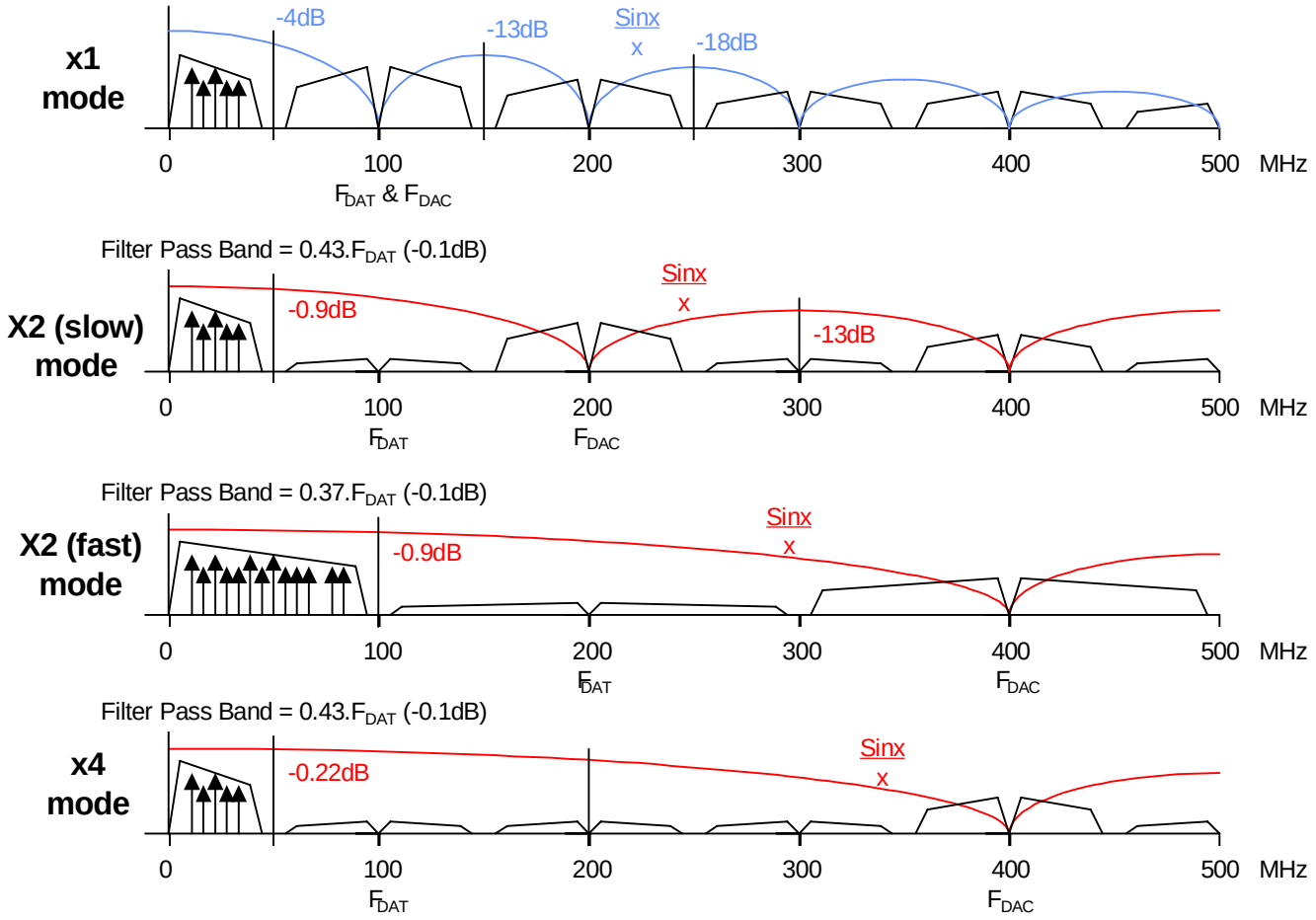
Clock

The MB86060 incorporates a clock multiplier to generate the required internal x1, x2 and x4 clock signals from an external reference. The clock multiplier is based on a delay-lock-loop whose delay is adjusted by a charge pump controlled by a phase detector. A 'Lock' indicator is provided so that the system can monitor the multiplier's condition. For systems where a high frequency clock is available, or the lowest possible jitter is required, then the clock multiplier may be disabled and the external clock used directly.

Interpolating Filters

The integration of interpolating filters provides a number of benefits to the system implementation. In general, improved performance can be gained by using a higher DAC conversion rate effectively providing a higher level of oversampling from the generated signal. For the designer, the problem with this approach is generating the required high speed digital data, especially when considering high performance wide-band designs with up to 50MHz of signal. Integrating this processing on-chip with the DAC alleviates this problem.

Other benefits include a reduced effect due to the sinx/x roll-off due to the DAC sample and hold output stage, which for a conventional DAC represents -4dB at Nyquist, compared to only -0.22dB when operating in the x4 interpolating mode. Also the digital interpolation filters sharp cutoff and effective stop-band attentuation improves both in and out-of-band SFDR. This is illustrated below.



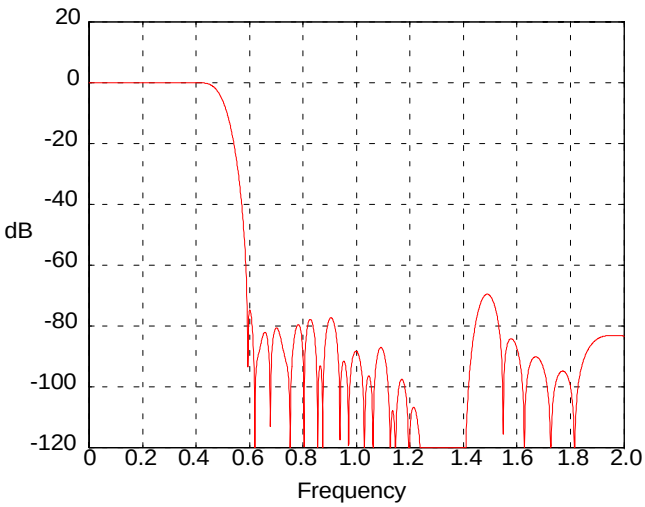
The MB86060 features four interpolation filter modes x1, x2(slow), x2(fast) and x4. Mode x1 is as per a conventional DAC, and choosing between the remaining three modes would depend on the system requirements. Mode x2(slow) may be advantageous to a system requiring the benefits of interpolation filtering but saving some power by not running the DAC core at full rate. Mode x2(fast) gives access to the wider band, slower roll-off interpolation filter allowing wider band signals to be generated compared to the other modes, for example 74MHz (-0.1dB) for 200MSa/s data rate. Mode x4 for the complete interpolation filter operation.

Interpolation Filter Response

Pass Band 0.43fs (-0.1dB)
Stop Band -75dBFS from 0.59Fs -
(Excluding transition band image around 1.5Fs)

[Frequency axis normalised to input data rate]

[Simulated overall x 4 Interpolation filter response]



Combined Filter Characteristics

Programmable Dither

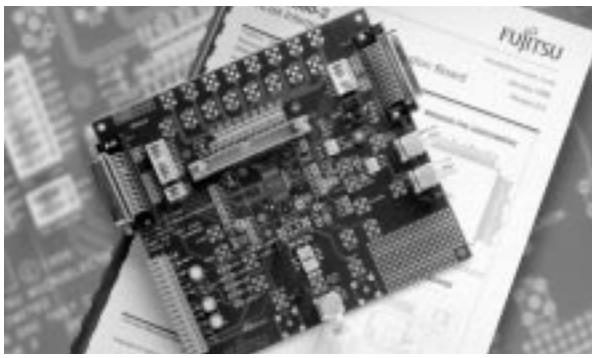
Dither can be added to improve low-level performance and reduce effects due to nonlinearities within the DAC, and reducing DNL and glitch energy. The dither has programmable amplitude, and is high pass filtered to fall out of the pass band.

For dither to be used effectively both amplitude and frequency characteristics must be carefully considered. Obviously the dither amplitude should be larger than the nonlinearities to be masked, but levels significantly larger than this will ultimately limit available dynamic range for the wanted signal. Similar considerations should be made for the frequency characteristics, which in the MB86060 the dither is highpass filtered such that the majority of the energy is concentrated at Nyquist of the DAC output rate.

Development Kit

A development kit, reference DK86060, is available for the MB86060 16-bit Interpolating DAC. The kit includes an evaluation board that enables simple and effective evaluation of the device.

The board provides a complete evaluation environment for the DAC. A transformer coupled differential output interface is provided to simplify integration into target applications and development environments. An RF clock source can be connected via the transformer coupled input, and 16-bit data via a 40-way IDC header.



The development kit includes,

- Evaluation board with MB86060 device fitted
- Spare MB86060 for customer development
- User Manual

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