

Octal buffer/line driver with 5-volt tolerant inputs/outputs; 3-state; inverting

74LVC240A 74LVCH240A

FEATURES

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0$ V
- Bushold on all data inputs (LVCH240A only).

DESCRIPTION

The 74LVC(H)240A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)240A is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{1OE}$ and $\overline{2OE}$. A HIGH on $\overline{nOE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The '240' is identical to the '244' but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	$C_L = 50$ pF $V_{CC} = 3.3$ V	3.8	ns
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)240AD	20	SO	plastic	SOT163-1
74LVC(H)240ADB	20	SSOP	plastic	SOT339-1
74LVC(H)240APW	20	TSSOP	plastic	SOT360-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$\overline{2OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

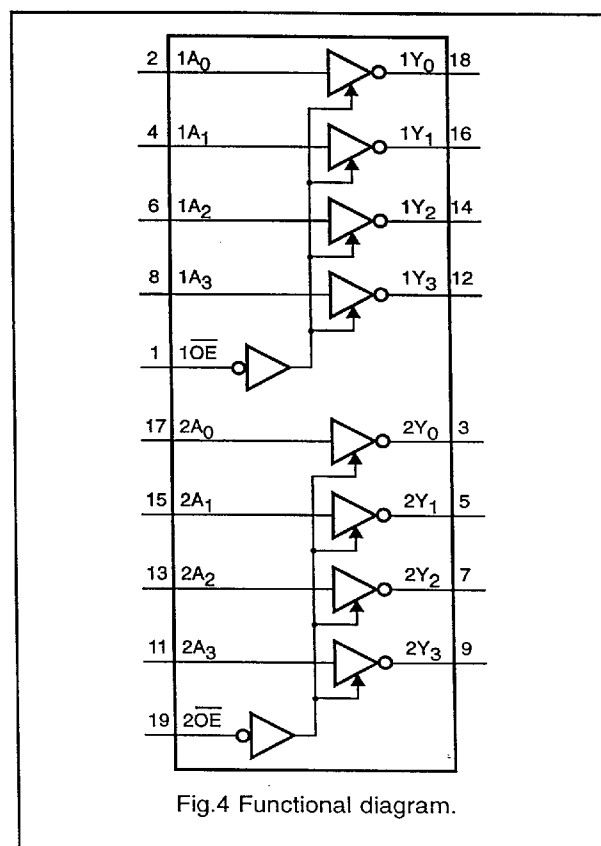
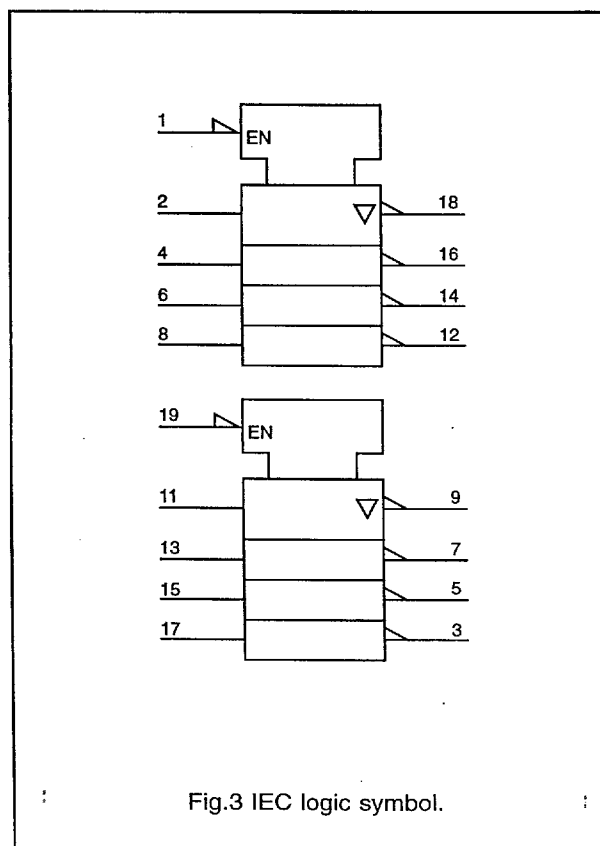
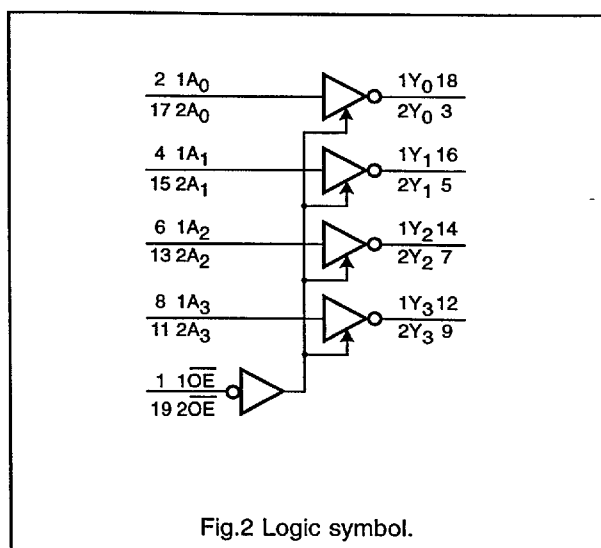
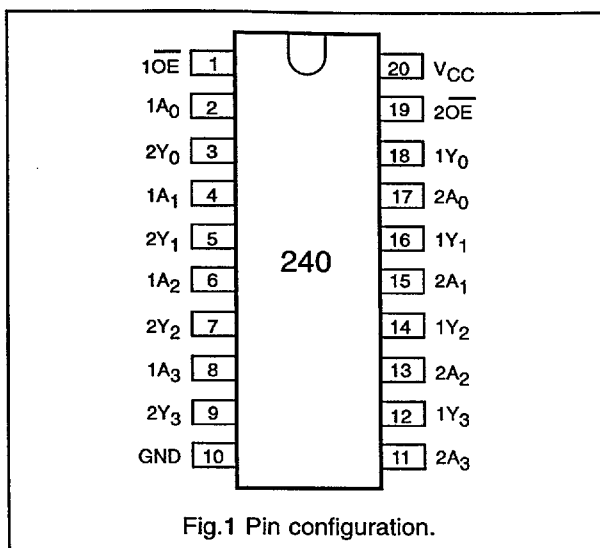
FUNCTION TABLE

INPUTS		OUTPUT
$\overline{nOE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74LVC(H)240A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)240A

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V _{CC} (V)	WAVEFORMS
t _{PHL} /t _{PLH}	propagation delay	—	—	—	ns	1.2	Figs 5, 7
	1A _n to 1Y _n ;	1.5	—	7.5		2.7	
	2A _n to 2Y _n	1.5	—	6.5		3.0 to 3.6	
t _{PZH} /t _{PZL}	3-state output enable time	—	—	—	ns	1.2	Figs 6, 7
	1OE to 1Y _n ;	1.5	—	9.0		2.7	
	2OE to 2Y _n	1.5	—	8.0		3.0 to 3.6	
t _{PHZ} /t _{PLZ}	3-state output disable time	—	—	—	ns	1.2	Figs 6, 7
	1OE to 1Y _n ;	1.5	—	8.0		2.7	
	2OE to 2Y _n	1.5	—	7.0		3.0 to 3.6	

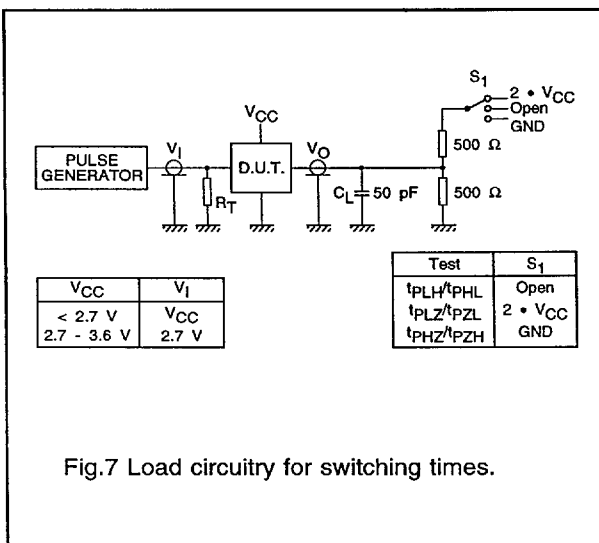
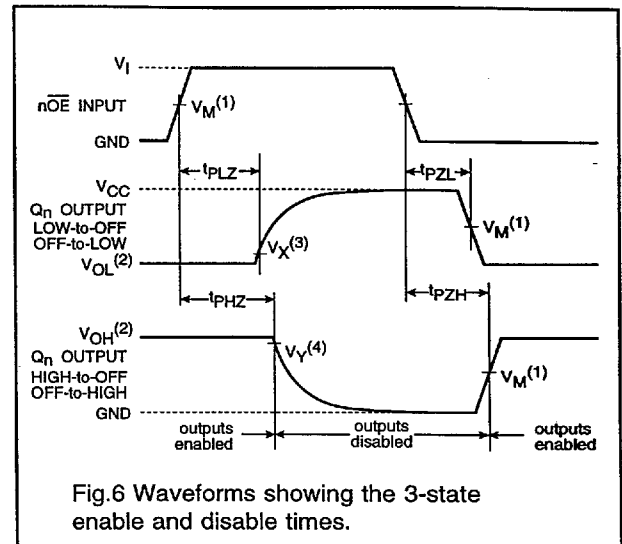
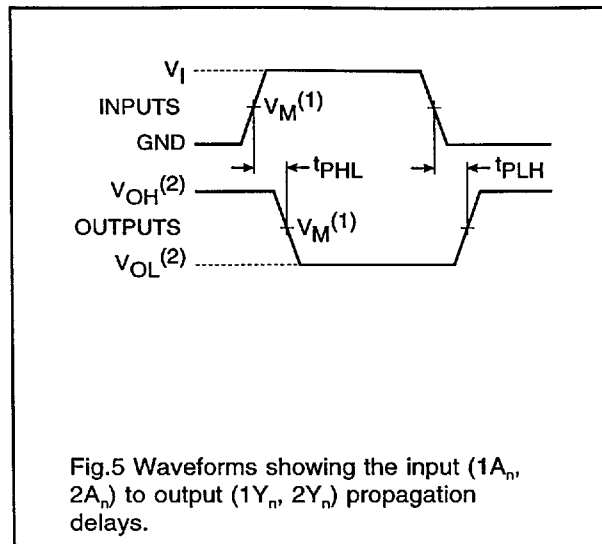
Notes: All typical values are measured at T_{amb} = 25 °C.

* Typical values are measured at V_{CC} = 3.3 V.

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AC WAVEFORMS



- Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 (3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 (4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V