ICL7660, ICL7660A

November 1995

CMOS Voltage Converters

Features

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication (V_{OUT} = (-) nV_{IN})**
- **Typical Open Circuit Voltage Conversion Efficiency 99.9%**
- **Typical Power Efficiency 98%**
- **Wide Operating Voltage Range**
  - **ICL7660 . . . . . 1.5V to 10.0V**
  - **ICL7660A . . . . . 1.5V to 12.0V**
- **ICL7660A 100% Tested at 3V**
- **Easy to Use - Requires Only 2 External Non-Critical Passive Components**
- **No External Diode Over Full Temp. and Voltage Range**

Applications

- **On Board Negative Supply for Dynamic RAMs**
- **Localized μProcessor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**

Ordering Information

PART NUMBER	TEMP RANGE	PACKAGE
ICL7660CTV	0°C to +70°C	8 Pin Metal Can
ICL7660CBA	0°C to +70°C	8 Lead Plastic SOIC (N)
ICL7660CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660MTV (Note)	0°C to +70°C	8 Pin Metal Can
ICL7660ACBA	0°C to +70°C	8 Lead Plastic SOIC (N)
ICL7660ACBAT	0°C to +70°C	8 Lead Plastic SOIC (N) Tape and Reel
ICL7660ACPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660AIBA	-40°C to +85°C	8 Lead Plastic SOIC (N)
ICL7660AIBAT	0°C to +85°C	8 Lead Plastic SOIC (N) Tape and Reel
ICL7660AIPA	-40°C to +85°C	8 Lead Plastic DIP

NOTE: Add /883B to part number if 883B processing is required.

Description

The Harris ICL7660 and ICL7660A are monolithic CMOS power supply circuits which offer unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of -1.5V to -10.0V and the ICL7660A does the same conversions with an input range of +1.5V to +12.0V resulting in complementary output voltages of -1.5V to -12.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 and ICL7660A can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input.

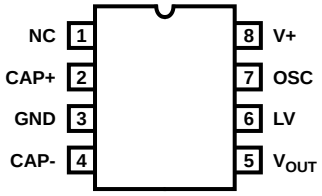
Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

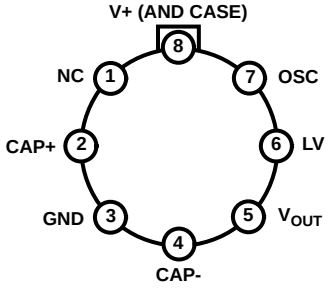
The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the ICL7660 and +3.5V to +12.0V for the ICL7660A), the LV pin is left floating to prevent device latchup.

Pinouts

ICL7660, ICL7660A (PDIP, SOIC)
TOP VIEW



ICL7660 (CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3072.2**

Absolute Maximum Ratings

Supply Voltage
- ICL7660 . . . . . +10.5V
- ICL7660A . . . . . +13.0V

LV and OSC Input Voltage . . . . . -0.3V to (V+ +0.3V) for V+ < 5.5V
(Note 1) (V+ -5.5V) to (V+ +0.3V) for V+ > 5.5V
Current into LV (Note 1) . . . . . 20µA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) . . . . . Continuous

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	170°C/W	-
Metal Can Package (ICL7660 Only)	156°C/W	68°C/W

Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
- ICL7660M . . . . . -55°C to +125°C
- ICL7660C . . . . . 0°C to +70°C
- ICL7660AI . . . . . -40°C to +85°C
- ICL7660AC . . . . . 0°C to +70°C

Electrical Specifications

ICL7660 and ICL7660A, $V^+ = 5V$, $T_A = +25°C$, $C_{OSC} = 0$, Test Circuit Figure 11 Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$	-	170	500	-	80	165	µA
Supply Voltage Range - Lo	V_L+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GND	1.5	-	3.5	1.5	-	3.5	V
Supply Voltage Range - Hi	V_H+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to Open	3.0	-	10.0	3	-	12	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA, $T_A = +25°C$	-	55	100	-	60	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C	-	-	120	-	-	120	Ω
		I_{OUT} = 20mA, -55°C ≤ T_A ≤ +125°C	-	-	150	-	-	-	Ω
		I_{OUT} = 20mA, -40°C ≤ T_A ≤ +85°C	-	-	-	-	-	120	Ω
		$V^+ = 2V$, I_{OUT} = 3mA, LV to GND 0°C ≤ T_A ≤ +70°C	-	-	300	-	-	300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GND, -55°C ≤ T_A ≤ +125°C	-	-	400	-	-	-	Ω
Oscillator Frequency	f_{OSC}		-	10	-	-	10	-	kHz
Power Efficiency	P_{EF}	R_L = 5kΩ	95	98	-	96	98	-	%
Voltage Conversion Efficiency	$V_{OUT\ EF}$	$R_L = \infty$	97	99.9	-	99	99.9	-	%
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1.0	-	-	1	-	MΩ
		V = 5V	-	100	-	-	-	-	kΩ
ICL7660A, V+ = 3V, $T_A = +25°C$, OSC = Free running, Test Circuit Figure 11, Unless Otherwise Specified									
Supply Current (Note 3)	I+	V+ = 3V, $R_L = \infty$, +25°C	-	-	-	-	26	100	µA
		0°C < T_A < +70°C	-	-	-	-	-	125	µA
		-40°C < T_A < +85°C	-	-	-	-	-	125	µA
Output Source Resistance	R_{OUT}	V+ = 3V, I_{OUT} = 10mA	-	-	-	-	97	150	Ω
		0°C < T_A < +70°C	-	-	-	-	-	200	Ω
		-40°C < T_A < +85°C	-	-	-	-	-	200	Ω

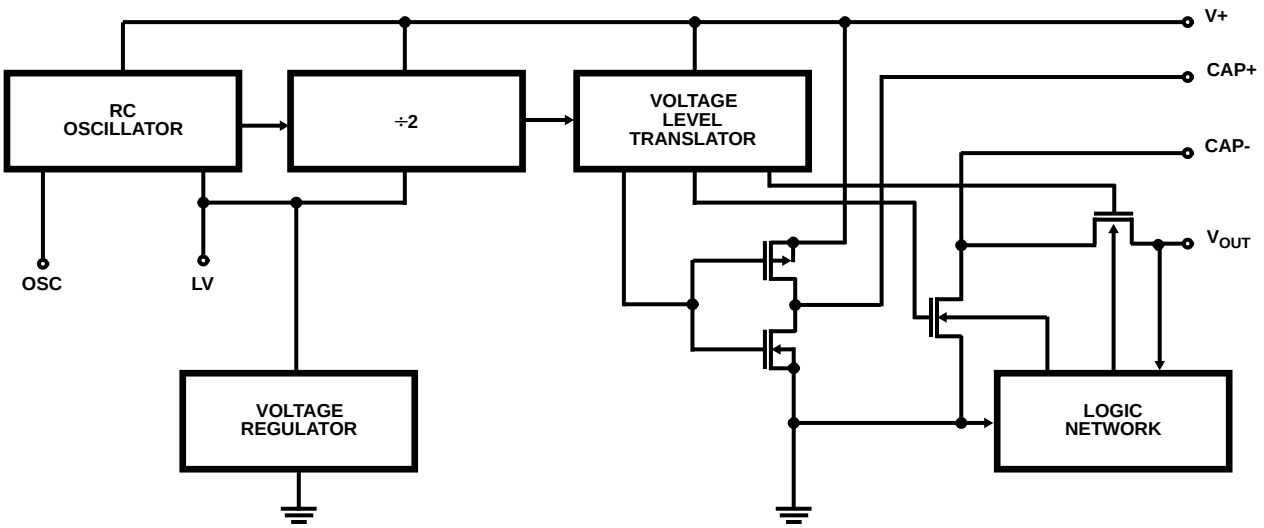
Electrical Specifications ICL7660 and ICL7660A, V^+ = 5V, T_A = +25°C, C_{OSC} = 0, Test Circuit Figure 11 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Frequency (Note 3)	f_{OSC}	V+ = 3V (same as 5V conditions)	-	-	-	5.0	8	-	kHz
		$0^oC < T_A < +70^oC$	-	-	-	3.0	-	-	kHz
		$-40^oC < T_A < +85^oC$	-	-	-	3.0	-	-	kHz
Voltage Conversion Efficiency	$V_{OUT}EFF$	V+ = 3V, $R_L = \infty$	-	-	-	99	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	99	-	-	%
Power Efficiency	P_{EFF}	V+ = 3V, R_L = 5kΩ	-	-	-	96	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	95	-	-	%

NOTE:

1. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the ICL7660, ICL7660A.
2. Derate linearly above $+50^oC$ by 5.5mW/°C
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The Harris ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

Functional Block Diagram



Typical Performance Curves (Test Circuit of Figure 11)

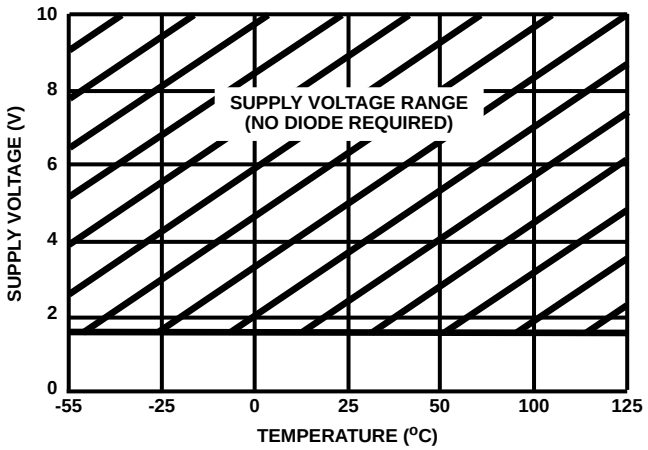


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

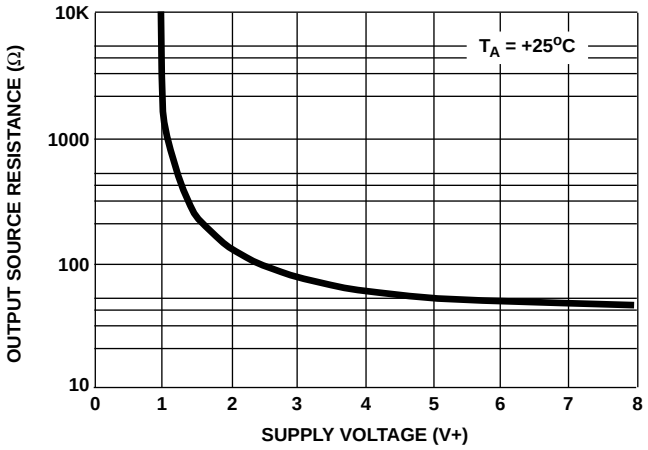


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

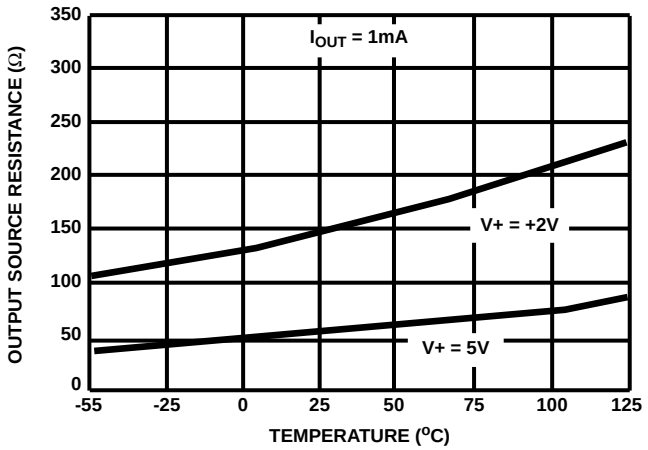


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

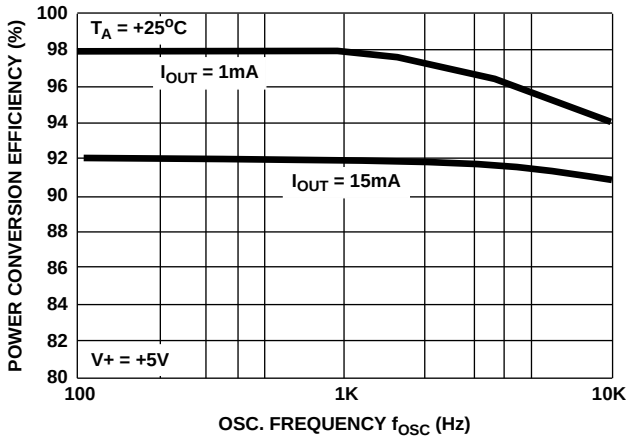


FIGURE 4. POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY

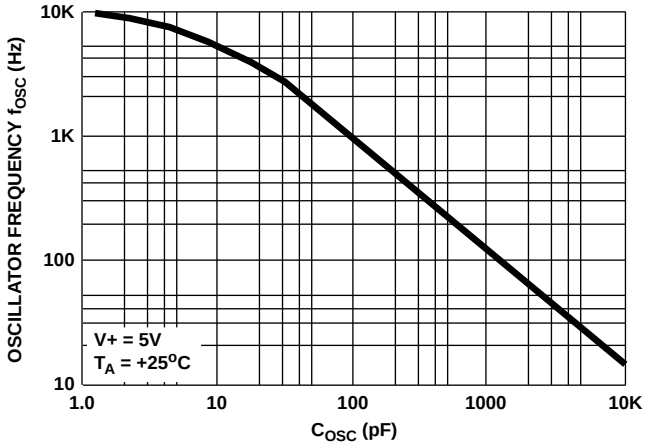


FIGURE 5. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

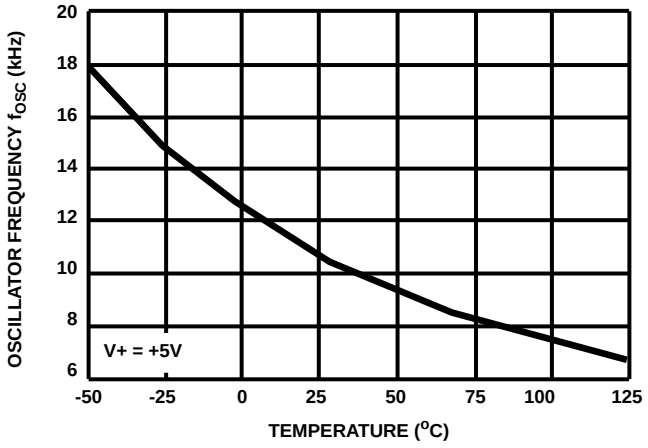


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

Typical Performance Curves (Test Circuit of Figure 11) (Continued)

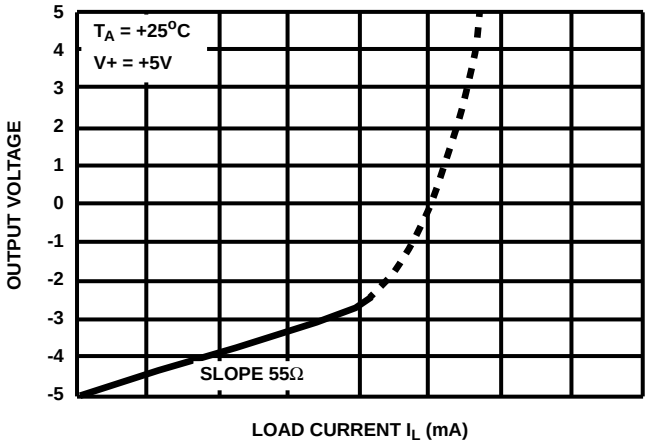


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

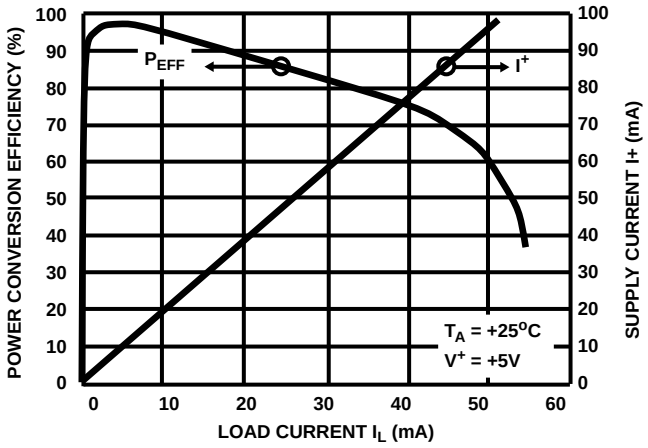


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS AFUNCTION OF LOAD CURRENT

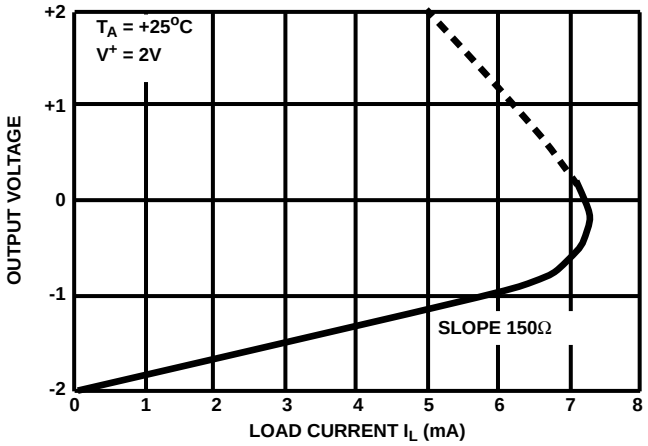


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

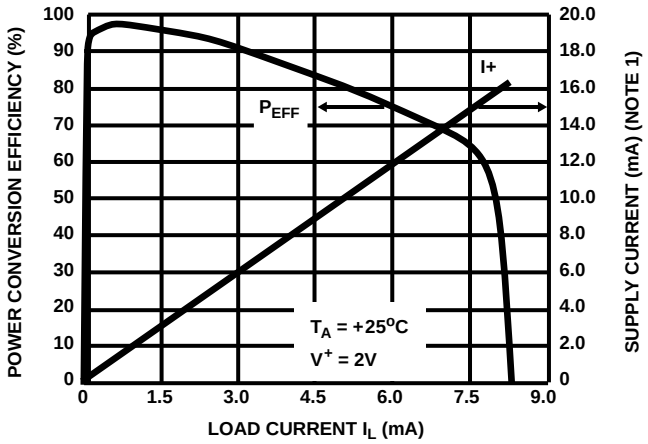
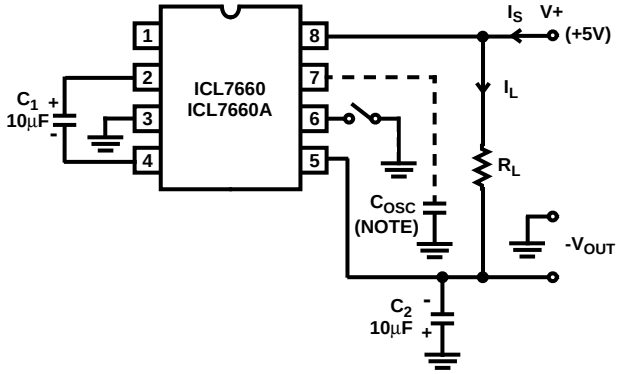


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

NOTE 1. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660/ICL7660A, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C2 should be increased to 100µF.

FIGURE 11. ICL7660, ICL7660A TEST CIRCUIT

Detailed Description

The ICL7660 and ICL7660A contain all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 12, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660 and ICL7660A, the 4 switches of Figure 12 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON” resistances. In addition, at circuit start-up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 and ICL7660A by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 and ICL7660A is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the “LV” pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

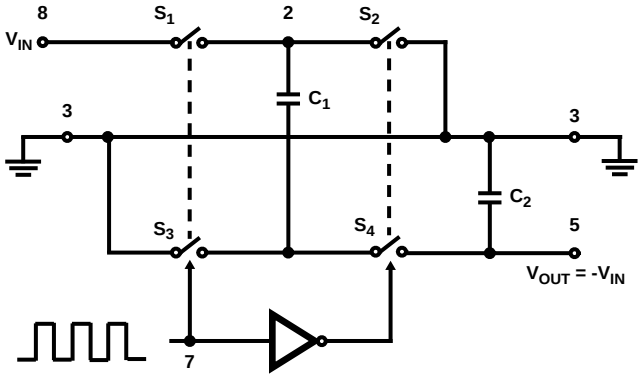


FIGURE 12. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met.

A The driver circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 and ICL7660A approach these conditions for negative voltage conversion if large values of C_1 and C_2 are used.

ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 12) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do’s And Don’ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and ICL7660A and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the ICL7660 and ICL7660A has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

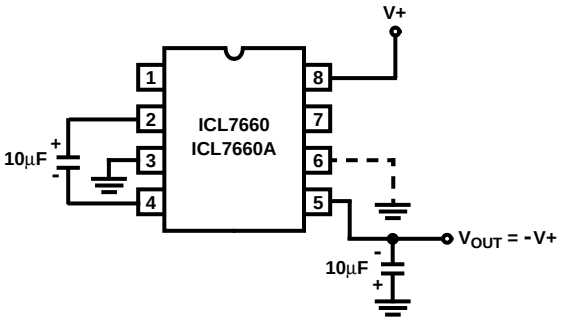


FIGURE 13A. CONFIGURATION

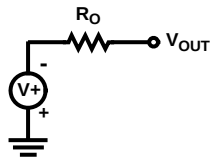


FIGURE 13B. THEVENIN EQUIVALENT

FIGURE 13. SIMPLE NEGATIVE CONVERTER

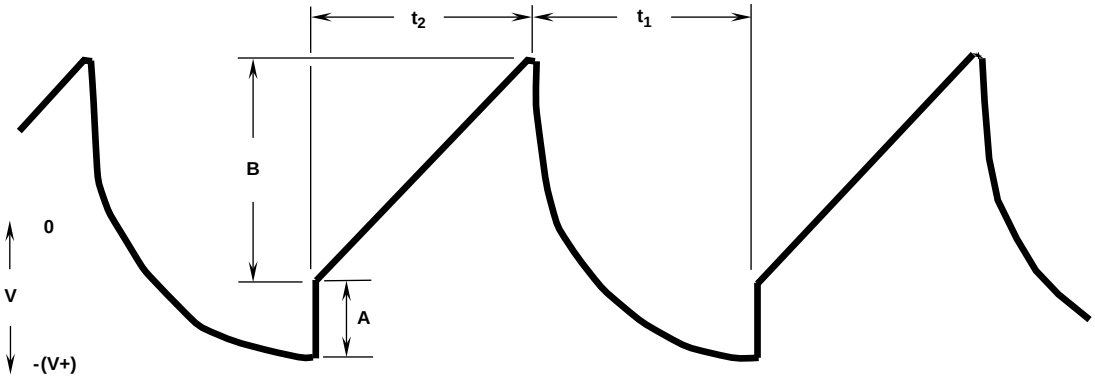


FIGURE 14. OUTPUT RIPPLE

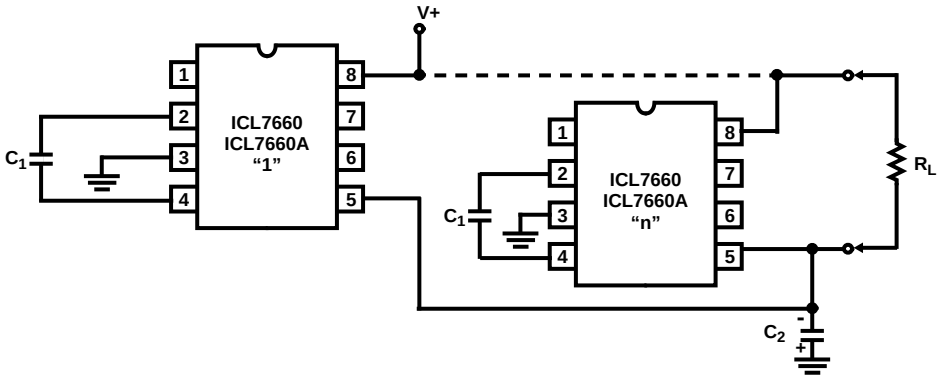


FIGURE 15. PARALLELING DEVICES

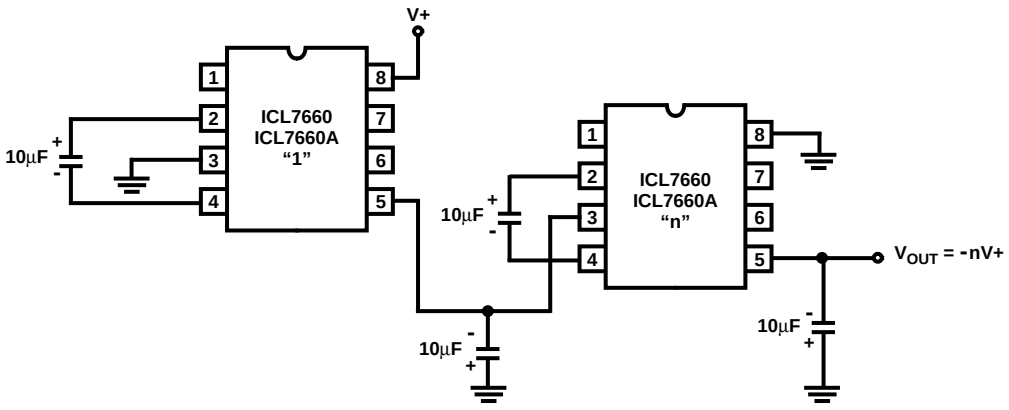


FIGURE 16. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 and ICL7660A for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 13A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 13B. The voltage source has a value of -V+. The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 12), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{(f_{PUMP})\,(C1)} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O \cong 2(R_{SW}) + \frac{1}{(f_{PUMP})\,(C1)} + 4(ESR_{C1}) + ESR_{C2}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \bullet C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \bullet C1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2(23) + \frac{1}{(5 \bullet 10^3)\,(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_O \cong 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

$$R_O \cong 2(23) + \frac{1}{(5 \bullet 10^3)\,(10\text{-}5)} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_{O/} \cong 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 14. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flow into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is $2\bullet I_{OUT}$, hence the total drop is $2\bullet I_{OUT} \bullet eSR_{C2}V$. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is $I_{OUT} \bullet t2/C_2V$. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left[\frac{1}{2\,(f_{PUMP})\,(C2)} + 2\,(ESR_{C2})\right] I_{OUT}$$

Again, a low ESR capacitor will reset in a higher performance output.

Paralleling Devices

Any number of ICL7660 and ICL7660A voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660/ICL7660A})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7660 and ICL7660A may be cascaded as shown to produced larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 and ICL7660A R_{OUT} values.

Changing the ICL7660/ICL7660A Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 17. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

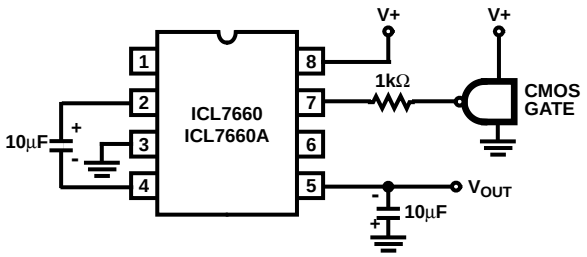


FIGURE 17. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660 and ICL7660A at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 18. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

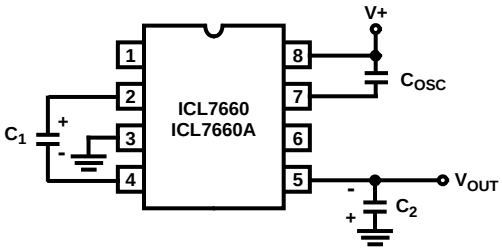


FIGURE 18. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660 and ICL7660A may be employed to achieve positive voltage doubling using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 and ICL7660A are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.

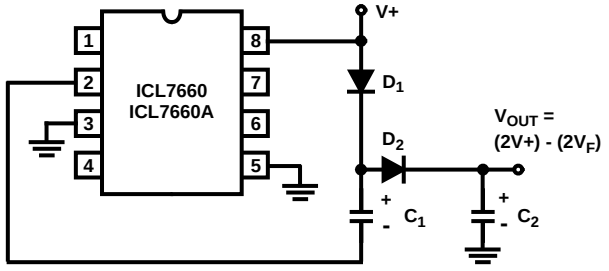


FIGURE 19. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 20 combines the functions shown in Figures 13 and Figure 19 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

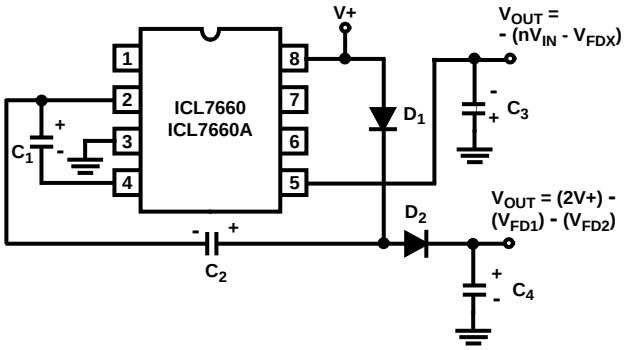


FIGURE 20. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 21. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 16, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).

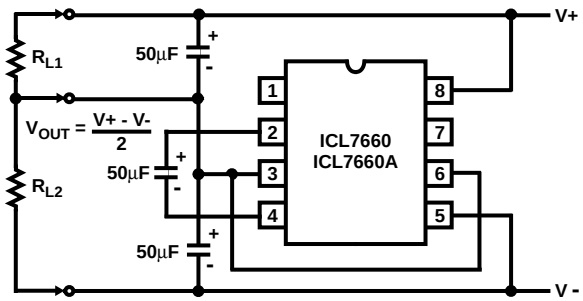


FIGURE 21. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 and ICL7660A can be a problem, particularly if the load current varies substantially. The circuit of Figure 22 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660s and ICL7660As output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660 and ICL7660A, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

Other Applications

Further information on the operation and use of the ICL7660 and ICL7660A may be found in A051 “Principals and Applications of the ICL7660 and ICL7660A CMOS Voltage Converter”.

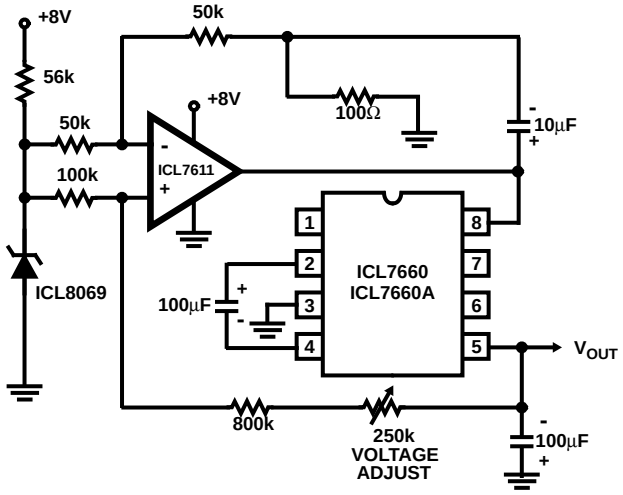


FIGURE 22. REGULATING THE OUTPUT VOLTAGE

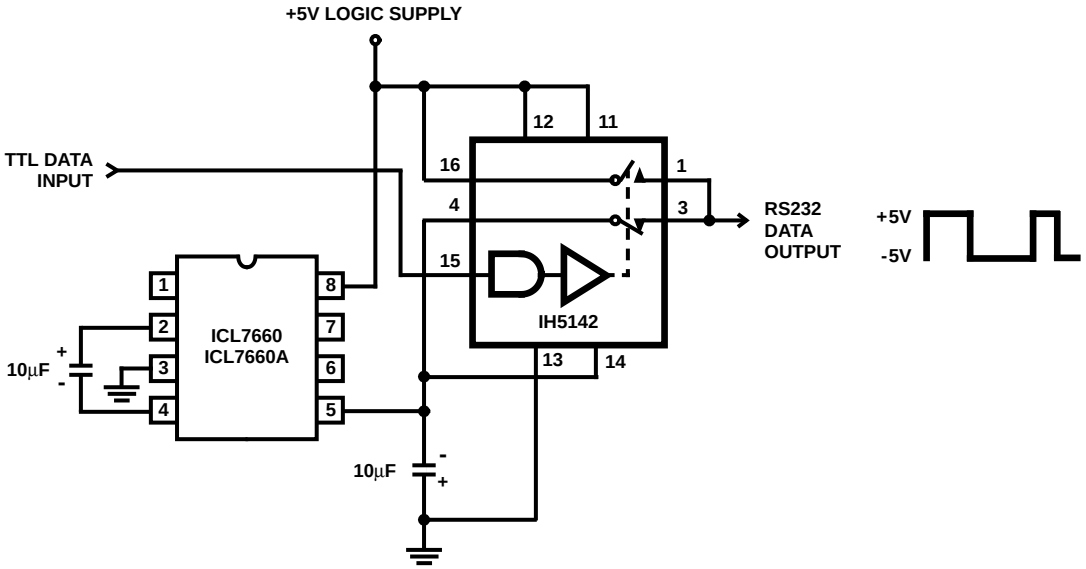
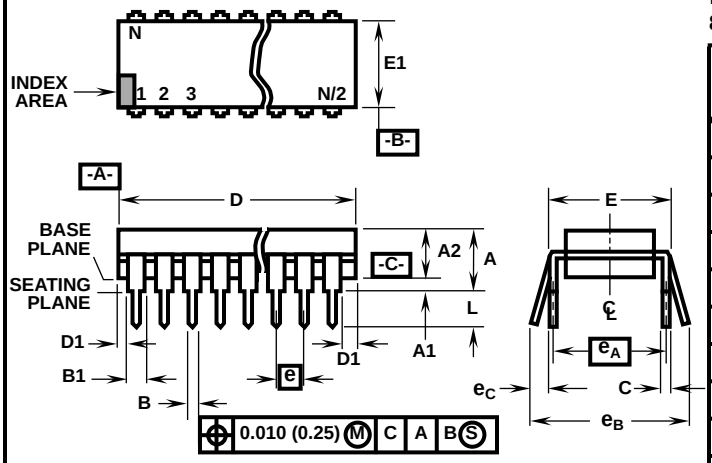


FIGURE 23. RS232 LEVELS FROM A SINGLE 5V SUPPLY

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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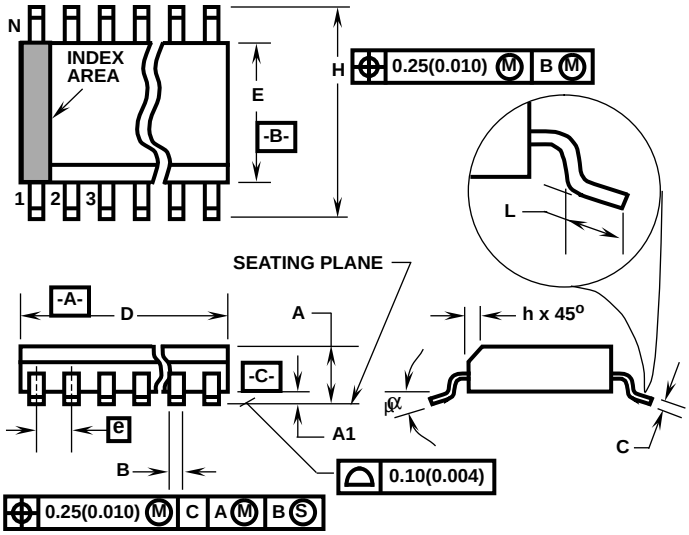
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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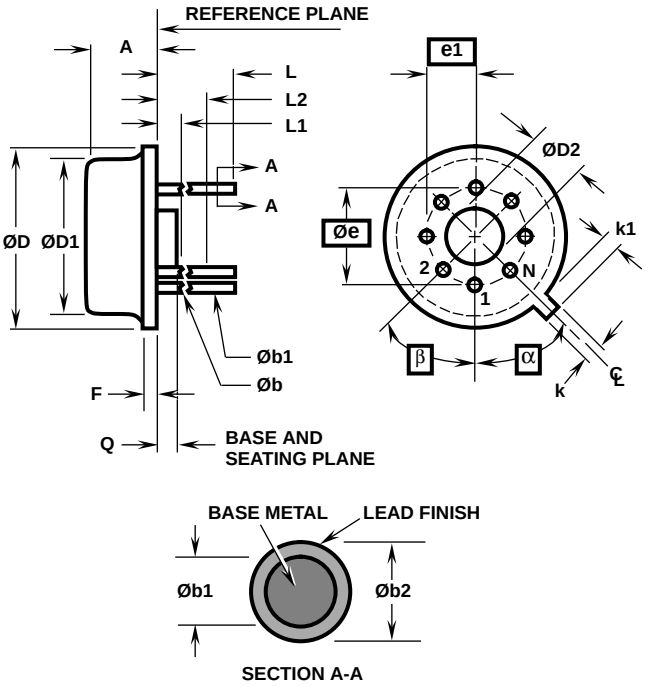
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Metal Can Packages (Can)



T8.C **MIL-STD-1835 MACY1-X8 (A1)**
8 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45^o BSC		45^o BSC		3
β	45^o BSC		45^o BSC		3
N	8		8		4

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NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

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100, Rue de la Fusee
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