



BUK92150-55A

N-channel TrenchMOS logic level FET

12 June 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

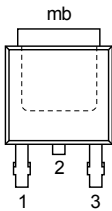
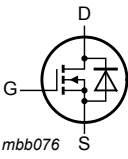
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _J ≥ 25 °C; T _J ≤ 175 °C		-	-	55	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2 ; Fig. 3		-	-	11	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	36	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _J = 25 °C		-	97	125	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _J = 175 °C; Fig. 11 ; Fig. 12		-	-	280	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 25 °C		-	-	155	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _J = 25 °C; Fig. 11 ; Fig. 12		-	120	140	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 5 A; V _{DS} = 44 V; T _J = 25 °C; Fig. 13		-	2.6	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 11\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	-	16	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 DPAK (SOT428)	 mbb076
2	D	Drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK92150-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428
BUK92150-55A/CD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK92150-55A	9215055A
BUK92150-55A/CD	

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$	-	55	V

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DGR}	drain-gate voltage	R _{GS} 20 kΩ		-	55	V
V _{GS}	gate-source voltage			-15	15	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	36	W
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; Fig. 2 ; Fig. 3		-	11	A
		T _{mb} = 100 °C; V _{GS} = 5 V; Fig. 3		-	7.8	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Fig. 2		-	44	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	11	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	44	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 11 A; V _{sup} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped		-	16	mJ

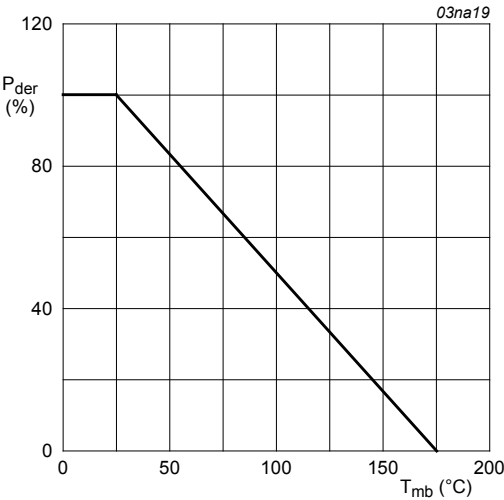


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

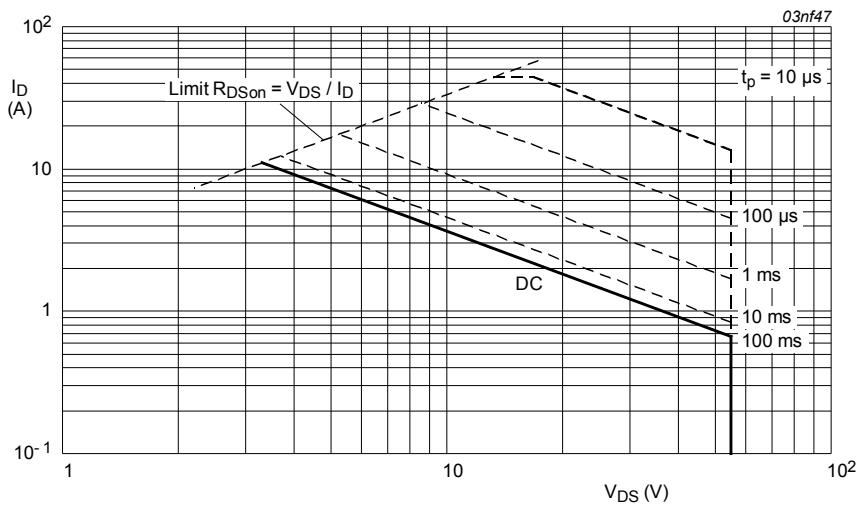


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is single pulse

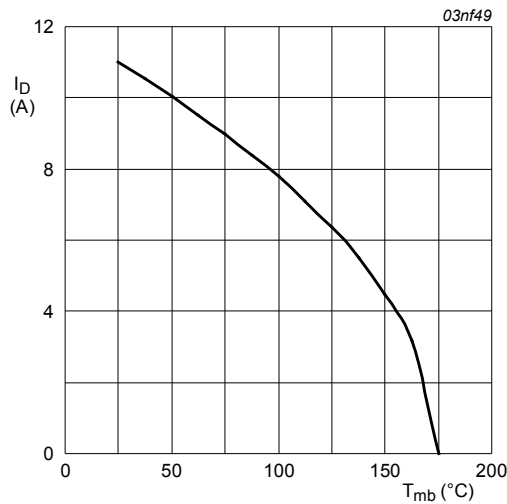


Fig. 3. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 4.5V I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	-	4.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W

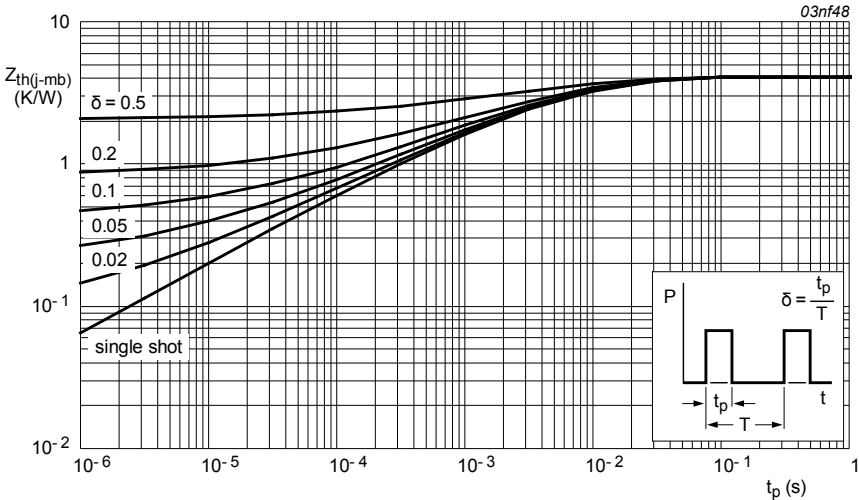


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _J = 25 °C	55	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _J = -55 °C	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 10	-	-	2.3	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 10	1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 10	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 25 °C	-	0.05	10	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _J = 25 °C	-	97	125	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _J = 175 °C; Fig. 11; Fig. 12	-	-	280	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _J = 25 °C	-	-	155	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _J = 25 °C; Fig. 11; Fig. 12	-	120	140	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 5\text{ A}$; $V_{DS} = 44\text{ V}$; $V_{GS} = 5\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 13		-	6	-	nC
Q_{GS}	gate-source charge			-	0.76	-	nC
Q_{GD}	gate-drain charge			-	2.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 14		-	240	338	pF
C_{oss}	output capacitance			-	50	65	pF
C_{rss}	reverse transfer capacitance			-	40	58	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 3.3\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $R_{G(ext)} = 10\text{ }\Omega$; $T_J = 25\text{ }^\circ\text{C}$		-	8	-	ns
t_r	rise time			-	57	-	ns
$t_{d(off)}$	turn-off delay time			-	16	-	ns
t_f	fall time			-	13	-	ns
L_D	internal drain inductance	measured from drain to centre of die; $T_J = 25\text{ }^\circ\text{C}$		-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; $T_J = 25\text{ }^\circ\text{C}$		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 15\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 15		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	24	-	ns
Q_r	recovered charge			-	26	-	nC

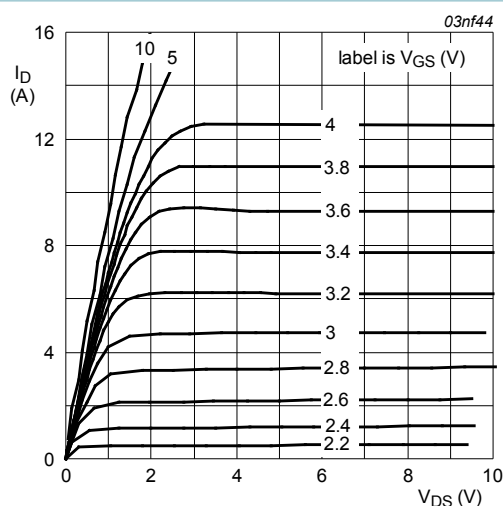


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_J = 25^\circ\text{C}$

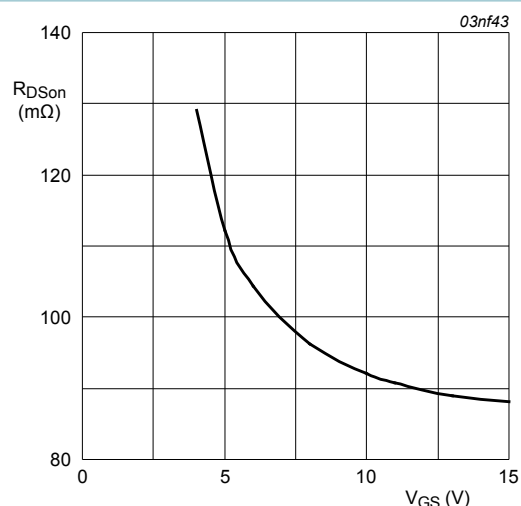
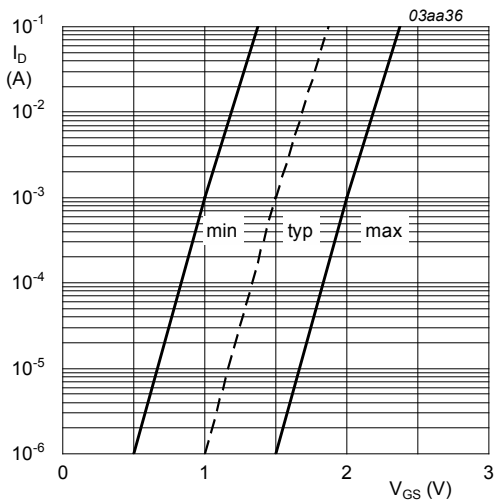


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^\circ\text{C}; I_D = 5\text{ A}$



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

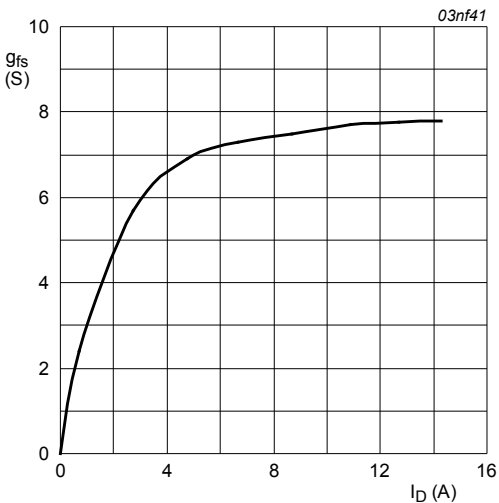


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 25\text{ V}$

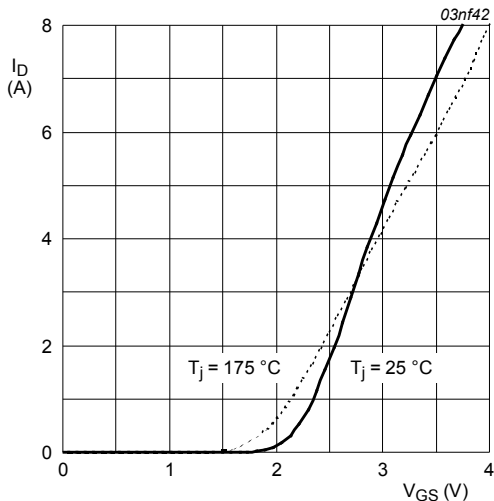


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25\text{ V}$

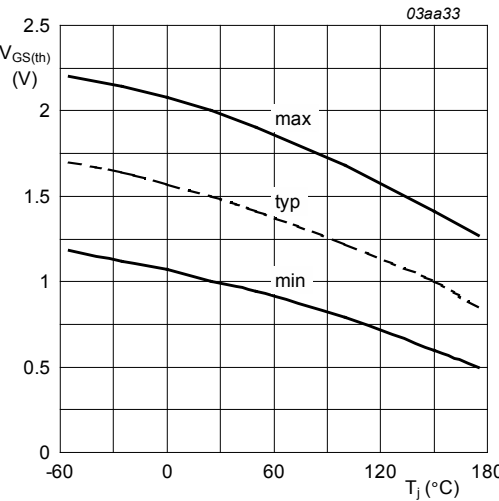


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

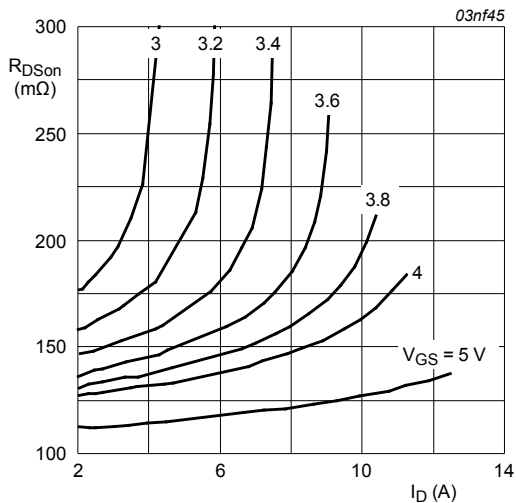


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}\text{C}$$

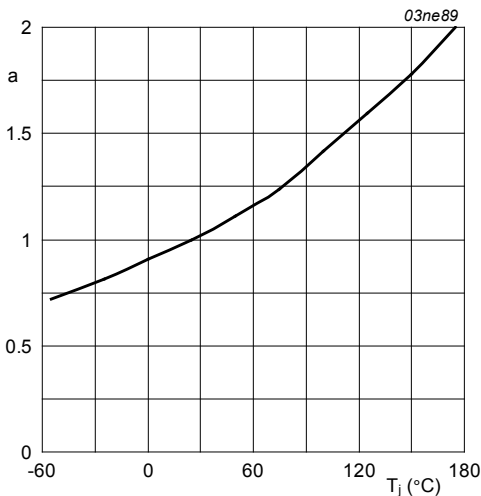


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

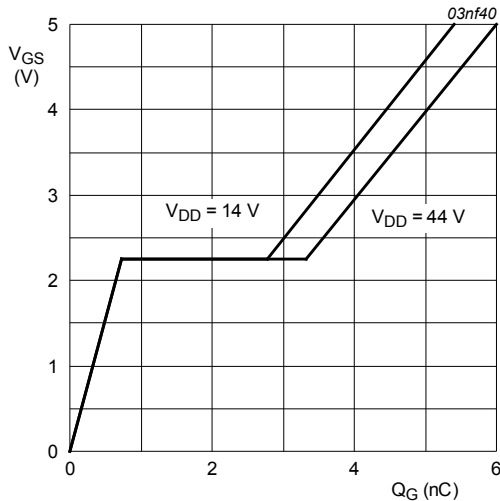


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 5\text{A}$$

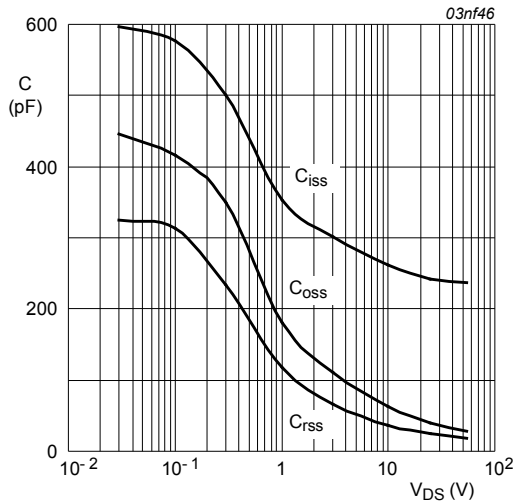


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

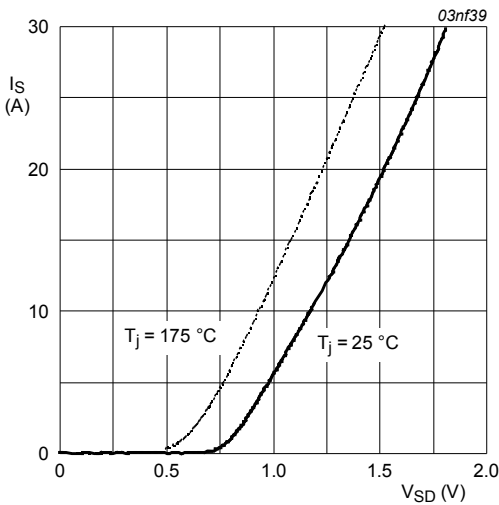


Fig. 15. Reverse diode current as a function of reverse diode voltage; typical values

$V_{GS} = 0V$

11. Package outline

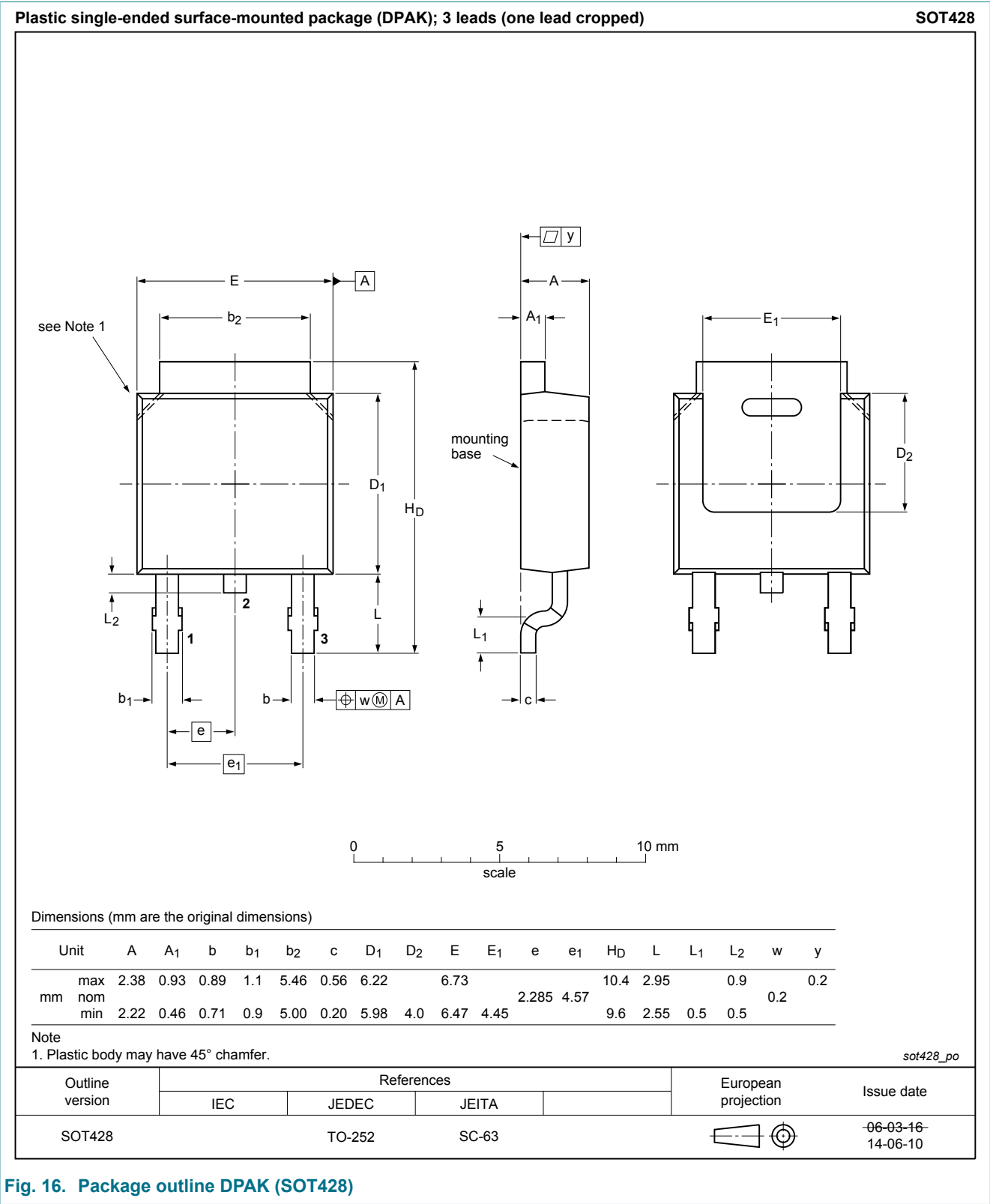


Fig. 16. Package outline DPAK (SOT428)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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