M80C86/M80C86-2
16-BIT CHMOS MICROPROCESSOR

MILITARY

- **Pin-for-Pin and Functionally Compatible to Industry Standard HMOS M8086**
- **Fully Static Design with Frequency Range from D.C. to:**
  - **— 5 MHz for M80C86**
  - **— 8 MHz for M80C86-2**
- **Low Power Operation**
  - **— Operating I_{CC} = 10 mA/MHz**
  - **— Standby I_{CCS} = 500 μA max**
- **Bus-Hold Circuitry Eliminates Pull-Up Resistors**
- **Direct Addressing Capability of 1 MByte of Memory**
- **Architecture Designed for Powerful Assembly Language and Efficient High Level Languages**
- **24 Operand Addressing Modes**
- **Byte, Word and Block Operations**
- **8 and 16-Bit Signed and Unsigned Arithmetic**
  - **— Binary or Decimal**
  - **— Multiply and Divide**
- **Military Temperature Range: −55°C to +125°C (T_C)**

The Intel M80C86 is a high performance, CHMOS version of the industry standard HMOS M8086 16-bit CPU. It is available in 5 and 8 MHz clock rates. The M80C86 offers two modes of operation: MINimum for small systems and MAXimum for larger applications such as multiprocessing. It is available in 40-pin DIP package.

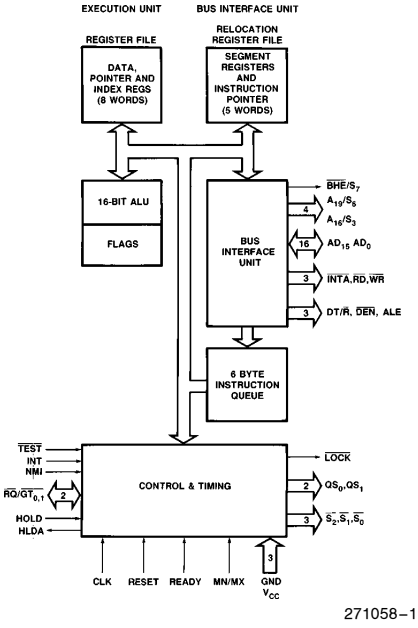


Figure 1. M80C86 CPU Block Diagram

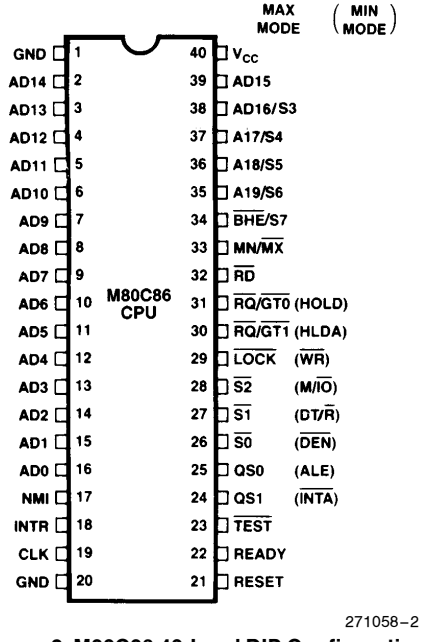


Figure 2. M80C86 40-Lead DIP Configuration

Table 1. Pin Description

The following pin function descriptions are for M80C86 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the M80C86 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function
AD_{15}–AD_0	2–16, 39	I/O	**ADDRESS DATA BUS:** These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7–D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See $\overline{BHE}$.) These lines are active HIGH and float to 3-state OFF(1) during interrupt acknowledge and local bus "hold acknowledge."
A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3	35–38	O	**ADDRESS/STATUS:** During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown. This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF(1) during local bus "hold acknowledge."

A_{17}/S_4	A_{16}/S_3	Characteristics
0 (LOW)	0	Alternate Data
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data
S_6 is 0 (LOW)		

$\overline{BHE}/S_7$	34	O	**BUS HIGH ENABLE/STATUS:** During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}–D_8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF(1) in "hold." It is LOW during T_1 for the first interrupt acknowledge cycle.

$\overline{BHE}$	A_0	Characteristics
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$	32	O	**READ:** Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the M80C86 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the M80C86 local bus has floated. This floats to 3-state OFF in ''hold acknowledge.''
READY	22	I	**READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/IO is synchronized by the M82C84A Clock Generator to form READY. This signal is active HIGH. The M80C86 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	**INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	**$\overline{TEST}$:** input is examined by the ''Wait'' instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an ''Idle'' state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	**NON-MASKABLE INTERRUPT:** an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** +5V power supply pin.
GND	1, 20		**GROUND:** Both must be connected.
MN/$\overline{MX}$	33	I	**MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Table 1. Pin Description (Continued)

The following pin function descriptions are for the M80C86/M82C88 system in maximum mode (i.e., MN/$\overline{MX}$ = V_{SS}). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$</td><td>26–28</td><td>O</td><td>STATUS: active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the M82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.
These signals float to 3-state OFF(1) in ‘‘hold acknowledge.’’ These status lines are encoded as shown.
<table>
<tr><th>$\overline{S_2}$</th><th>$\overline{S_1}$</th><th>$\overline{S_0}$</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT}_0$, $\overline{RQ}/\overline{GT}_1$</td><td>30, 31</td><td>I/O</td><td>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor’s current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT}_0$ having higher priority than $\overline{RQ}/\overline{GT}_1$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see timing diagram):
1. A pulse of 1 CLK wide from another local bus master indicates a local bus request (‘‘hold’’) to the M80C86 (pulse 1).
2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the M80C86 to the requesting master (pulse 2), indicates that the M80C86 has allowed the local bus to float and that it will enter the ‘‘hold acknowledge’’ state at the next CLK. The CPU’s bus interface unit is disconnected logically from the local bus during ‘‘hold acknowledge.’’
3. A pulse 1 CLK wide from the requesting master indicates to the M80C86 (pulse 3) that the ‘‘hold’’ request is about to end and that M80C86 can reclaim the local bus at the next CLK.
Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:
1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.</td></tr>
</table>

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
			If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	**$\overline{LOCK}$:** output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the ''LOCK'' prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF(1) in ''hold acknowledge.''
QS_1, QS_0	24, 25	O	**QUEUE STATUS:** The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal M80C86 instruction queue.

QS_1	QS_0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are for the M80C86 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are described above.

M/$\overline{IO}$	28	O	**STATUS LINE:** logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF(1) in local bus ''hold acknowledge.''
$\overline{WR}$	29	O	**WRITE:** indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF(1) in local bus ''hold acknowledge.''
$\overline{INTA}$	24	O	$\overline{INTA}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and T_W of each interrupt acknowledge cycle.
ALE	25	O	**ADDRESS LATCH ENABLE:** provided by the processor to latch the address into an address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**DATA TRANSMIT/RECEIVE:** needed in minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF(1) in local bus ''hold acknowledge.''

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{DEN}$	26	O	**DATA ENABLE:** provided as an output enable for the transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF(1) in local bus ''hold acknowledge.''
HOLD, HLDA	31, 30	I/O	**HOLD:** indicates that another master is requesting a local bus ''hold.'' To be acknowledged, HOLD must be active HIGH. The processor receiving the ''hold'' request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{RQ}/\overline{GT}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

NOTE:
1. See the section on Bus Hold Circuitry.

FUNCTIONAL DESCRIPTION

STATIC OPERATION

All M80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS M80C86 can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The M80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation. In a power critical situation, this can provide extremely low power operation since M80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the M80C86 power requirement is the standby current.

INTERNAL ARCHITECTURE

The internal functions of the M80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces ''dead time'' on the memory bus. The queue acts as a First-In-First Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution units receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

NOTE:
Additional information on memory organization, requirements for supporting minimum and maximum modes, bus operation, basic system timing, and external interface of the M80C86 is described in the Microsystems Components Handbook.

DEVIATION DESCRIPTION

A 20–25 ns glitch occurs on the 80C86/80C88 $\overline{RD}$ pin immediately following a read cycle. The problem has been fully characterized with the following results:

1. The read cycle must be 4 clocks followed by 2 passive clocks.
2. Cycle following the read cycle must be a data read/write or an I/O read/write.
3. The # of bytes in the queue required to cause the glitch varies by instruction.
4. The glitch appears on the falling edge of the first passive clock.
5. The magnitude of the glitch depends on the capacitive loading of the RD# pin.
6. The glitch occurs for both Min and Max mode operations.
7. V_{CC} variations from 4.5V through 5.5V have no effect on the glitch.
8. Temperature variations (within allowed temperature range) also have no effect on the glitch.

IMPACT ON SYSTEM DESIGN

Systems which use the $\overline{RD}$ strobe to clock a state machine or any other edge triggered device are most vulnerable and most likely to malfunction.

The problem may also impact other Min mode systems, particularly those in which the system address latches are enabled all the time (such as the example minimum mode system illustrated in the 80C86 data sheet). In such designs, the $\overline{RD}$ signal is used to turn off the output buffers of the memory and peripheral devices connected to the local bus at the end of a bus cycle. A false pulse on the $\overline{RD}$ pin in a TP or a T1 state following a read cycle may not allow for sufficient recovery time for a previously accessed device. The probability of a failure is higher for low speed designs using slow memory and peripheral devices which require high recovery times between successive accesses. The problem will not be seen if the address latches are disabled at the end of any bus cycle since all the devices connected to the bus will then be deselected when the false pulse occurs.

Most Max mode systems do not use the $\overline{RD}$ signal and are therefore not likely to be affected.

WORKAROUND

A hardware workaround has been designed and tested. The workaround circuit (Figure 3) qualifies the $\overline{RD}$ signal coming out of the M80C86/80C88 during valid read cycles and forces it to be inactive otherwise (see the timing diagram in Figure 4). The-delay in the $\overline{RDM}$ signal is limited to 6 ns (Max) by using fast gate devices. This should not have any impact in the design since the $\overline{RDM}$ pulse width is still the same as the orginal $\overline{RD}$ pulse width. $\overline{RDM}$ is also guaranteed to go inactive during the T4 state of all read cycles.

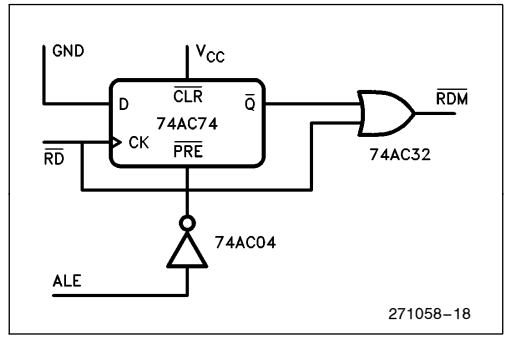


Figure 3

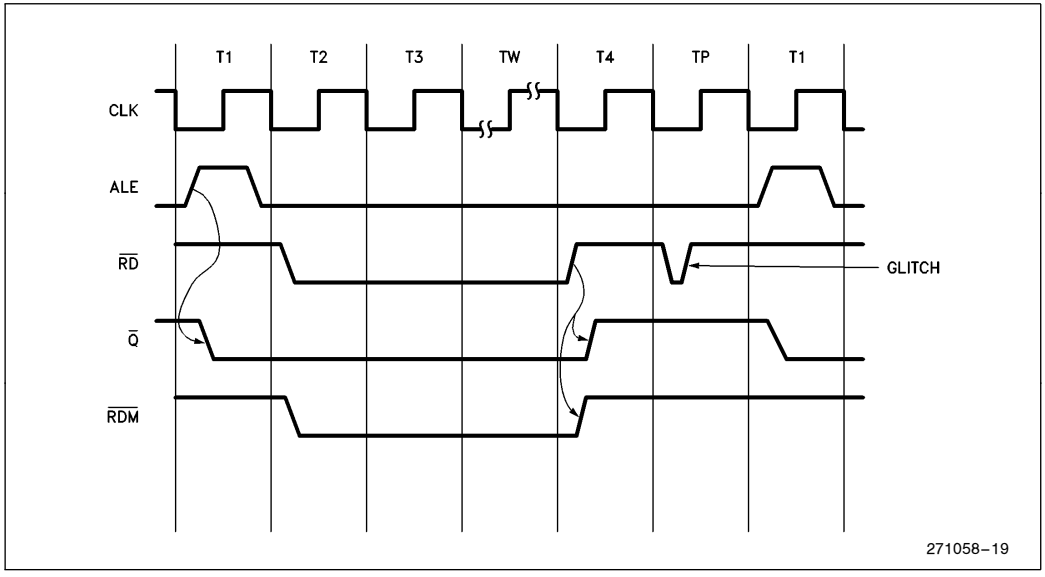


Figure 4

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
(With respect to ground) . . . . . −0.5 to 8.0V
Input Voltage Applied
(w.r.t. ground) . . . . . −2.0 to V_{CC} + 0.5V
Output Voltage Applied
(w.r.t. ground) . . . . . −0.5 to V_{CC} + 0.5V
Power Dissipation 1.0W
Storage Temperature . . . . . −65°C to 150°C
Case Temperature Under Bias . . . −55°C to +125°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage (M80C86)	4.50	5.50	V
V_{CC}	Digital Supply Voltage (M80C86-2)	4.75	5.25	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Comments
V_{IL}	Input Low Voltage		+0.8	V	
V_{IH}	Input High Voltage (All inputs except clock and MN/$\overline{MX}$)	2.2		V	
V_{CH}	Clock and MN/$\overline{MX}$ Input High Voltage	V_{CC}−0.8		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC}−0.4		V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{CC}	Power Supply Current		10 mA/MHz		V_{IL} = GND, V_{IH} = V_{CC}
I_{CCS}	Standby Supply Current		500	μA	V_{IN} = V_{CC} or GND Outputs Unloaded CLK = GND or V_{CC}
I_{LI}	Input Leakage Current		±1.0	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{BHL}	Input Leakage Current (Bus Hold Low) (Note 2)	40	400	μA	V_{IN} = 0.8V
I_{BHH}	Input Leakage Current (Bus Hold High) (Note 3)	−40	−400	μA	V_{IN} = 3.0V
I_{LO}	Output Leakage Current		±10	μA	V_{OUT} = GND or V_{CC}
C_{IN}	Capacitance of Input Buffer (All inputs except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		10	pF	(Note 1)
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		20	pF	(Note 1)
C_{OUT}	Output Capacitance		15	pF	(Note 1)

NOTES:
1. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at +5.0V or GND.
2. I_{BHL} should be measured after lowering V_{IN} to GND and then raising V_{IN} to 0.8V on the following pins: 2–16, 34–39.
3. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering V_{IN} to 3.0V on the following pins: 2–16, 26–32, 34–39.

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	M80C86		M80C86-2		Units	Comments
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into M82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into M82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into M80C86	118		68		ns	
TCHRYX	READY Hold Time into M80C86	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 3)	−5		−5		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

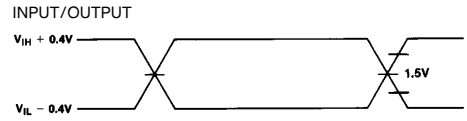
A.C. CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Timing Responses

Symbol	Parameter	M80C86		M80C86-2		Units	Comments
		Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH−30		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL−75		2TCLCL−50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL−60		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

NOTES:
1. Signal at M82C84A shown for reference only. See M82C84A data sheet for the most recent specifications.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (5 ns into T3).

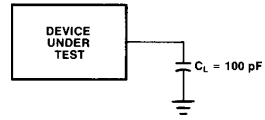
A.C. TESTING INPUT, OUTPUT WAVEFORM



271058–3

A.C. Testing inputs are driven at V_{IH} + 0.4V for a logic "1" and V_{IL} − 0.4V for a logic "0". The clock is driven at V_{CH} + 0.4V and V_{CL} − 0.4V. Timing measurements are made at 1.5V.

A.C. TESTING LOAD CIRCUIT

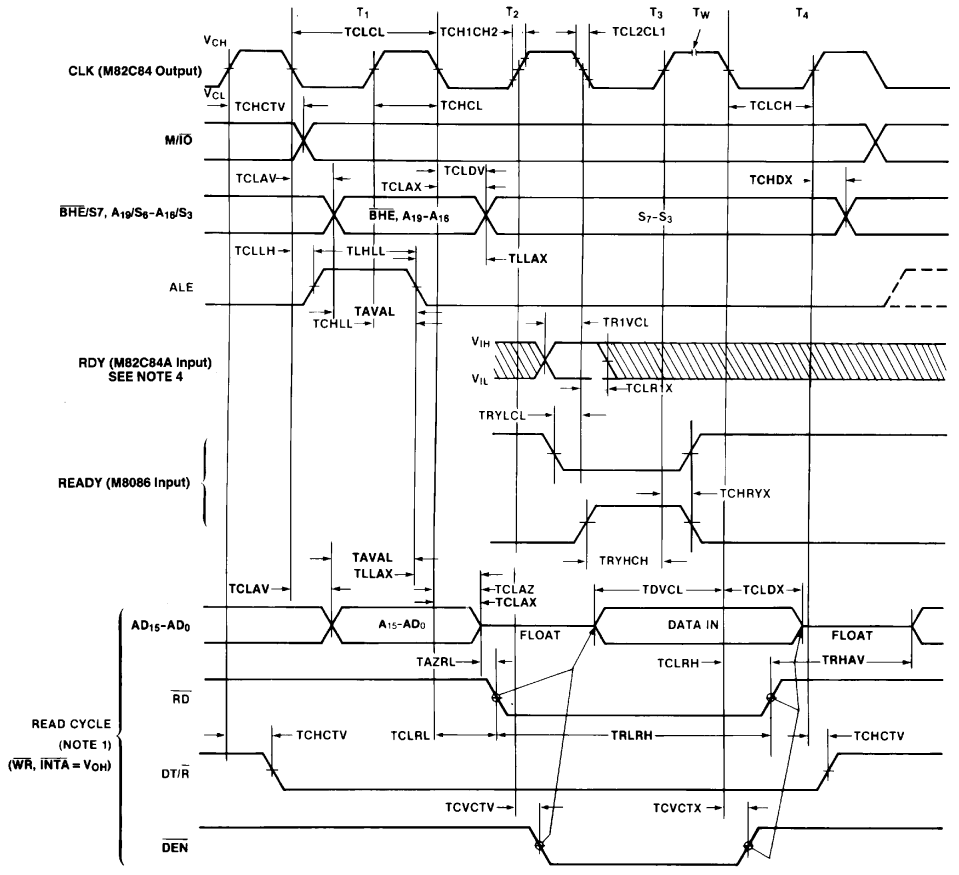


271058–4

C_L Includes Jig Capacitance

WAVEFORMS

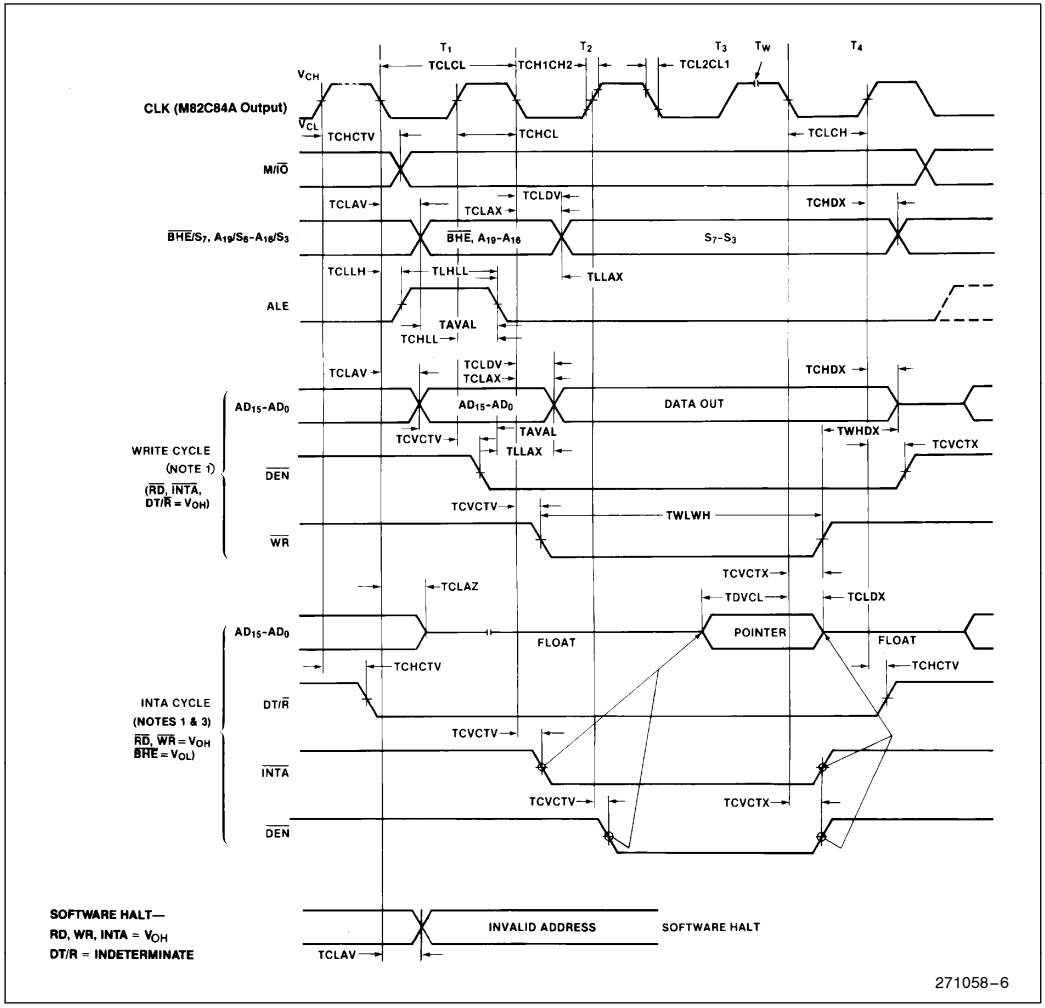
MINIMUM MODE



271058–5

WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:
1. All output timing measurements are made at 1.5V.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The M80C86 local ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at M82C84A are shown for reference only.

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING M82C88 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	M80C86		M80C86-2		Units	Comments
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into M82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into M82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into M80C86	118		68		ns	
TCHRYX	READY Hold Time into M80C86	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 4)	−5		−5		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 2)	30		15		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		15		ns	
TCHGX	$\overline{RQ}$ Hold Time into M80C86	40		30		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

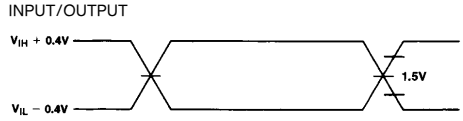
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	M80C86		M80C86-2		Units	Comments
		Min	Max	Min	Max		
TCLML	Command Active Delay (Note 1)	5	45	5	35	ns	
TCLMH	Command Inactive Delay (Note 1)	5	45	5	35	ns	
TRYHSH	READY Active to Status Passive (Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (Note 1)		35		20	ns	
TSVMCH	Status Valid to MCE High (Note 1)		35		30	ns	
TCLLH	CLK Low to ALE Valid (Note 1)		35		20	ns	
TCLMCH	CLK Low to MCE High (Note 1)		35		25	ns	
TCHLL	ALE Inactive Delay (Note 1)	4	35	4	25	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (Note 1)	5	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCHDTL	Direction Control Active Delay (Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (Note 1)		35		30	ns	
TCLGL	GT Active Delay	0	85	0	50	ns	
TCLGH	GT Inactive Delay	0	85	0	50	ns	
TRLRH	RD Width	2TCLCL−75		2TCLCL−50		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

NOTES:
1. Signal at M82C84A or M82C88 shown for reference only. See M82C84A and M82C88 for the most recent specifications.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (5 ns into T3).

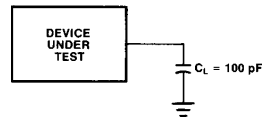
A.C. TESTING INPUT, OUTPUT WAVEFORM



271058–7

A.C. Testing inputs are driven at V_{IH} + 0.4V for a logic "1" and V_{IL} − 0.4V for a logic "0". The clock is driven at V_{CH} + 0.4V and V_{CL} − 0.4V. Timing measurements are made at 1.5V.

A.C. TESTING LOAD CIRCUIT

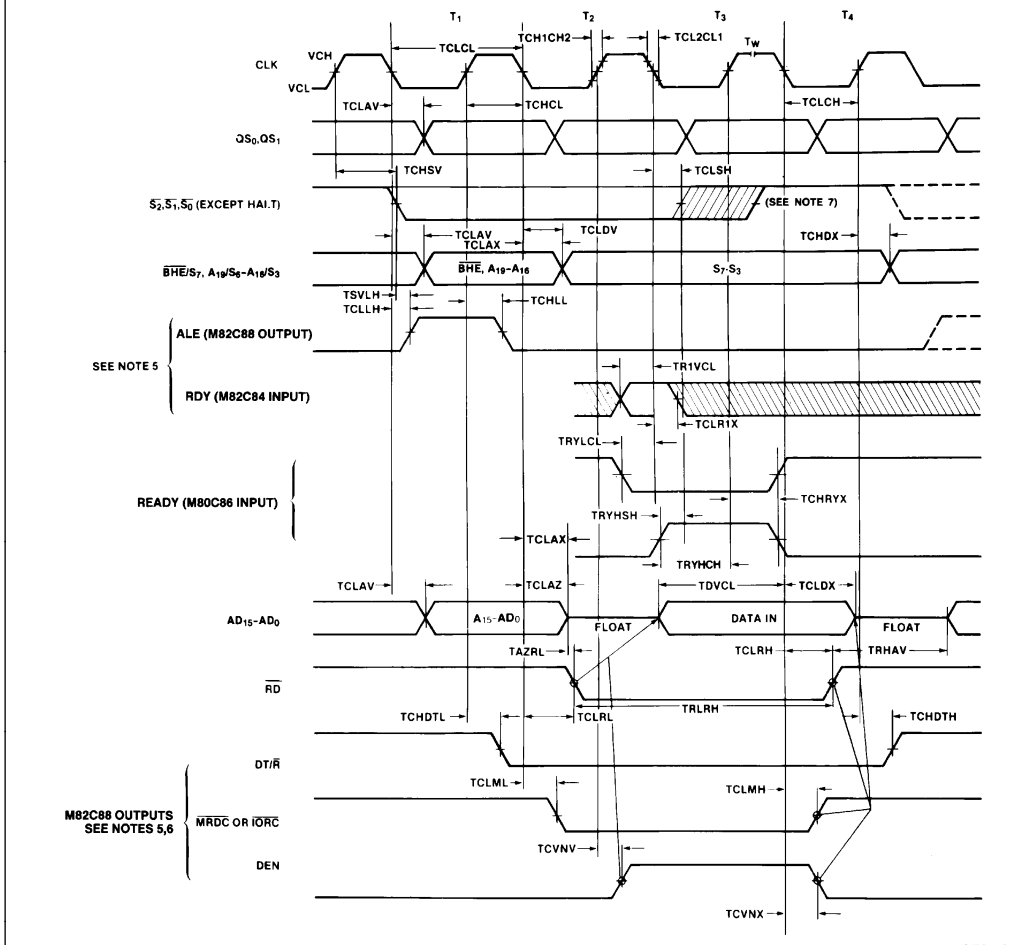


271058–8

C_L Includes Jig Capacitance

WAVEFORMS

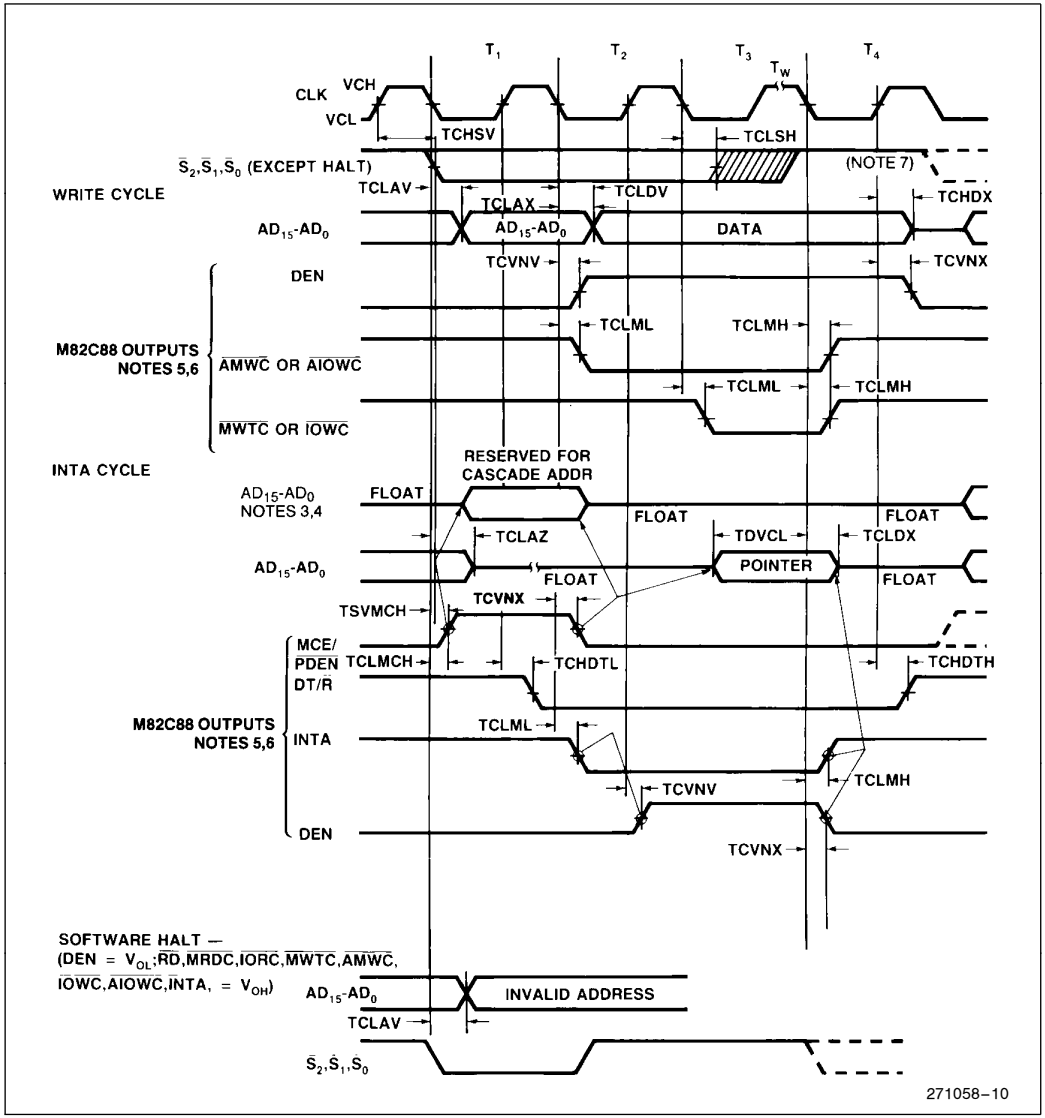
MAXIMUM MODE



271058–9

WAVEFORMS (Continued)

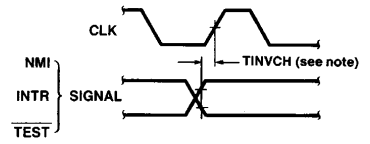
MAXIMUM MODE (Continued)



NOTES:
1. All timing measurements are made at 1.5V.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The M80C86 local ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at M82C84A or M82C88 are shown for reference only.
6. The issuance of the M82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high M82C88 CEN.
7. Status inactive in state just prior to T_4.

WAVEFORMS (Continued)

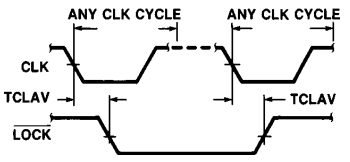
ASYNCHRONOUS SIGNAL RECOGNITION



271058–11

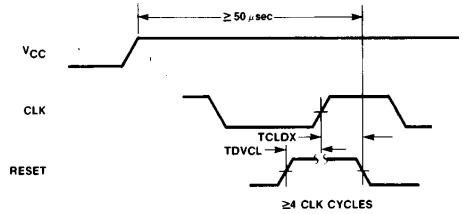
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



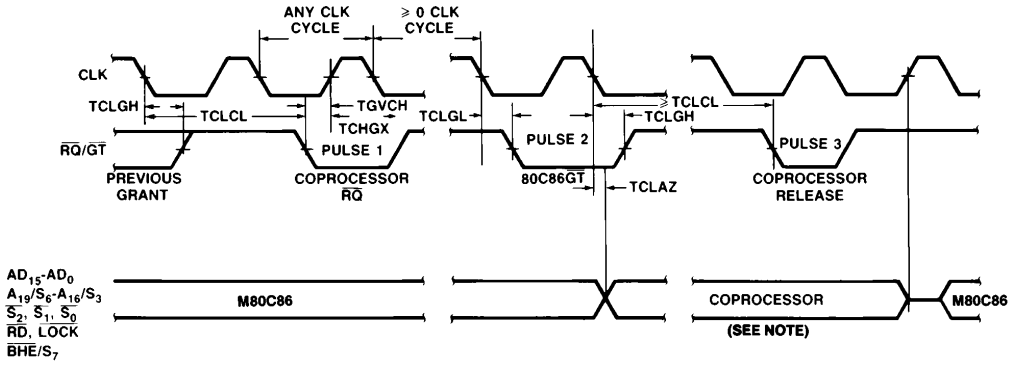
271058–12

RESET TIMING



271058–13

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

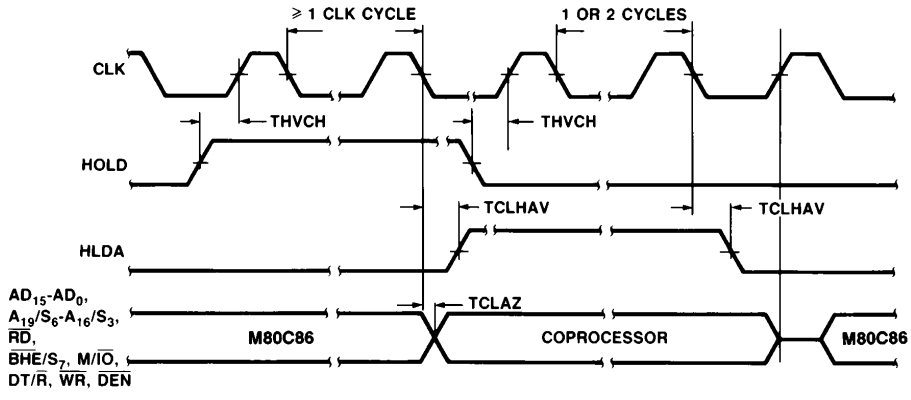


271058–14

NOTE: The coprocessor may not drive the buses outside the region shown without risking contention.

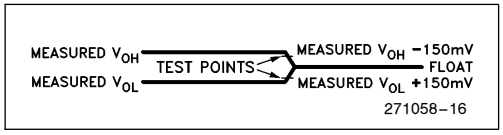
WAVEFORMS (Continued)

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



A.C. TESTING

V_{FLOAT} TIMING



NOTE:
1. V_L for High to float tests is 0V and V_L for Low to float tests is 4.0V.

V_{FLOAT} TIMING TESTING LOAD CIRCUIT