

# NVD5C434N

## MOSFET – Power, Single, N-Channel 40 V, 2.1 mΩ, 163 A

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	40	V
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	$T_C = 25^\circ\text{C}$ Steady State	$I_D$	163	A
			115	
	$T_C = 100^\circ\text{C}$ Steady State	$P_D$	117	W
			58	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	$T_A = 25^\circ\text{C}$ Steady State	$I_D$	26	A
			22	
	$T_A = 100^\circ\text{C}$ Steady State	$P_D$	3.2	W
			2.2	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10\ \mu\text{s}$	$I_{DM}$	900	A
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to 175	°C
Source Current (Body Diode)		$I_S$	130	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $I_{L(pk)} = 25\text{ A}$ )		$E_{AS}$	420	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	1.28	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	48	

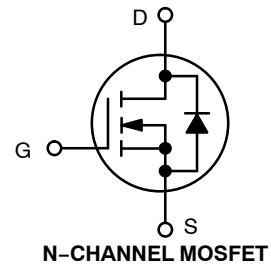
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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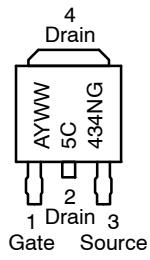
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$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
40 V	2.1 mΩ @ 10 V	163 A



DPAK  
CASE 369C  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location  
Y = Year  
WW = Work Week  
5C434N = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NVD5C434N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS/T<sub>J</sub></sub>			18		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25°C		10	μA
			T <sub>J</sub> = 125°C		250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)/T<sub>J</sub></sub>			7.9		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		1.7	2.1	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 50 A		155		S

### CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		5400		pF
Output Capacitance	C <sub>oss</sub>			3000		
Reverse Transfer Capacitance	C <sub>rss</sub>			71		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 50 A		80.6		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			15.2		
Gate-to-Source Charge	Q <sub>GS</sub>			25.2		
Gate-to-Drain Charge	Q <sub>GD</sub>			15.4		
Plateau Voltage	V <sub>GP</sub>			4.8		V

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 50 A, R <sub>G</sub> = 2.5 Ω		15		ns
Rise Time	t <sub>r</sub>			78		
Turn-Off Delay Time	t <sub>d(off)</sub>			43		
Fall Time	t <sub>f</sub>			14		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 50 A			73		ns
Charge Time	t <sub>a</sub>				36		
Discharge Time	t <sub>b</sub>				37		
Reverse Recovery Charge	Q <sub>RR</sub>				120		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

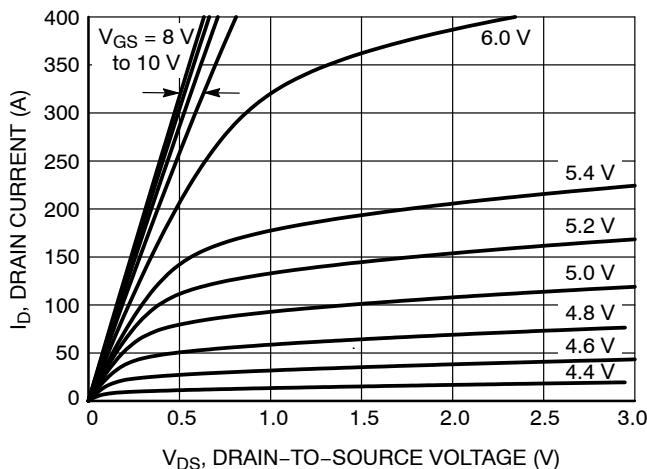


Figure 1. On-Region Characteristics

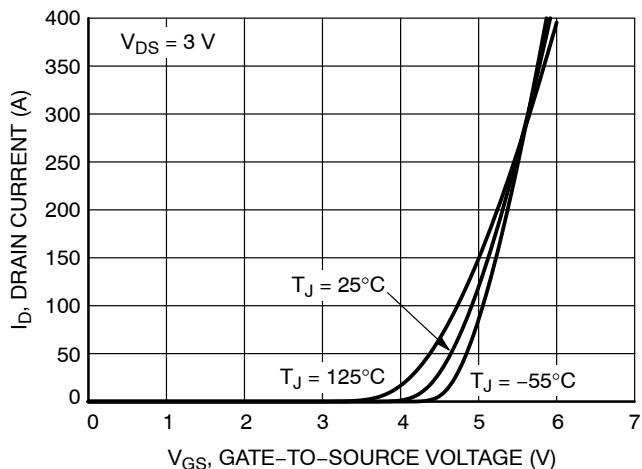


Figure 2. Transfer Characteristics

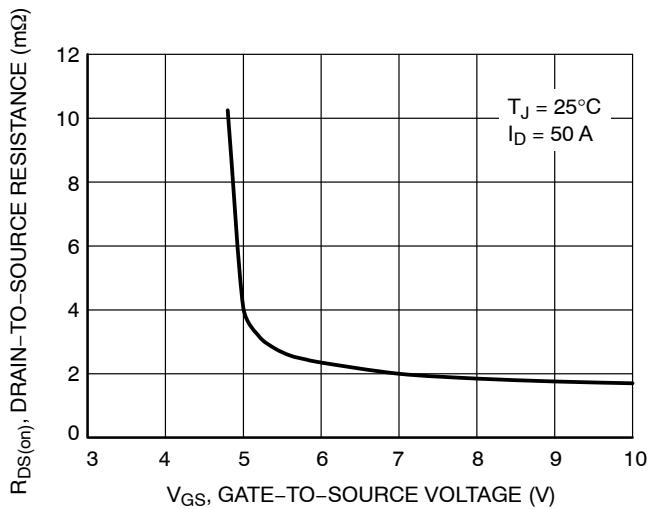


Figure 3. On-Resistance vs. Gate-to-Source Voltage

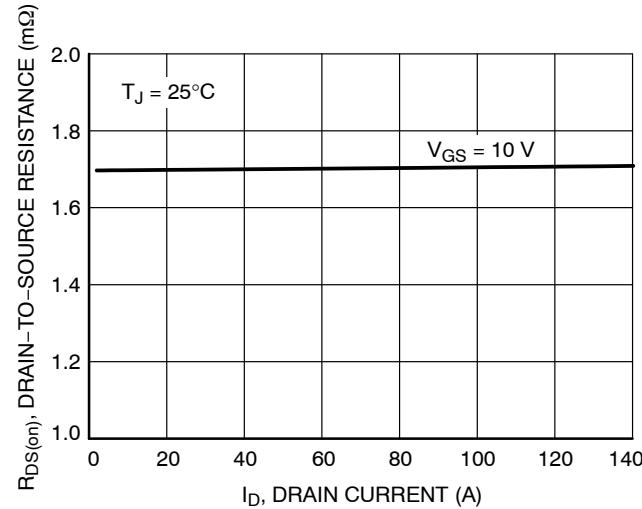


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

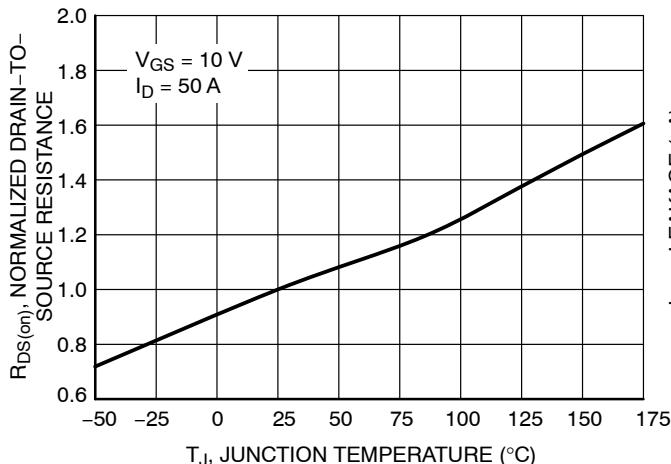


Figure 5. On-Resistance Variation with Temperature

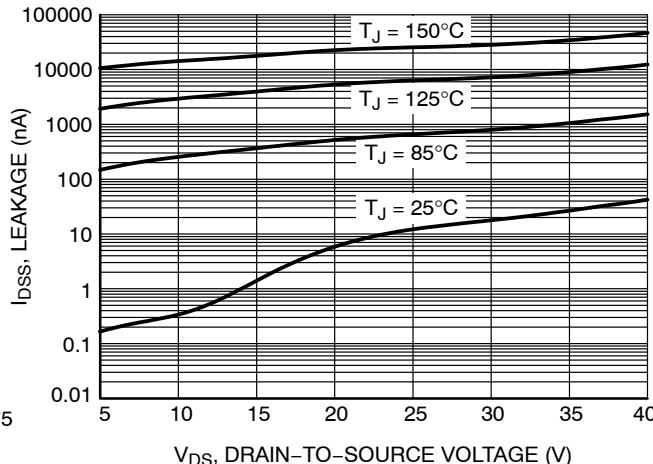


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

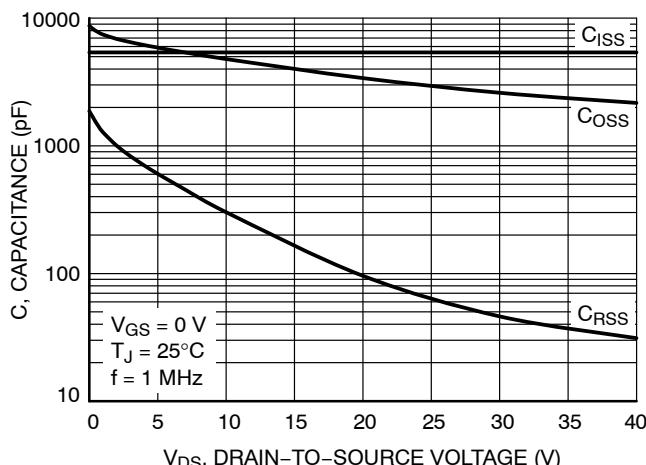


Figure 7. Capacitance Variation

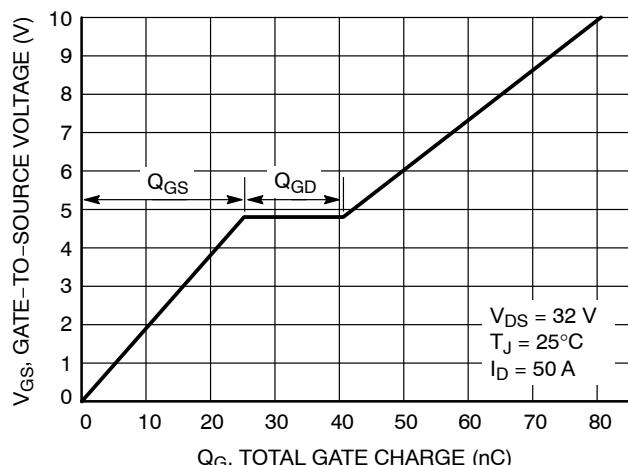


Figure 8. Gate-to-Source vs. Total Charge

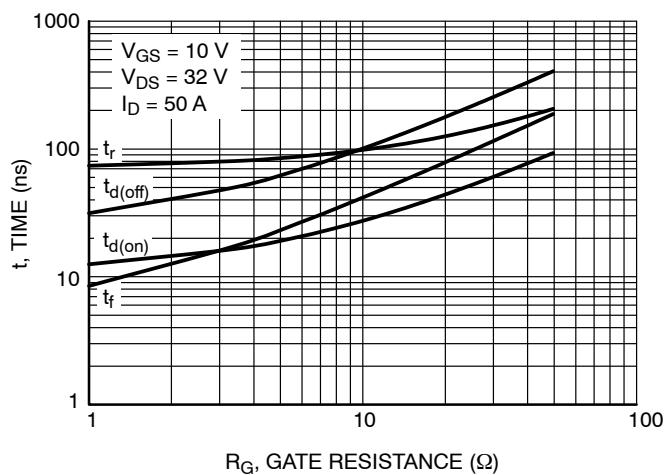


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

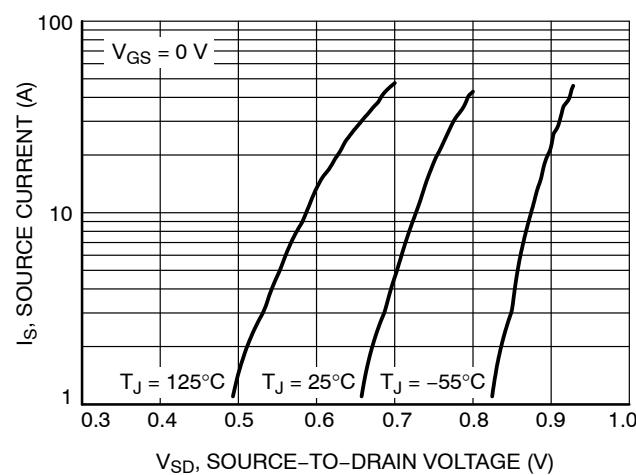


Figure 10. Diode Forward Voltage vs. Current

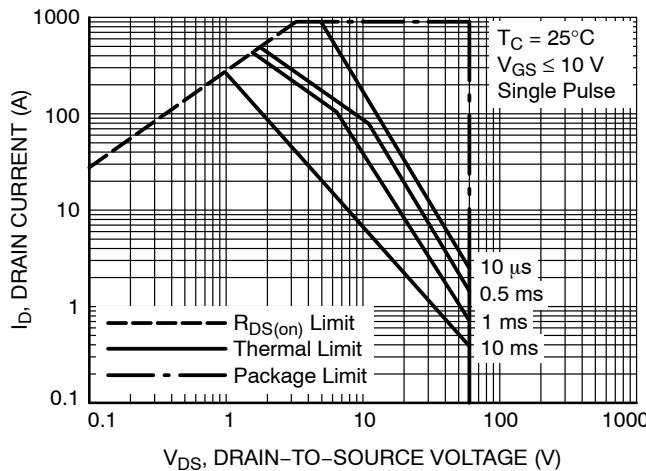


Figure 11. Maximum Rated Forward Biased Safe Operating Area

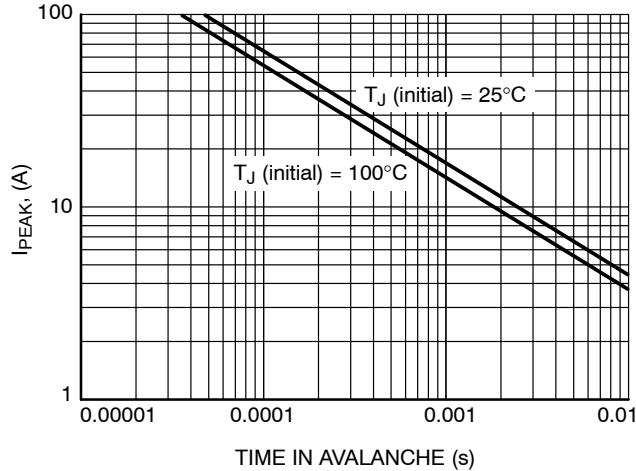
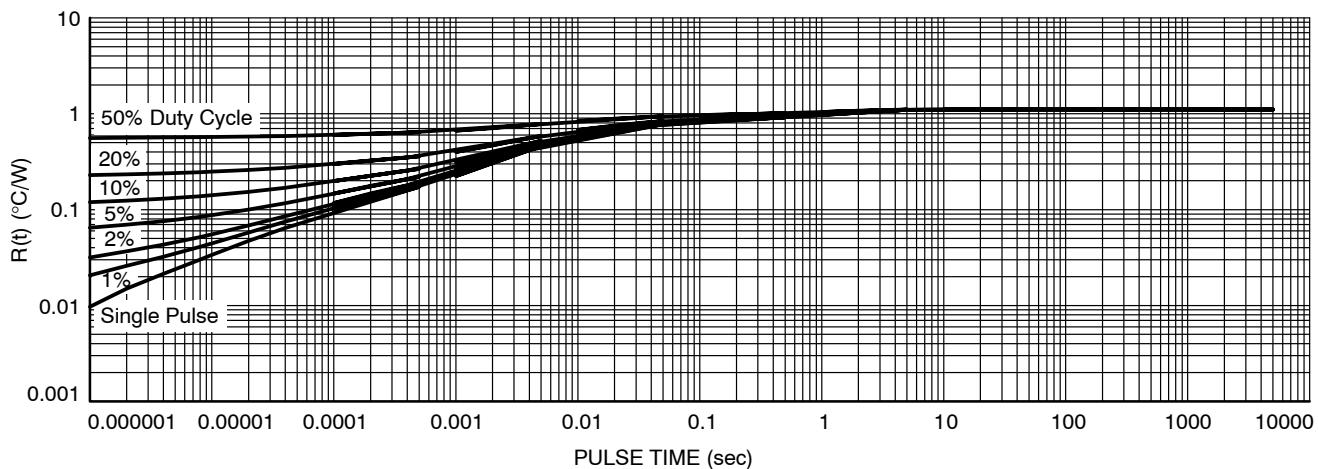
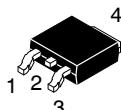


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

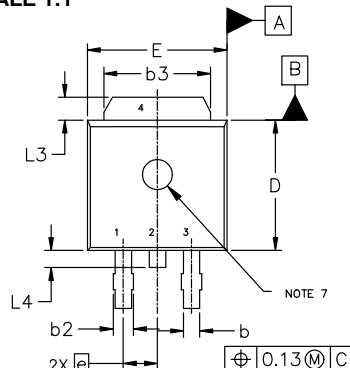
**TYPICAL CHARACTERISTICS****Figure 13. Thermal Characteristics****ORDERING INFORMATION**

Order Number	Package	Shipping <sup>†</sup>
NVD5C434NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



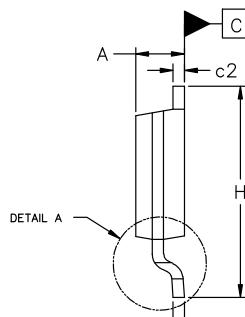
SCALE 1:1



TOP VIEW

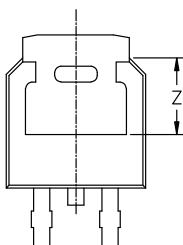
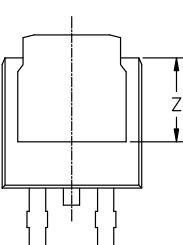
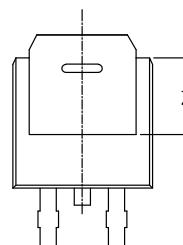
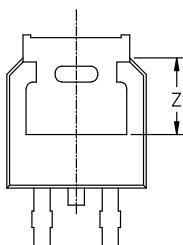
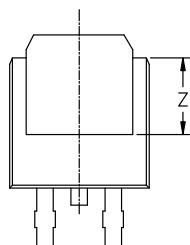
**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE H

DATE 15 JUL 2025



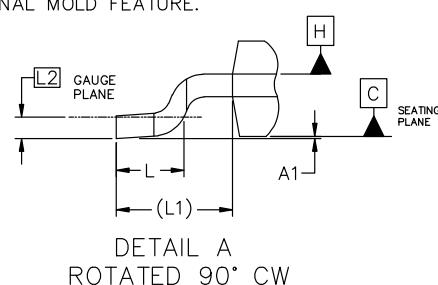
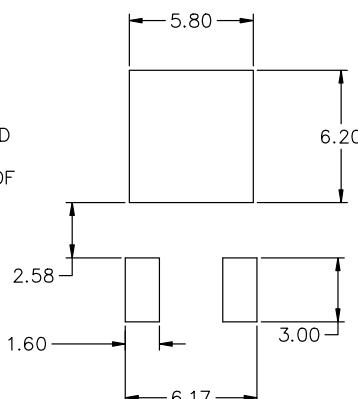
SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29	BSC	
H	9.40	9.91	10.41
L	1.40	10.10	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

DETAIL A  
ROTATED 90° CW

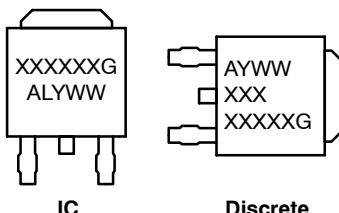
RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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**GENERIC  
MARKING DIAGRAM\***



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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