SIEMENS

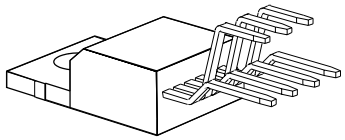
Intelligent Double Low-Side Switch 2 × 2 A

TLE 4211

Bipolar IC

Features

- Double low-side switch, 2 x 2 A
- Power limitation
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Reverse polarity protection
- Integrated clamp Z-Diodes
- Voltage proof up to 70 V
- Temperature range – 40 to 125 °C



P-TO220-7-1

Type	Ordering Code	Package
TLE 4211	Q67000-A8118	P-TO220-7-1

Application

Applications in automotive electronics require intelligent power switches activated by logic signals, which are shorted-load protected and provide error feedback.

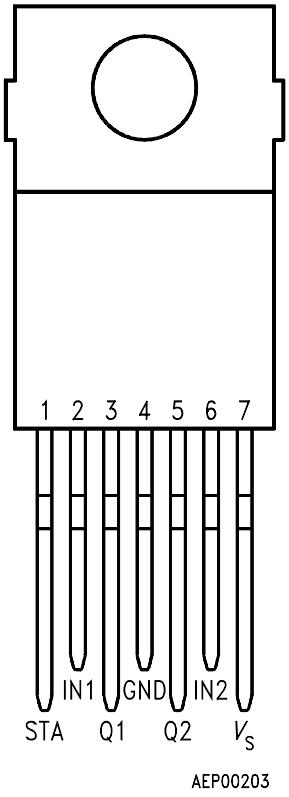
The IC contains two of these power switches (low-side switch). In case of inductive loads the integrated power Z-diodes clamp the discharging voltage.

With TTL signals at the control inputs (active low) both switches can be activated independently of one another. If one of the inputs is not in use, it must be applied to high potential.

The status output (open collector) signals the following malfunctions through low potential:

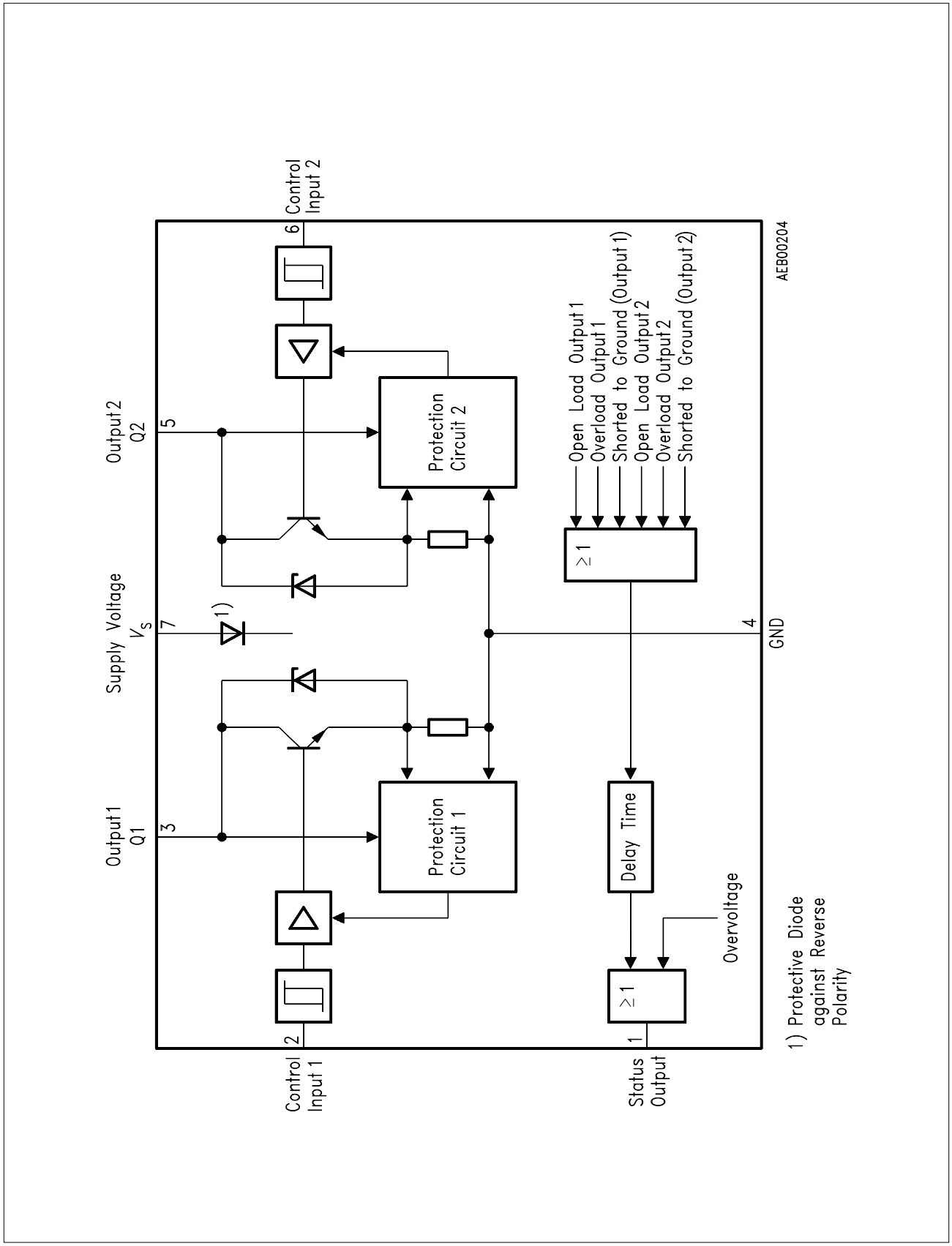
- Overload,
- Open load,
- Output shorted to ground,
- Overvoltage.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	STA	**Status output (open collector)** for both outputs; indicates overload, open load and shorted load to ground as well as overvoltage at pin 7. In case of malfunction the status output is switched to low after a delay time (except overvoltage).
2	IN1	**Control input 1 (TTL-compatible)** activates output transistor 1 in case of low-potential.
3	Q1	**Output 1** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
4	GND	**Ground** Wiring must be designed for a max. short-circuit current (2 x 3.5 A).
5	Q2	**Output 2** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
6	IN2	**Control input 2 (TTL-compatible)** activates output transistor 2 in case of low-potential.
7	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are deactivated. The status output indicates the malfunction without delay time.



Block Diagram

Circuit Description

Input Circuits

The control inputs comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the inverting buffer amplifiers convert the logic signal for driving the NPN power transistors.

Switching Stages

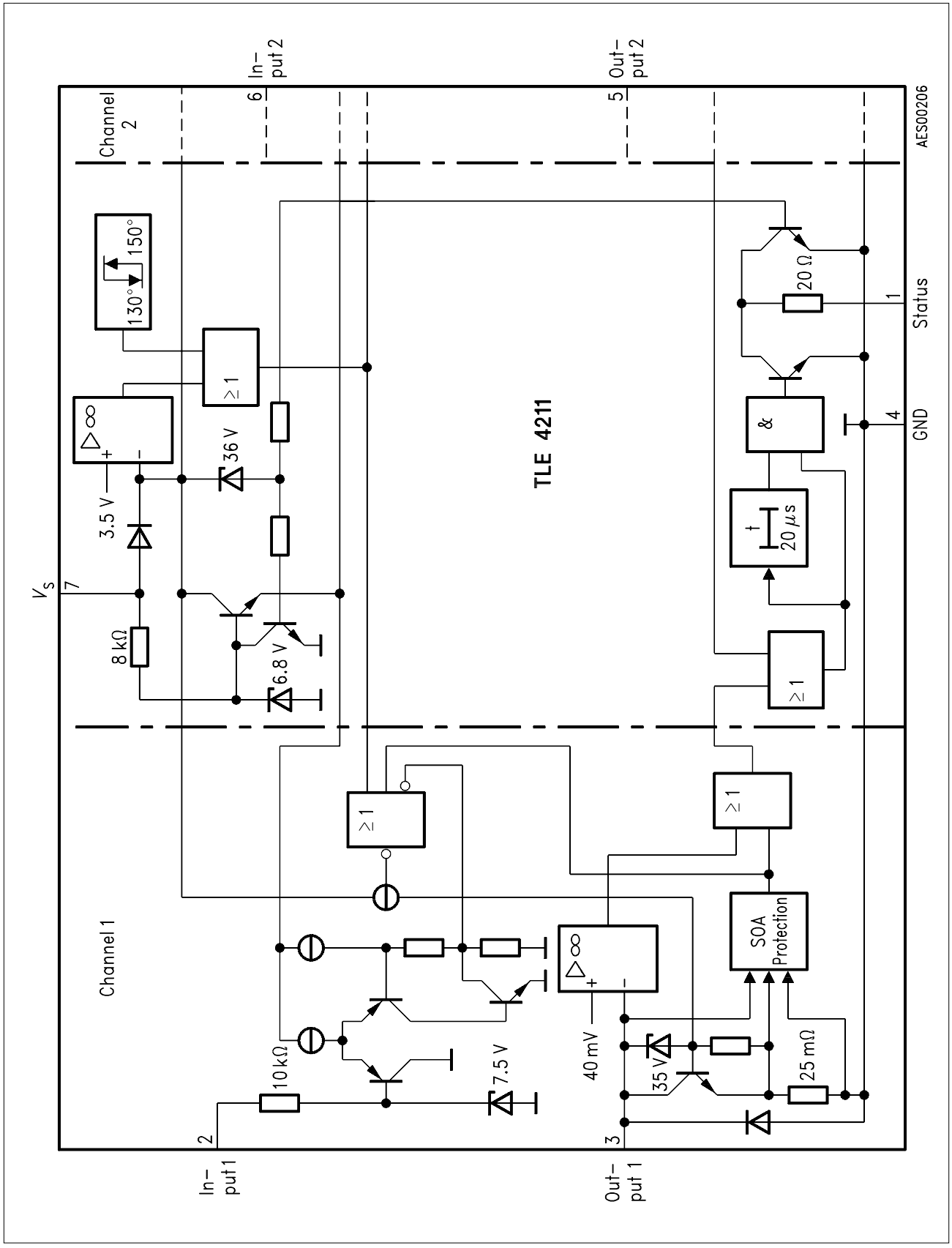
The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp Z-diodes.

Monitoring and Protective Functions

The outputs are monitored for open load, overload, and shorted output to ground (**see table below**). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active low). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated.

Status Output (L = Error)

	Undervoltage	**Operating Range**		**Overvoltage**
		V_I = L (active)	V_I = H (passive)	
Normal function	H	H	H	L
Overload	H	L	H	L
Open load	H	L	H	L
Shorted output to ground	H	L	L	L



Circuit Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage (pin 7) [1]	V_S	– 45	45	V
Supply voltage (pin 7) $t \leq 500$ ms	V_S	–	70	V
Input voltage (pin 2; pin 6)	V_I	– 5	45	V
Output voltage (pin 1)	V_Q	– 0.3	45	V
Currents				
Switching current (pin 3; pin 5)	I_Q	limited internally		
Current with reverse polarity (pin 3; pin 5) $T_C \leq 85$ °C	I_Q	– 2.2	–	A
Output current (pin 1)	I_Q	–	10	mA
Max. current at inductive load	I_Q	–	**see Diagram**	
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	5.6 [2]	20	V
Supply voltage slew rate	dV_S/dV	– 1	1	V/µs
Case temperature	T_C	– 40	125	°C
Thermal resistance				
junction to case	$R_{th\ JC}$	–	4	K/W
junction to ambient	$R_{th\ JA}$	–	65	K/W

[1] Refer to monitoring and protective functions
[2] Lower limit = 4.6 V, if previously V_S greater than 5.6 V (turn-on hysteresis)

Characteristics

V_S = 6 to 18 V and T_j = – 40 to 125 °C

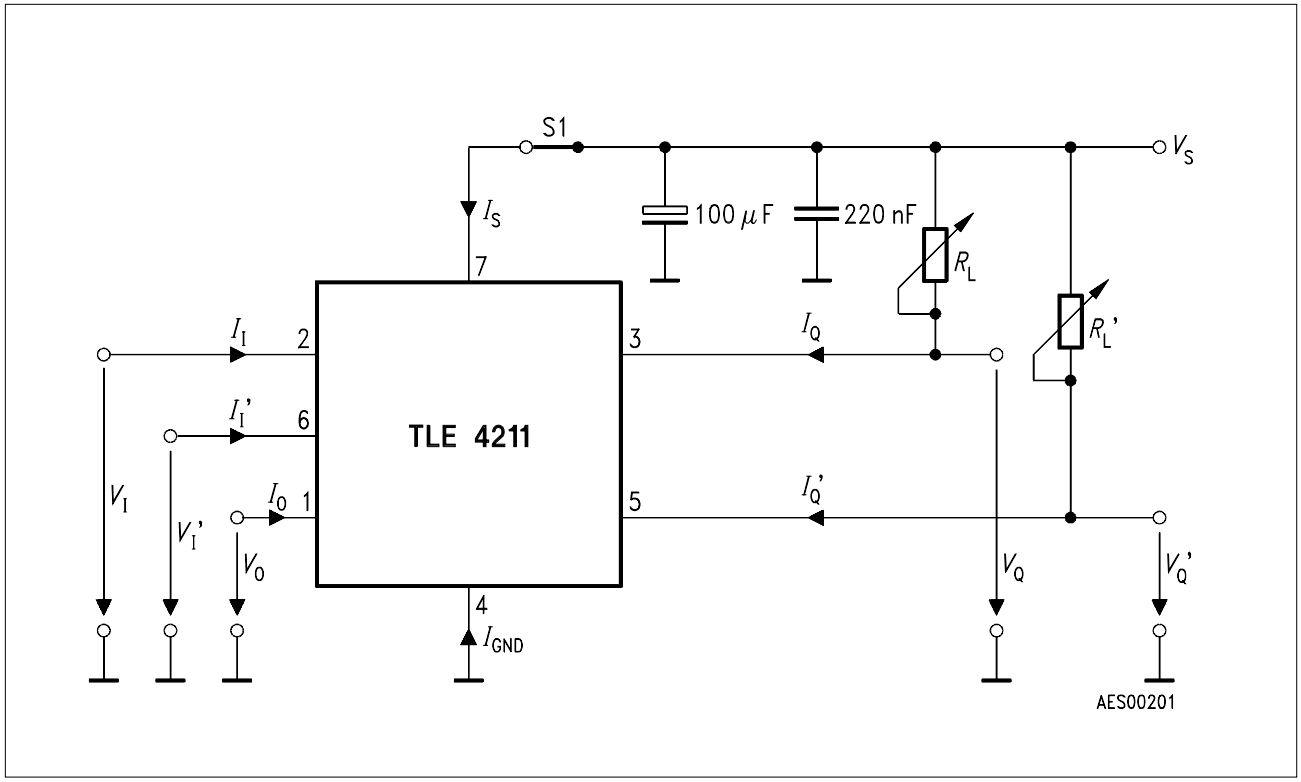
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current	I_S	–	3.5	10	mA	$V_I = V_I > V_{IH}$
Supply voltage	I_S	–	100	180	mA	$V_I = V_I < V_{IL}$
Supply overvoltage shutdown threshold	V_{SO}	34	36	42	V	$I_O = 5$ mA; $V_O < 0.4$ V
Open load error threshold voltage	V_{QU}	–	40	–	mV	$I_O = 5$ mA; $V_O < 0.4$ V
Open load error threshold current	I_{QU}	–	50	120	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	250	mA	$V_{Q1} = V_{Q2} = V_{QU}$
Logic						
Control input H-input voltage L-input voltage	 V_{IH} V_{IL}	 – 0.7	 1.7 1.1	 2.4 –	 V V	 – –
Hysteresis of input voltage	ΔV_I	–	0.6	–	V	–
H-input current L-input current	I_{IH} $-I_{IL}$	– –	– –	10 10	µA µA	$V_I = 5$ V $V_I = 0.5$ V
Status output (open coll.) L-saturation voltage	V_{OSat}	–	–	0.4	V	$I_O = 5$ mA
Status delay time	t_{dS}	12	20	30	µs	[1]

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

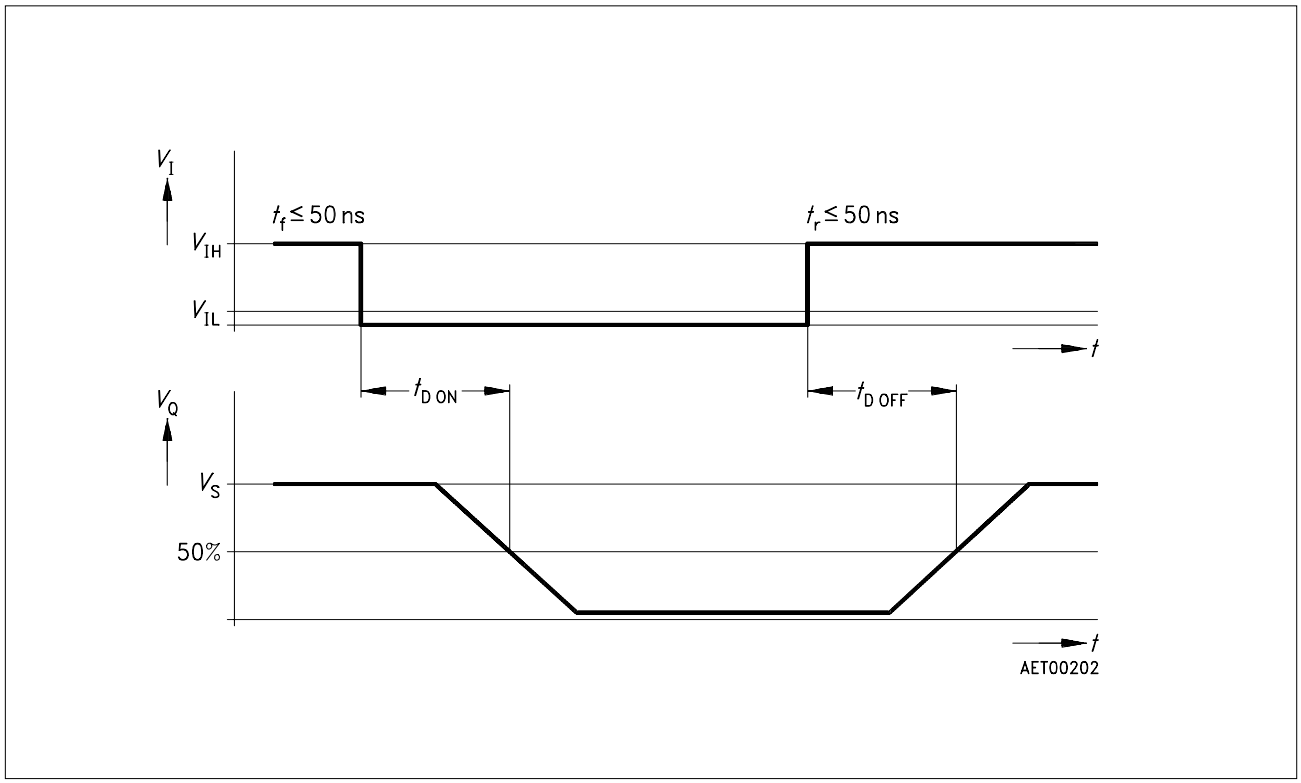
Characteristics (cont'd)

V_S = 6 to 18 V and T_j = – 40 to 125 °C

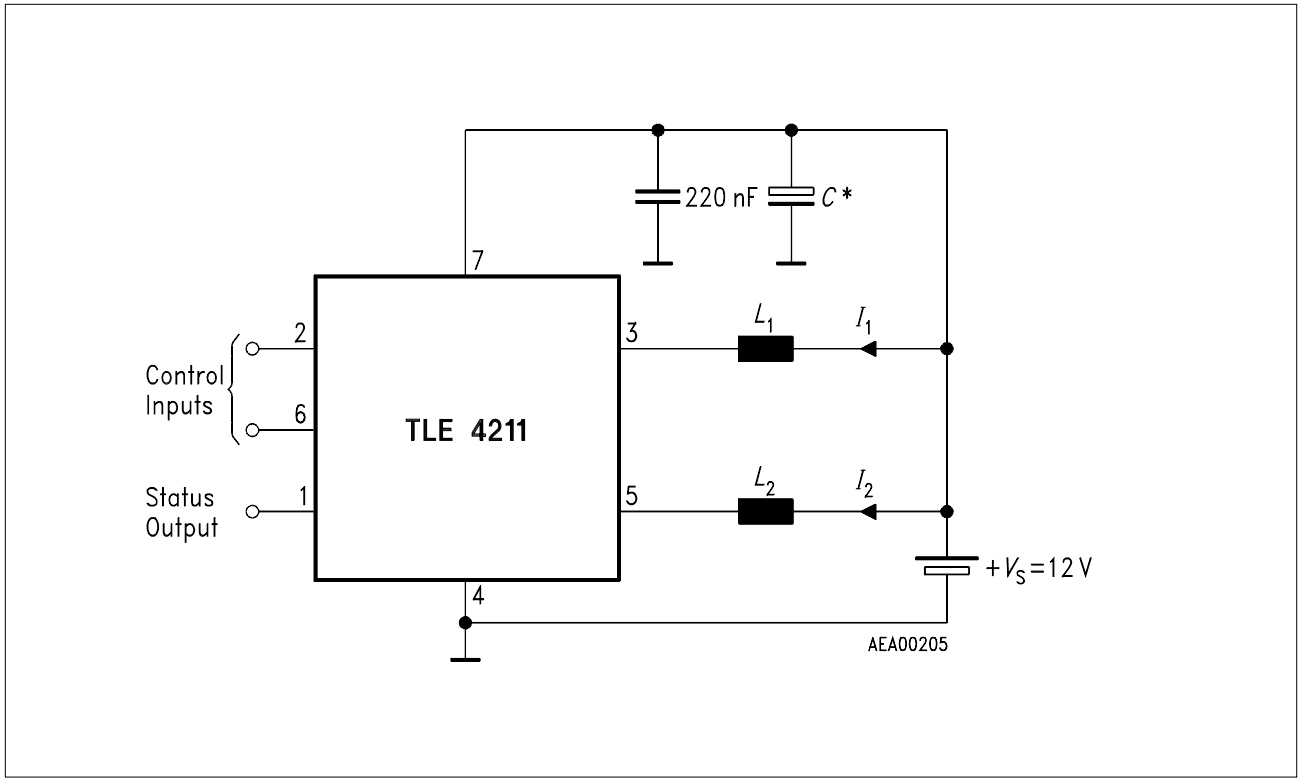
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Output						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 1.6 A; V_I < V_{IL}; T_j = 25 °C
Leakage current	I_Q	–	–	300	µA	V_Q = 6 V; V_I > V_{IH}
Switch-ON time Switch-OFF time	$t_{D\ ON}$ $t_{D\ OFF}$	– –	0.5 2.5	5 10	µs µs	**see Timing Diagram**; I_Q = 1 A
Output voltage Negative clamp	– V_{QF}	–	1.4	1.8	V	I_Q = – 2.0 A
Power Clamp Diode (V_S = 42 V; S_1 open)						
Output voltage positive clamp	V_{QZ}	34	36	40	V	I_Q = 0.1 A
Serial resistance	r_z	–	2	–	Ω	0 A < I_Q < 2 A



Test Circuit



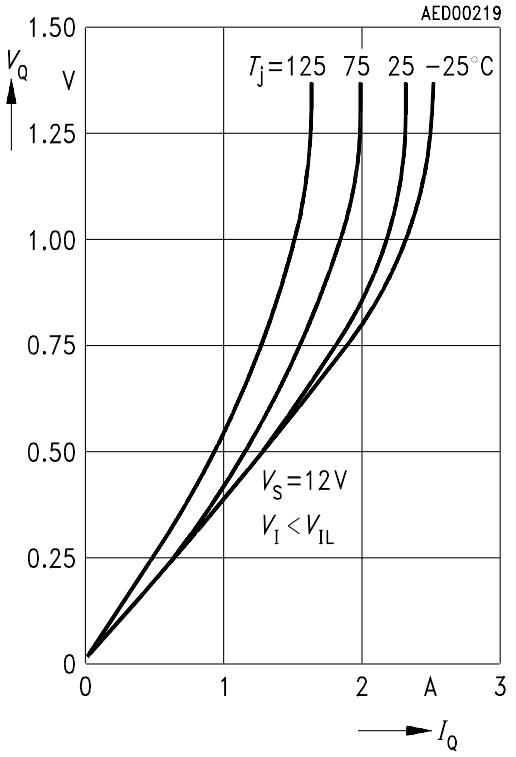
Timing Diagram



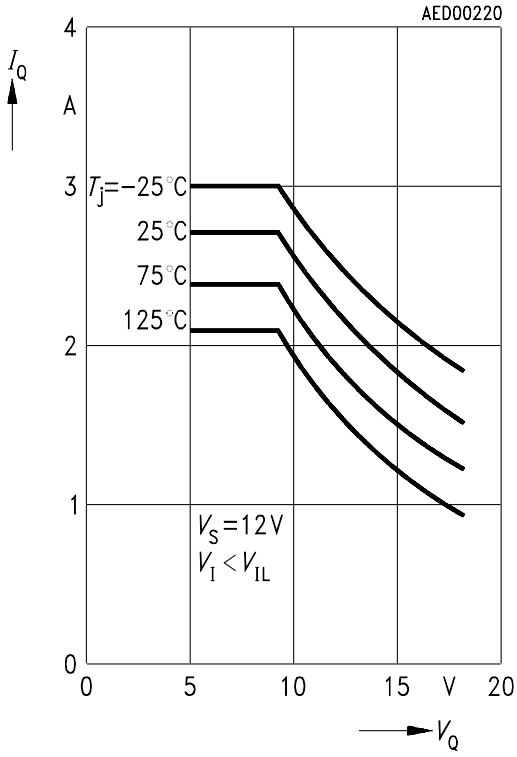
Application Circuit

C* is to be dimensioned such that e.g. in case of a battery voltage failure the maximum ratings of the IC are not exceeded by the recirculation energy L_1, L_2.

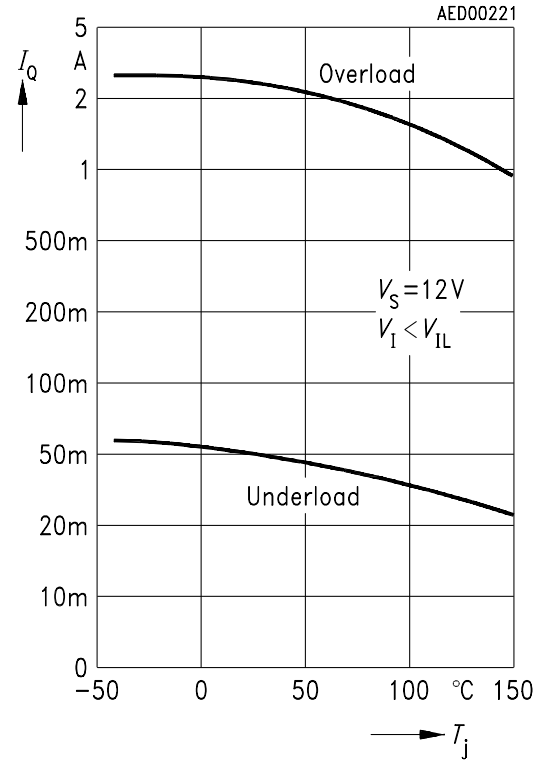
Output Voltage V_Q versus Output Current I_Q



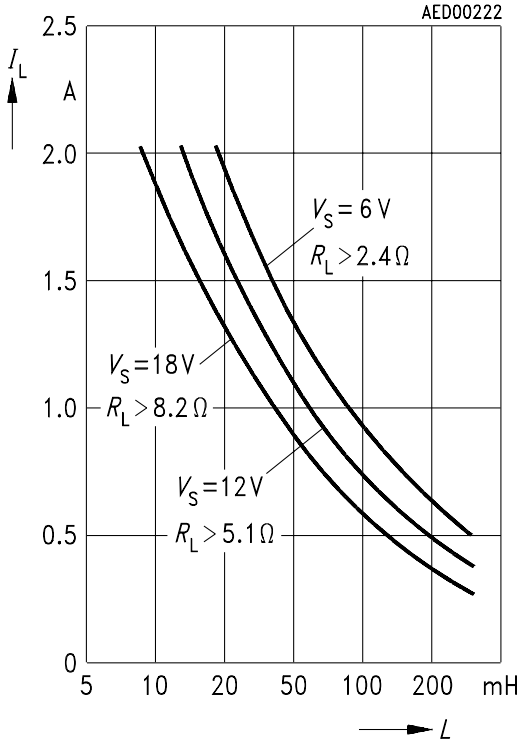
Shorted Load Current I_{Q0} versus Output Voltage V_Q



Status Signal Threshold versus Chip Temperature T_j

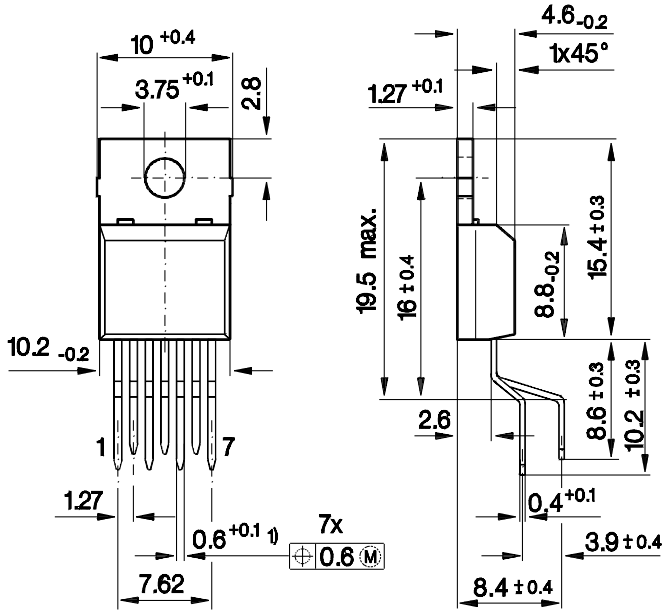


Maximum Load Current I_L versus Load Inductance L



Package Outlines

P-TO220-7-1
(Plastic Transistor Single Outline)



1) 0.75 -0.15 at dam bar (max. 1.8 from body)
1) 0.75 -0.15 im Dichtstegbereich (max. 1.8 vom Körper)

GPT05108

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm