

HiPerFET™ Power MOSFETs Q-Class

IXFK 60N55Q2

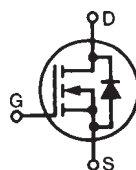
IXFX 60N55Q2

$$\begin{aligned} V_{DSS} &= 550 \text{ V} \\ I_{D25} &= 60 \text{ A} \\ R_{DS(on)} &= 88 \text{ m}\Omega \end{aligned}$$

$$t_{rr} \leq 250 \text{ ns}$$

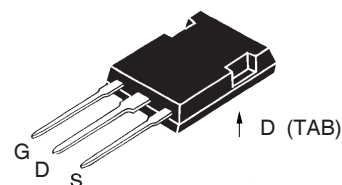
N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low Q_g
Low intrinsic R_g , low t_{rr}

Preliminary Data Sheet

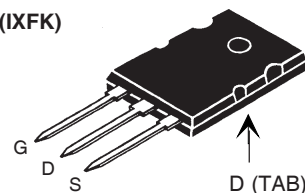


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	550	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	550	V
V_{GS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	60	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	240	A
I_{AR}	$T_C = 25^\circ\text{C}$	60	A
E_{AR}	$T_C = 25^\circ\text{C}$	75	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	4.0	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_g = 2 \Omega$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	735	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.063 in) from case for 10 s	300	$^\circ\text{C}$
M_d	Mounting torque	TO-264	0.9/6 Nm/lb.in.
Weight		PLUS-247	6 g
		TO-264	10 g

PLUS247™ (IXFX)



TO-264 AA (IXFK)



G = Gate
S = Source

D = Drain
TAB = Drain

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ mA}$	550		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	2.0		4.5 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0 \text{ V}$			50 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 \cdot I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2 \%$			88 m Ω

Features

- Double metal process for low gate resistance
- International standard packages
- Epoxy meet UL 94 V-0, flammability classification
- Avalanche energy and current rated
- Fast intrinsic Rectifier

Advantages

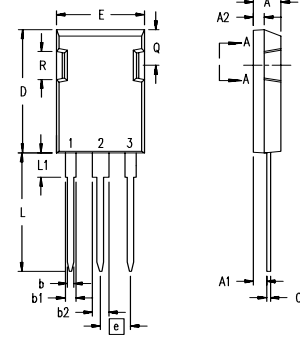
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 0.5 \cdot I_{D25}$, pulse test	30	44	S
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		7300	pF
C_{oss}			1150	pF
C_{rss}			340	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1.0\ \Omega$ (External),		22	ns
t_r			14	ns
$t_{d(off)}$			57	ns
t_f			9	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		200	nC
Q_{gs}			42	nC
Q_{gd}			100	nC
R_{thJC}	TO-264			0.17 K/W
R_{thCK}			0.15	K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			60 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			240 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.5 V
t_{rr}	$I_F = 25\text{ A}, -di/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$			250 ns
Q_{RM}			1	μC
I_{RM}			10	A

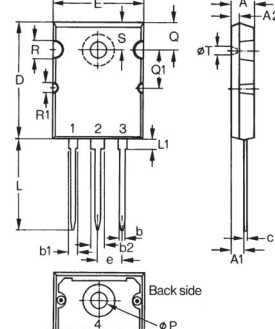
PLUS 247™ Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A ₁	2.29	2.54	.090	.100
A ₂	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b ₁	1.91	2.13	.075	.084
b ₂	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L ₁	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190

TO-264 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A ₁	2.54	2.89	.100	.114
A ₂	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b ₁	2.39	2.69	.094	.106
b ₂	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L ₁	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q ₁	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R ₁	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025	6,404,065B1	6,162,665	6,534,343	6,583,505
4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715	6,306,728B1	6,259,123B1	6,306,728B1	6,683,344

Fig. 1. Output Characteristics
@ 25°C

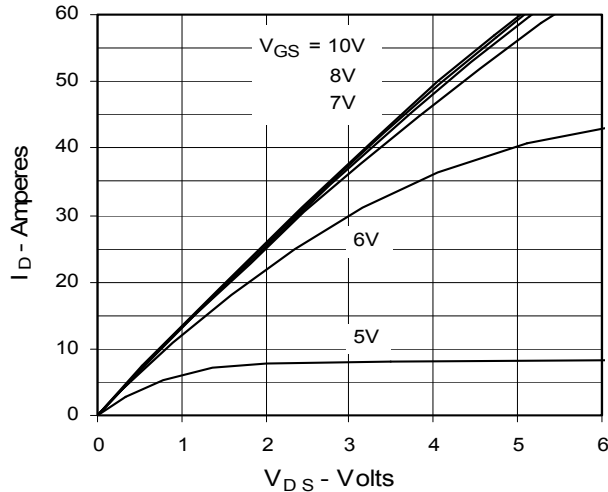


Fig. 2. Extended Output Characteristics
@ 25°C

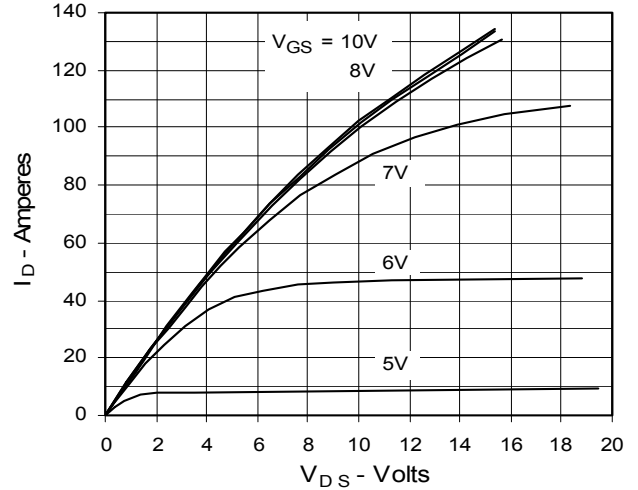


Fig. 3. Output Characteristics
@ 125°C

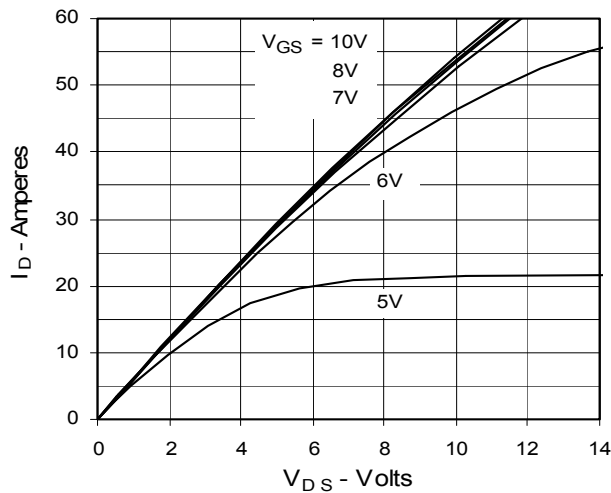


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

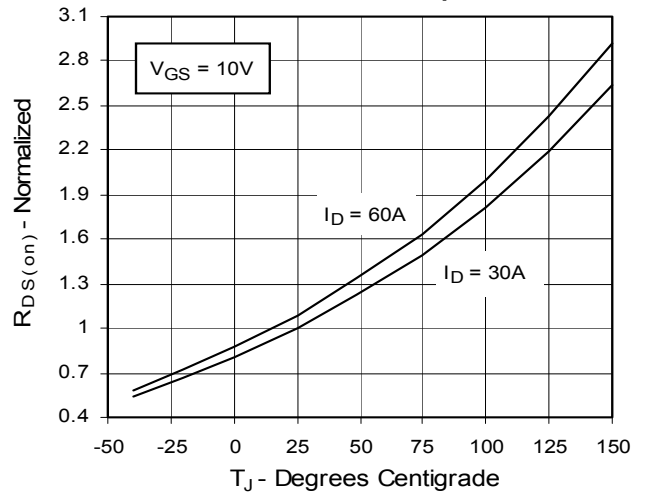


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

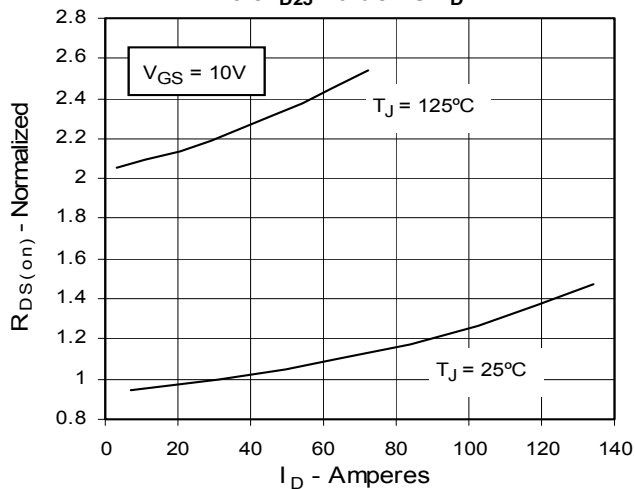


Fig. 6. Drain Current vs. Case Temperature

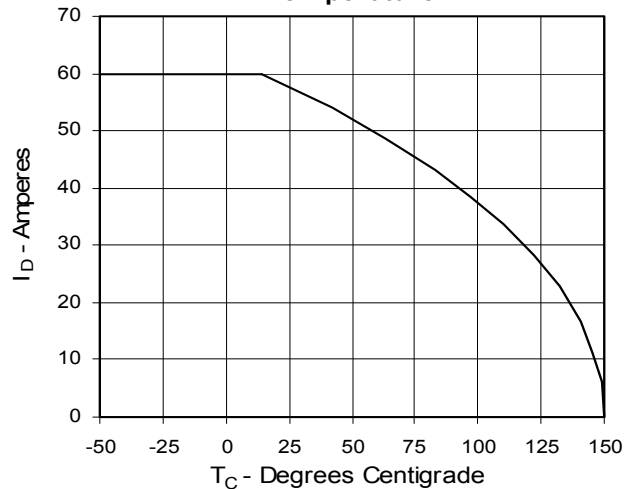


Fig. 7. Input Admittance

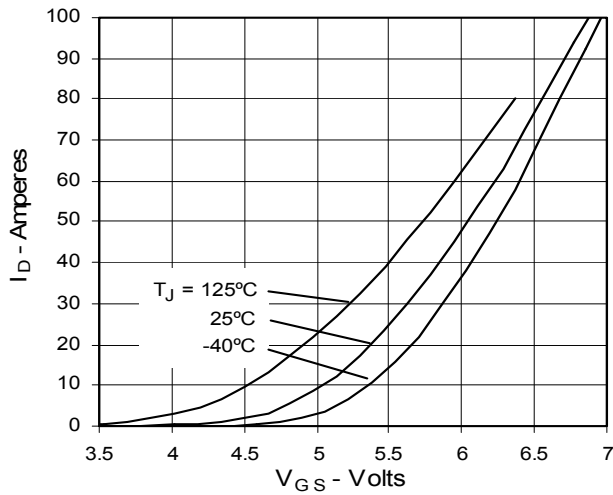


Fig. 8. Transconductance

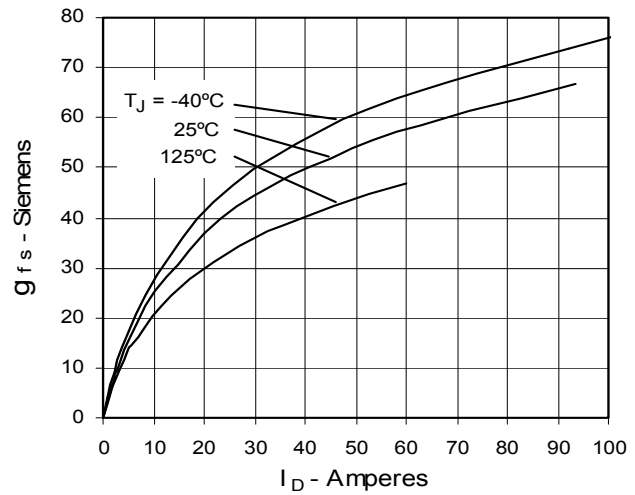


Fig. 9. Source Current vs. Source-To-Drain Voltage

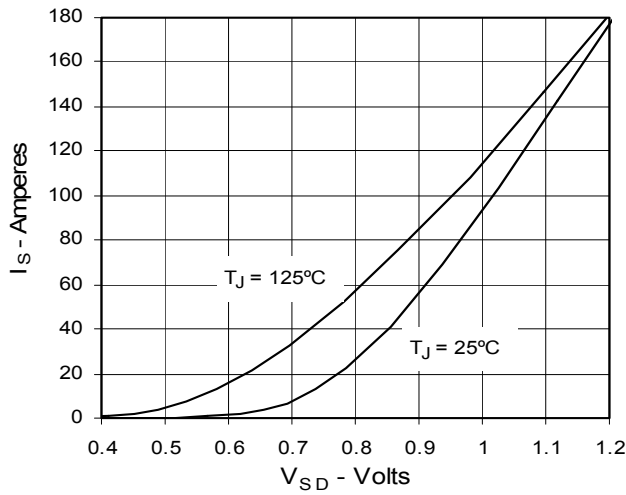


Fig. 10. Gate Charge

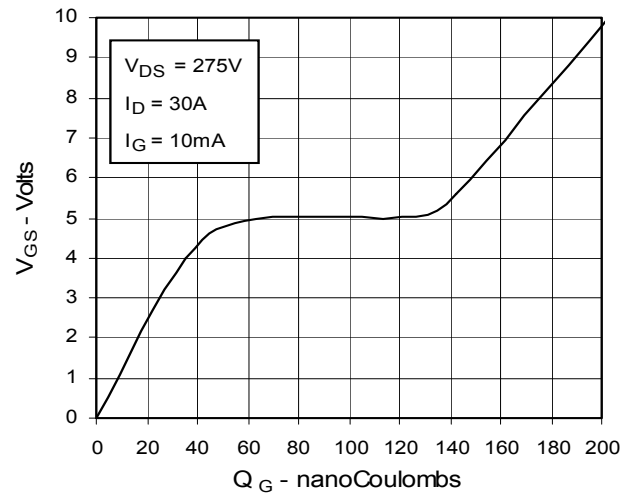


Fig. 11. Capacitance

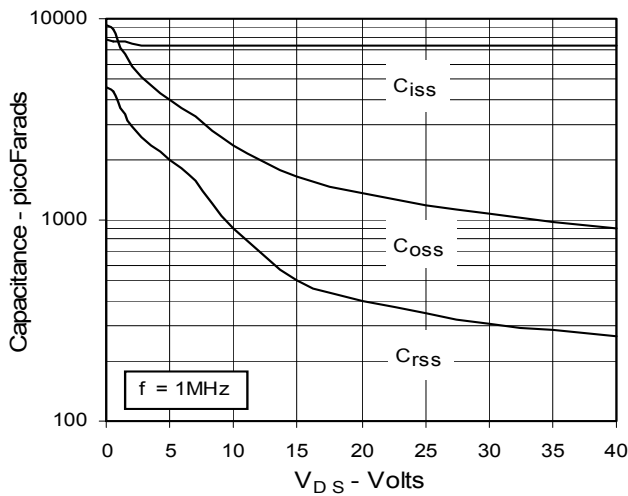
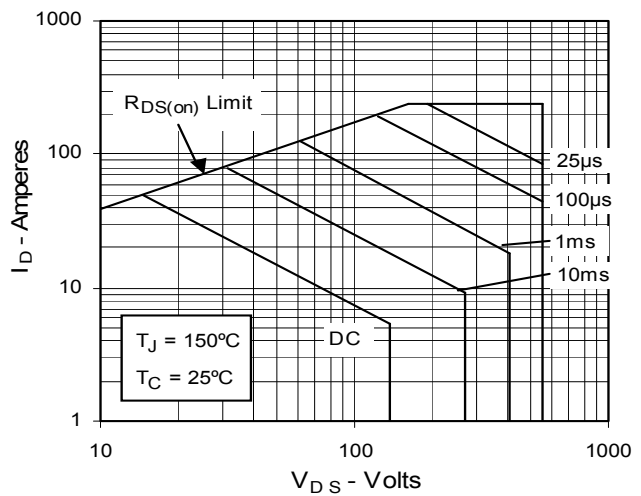


Fig. 12. Forward-Bias Safe Operating Area



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Fig. 13. Maximum Transient Thermal Resistance

