

BGF106C

SIM Card Interface Filter and ESD Protection

Small Signal Discretes



Never stop thinking

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BGF106C

Revision History: 2009-04-14, V2.0

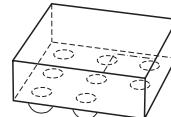
Previous Version: 2009-03-31, V1.0

Page	Subjects (major changes since last revision)
all	target status removed
5	Table 1 : maximum voltage on all pins increased to 5.5 V

BGF106C

Features

- ESD protection circuit and interface filter for SIM cards
- ESD protection according to IEC61000-4-2 for ± 15 kV contact discharge on external IOs
- Wafer level package with SnAgCu solder balls
- 400 μm solder ball pitch
- RoHS and WEEE compliant package

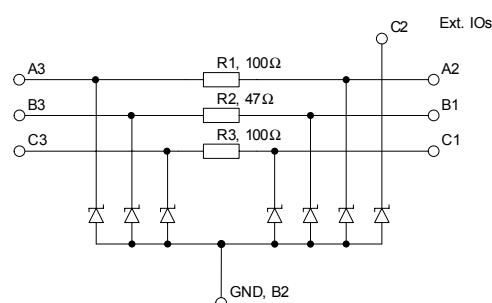


WLP-8-11-N-3D



Description

BGF106C is an ESD protection circuit and filtering interface for SIM cards. All external IOs are protected against ESD pulses of ± 15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green lead-free and halogen-free package with a size of only 1.2 mm x 1.2 mm and a total height of 0.6 mm



BGF106_schematic.vsd

Figure 1 Schematic

Type	Package	Marking	Chip
BGF106C	WLP-8-11	6C	N0727

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	0	–	5.5	V	–
Operating temperature range	T_{OP}	-40	–	+85	°C	–
Storage temperature range	T_{STG}	-65	–	+150	°C	–
Summed up input power for all pins	P_{in}	–	–	60	mW	$T_S < 70 \text{ }^{\circ}\text{C}$

Electrostatic discharge according to IEC61000-4-2

Contact discharge at internal pins A3, B3, C3 to any other pin	V_{ESD}	-2	–	2	kV	–
Contact discharge at external pins A2, B1, C1, C2 to GND	V_{ESD}	-15	–	15	kV	–

Table 2 Electrical Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistors R_1, R_3	$R_{1,3}$	80	100	120	Ω	–
Resistor R_2	R_2	37.6	47	56.4	Ω	–
Reverse current of ESD protection diodes	I_R	–	1	100	nA	$V = 3 \text{ V}$
		–	2	1000	nA	$V = 5 \text{ V}$
Breakdown voltage of ESD diodes	$V_{(BR)}$	6.5	7.8	–	V	$I_{(BR)} = 1 \text{ mA}$
Line capacitance	C_T	–	16.5	20	pF	$V = 0 \text{ V}$
Capacitance of all lines to GND						

 1) at $T_A = 25 \text{ }^{\circ}\text{C}$



Figure 2 Insertion loss, $Z_S=Z_L=50 \Omega$

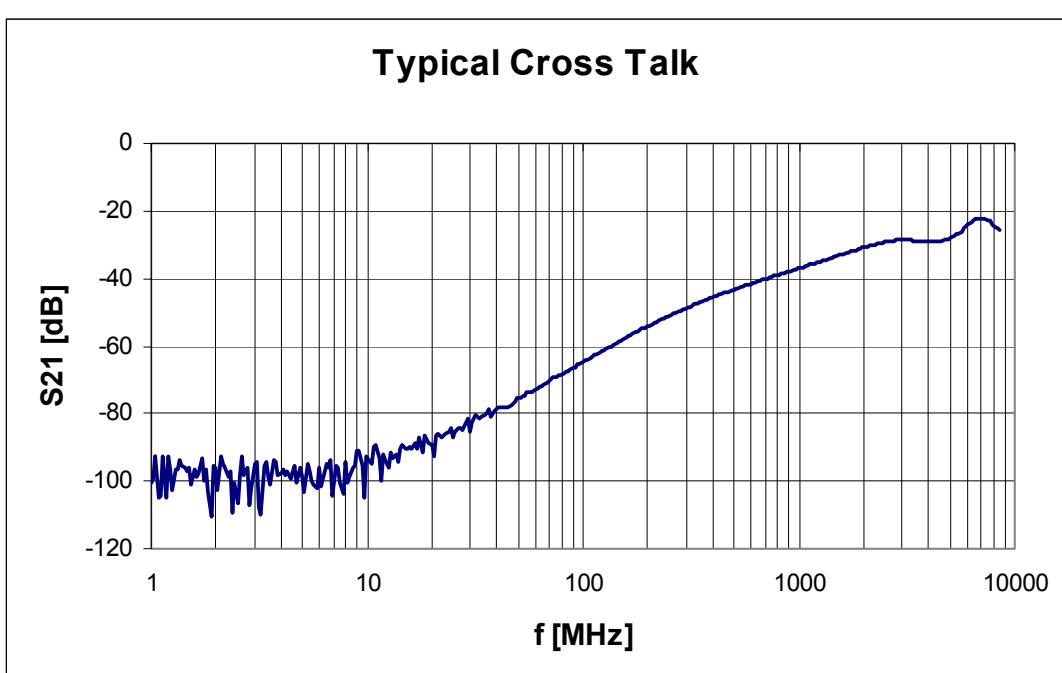


Figure 3 Cross talk, $Z_S=Z_L=50 \Omega$ (all unused input and output pins are terminated with 50Ω)

Package Outlines

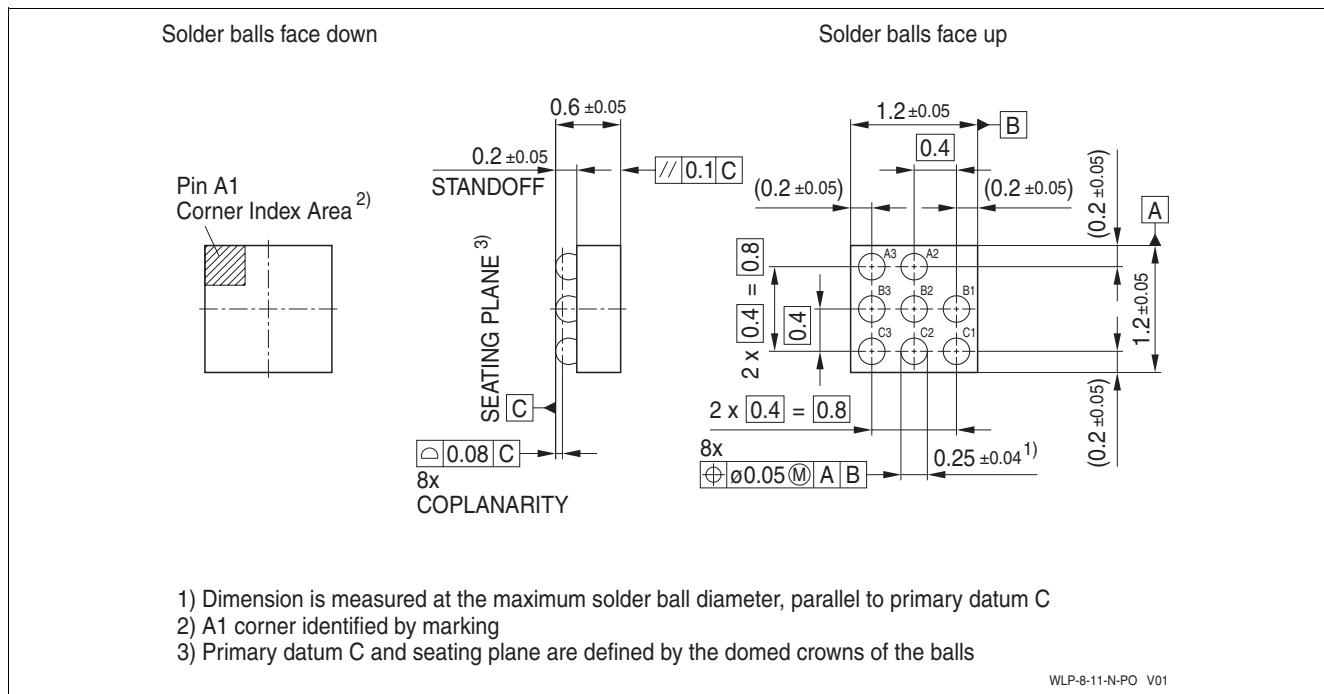


Figure 4 WLP-8-11 (Wafer Level Package)

Footprint

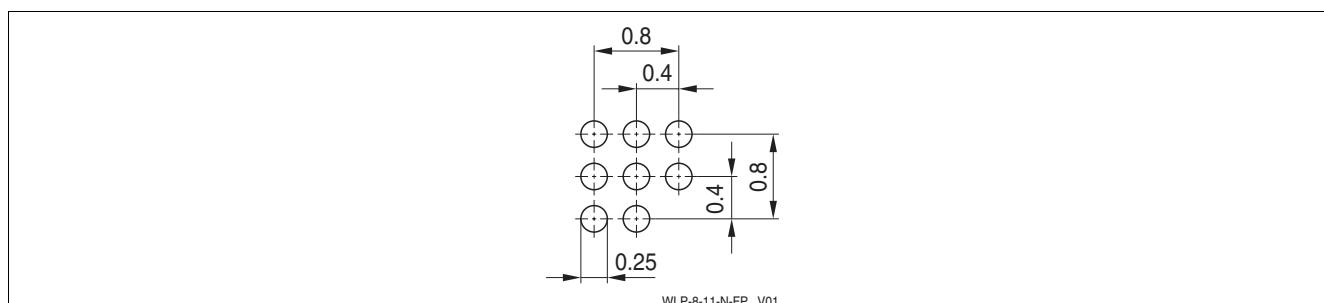


Figure 5 Recommended PCB pad design for reflow soldering

Tape

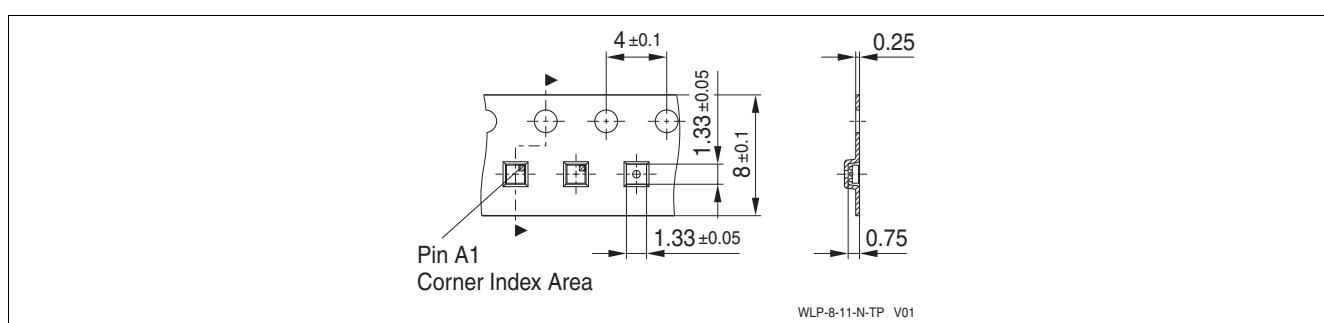


Figure 6 Tape for BGF106C / WLP-8-11

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