

HD74LV123A

Dual Retriggerable Monostable Multivibrators

REJ03D0314-0600Z
(Previous ADE-205-258D (Z))
Rev.6.00
Jun. 02, 2004

Description

The HD74LV123A features output pulse-duration control by three methods. In the first method, the A input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear (CLR) input goes high.

The basic pulse duration is programmed by selecting external resistance and capacitance values.

The external timing capacitor must be connected between Cext and Rext/Cext (positive) and an external resistor connected between Rext/Cext and Vcc

To obtain variable pulse durations, connect an external variable resistance between Rext/Cext and Vcc.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$)
- Output current $\pm 6\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV123AFPEL	SOP-16 pin(JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV123ARPEL	SOP-16 pin(JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV123ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

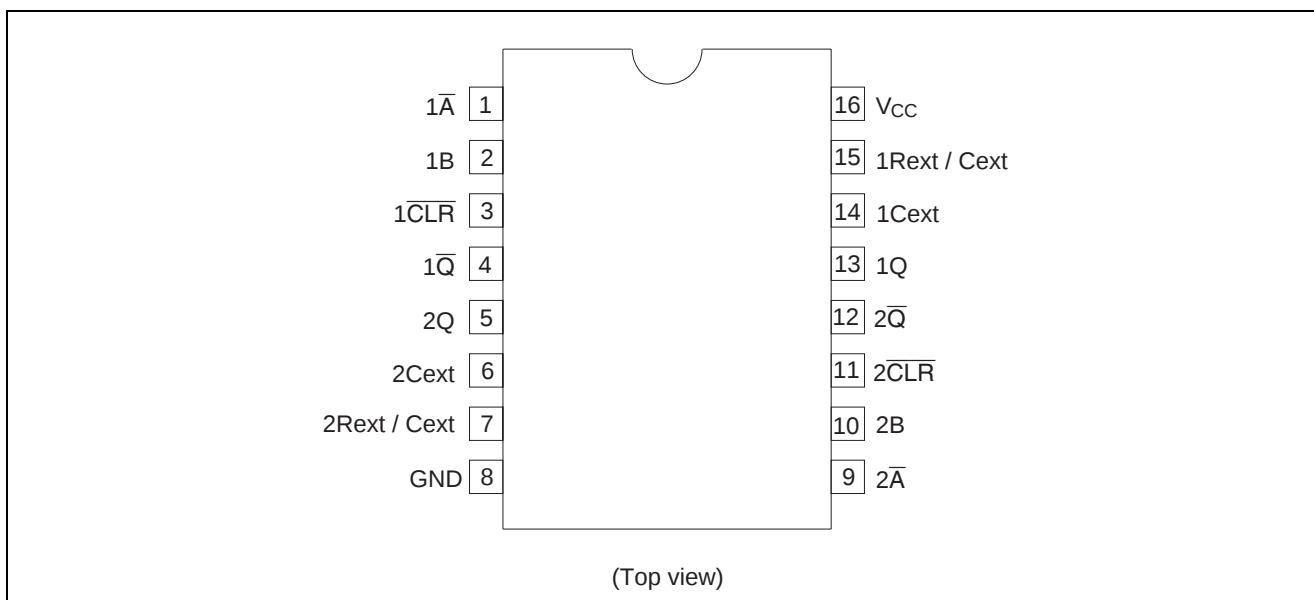
Note: Please consult the sales office for the above package availability.

Function Table

Inputs			Outputs	
$\overline{\text{CLR}}$	$\overline{\text{A}}$	B	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	$\uparrow$	H	H
H	$\downarrow$	H	H	H
$\uparrow$	L	H	H	H

Note: H: High level
 L: Low level
 X: Immaterial
 $\uparrow$: Low to high transition
 $\downarrow$: High to low transition
 H : High level pulse
 H : Low level pulse

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to 7.0	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

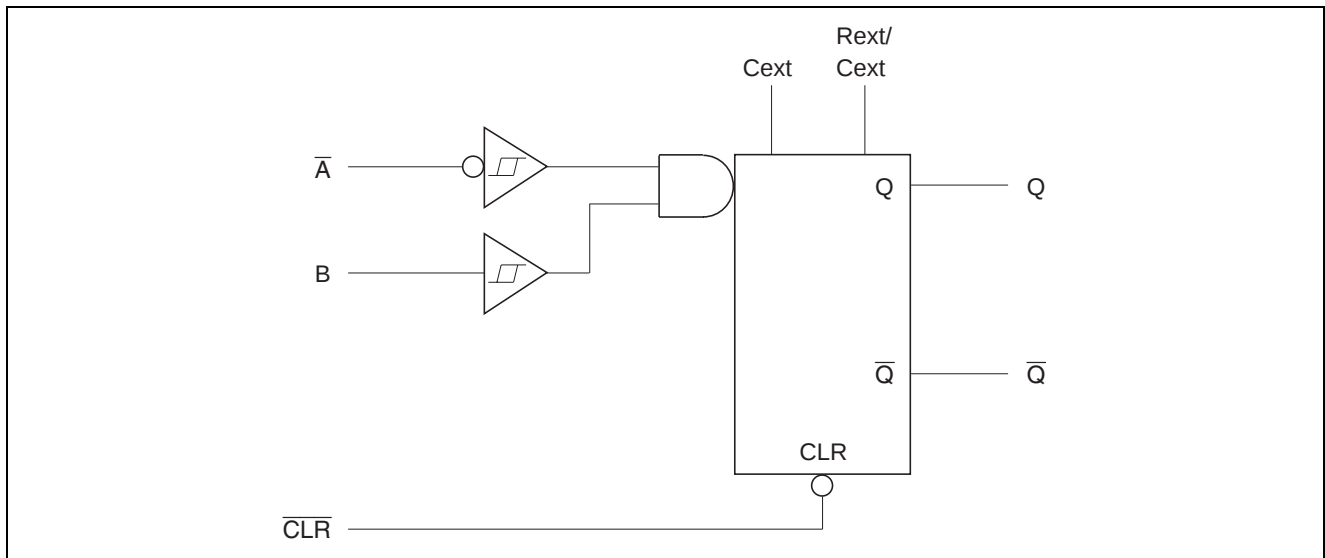
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	—	5.5	V	
Input voltage range	V_I	0	—	5.5	V	
Output voltage range	V_O	0	—	V_{CC}	V	
Output current	I_{OH}	—	—	-50	μA	$V_{CC} = 2.0\text{ V}$
		—	—	-2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	—	-6		$V_{CC} = 3.0$ to 3.6 V
		—	—	-12		$V_{CC} = 4.5$ to 5.5 V
	I_{OL}	—	—	50	μA	$V_{CC} = 2.0\text{ V}$
		—	—	2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	—	6		$V_{CC} = 3.0$ to 3.6 V
		—	—	12		$V_{CC} = 4.5$ to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	—	200	ns/V	$V_{CC} = 2.3$ to 2.7 V
		0	—	100		$V_{CC} = 3.0$ to 3.6 V
		0	—	20		$V_{CC} = 4.5$ to 5.5 V
External timing resistance	R_{ext}	5	—	—	kΩ	$V_{CC} = 2.0\text{ V}$
		1	—	—		$V_{CC} \geq 2.3\text{ V}$
External timing capacitance	C_{ext}	—	Unlimited	—	F	
Power-up ramp rate	$\Delta t / \Delta V_{CC}$	1	—	—	ms/V	
Operating free-air temperature	T_a	-40	—	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} × 0.7	—	—		
		3.0 to 3.6	V _{CC} × 0.7	—	—		
		4.5 to 5.5	V _{CC} × 0.7	—	—		
	V _{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	V _{CC} × 0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -6 mA
		4.5	3.8	—	—		I _{OH} = -12 mA
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Input current Rext / Cext	I _{IN}	5.5	—	—	±2.5	μA	V _{IN} = V _{CC} or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Active state supply current (per circuit)	ΔI _{CC}	2.3	—	—	220	μA	V _{IN} = V _{CC} or GND Rext/Cext = 0.5 V _{CC}
		3.0	—	—	280		
		4.5	—	—	650		
		5.5	—	—	975		
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V
Input capacitance	C _{IN}	3.3	—	4.0	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	13.5	31.4	1.0	37.0	ns	C _L = 15 pF	A or B	Q or $\overline{Q}$
	t _{PHL}	—	16.0	36.0	1.0	42.0		C _L = 50 pF		
		—	11.0	25.0	1.0	29.5		C _L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	13.0	32.8	1.0	34.5		C _L = 50 pF		
		—	14.0	33.4	1.0	39.0		C _L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	16.0	38.0	1.0	44.0		C _L = 50 pF	(Trigger)	
Output pulse width	t _{wQ}	—	170	260	—	320	ns	C _L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	μs	C _L = 50 pF, Cext = 0.01 μF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C _L = 50 pF, Cext = 0.1 μF, Rext = 10 kΩ		
	Δt _{wQ}	—	±1	—	—	—	%	C _L = 50 pF		
Pulse width	t _w	6.0	—	—	6.5	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Retrigger time	t _{rr}	—	40	—	—	—	ns	$\overline{A}$, or B (Rext = 1 kΩ, Cext = 100 pF)		
		—	1.5	—	—	—	μs	$\overline{A}$, or B (Rext = 1 kΩ, Cext = 0.01 μF)		

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	9.7	20.6	1.0	24.0	ns	C _L = 15 pF	A or B	Q or $\overline{Q}$
	t _{PHL}	—	11.5	24.1	1.0	27.5		C _L = 50 pF		
		—	8.0	15.8	1.0	18.5		C _L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	9.5	19.3	1.0	22.0		C _L = 50 pF		
		—	9.9	22.4	1.0	26.0		C _L = 15 pF	$\overline{CLR}$	Q or $\overline{Q}$
		—	11.5	25.9	1.0	29.5		C _L = 50 pF	(Trigger)	
Output pulse width	t _{wQ}	—	150	240	—	300	ns	C _L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	μs	C _L = 50 pF, Cext = 0.01 μF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C _L = 50 pF, Cext = 0.1 μF, Rext = 10 kΩ		
	Δt _{wQ}	—	±1	—	—	—	%	C _L = 50 pF		
Pulse width	t _w	5.0	—	—	5.0	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Retrigger time	t _{rr}	—	30	—	—	—	ns	$\overline{A}$, or B (Rext = 1 kΩ, Cext = 100 pF)		
		—	1.2	—	—	—	μs	$\overline{A}$, or B (Rext = 1 kΩ, Cext = 0.01 μF)		

Switching Characteristics (cont)

$$V_{CC} = 5.0 \pm 0.5 \text{ V}$$

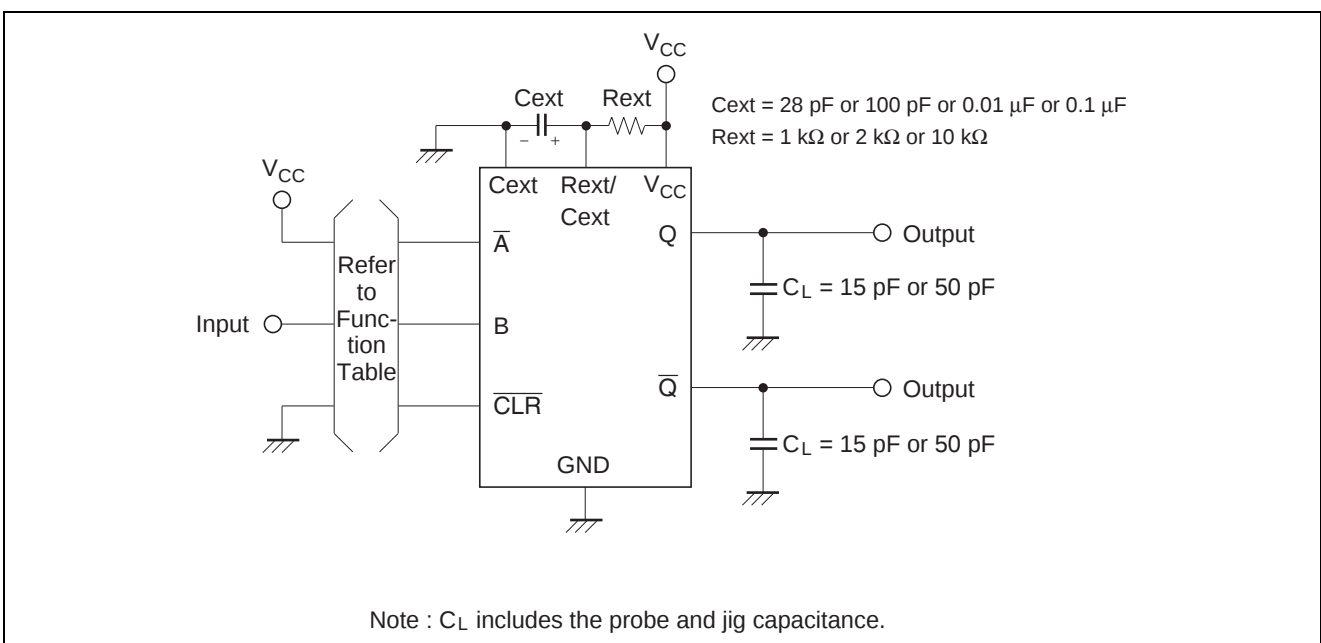
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	7.3	12.0	1.0	14.0	ns	$C_L = 15 \text{ pF}$	A or B	Q or $\bar{Q}$
	t_{PHL}	—	8.5	14.0	1.0	16.0		$C_L = 50 \text{ pF}$		
		—	5.9	9.4	1.0	11.0		$C_L = 15 \text{ pF}$	$\bar{CLR}$	Q or $\bar{Q}$
		—	7.5	11.4	1.0	13.0		$C_L = 50 \text{ pF}$		
		—	7.3	12.9	1.0	15.0		$C_L = 15 \text{ pF}$	$\bar{CLR}$	Q or $\bar{Q}$
		—	8.7	14.9	1.0	17.0		$C_L = 50 \text{ pF}$	(Trigger)	
Output pulse width	t_{wQ}	—	140	200	—	240	ns	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$		
		90	100	110	90	110	μs	$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \text{ }\mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$		
		0.9	1.0	1.1	0.9	1.1	ms	$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \text{ }\mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$		
	Δt_{wQ}	—	± 1	—	—	—	%	$C_L = 50 \text{ pF}$		
Pulse width	t_w	5.0	—	—	5.0	—	ns	$\bar{A}$, B or $\bar{CLR}$		
Retrigger time	t_{rr}	—	20	—	—	—	ns	$\bar{A}$, or B ($R_{ext} = 1 \text{ k}\Omega$, $C_{ext} = 100 \text{ pF}$)		
		—	0.95	—	—	—	μs	$\bar{A}$, or B ($R_{ext} = 1 \text{ k}\Omega$, $C_{ext} = 0.01 \text{ }\mu\text{F}$)		

Operating Characteristics

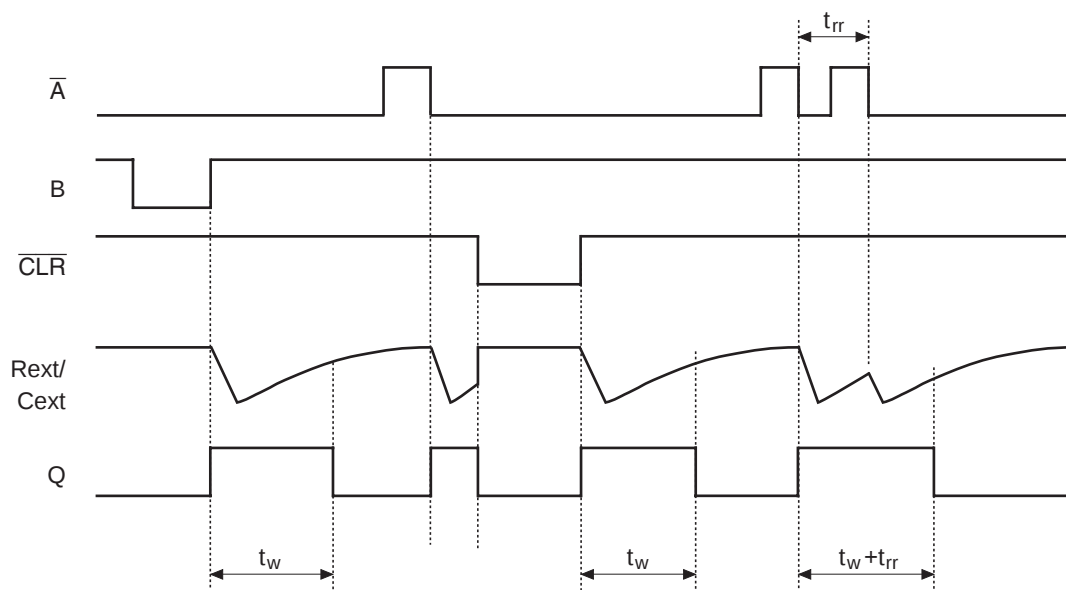
$$C_L = 50 \text{ pF}$$

Item	Symbol	$V_{CC} \text{ (V)}$	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	74.0	—	pF	$f = 10 \text{ MHz}$
		5.0	—	86.0	—		

Test Circuit



Timing diagram



Caution in use

In order to prevent any malfunctions due to noise, connect a high frequency performance capacitor between Vcc and GND, and keep the wiring between the External components and Cext, Rext/Cext pins as short as possible.

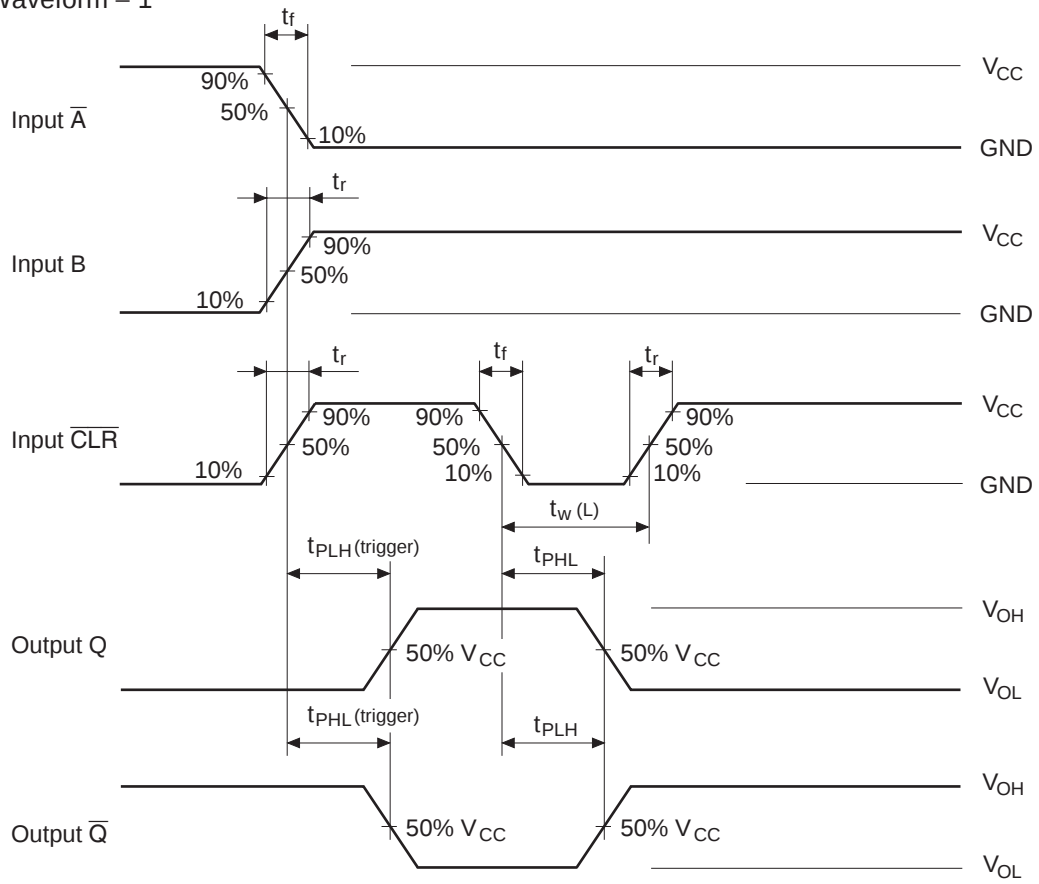
Large values of Cext may cause problems when powering down the HD74LV123A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from Vcc through the protection diodes at pin 7 or pin 15.

Current through the input protection diodes must be limited to 20 mA; therefore, the turn-off time of the Vcc power supply must not be faster than $t = V_{cc} \cdot C_{ext} / (20 \text{ mA})$. For example, if $V_{cc} = 5 \text{ V}$ and $C_{ext} = 22 \mu\text{F}$, the Vcc supply must turn off no faster than $t = (5 \text{ V}) \cdot (22 \mu\text{F}) / 20 \text{ mA} = 5.5 \text{ ms}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

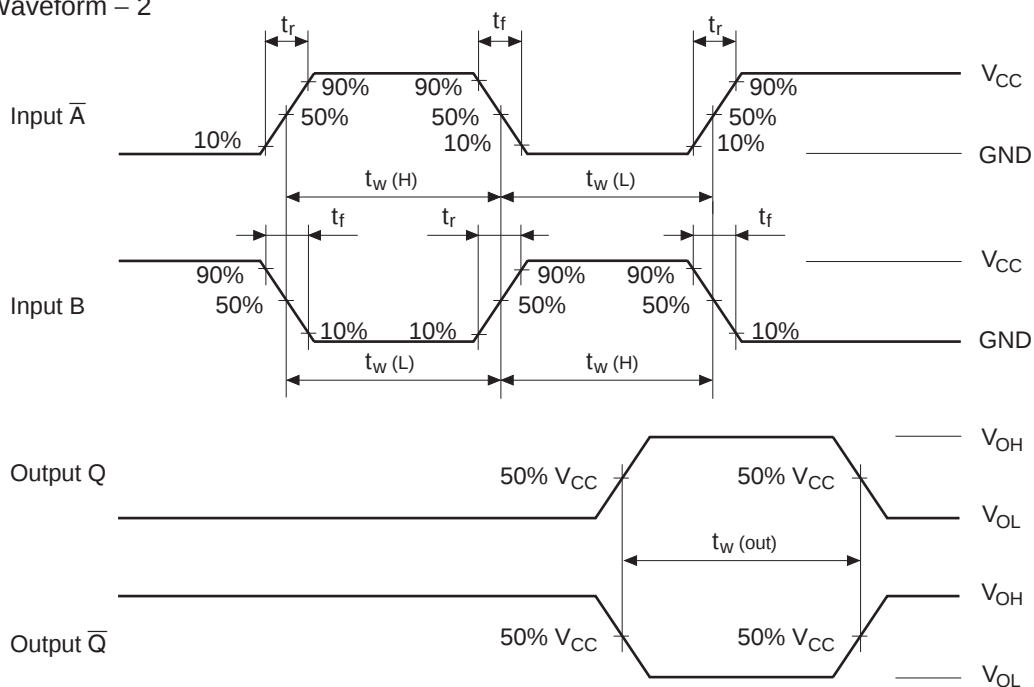
When a more rapid decrease of Vcc to zero volts occurs, the HD74LV123A may sustain damage. To avoid this possibility, use an external clamping diode.

The input pins for unused circuit should be used under conditions to fix the outputs to avoid malfunction caused by noises. Also, it's recommended that Rext / Cext terminals are open and external parts are not connected to.

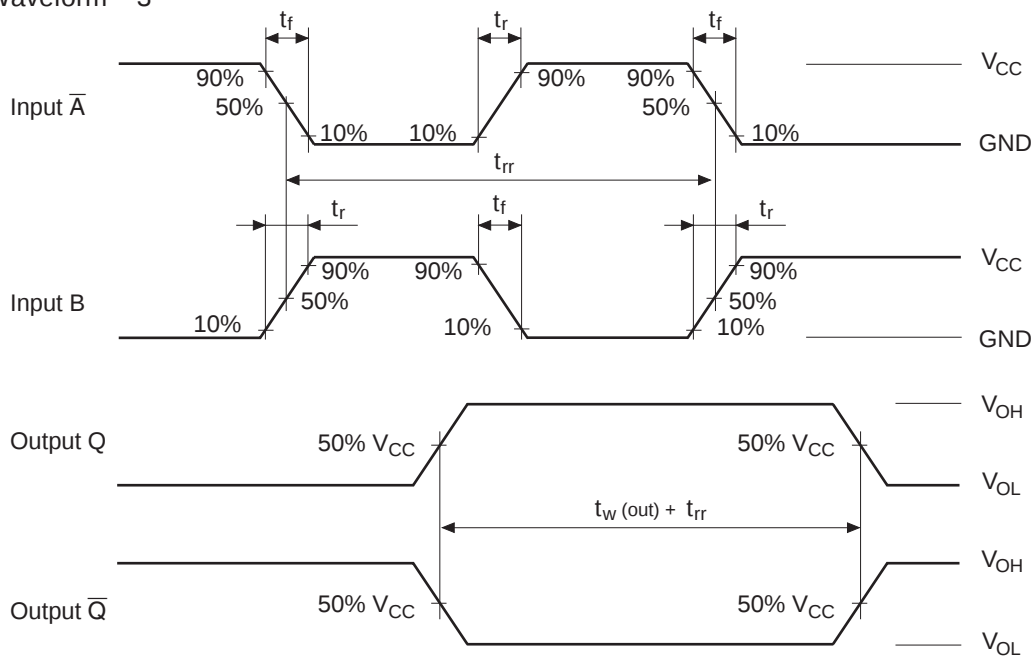
• Waveform – 1



• Waveform – 2

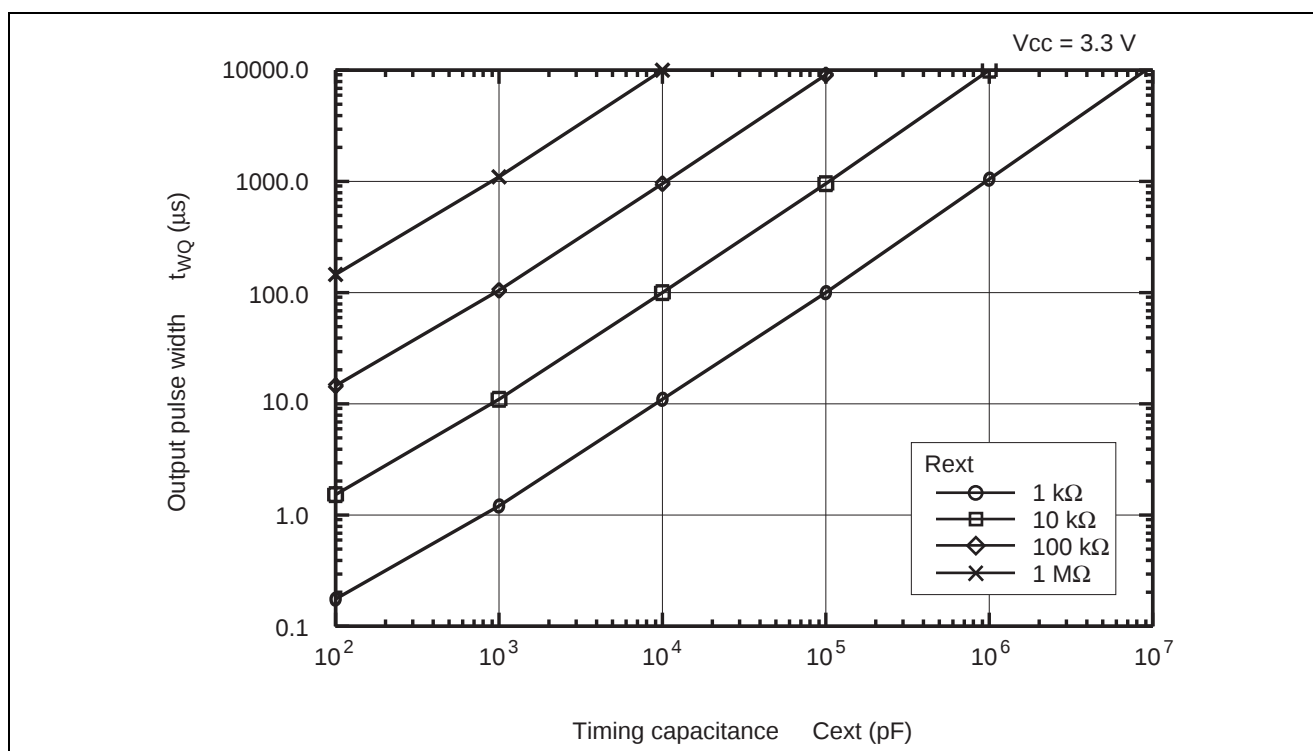
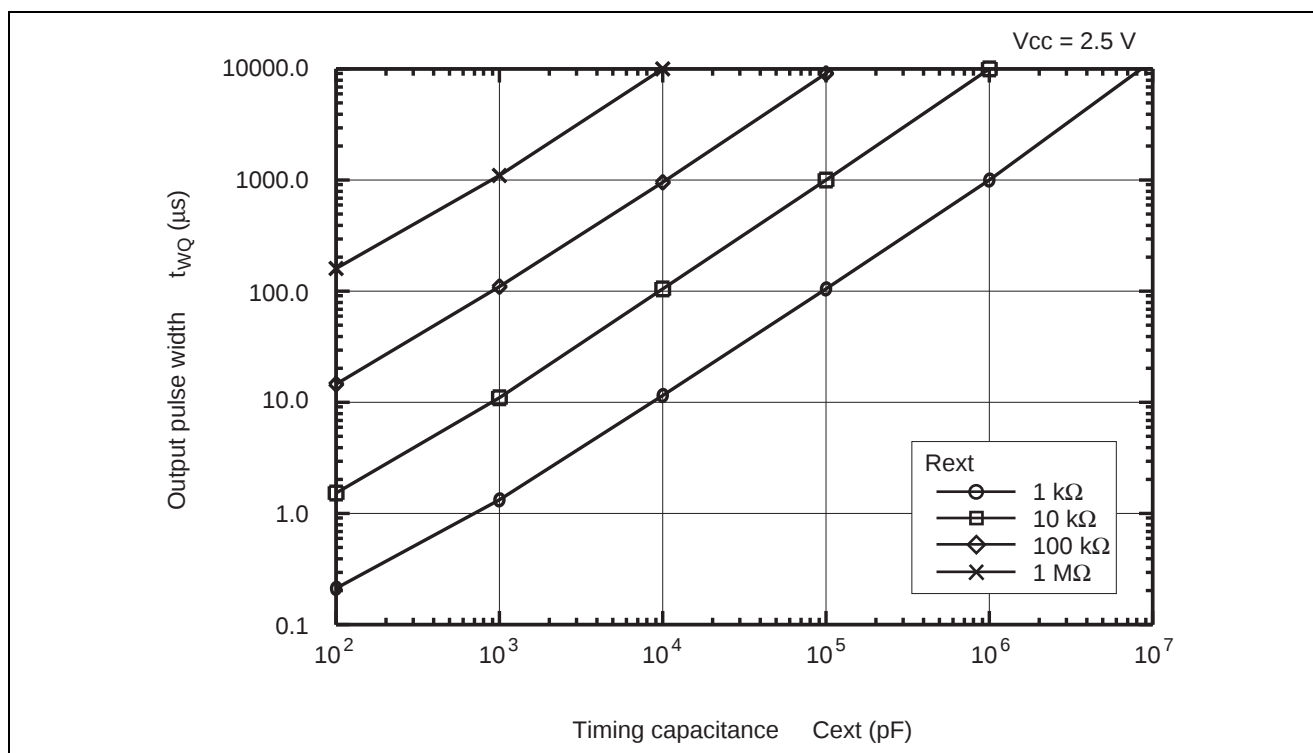


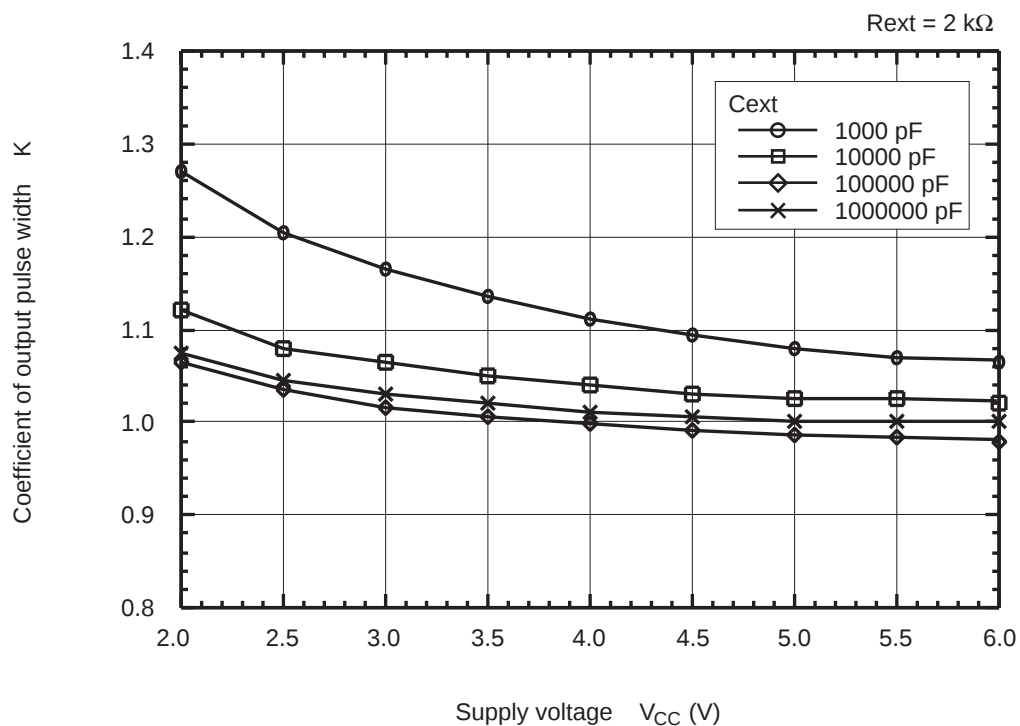
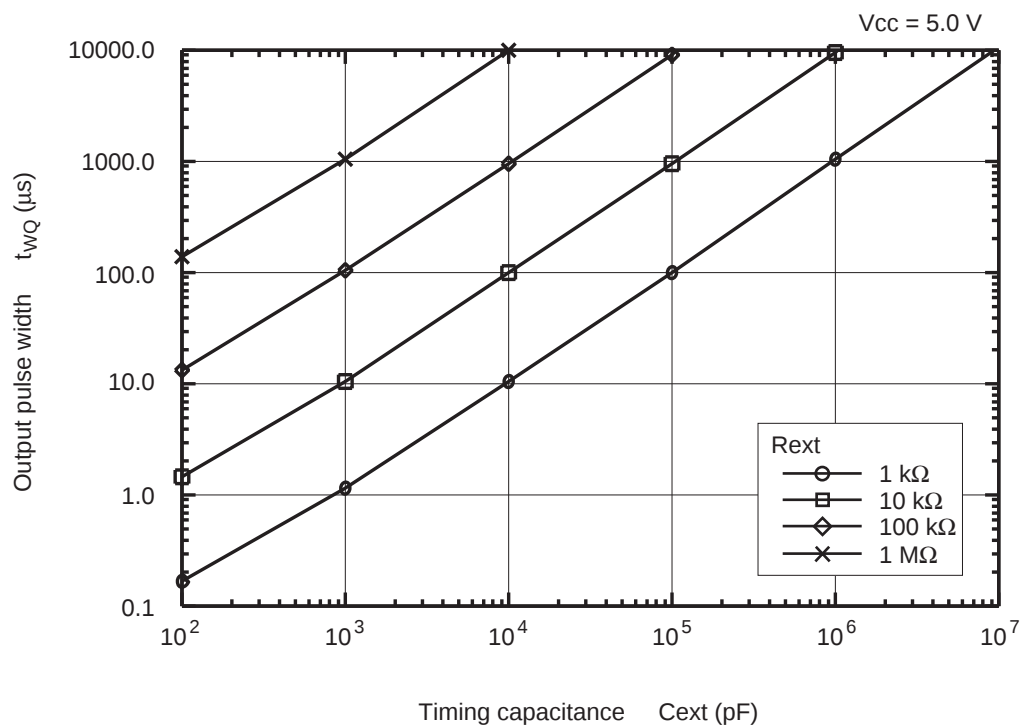
• Waveform – 3

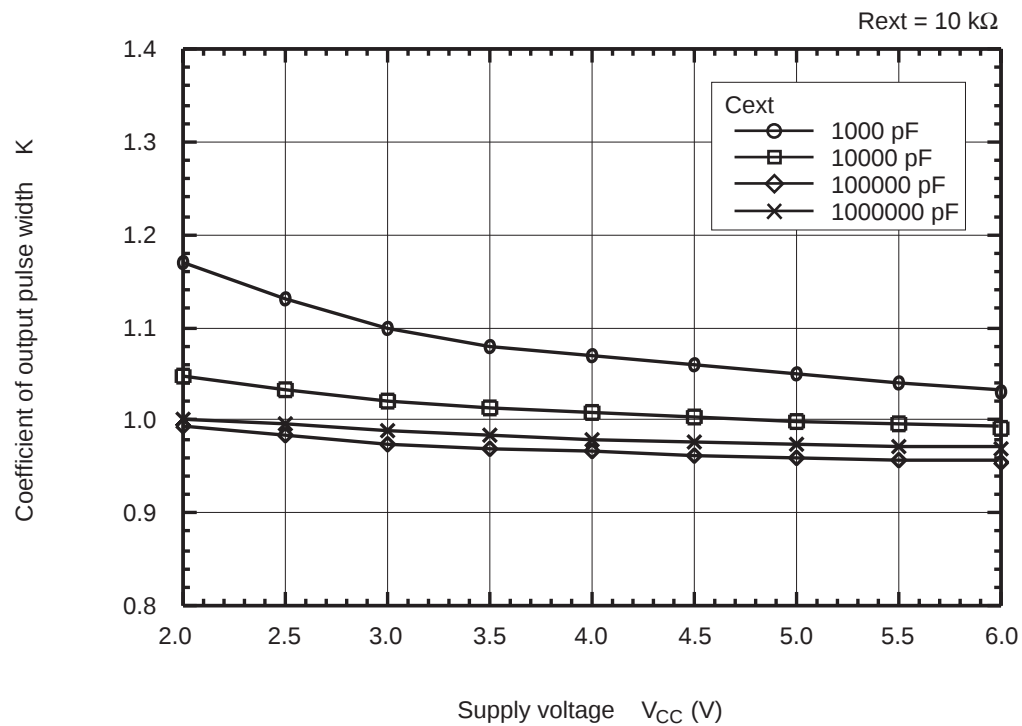


Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

Application Data



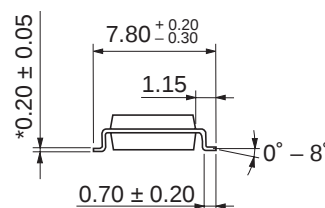
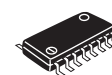
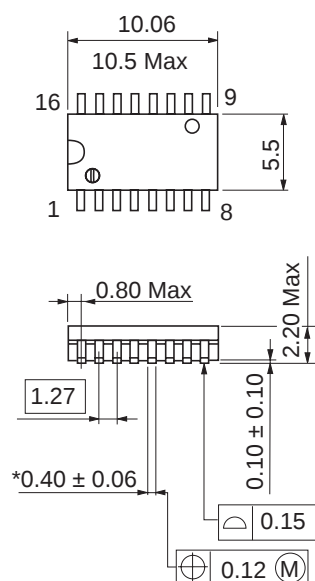




Package Dimensions

As of January, 2003

Unit: mm

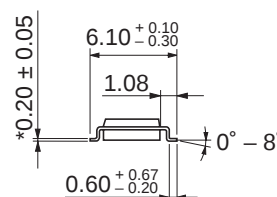
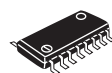
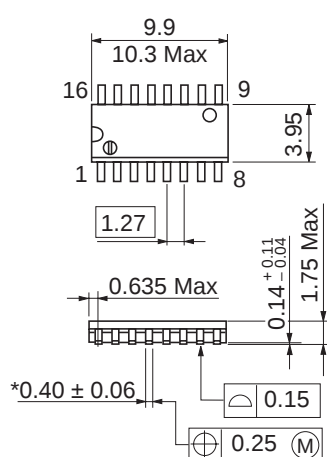


*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003

Unit: mm

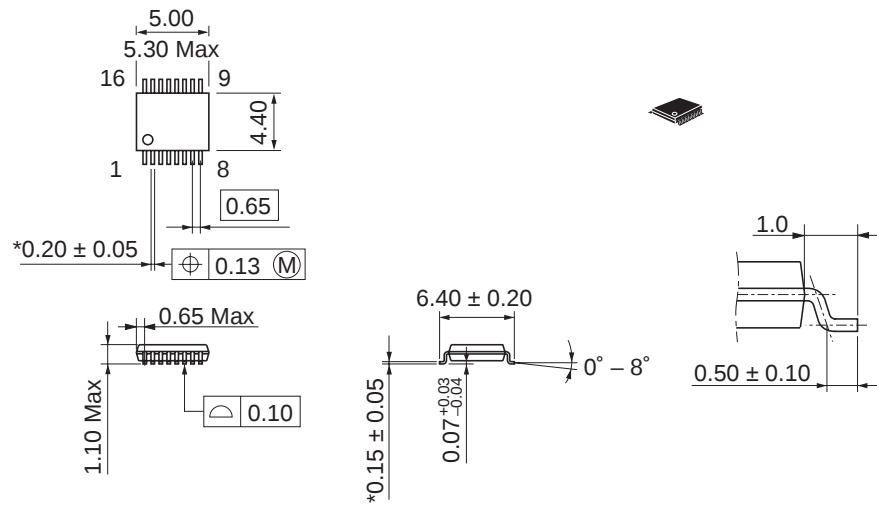


*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001