

□ MN102H51K

Type	MN102H51K		
ROM (x16-bit)	256 K		
RAM (x16-bit)	8 K		
Package (Old Package)	SDIP064-P-0750C *Pb free (SDIP064-P-0750)		
Minimum Instruction Execution Time	83 ns (at 3.6 V to 3.0 V, 12 MHz)		
Interrupts	External (6 lines) Internal (30 lines) : Timer × 11, A/D × 1, Undefined command × 1, RESET × 1, OSD × 2, Serial × 4, I ² C × 1, Caption × 4, Remote control × 1, Address coincidence × 4		
Timer Counter	8-bit timer × 4 16-bit timer × 2 Watchdog timer: 17-bit × 1		
Serial Interface	I ² C × 1: for multimaster mode, bus line (output) has 2 systems Sync serial / I ² C (master) / UART × 2		
Caption	• Built-in sync separator × 2		
I/O Pins	I/O	50	• Common use
A/D Inputs	8-bit × 12-ch. (with S/H)		
D/A Inputs	4-bit × 4-ch. (analog R, G, B, YM output)		
PWM	8-bit × 7-ch.		
Special Ports	Remote control reception		
CRTC	3-layer display (graphics, characters, splits)		
Notes	Remote control input discriminant circuit built-in		
Electrical Characteristics			

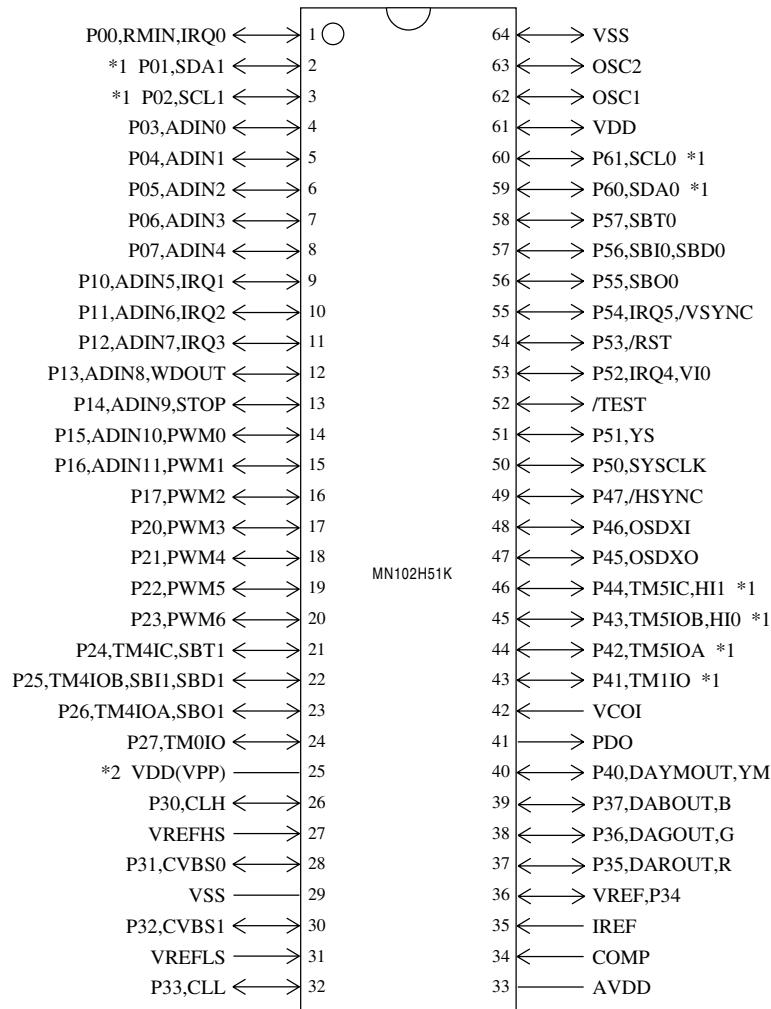
D/A characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
D/A full-scale output current	IFS	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	4.5	5.0	5.5	mA
D/A output voltage setting range	VO	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ	0.9		1.1	V
D/A non-linear error	NLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			±0.5	LSB
D/A differential non-linear error	DNLE	RL = 200 Ω, VREF = 1.2 V, RIREF = 1.2 kΩ			±0.5	LSB
D/A channel interval error	IFS	VREF = 1.2 V, RIREF = 1.2 kΩ, Error from 4-channel average IFS			±5	%

(Ta = 25°C, VDD = AVDD = 3.3 V, VSS = 0 V, fosc = 4 MHz)

■ Pin Assignment

() : Old Package



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(SDIP064-P-0750)

*1: 5 V dielectric Nch open drain output pin

*2: MN102H51K (VDD), MN102HF51K (VPP)

■ Support Tool

■ In-circuit Emulator	PX-ICE102H51-SDIP064-P-0750	
■ Flash Memory Built-in Type	Type	MN102HF51K
	ROM (× 16-bit)	256 K
	RAM (× 16-bit)	8 K
	Minimum instruction execution time	83 ns (at 3.6 V to 3.0 V, 12 MHz)
	Package	SDIP064-P-0750C *Pb free
	(Old Package)	(SDIP064-P-0750)

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