MAX5096/MAX5097

40V, 600mA Buck Converters with Low-Quiescent-Current Linear Regulator Mode

General Description

The MAX5096/MAX5097 easy-to-use, Dual Mode™, DC-DC converters operate as LDO (low dropout) or switch-mode buck converters. At a high output load, the converters operate as high-efficiency pulse-width modulated (PWM) switch-mode converters and reduce the power dissipation. The devices switch to a low-quiescent-current (I_Q) LDO mode of operation at light load. During the key-off condition, the system's microcontroller drives the LDO/$\overline{BUCK}$ input on the fly and forces the MAX5096/MAX5097 into LDO mode, thereby reducing the quiescent current significantly.

In Buck mode, the MAX5096/MAX5097 operate from a 5V to 40V input voltage range and deliver up to 600mA of load current with excellent load and line regulation. The fixed-switching frequency versions of 135kHz and 330kHz are available. The MAX5096/MAX5097 DC-DC internal oscillator can be synchronized to an external clock. External compensation and a current-mode control scheme make it easy to design with.

In LDO mode, the MAX5096/MAX5097 operate from a 4V to 40V input voltage. The LDO mode operation is intended for a lower output load current of up to 100mA. The quiescent current at 100µA load in LDO mode is only 41µA (typ).

The MAX5096/MAX5097 feature an enable input that shuts down the device, reducing the current consumption to 6µA (typ). Additional features include a power-on-reset output with a capacitor-adjustable timeout period, programmable soft-start, output tracking, output overload, short-circuit, and thermal-shutdown protections.

The MAX5096/MAX5097 operate over the -40°C to +125°C automotive temperature range and are available in thermally enhanced 20-pin TSSOP or 16-pin TQFN packages.

Applications

- Industrial

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Features

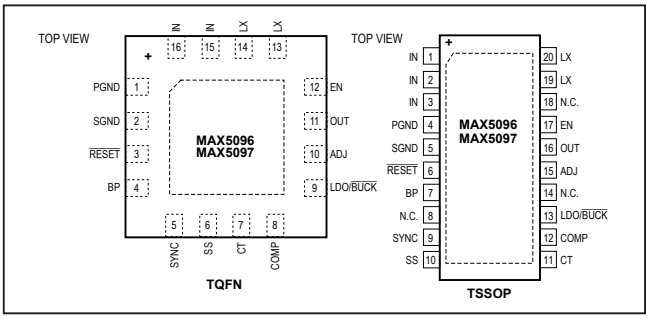
- High-Efficiency Switcher Mode (Buck Mode) or Low-Quiescent-Current Linear Regulator (LDO Mode) Operation
- Wide Operating Input Voltage Range
  - +5V to +40V Buck Mode
  - +4V to +40V LDO Mode
- Fixed 3.3V or 5V and Adjustable (1.24V to 11V) Output Voltage Versions
- 6µA (typ) Shutdown Current
- Fixed 135kHz or 330kHz Switching Frequency
- External Frequency Synchronization
- Programmable Soft-Start
- Integrated Microprocessor-Reset ($\overline{RESET}$) Circuit with Programmable Timeout Period
- Thermal and Short-Circuit Protection
- -40°C to +125°C Automotive Temperature Range
- Thermally Enhanced Package Dissipates 2.6W at T_A = +70°C (16-Pin TQFN) and 1.7W at T_A = +70°C (20-Pin TSSOP)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5096AATE+	-40°C to +125°C	16 TQFN-EP*
MAX5096BATE+	-40°C to +125°C	16 TQFN-EP*
MAX5096AAUP+	-40°C to +125°C	20 TSSOP-EP*
MAX5096BAUP+	-40°C to +125°C	20 TSSOP-EP*
MAX5097AATE+	-40°C to +125°C	16 TQFN-EP*
MAX5097BATE+	-40°C to +125°C	16 TQFN-EP*
MAX5097AAUP+	-40°C to +125°C	20 TSSOP-EP*
MAX5097BAUP+	-40°C to +125°C	20 TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configurations



Absolute Maximum Ratings

(All voltages referenced to PGND, unless otherwise noted.)
IN (transient, 1ms).....-0.3V to +45V
SGND.....-0.3V to +0.3V
LX.....-1V to (V_{IN} + 0.3V)
LX Current.....2A
EN.....-0.3V to (V_{IN} + 0.3V)
BP, SYNC, LDO/$\overline{BUCK}$, $\overline{RESET}$ to SGND.....-0.3V to +12V
BP, $\overline{RESET}$ Output Current.....25mA
CT, SS, ADJ, COMP to SGND.....-0.3V to (V_{BP} + 0.3V)
OUT.....-0.3V to +11V
OUT Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)*
16-Pin TQFN (derate 33.3mW/°C above +70°C).....2666mW
20-Pin TSSOP (derate 21.7mW/°C above +70°C)...1739mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

**As per JEDEC 51 Standard—Multilayer Board.*

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....30.0°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.7°C/W
TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....46.0°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +14V, I_{OUT} = 1mA, C_{IN} = 100µF, C_{OUT} = 22µF, L = 22µH, C_{BP} = 1µF, V_{EN} = +2.4V, SGND = PGND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM INPUT							
Input Voltage Range (LDO Mode)	V_{IN_LDO}	LDO/$\overline{BUCK}$ = high		4		40	V
Input Voltage Range (Buck Mode)	V_{IN_BUCK}	LDO/$\overline{BUCK}$ = low		5		40	V
Internal Input Undervoltage Lockout	V_{UVLO}	V_{BP} rising		3.5	3.65	3.9	V
Internal Input Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}	V_{BP} rising			0.2		V
BP (Internal Regulator) Output Voltage	V_{BP}	V_{IN} = +4.5V, I_{BP} = 100µA		3.75	4	4.20	V
Quiescent Supply Current (LDO Mode)	I_Q	LDO/$\overline{BUCK}$ = high, measured at input supply return, V_{OUT} = 5V, I_{OUT} = 100µA	T_A = -40°C to +125°C		38	70	µA
	I_Q	LDO/$\overline{BUCK}$ = high, measured at input supply return, V_{OUT} = 5V, I_{OUT} = 100mA	T_A = -40°C to +125°C		44	100	
Buck Converter No-Load Supply Current	I_{Q_BUCK}	V_{IN} = 14V, V_{OUT} = 5V, I_{OUT} = 0			680		µA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, measured from V_{IN}	T_A = -40°C to +125°C		6	19	µA
			T_A = -40°C to +125°C		6	12	

Electrical Characteristics (continued)

(V_{IN} = +14V, I_{OUT} = 1mA, C_{IN} = 100µF, C_{OUT} = 22µF, L = 22µH, C_{BP} = 1µF, V_{EN} = +2.4V, SGND = PGND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BUCK MODE							
Supply Current (Buck Converter On)	I_S	LDO/$\overline{BUCK}$ = low, V_{ADJ} = 1.4V, MAX5096, no switching	135kHz version		693	980	µA
Supply Current (Buck Converter On)	I_S	LDO/$\overline{BUCK}$ = low, V_{ADJ} = 1.4V, MAX5097, no switching	330kHz version		720	1000	µA
Fixed Output Voltage	V_{OUT}	5V version, 5.5V ≤ V_{IN} ≤ 40V, no load		4.85	5	5.12	V
		3.3V version, 5.5V ≤ V_{IN} ≤ 40V, no load		3.196	3.3	3.391	
ADJ Set Point	V_{FB}	50% duty cycle, no load					V
ADJ Input Bias Current	I_{FB}	V_{ADJ} = 1.5V			5	100	nA
Dual Mode ADJ Threshold	V_{ADJTH_R}	ADJ rising			125		mV
	V_{ADJTH_F}	ADJ rising			62		
Maximum Duty Cycle	D_{MAX}	V_{ADJ} = 0.5V			100		%
Error-Amplifier Transconductance	Gm_{EA}	V_{COMP} = V_{ADJ}, I_{COMP} = ±10µA		55	136	210	µS
Adjustable Output Voltage Range	V_{ADJ}			1.235		11.000	
Minimum Output Current	I_{OUT}	V_{IN} = 6.5V to 40V			600		mA
Switch Current Limit	I_{SW_LIM}	V_{IN} = 6V to 40V		1.15	1.5	1.90	A
Internal Switch On-Resistance	$R_{DS(ON)}$	V_{IN} = 14V, I_{DRAIN} = 100mA			0.9	2.1	Ω
Switch Leakage Current	I_{SW_L}	V_{EN} = 0V			0.05	3	µA
Efficiency	η	V_{IN} = 14V, V_{OUT} = 5V, I_{OUT} = 400mA			85		%
		V_{IN} = 14V, V_{OUT} = 3.3V, I_{OUT} = 400mA			81		
Switching Frequency	f_{SW}	MAX5096		120	135	148	kHz
		MAX5097		300	330	350	kHz
Synchronization SYNC Input	f_{SYNC}	MAX5096		120		500	kHz
		MAX5097		300		500	kHz
SYNC Input High Threshold	V_{SYNCH}	V_{BP} = 4V		2.0			V
SYNC Input Low Threshold	V_{SYNCL}	V_{BP} = 4V				0.8	V
SYNC Input Minimum High Pulse Width					250		ns
SYNC Input Leakage		V_{SYNC} = 11V				1	µA
LDO MODE							
Guaranteed Output Current	I_{OUT}	(Note 2)		100			mA

Electrical Characteristics (continued)

(V_{IN} = +14V, I_{OUT} = 1mA, C_{IN} = 100µF, C_{OUT} = 22µF, L = 22µH, C_{BP} = 1µF, V_{EN} = +2.4V, SGND = PGND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	5V version, MAX5096B/MAX5097B, 5.5V ≤ V_{IN} ≤ 40V, I_{OUT} = 10mA		4.89	5	5.09	V
		3.3V version, MAX5096A/MAX5097A, 4V ≤ V_{IN} ≤ 40V, I_{OUT} = 10mA		3.219	3.3	3.378	V
ADJ Set Point	V_{ADJ}	I_{OUT} = 10mA		1.21	1.2375	1.26	V
ADJ Input Bias Current	I_{FB}	V_{ADJ} = 4V			0.5	100	nA
Adjustable Output Voltage Range	V_{ADJ}	I_{OUT} = 10mA		1.237		11.000	V
Dropout Voltage	ΔV_{DO}	I_{OUT} = 100mA, V_{OUT} = 0.98 x V_{OUT} (nominal) (5V version only), MAX5096B/MAX5097B				0.37	V
Startup Response Time		Rising edge of EN to V_{OUT} = 10% V_{OUT} (nominal), R_L = 500Ω, V_{ADJ} = SGND, $V_{LDO/\overline{BUCK}}$ = 4V, C_{SS} = 2nF			300		µs
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	5V version, +5.5V ≤ V_{IN} ≤ +40V, I_{OUT} = 100mA			0.125		mV/V
		3.3V version, +4V ≤ V_{IN} ≤ +40V, I_{OUT} = 100mA			0.093		
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	5V version, I_{OUT} = 100µA to 100mA, V_{IN} = 14V	T_J = +25°C		0.242	0.374	mV/mA
			T_J = -40°C to +125°C		0.242	1	
		3.3V version, I_{OUT} = 100µA to 100mA, V_{IN} = 14V	T_J = +25°C		0.164	0.237	
			T_J = -40°C to +125°C		0.164	1	
Power-Supply Rejection Ratio	PSRR	I_{OUT} = 10mA, f = 100Hz, 500mV_{P-P}, V_{OUT} = +5V, V_{IN} = +14V			60		dB
Short-Circuit Current	I_{SC}	V_{IN} = 6V		150	330	500	mA
LDO/$\overline{BUCK}$ High Threshold				2.0			V
LDO/$\overline{BUCK}$ Low Threshold						0.8	V
LDO/$\overline{BUCK}$ Input Leakage		$V_{LDO/\overline{BUCK}}$ = 11V				1	µA
Transition Timing from LDO Mode to Buck Mode		Falling edge of LDO/$\overline{BUCK}$ to buck converter on			32		Clock Periods
Transition Timing from Buck Mode to LDO Mode		Rising edge of LDO/$\overline{BUCK}$ to LDO operation			100		µs
SOFT-START, ENABLE (EN) AND $\overline{RESET}$							
Soft-Start Charge Current	I_{SS}	V_{SS} = 0.1V		3	5	7	µA
Soft-Start Reference Voltage	V_{SS-REF}	V_{OUT} = $V_{OUT\ (nominal)}$ - 20%		0.9	0.99	1.1	V
EN High-Voltage Threshold	V_{ENH}	EN = high, regulator on		1.4			V

Electrical Characteristics (continued)

(V_{IN} = +14V, I_{OUT} = 1mA, C_{IN} = 100µF, C_{OUT} = 22µF, L = 22µH, C_{BP} = 1µF, V_{EN} = +2.4V, SGND = PGND = 0V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

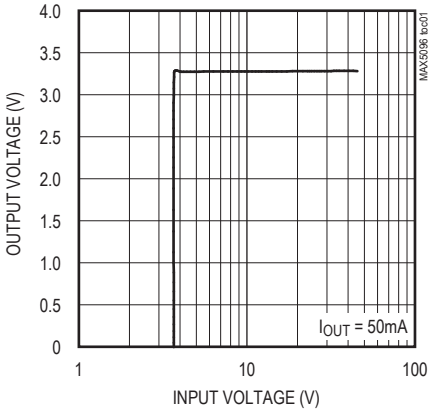
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Low-Voltage Threshold	V_{ENL}	Regulator off			0.4	V
EN Input Pulldown		V_{EN} = 2V, $V_{LDO/\overline{BUCK}}$ = 4V		0.5		µA
$\overline{RESET}$ Voltage Threshold High	V_{RESET_H}	V_{OUT} rising	89	92	94	% V_{OUT}
$\overline{RESET}$ Voltage Threshold Low	V_{RESET_L}	V_{OUT} falling	97	90	92	% V_{OUT}
$\overline{RESET}$ Output Low Voltage	V_{RL}	I_{SINK} = 1mA			0.2	V
$\overline{RESET}$ Output High Leakage Current	I_{RH}	V_{RESET} = 5V, V_{ADJ} = 1.5V			1	µA
$\overline{RESET}$ Output Minimum Timeout Period		C_{CT} = 0		25		µs
V_{OUT} to $\overline{RESET}$ Delay		V_{OUT} falling 10mV/µs, C_{CT} = 0		6		µs
Delay Comparator Threshold	V_{CT_TH}	V_{CT} rising	1.18	1.2374	1.29	V
Delay Comparator Threshold Hysteresis				100		mV
CT Charge Current	I_{CH}		0.74	1	1.20	µA
CT Discharge Current	I_{DISCH}	V_{CT} = 1V		13.8		mA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature	$T_{J(SHDN)}$	Temperature rising		+165		°C
Thermal-Shutdown Hysteresis,	$\Delta T_{J(SHDN)}$			20		°C

Note 1: Limits to -40°C are guaranteed by design.
Note 2: The continuous maximum output current from LDO is limited by package power dissipation.

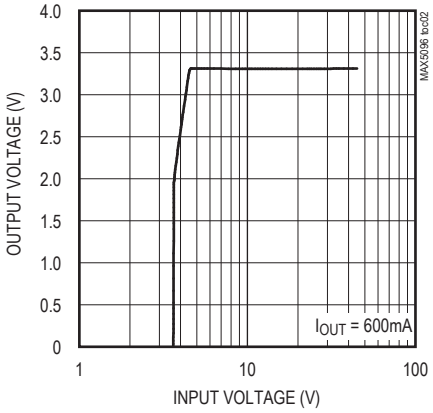
Typical Operating Characteristics

(V_{IN} = +14V, V_{EN} = +2.4V, MAX5097AATE+, Figures 2 and 4, T_A = +25°C, unless otherwise specified.)

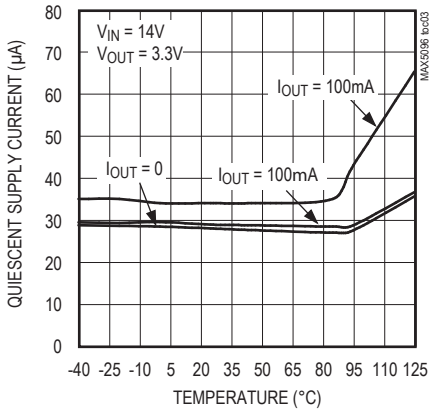
OUTPUT VOLTAGE vs. INPUT VOLTAGE (LDO MODE)



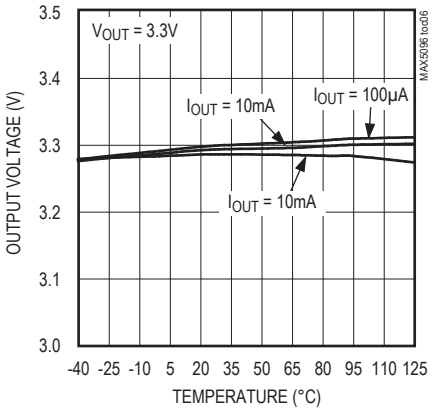
OUTPUT VOLTAGE vs. INPUT VOLTAGE (BUCK MODE)



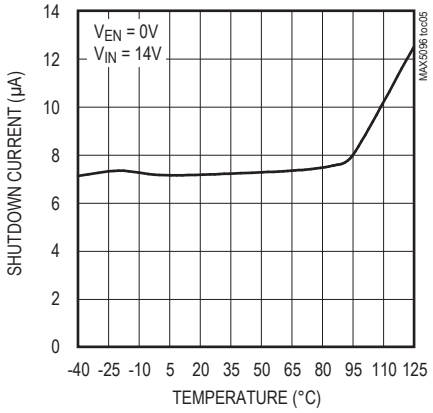
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE (LDO MODE)



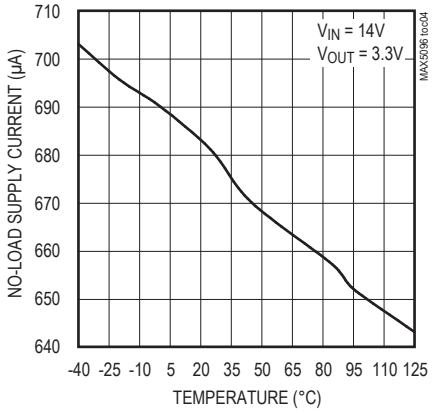
OUTPUT VOLTAGE vs. TEMPERATURE (LDO MODE)



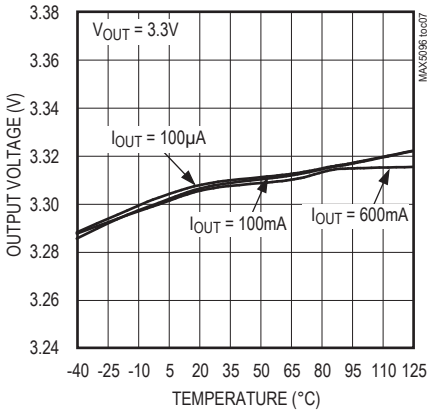
SHUTDOWN CURRENT vs. TEMPERATURE



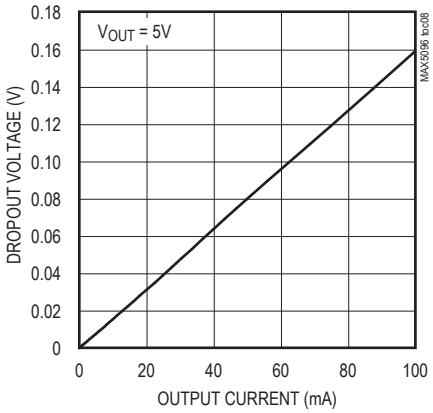
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE (BUCK MODE)



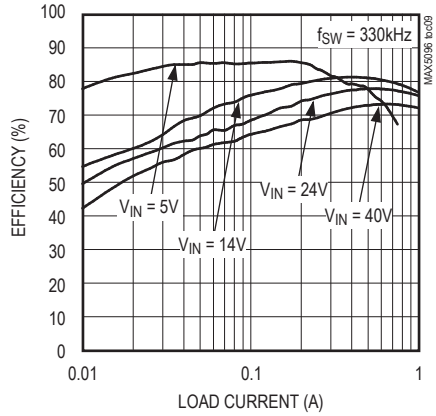
OUTPUT VOLTAGE vs. TEMPERATURE (BUCK MODE)



DROPOUT VOLTAGE vs. OUTPUT CURRENT (LDO MODE)



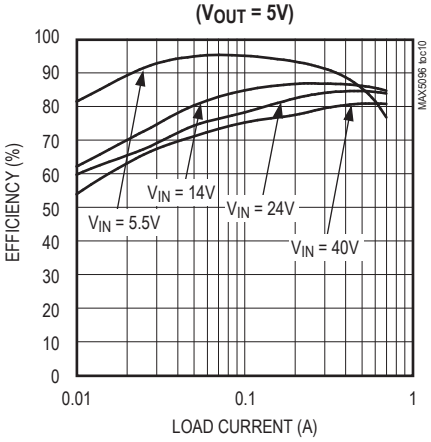
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



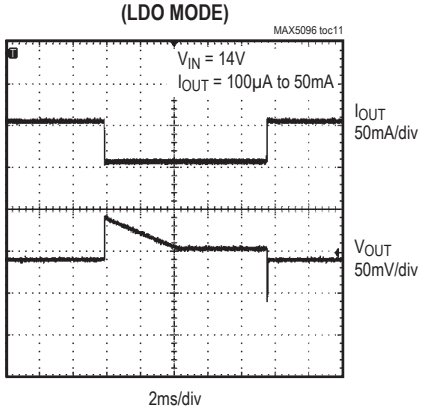
Typical Operating Characteristics (continued)

(V_{IN} = +14V, V_{EN} = +2.4V, MAX5097AATE+, Figures 2 and 4, T_A = +25°C, unless otherwise specified.)

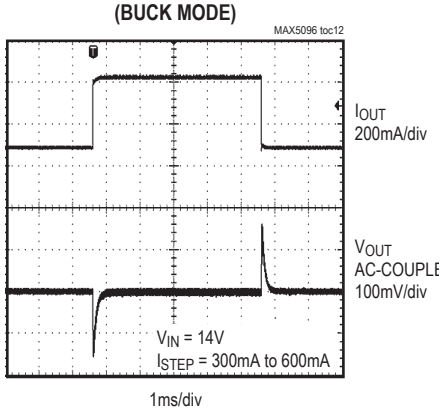
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



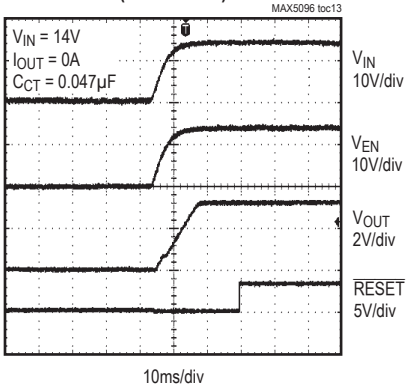
LOAD-TRANSIENT RESPONSE (LDO MODE)



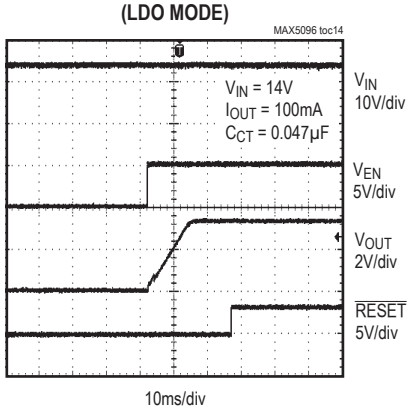
LOAD-TRANSIENT RESPONSE (BUCK MODE)



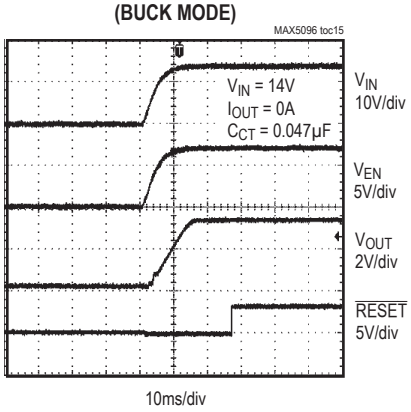
V_{IN} STARTUP RESPONSE (LDO MODE)



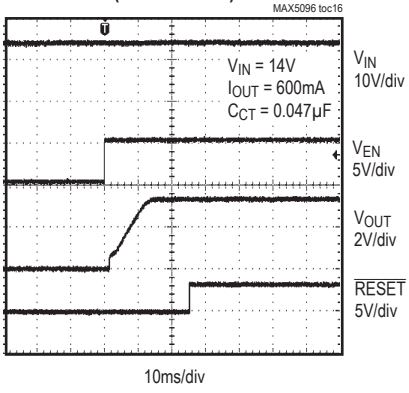
ENABLE STARTUP RESPONSE (LDO MODE)



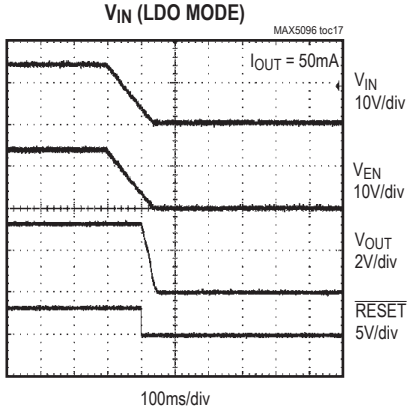
V_{IN} STARTUP RESPONSE (BUCK MODE)



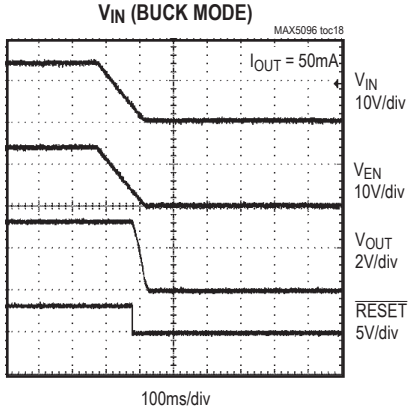
ENABLE STARTUP RESPONSE (BUCK MODE)



SHUTDOWN RESPONSE THROUGH V_{IN} (LDO MODE)



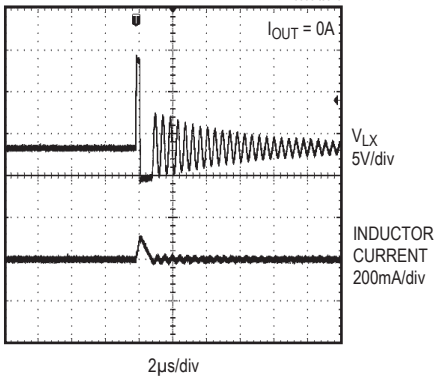
SHUTDOWN RESPONSE THROUGH V_{IN} (BUCK MODE)



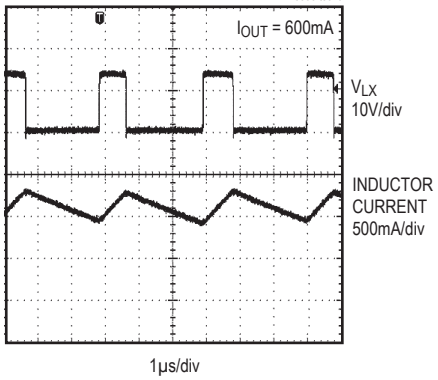
Typical Operating Characteristics (continued)

(V_{IN} = +14V, V_{EN} = +2.4V, MAX5097AATE+, Figures 2 and 4, T_A = +25°C, unless otherwise specified.)

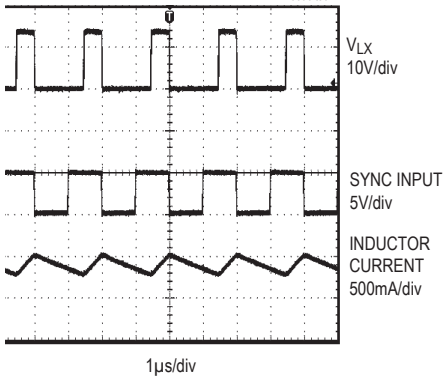
LX VOLTAGE AND INDUCTOR CURRENT



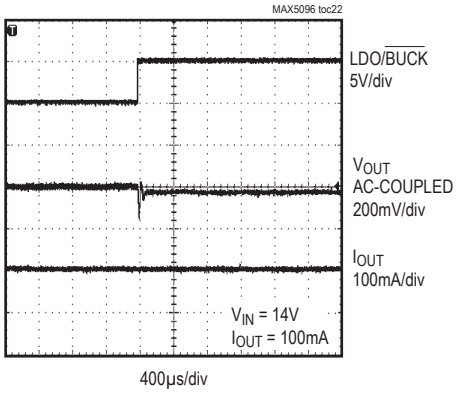
LX VOLTAGE AND INDUCTOR CURRENT



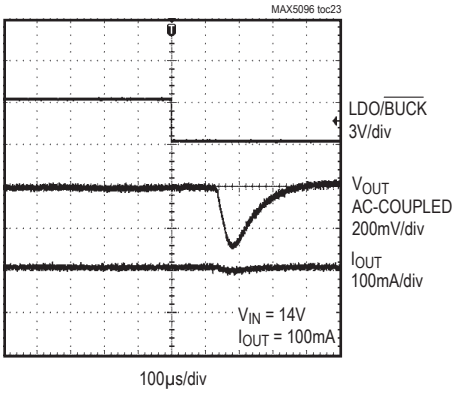
LX VOLTAGE, SYNC INPUT, AND INDUCTOR CURRENT



TRANSITION FROM BUCK MODE TO LDO MODE



TRANSITION FROM LDO MODE TO BUCK MODE



Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	4	PGND	Power Ground. Return path for p-channel power MOSFET driver. Connect the input capacitor return, freewheeling diode anode, and output capacitor return terminals to PGND.
2	5	SGND	Signal Ground. Connect SGND to PGND near the input bypass capacitor return terminal.
3	6	$\overline{\text{RESET}}$	Open-Drain, Active-Low Reset Output. $\overline{\text{RESET}}$ asserts low when OUT drops below the reset threshold. When output rises above 92% of the programmed level, $\overline{\text{RESET}}$ becomes high impedance after the reset timeout period. Connect a pullup resistor from $\overline{\text{RESET}}$ to the converter output to create a logic output.
4	7	BP	4V Internal Regulator Output. Bypass BP to SGND with a 1µF or greater ceramic capacitor.
5	9	SYNC	Synchronization Input. Connect SYNC to an external clock for synchronization. Connect SYNC to SGND when not used.
6	10	SS	Soft-Start Timer Input. Connect an external capacitor from SS to SGND to adjust the soft-start timeout period (see the *Soft-Start (SS)* section).
7	11	CT	Reset Timeout Period. Connect a capacitor from CT to SGND to set the reset-timeout period (see the *Power-On Reset Output* $\overline{\text{RESET}}$ section).
8	12	COMP	Buck Converter (Buck Mode) Control-Loop Compensation. See the *Compensation Network* section for compensation network design. LDO mode does not need external compensation.
9	13	LDO/$\overline{\text{BUCK}}$	LDO Mode/Buck Mode Select. Drive LDO/$\overline{\text{BUCK}}$ low to select the buck mode. The buck mode activates after 32 internal/external clock cycles. Force the LDO/$\overline{\text{BUCK}}$ high (> 2V), to select LDO mode. The buck mode stops and LDO mode is activated with a 100µs delay.
10	15	ADJ	Regulator Output-Feedback Point. Connect ADJ to SGND for a fixed 3.3V (MAX5096A/MAX5097A) or 5V (MAX5096B/MAX5097B). For adjustable output voltage, use an external resistive divider to set V_{OUT}. V_{ADJ} regulating set point is 1.237V.
11	16	OUT	Converter Output. OUT must always be connected to the regulator output. Connect at least a 22µF low-ESR (equivalent series resistance) capacitor from OUT to PGND for stable operation.
12	17	EN	Enable Input. EN is internally pulled to ground. Drive EN high to turn on the regulator. Force EN low or leave unconnected to place the device in shutdown mode.
13, 14	19, 20	LX	Drain Connection of Internal p-Channel High-Side Switch
15, 16	1, 2, 3	IN	Regulator Input. Bypass IN to PGND with a parallel combination of low-ESR ceramic and aluminum capacitor to handle the input ripple current.
—	8, 14, 18	N. C.	No Connection. Not internally connected.
EP	EP	EP	Exposed Pad. Connect externally to a large ground plane (SGND) for improved heat dissipation. Do not use EP as an electrical ground connection.

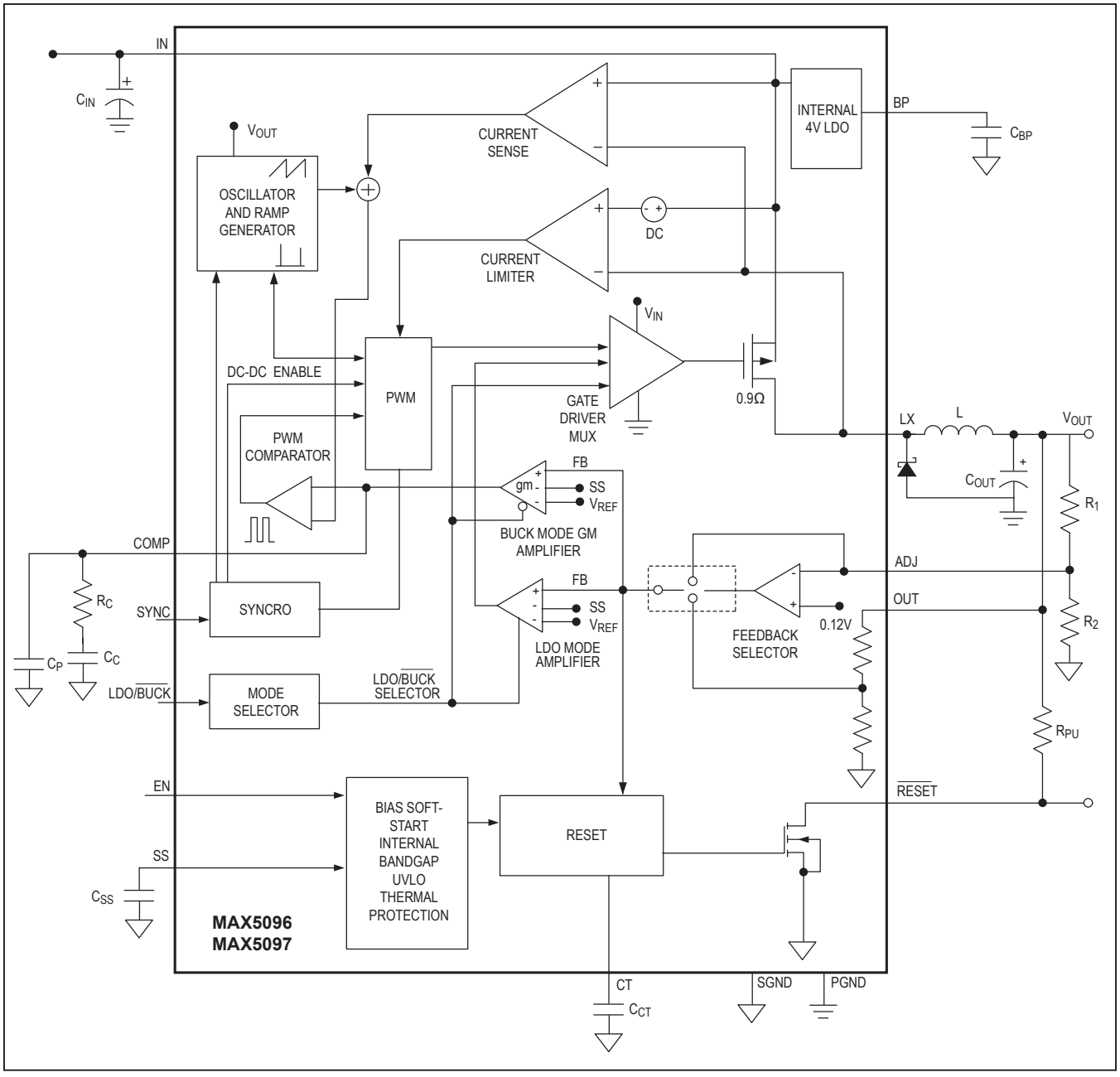


Figure 1. Simplified Diagram

Detailed Description

The MAX5096/MAX5097 are easy-to-use, high-efficiency, PWM current-mode, step-down switching converters in normal operation. The MAX5096/MAX5097 have an internal high-side p-channel 0.9Ω switch and use a low forward-drop freewheeling diode for rectification. In buck mode, the p-channel switches at the 135kHz or 330kHz frequency. Buck mode uses a current-mode control architecture that offers excellent line-transient response, easier frequency compensation, and cycle-by-cycle current limiting. The buck converter is compensated externally for a selected value/type of output inductor and capacitor.

The internal p-channel switch acts as a pass element when operating in the low-quiescent-current LDO mode.

The LDO mode can be selected on the fly through the LDO/$\overline{\text{BUCK}}$ input. During the key-off condition, the system's microcontroller drives the LDO/$\overline{\text{BUCK}}$ input high and forces the MAX5096/MAX5097 into LDO mode, reducing the quiescent current to 1µA (typ). When in LDO mode, the device is capable of delivering up to 100mA, which may be limited by the device power dissipation. The LDO and switcher share the same pass element and the reference; however, the error amplifiers are different with their own compensation schemes.

The MAX5096/MAX5097 include an integrated microprocessor reset circuit with an adjustable reset timeout period. The internal reset circuit monitors the regulator output voltage and asserts $\overline{\text{RESET}}$ low when the regulator output falls below the reset threshold voltage. Other features include an enable input, externally programmable soft-start, optimized current-limit protection in both LDO and buck modes, and thermal shutdown.

Enable Input (EN)

EN is a logic-level enable input that turns the device on or off. The logic-high and logic-low voltages for the EN input are 1.4V and 0.4V, respectively. Drive EN high to turn on the device, and drive it low to place the device in shutdown. Leaving EN unconnected disables the device since the EN is internally pulled low with a 0.5µA current, however, a forced pulldown of EN improves the noise immunity. The MAX5096/MAX5097 draw 6µA (typ) of supply current when in shutdown. EN withstands up to +40V, allowing EN to be connected directly to IN for always-on operation. The converter may be turned on and off while in both buck and LDO modes. Each time the EN is toggled, the output rises with a programmed soft-start period.

Internal Regulator (BP)/Undervoltage Lockout

The MAX5096/MAX5097 include an internal 4V auxiliary regulator to power internal circuitry. Bypass the auxiliary regulator output (BP) to SGND with a 1µF ceramic capacitor physically located close to the device. The regulator is not intended to supply the external circuit other than pulling up the LDO/$\overline{\text{BUCK}}$ input or $\overline{\text{RESET}}$. Do not load BP externally by more than 2mA. The regulator output is regulated to 4V with 7% accuracy during steady state. During turn-on, the BP voltage stabilizes after 250µs with a 1µF capacitor at BP. Drive EN high to turn on the internal regulator. The internal UVLO with hysteresis ensures stable operation, resulting in the monotonic rise of the output voltage. The UVLO circuit monitors the output of the regulator. The rising UVLO threshold is internally set to 3.65V (BP rising) with a 185mV hysteresis (BP falling). The 3.65V UVLO at the no-load BP output guarantees operation at VIN lower than 4V.

Soft-Start (SS)

Soft-start provides for the monotonic, glitch-free turn-on of the converter. Soft-start limits the input inrush current which may cause a glitch, especially if the source impedance is high. The soft-start period required also depends on the output capacitance and the closed-loop bandwidth of converter. The soft-start period for the MAX5096/MAX5097 is externally programmable using a single capacitor (C_{SS}). The soft-start is achieved by the controlled ramping up of the error amplifier reference input. At startup, after VIN is applied and the UVLO threshold is reached, the device enters soft-start. During soft-start, 5µA is sourced into the capacitor (C_{SS}) connected from SS to SGND (Figure 2) causing the reference voltage to ramp up slowly. When V_{SS} reaches 1.237V, the output becomes fully active. Set the soft-start time (t_{SS}) using following equation:

$$t_{SS} = \frac{V_{SS}}{I_{SS}} \times C_{SS}$$

where V_{SS} is 1.237V, I_{SS} is 5µA, t_{SS} is in seconds, and C_{SS} is in Farads.

Pulling EN low quickly discharges the C_{SS} capacitor, making it ready for the next soft-start period.

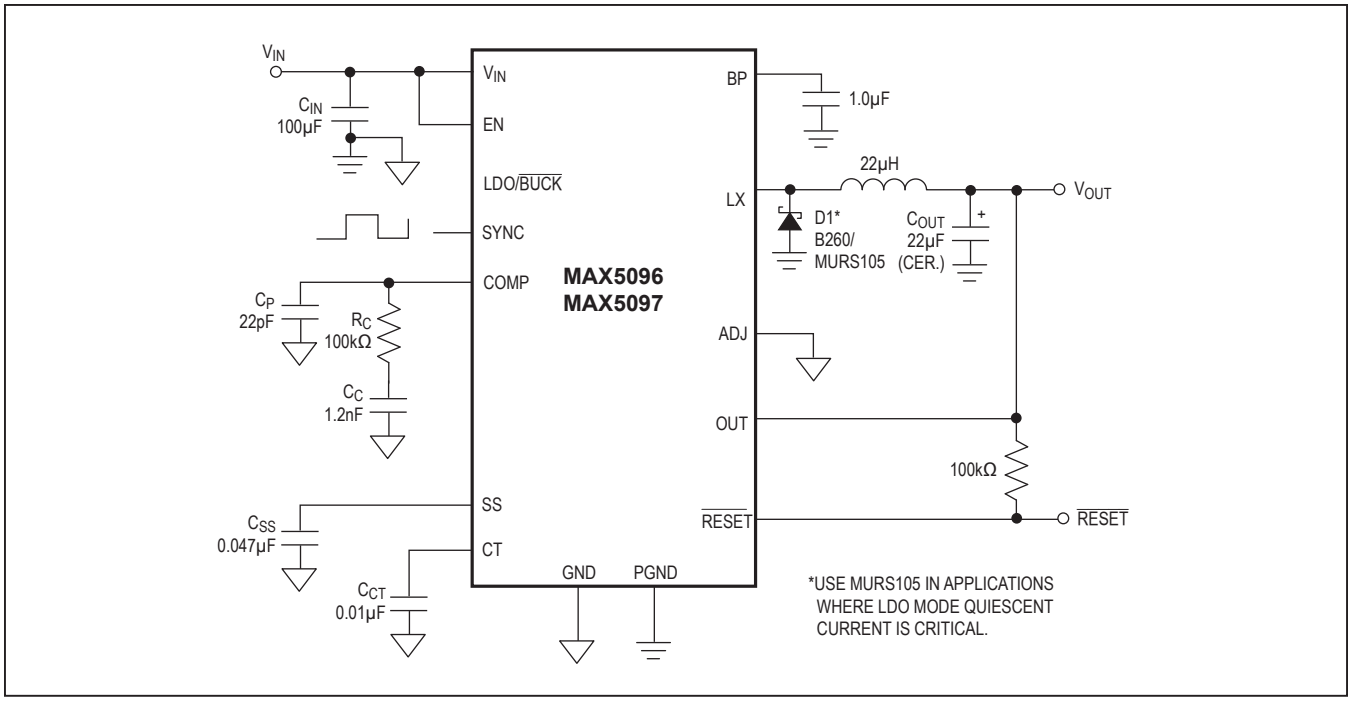


Figure 2. Fixed Output-Voltage Configuration

Output-Voltage Tracking/Sequencing

The output voltages of multiple MAX5096/MAX5097 converters can be made to track by using the SS pin during turn-on and turn-off (see Figure 3). SS is pulled up using a 5µA current source and connecting SS of multiple MAX5096/MAX5097s, raising the references with the same slope. Tracking the converters reduces the differential voltages between the core and I/O voltages during turn-on, turn-off, and brownout. If any one converter output drops due to shutdown or an overload-fault situation, the SS drops, pulling down all the converters simultaneously. The rate of fall of output voltages, however, depends on the output capacitance and load of the individual converter.

Multiple voltage sequencing can be done by daisy-chaining several MAX5096/MAX5097s. The $\overline{RESET}$ of the first converter can be connected to EN of the second converter. This allows the first converter to come up first every time the system is powered up.

Power-On-Reset Output ($\overline{RESET}$)

A supervisor circuit is integrated in the MAX5096/MAX5097. $\overline{RESET}$ is an open-drain output. $\overline{RESET}$ pulls low as soon as V_{OUT} drops below 90% of its nominal regulation voltage. Once the output voltage rises above 92% of the set output voltage, the $\overline{RESET}$ output enters a high-impedance state after the active timeout period (t_{RP}). The active timeout period is externally programmable using a single capacitor from CT to ground. Use the following equation to calculate the required timeout period for the power-on reset:

$$t_{RP} = \frac{V_{CT-TH}}{I_{CH}} \times C_{CT}$$

where V_{CT-TH} is 1.237V, I_{CH} is 1µA, t_{RP} is in seconds, and CCT is in Farads.

To obtain a logic-voltage output, connect a pullup resistor from $\overline{RESET}$ to a logic-supply voltage. The internal open-drain MOSFET can sink 1mA while providing a TTL logic-low signal. If unused, ground $\overline{RESET}$ or leave it unconnected.

The power-on-reset behavior is the same in both the LDO and buck modes of operation.

Oscillator/Synchronization Input (SYNC)

The MAX5096/MAX5097 internal oscillator generates a factory-preset frequency of either 135kHz (MAX5096) or 330kHz (MAX5097). The 135kHz version keeps the maximum fundamental frequency below 150kHz, which keeps the third harmonic below 450kHz and under the

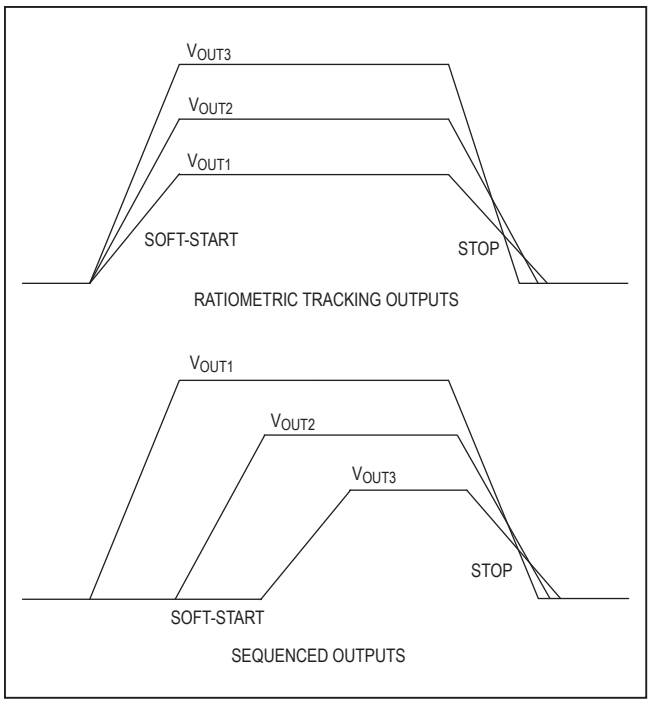


Figure 3. Output Voltage Tracking/Sequencing

lower end of the AM band. The MAX5096 is suitable for noise-sensitive applications like AM radio power supply. For an application where size is more important, use the MAX5097, which runs at 330kHz frequency. The high-frequency operation reduces the size and cost of the external inductor and capacitor. The MAX5096/MAX5097 can be synchronized using an external signal. The MAX5096 can be synchronized from 120kHz to 500kHz, while the MAX5097 is capable of synchronizing from 300kHz to 500kHz. The external synchronization feature makes frequency hopping possible depending on the selected AM channel. Connect SYNC to ground, if not used.

Thermal Protection

When the junction temperature exceeds T_J = +165°C, an internal thermal sensor signals the shutdown logic, which turns off the regulator (both in buck mode and LDO mode), and discharges the soft-start capacitor allowing the IC to cool. The thermal sensor turns the regulator on again after the IC's junction temperature cools by 20°C, resulting in a cycled output during continuous thermal-overload conditions. The thermal hysteresis and a soft-start period limit the average power dissipation into the device during continuous fault condition. During operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Applications Information

Output Voltage Selection

The MAX5096/MAX5097 can be configured as either a preset fixed-output voltage or an adjustable-output voltage device. Connect ADJ to ground to select the factory-preset output-voltage option (Figure 2). The MAX5096A/MAX5097A and MAX5096B/MAX5097B provide a fixed-output voltage equal to 3.3V and 5V, respectively (see the *Selector Guide*). The MAX5096/MAX5097 become an adjustable version as soon as the devices detect about 125mV at the ADJ pin. The resistor-divider at ADJ increases the ADJ voltage above 125mV and also adjusts the output voltage depending upon the resistor values. In adjustable mode, select an output between +1.273V and +11V using two external resistors connected as a voltage-divider to ADJ (Figure 4). Set the output voltage using the following equation:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{ADJ} = 1.273V and R2 is chosen to be approximately 100kΩ.

Connect ADJ to GND if adjustable mode is not used.

Inductor Selection

Three key inductor parameters must be specified for proper operation with the MAX5096/MAX5097: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output-voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value, while a lower ΔI_{P-P} requires a higher inductor value. A lower inductor value minimizes size and cost and improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple-current levels, especially when the inductance is increased while keeping the dimension of the inductor constant. A good compromise is to choose ΔI_{P-P} equal to 40% of the full load current. Calculate the inductor value using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

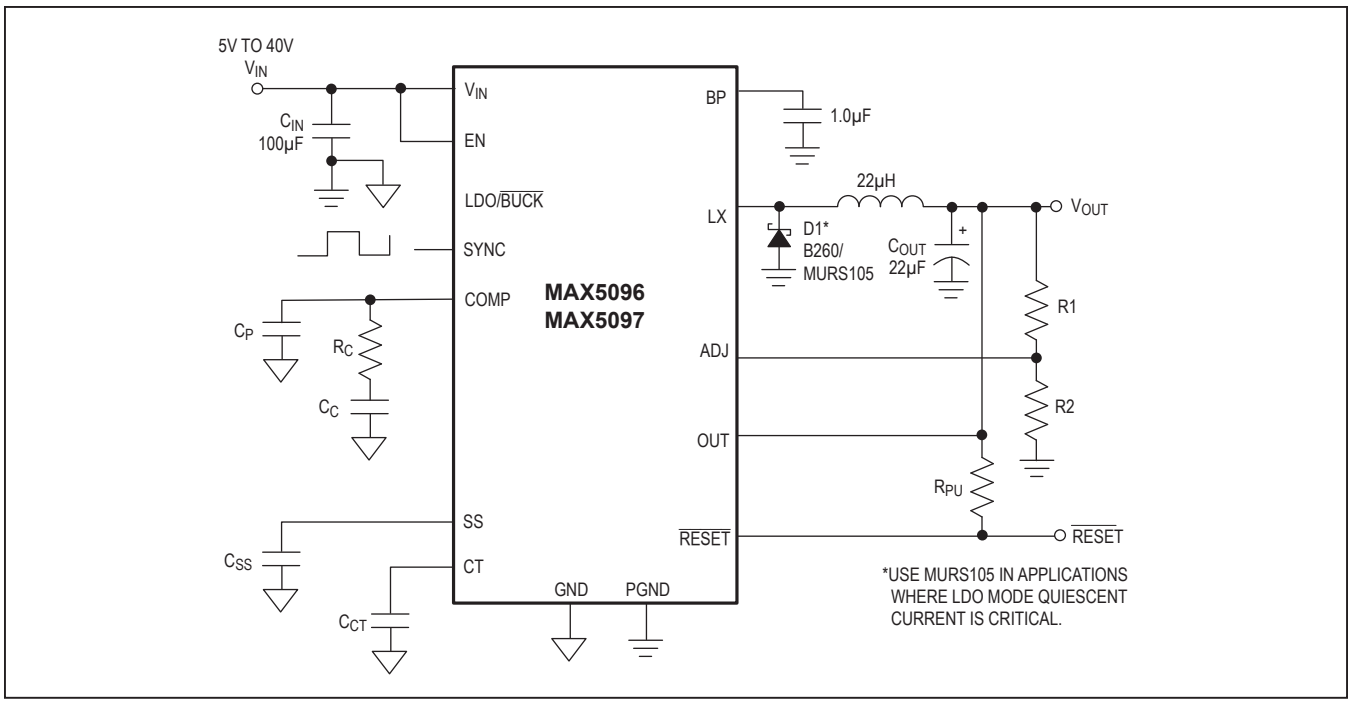


Figure 4. Adjustable Output Voltage Configuration

Use typical values of V_{IN} and f_{SW} so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is fixed at 135kHz (MAX5096) and 330kHz (MAX5097). f_{SW} can also be varied from 120kHz to 500kHz (MAX5096) and from 300kHz to 500kHz (MAX5097) when synchronized to an external clock (see the *Oscillator/Synchronization Input (SYNC)* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturating current (I_{SAT}) is also important to avoid runaway current during continuous output short circuit. Select an inductor with an I_{SAT} specification higher than the maximum peak current limit of 1.9A.

The buck mode operation determines the inductor and output capacitor values. However, the values of the inductor, its DCR, and the output capacitance/ESR affect the closed-loop-transfer function both in buck and LDO modes. The internal compensation of the MAX5096/MAX5097 in LDO mode limits the values of these external components. Make sure that the combination of output inductor, capacitor, and ESR falls within the range specified in Table 1.

Table 1. Inductor/Output Capacitor Selection

INDUCTOR	OUTPUT CAPACITOR (C_{OUT})
22µH	22µF, ESR = 5mΩ to 20mΩ (ceramic)
	47µF, ESR = 40mΩ to 150mΩ
	100µF, ESR = 30mΩ to 100mΩ
	470µF/ESR = 60Ω to 400mΩ
47µH	22µF, ESR = 5mΩ to 20mΩ (ceramic)
	47µF/ESR = 40mΩ to 150mΩ
	100µF/ESR = 30mΩ to 100mΩ
	470µF/ESR = 60mΩ to 400mΩ
100µH	22µF, ESR = 5mΩ to 20mΩ (ceramic)
	47µF/ESR = 40mΩ to 150mΩ
	100µF/ESR = 30mΩ to 100mΩ
	470µF/ESR = 60mΩ to 400mΩ

Output Capacitor Selection

The allowable output-voltage ripple and the maximum deviation of the output voltage during load steps determine the output capacitance and its ESR. The output

ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the ESR of the output capacitor). Normally, a good approximation of the output-voltage ripple is $\Delta V_{RIPPLE} \approx \Delta V_{ESR} + \Delta V_Q$. If using ceramic capacitors, assume the contribution to the output-voltage ripple from the ESR and the capacitor discharge to be equal to 20% and 80%, respectively. If using aluminum electrolyte capacitors, assume the contribution to the output-voltage ripple from the ESR and the capacitor discharge to be equal to 90% and 10%, respectively.

Use the following equations for calculating the output capacitance and its ESR for required peak-to-peak output-voltage ripple.

$$C_{OUT} = \frac{\Delta I_{P-P}}{16 \times \Delta V_Q \times f_{SW}}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

ΔI_{P-P} is the peak-to-peak inductor current and f_{SW} is the converter's switching frequency.

The allowable deviation of the output voltage during fast-load transients also determines the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation Network* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL, and the capacitor discharge, causes a voltage drop during the load step. Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for better transient-load and voltage-ripple performance. Nonleaded capacitors and/or multiple parallel capacitors help reduce the ESL. Keep the maximum output-voltage deviation below the tolerable limits of the electronics being powered. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller. The response time of the converter is approximately one third of the inverse of its closed-loop bandwidth and also depends on the phase margin.

Rectifier Selection

The MAX5096/MAX5097 require an external Schottky/fast-recovery diode rectifier as a freewheeling diode. Connect this rectifier close to the device using short leads and short PCB traces. Choose a rectifier with a continuous current rating greater than the highest output current-limit threshold (1.9A) and with a voltage rating greater than the maximum expected input voltage, V_{IN}. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops. Use a 60V (max) Schottky rectifier with a 2A current rating. The Schottky rectifier leakage current at high temperature significantly increases the quiescent current in LDO mode. In applications where LDO mode quiescent current is important, use an ultra-fast switching diode to limit the leakage current. In this type of application, use MURS105, MURS120 for their fast-switching and low-leakage features.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input-ripple currents and therefore, the input capacitor must be carefully chosen to keep the input voltage ripple within design requirements. The input voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Calculate the input capacitance and ESR required for a specified ripple using the following equations (continuous mode):

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT\_MAX} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT\_MAX} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{OUT_MAX} is the maximum output current and D is the duty cycle.

Compensation Network

The MAX5096/MAX5097 in LDO mode are compensated internally with a compensation network around the LDO error amplifier. When in buck mode, the DC-DC g_M amplifier must be externally compensated using a network connected from COMP to ground. The current-mode control architecture reduces the compensation network to a single pole-zero. The RC and C network, connected from the internal transconductance amplifier output to SGND, can provide a single pole-zero pair. Choose all the power components like the inductor, output capacitor, and ESR first and design the compensation network around them. Choose the closed-loop bandwidth (f_C) to be approximately 1/10 of the switching frequency. See the following equations to calculate the compensation values for the low-ESR output capacitor with ESR zero frequency, approximately a decade higher than f_C.

Calculate the dominant pole due to the output capacitor (C_{OUT}) and the load (R_{OUT}):

$$f_{PO} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}}$$

where $R_{OUT} = V_{OUT}/I_{LOAD}$

Calculate the R_C using following equation:

$$R_C = \frac{V_O \times f_C}{g_{MC} \times R_{OUT} \times g_m \times V_{ADJ} \times f_{PO}}$$

where g_{MC} is the control to output gain of the MAX5096/MAX5097 buck converter and is equal to 1.06. V_{ADJ} is the feedback set point equal to 1.237V and g_m (transconductance amplifier gain) is equal to 136µS. See Figure 2.

Place a zero (f_Z) at 0.9 x f_{PO}:

$$C_C = \frac{1}{2 \times \pi \times R_C \times f_{PO}}$$

Finally, place a high-frequency pole at the frequency equal to 1/2 of the converter switching frequency (f_{SW}).

$$C_P = \frac{1}{\pi \times R_C \times f_{SW}}$$

Place the compensation network physically close to the MAX5096/MAX5097.

Switching Between LDO Mode and Buck Mode

The MAX5096/MAX5097 switch between the buck mode and LDO mode on the fly. However, care must be taken to reduce output glitch or overshoot during the switching.

Buck Mode to LDO Mode

The LDO mode is intended for the low 100mA output current while the buck converter delivers up to 600mA output current. It is important to first reduce the output load below 100mA before switching to the LDO mode. If the output load is higher than 100mA, the MAX5096/MAX5097 can go into the current limit and the output drops significantly. Whenever the mode is changed, output is expected to glitch because the loop dynamics change due to different error amplifiers when operating in the LDO and buck modes. The output-voltage undershoot can be minimized by reducing the output load during switching and using larger output capacitance.

LDO Mode to Buck Mode

When switching from the LDO mode to buck mode, a fixed amount of delay (32 cycles) is applied so that the buck converter control loop and oscillator reach their steady-state conditions. The 32-cycle delay translates to approximately 250µs and 100µs for 150kHz and 330kHz switching frequency versions, respectively. It is recommended that the output load of 600mA must be delayed by at least this amount of time to allow the MAX5096/MAX5097 to switch to high-current buck mode. This ensures that the output does not drop due to the LDO current-limit protection mechanism.

PCB Layout Guidelines

1) Proper PCB layout is essential. Minimize ground noise by connecting the anode of the freewheeling rectifier, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a large PGND plane.
2) Minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, place the Schottky/fast recovery rectifier diode right next to the device.
3) Connect the exposed pad of the IC to the SGND plane. Do not make a direct connection between the exposed pad plane and SGND (pin 2) under the IC. Connect the exposed pad and pin 2 to the SGND plane separately. Connect the ground connection of the feedback resistive divider, the soft-start capacitor, the adjustable reset timeout capacitor, and the compensation network to the SGND plane. Connect the SGND plane and PGND plane at one point near the input bypass capacitor at V_{IN}.
4) Use the large SGND plane as a heatsink for the MAX5096/MAX5097. Use large PGND and LX planes as heatsinks for the rectifier diode and the inductor.

Selector Guide

PART	OUTPUT VOLTAGE (V)	SWITCHING FREQUENCY (kHz)
MAX5096A_ _ _	+3.3/Adjustable	135
MAX5096B_ _ _	+5.0/Adjustable	135
MAX5097A_ _ _	+3.3/Adjustable	330
MAX5097B_ _ _	+5.0/Adjustable	330

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1655+2	21-0140	90-0072
20 TSSOP	U20E+4	21-0108	90-0115

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/06	Initial release	—
1	6/07	Updated *Electrical Characteristics* table	1–3, 5, 20
2	9/07	Removed future product asterisks from *Ordering Information* table, Updated *Electrical Characteristics* table and TSSOP package outline	1, 4, 18, 19, 20
3	5/14	No /V OPNs; removed automotive reference from *Applications* section	1
4	1/15	Removed incorrect reference to Figure 2 in *Electrical Characteristics* globals	2–5

