LMH6672 Dual, High Output Current, High Speed Op Amp

1 Features

- **High Output Drive**
  - 19.2 V_{PP} Differential Output Voltage, R_L = 50 Ω
  - 9.6 V_{PP} Single-ended Output Voltage, R_L = 25 Ω
- **High Output Current**
  - ±200 mA @ V_O = 9 V_{PP}, V_S = 12 V
- **Low Distortion**
  - 105 dB SFDR @ 100 kHz, V_O = 8.4 V_{PP}, R_L = 25Ω
  - 98 dB SFDR @ 1MHz, V_O = 2 V_{PP}, R_L = 100 Ω
- **High Speed**
  - 90 MHz 3 dB Bandwidth (G = 2)
  - 135 V/µs Slew Rate
- **Low Noise**
  - 3.1 nV/√Hz: Input Noise Voltage
  - 1.8 pA/√Hz: Input Noise Current
- Low Supply Current: 7.2mA/amp
- Single-supply Operation: 5 V to 12 V
- Stable for Gain of +2V/V or Higher
- Available in 8-pin SOIC and SO PowerPAD (DDA)

2 Applications

- ADSL PCI Modem Cards
- xDSL External Modems
- Line Drivers

3 Description

The LMH6672 is a low cost, dual high speed op amp capable of driving signals to within 1 V of the power supply rails. It features the high output drive with low distortion required for the demanding application of a single supply xDSL line driver.

When connected as a differential output driver, the LMH6672 can drive a 50-Ω load to 16.8 V_{PP} swing with only −98 dBc distortion, fully supporting the peak upstream power levels for upstream full-rate ADSL. The LMH6672 is fully specified for operation with 5-V and 12-V supplies. Ideal for PCI modem cards and xDSL modems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6672	SOIC (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

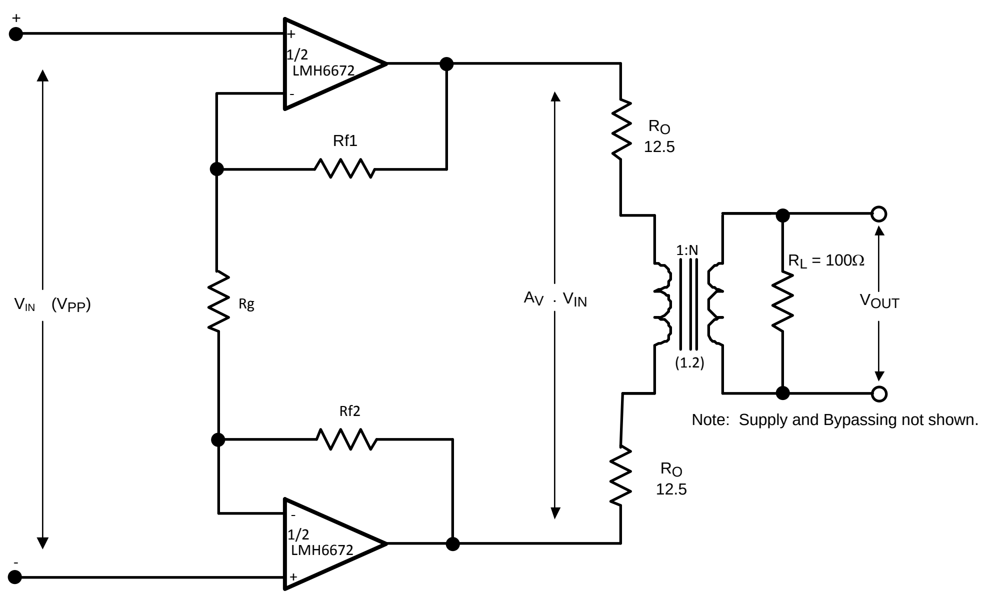


Table of Contents

4 Revision History

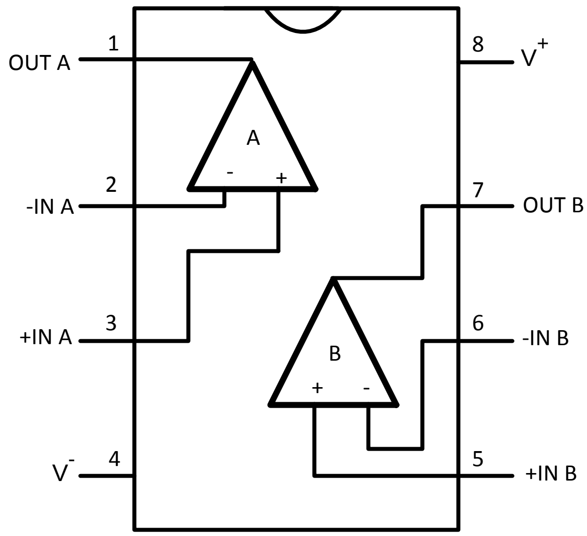
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H	Page
• Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Device Information Table, Application and Implementation; Device and Documentation Support; Mechanical, Packaging, and Ordering Information	1
• Added "Stable for Gain of +2V/V or Higher" in Features	1
• Changed from "Junction Temperature Range" to "Operating Temperature Range" in Recommended Operating Conditions	4
• Deleted T_J = 25°C in Electrical Characteristics	5
• Deleted T_J = 25°C and "Slew Rate" in ±2.5V Electrical Characteristics	6
• Added condition "Av = + 2V/V" in Typical Performance Characteristics	7
• Added "Vs= +/-2.5V" and "Vs=+/-6V" as curve labels for Figure 36	11
• Changed curve label from 31 MHz to 13 MHz. Changed title from +5V to +5V/V in Figure 37	12
• Changed "10V" to + "10V/V" in caption title for Figure 38	12
• Added "Vs = 12V" to Figure 39 caption title	13
• Added "Vs = 5V" to Figure 40 caption title	13
• Changed from "40 = 346 mW" to "40 mW lower or 346 mW" in Thermal Management	17
• Changed from 41 mW to 17 mW	17
• Added "from ambient"	17
• Changed sentence beginning with "Using the same P_{DRIVER} as above..."	17
• Added caution note	17

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	17

5 Pin Configuration and Functions

8-Pin
SOIC (D) / SO PowerPAD (DDA)
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	ChA Output
2	-IN A	I	ChA Inverting Input
3	+IN A	I	ChA Non-inverting Input
4	V^-	I	Negative Supply
5	+IN B	I	ChB Non-inverting Input
6	-IN B	I	ChB Inverting Input
7	OUT B	O	ChB Output
8	V^+	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN} Differential			±1.2	V
Output Short Circuit Duration		See[2]		
Supply Voltage ($V^+ - V^-$)			13.2	V
Voltage at Input/Output pins			V^+ +0.8 V^- −0.8	V
Junction Temperature			+150[3]	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering (10 sec)		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Shorting the output to either supply or ground will exceed the absolute maximum T_J and can result in failure.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge[1]	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]	2	2000	V
		Machine Model (MM)I[3]		200	

(1) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 200 Ω in series with 100 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-)	±2.5	±6.5	V
Operating Temperature Range	−40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		SOIC Package D	SO PowerPAD Package DDA	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172	58.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits are ensured for G = +2, V_S = ±2.5 to ±6V, R_F = R_{IN} = 470Ω, R_L = 100Ω.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
DYNAMIC PERFORMANCE						
	−3dB Bandwidth			90		MHz
	0.1dB Bandwidth	V_S = ±6V		12		MHz
	Slew Rate	V_S = ±6V, 4V Step, 10-90%		135		V/μs
	Rise and Fall Time	V_S = 6V, 4V Step, 10-90%		23.5		ns
DISTORTION and NOISE RESPONSE						
	2^{nd} Harmonic Distortion	V_O = 8.4 V_{PP}, f = 100 kHz, R_L = 25Ω		−105		dBc
		V_O = 8.4 V_{PP}, f = 1 MHz, R_L = 100Ω		−90		dBc
	3^{rd} Harmonic Distortion	V_O = 8.4 V_{PP}, f = 100 kHz, R_L = 25Ω		−110		dBc
		V_O = 8.4 V_{PP}, f = 1 MHz, R_L = 100Ω		−87		dBc
	Input Noise Voltage	f = 100 kHz		3.1		nV/√Hz
	Input Noise Current	f = 100 kHz		1.8		pA/√Hz
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	T_J = −40°C to 125°C	−5.5	0.1	5.5	mV
			−4	−0.2	4	
I_B	Input Bias Current	T_J = −40°C to 125°C		8	16	μA
I_{OS}	Input Offset Current	T_J = −40°C to 125°C	−2.1	0	2.1	μA
CMVR	Common Voltage Range	V_S = ±6V	−6.0	−5.7 to 4.5	4.5	V
CMRR	Common-Mode Rejection Ratio	V_S = ±6V, T_J = −40°C to 125°C	150	7.5		μV/V
TRANSFER CHARACTERISTICS						
A_{VOL}	Voltage Gain	R_L = 1k, T_J = −40°C to 125°C	1.0	5		V/mV
		R_L = 25Ω, T_J = −40°C to 125°C	0.67	3.4		V/mV
V_O	Output Swing	R_L = 25Ω, V_S = ±6V	−4.5	±4.8	4.5	V
		R_L = 25Ω, T_J = −40°C to 125°C, V_S = ±6V	−4.4	±4.8	4.4	
V_O	Output Swing	R_L = 1k, V_S = ±6V	−4.8	±4.8	4.8	V
		R_L = 1k, T_J = −40°C to 125°C, V_S = ±6V	−4.7	±4.8	4.7	
I_{SC}	Output Current(3)	V_O = 0, V_S = ±6V	350	525		mA
		V_O = 0, V_S = ±6V, T_J = −40°C to 125°C	260	600		mA
POWER SUPPLY						
I_S	Supply Current/Amp	V_S = ±6V			8	mA
		V_S = ±6V, T_J = −40°C to 125°C		7.2	9	
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±6V, T_J = −40°C to 125°C	72	88.5		dB

(1) All limits are specified by testing, characterization or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Shorting the output to either supply or ground will exceed the absolute maximum T_J and can result in failure.

6.6 ±2.5V Electrical Characteristics

Unless otherwise specified, all limits are ensured for G = +2, V_S = ±2.5 to ±6V, R_F = R_{IN} = 470Ω, R_L = 100Ω.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
DYNAMIC PERFORMANCE						
	−3 dB Bandwidth			80		MHz
	0.1 dB Bandwidth			12		MHz
	Rise and Fall Time	2V Step, 10-90%		14		ns
DISTORTION and NOISE RESPONSE						
	2^{nd} Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz, R_L = 25Ω		−96		dBc
		V_O = 2 V_{PP}, f = 1 MHz, R_L = 100Ω		−85		dBc
	3^{rd} Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz, R_L = 25Ω		−98		dBc
		V_O = 2 V_{PP}, f = 1 MHz, R_L = 100Ω		−87		dBc
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	T_J = −40°C to 125°C	−5.5		5.5	mV
			−4.0	0.02	4.0	
I_B	Input Bias Current	T_J = −40°C to 125°C		8.0	16	µA
CMVR	Common-Mode Voltage Range		−2.5		1.0	V
CMRR	Common-Mode Rejection Ratio	T_J = −40°C to 125°C	150	8		µV/V
TRANSFER CHARACTERISTICS						
A_{VOL}	Voltage Gain	R_L = 25Ω, T_J = −40°C to 125°C	0.67	3		V/mV
		R_L = 1k, T_J = −40°C to 125°C	1.0	4		
OUTPUT CHARACTERISTICS						
V_O	Output Voltage Swing	R_L = 25Ω	1.20	1.45		V
		R_L = 25Ω, T_J = −40°C to 125°C	1.10	1.35		
		R_L = 1k	1.30	1.60		
		R_L = 1k, T_J = −40°C to 125°C	1.25	1.50		
POWER SUPPLY						
I_S	Supply Current/Amp				8.0	mA
		T_J = −40°C to 125°C		6.7	9.0	

(1) All limits are specified by testing, characterization or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.7 Typical Performance Characteristics

Av = + 2V/V

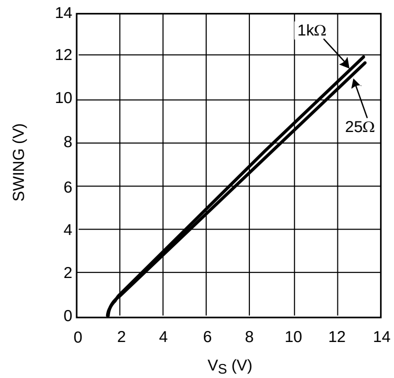


Figure 1. Output Swing R_L = 25Ω, 1 kΩ @ −40°C, 25°C, 85°C

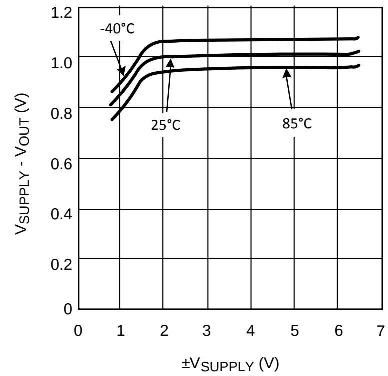


Figure 2. Positive Output Swing into 1kΩ

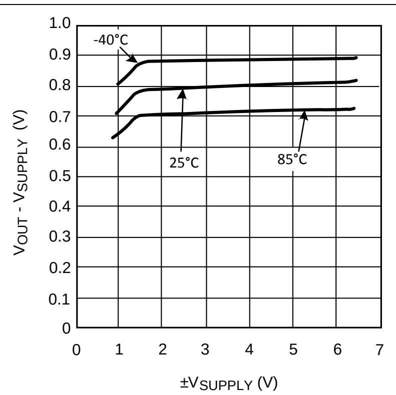


Figure 3. Negative Output Swing into 1 kΩ

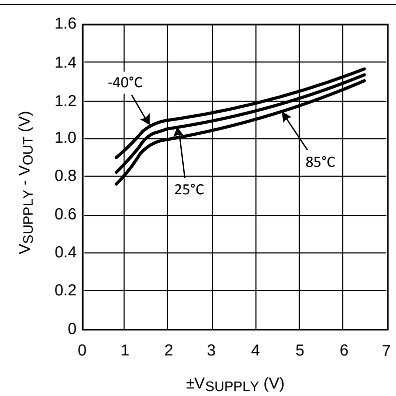


Figure 4. Positive Output Swing into 25Ω

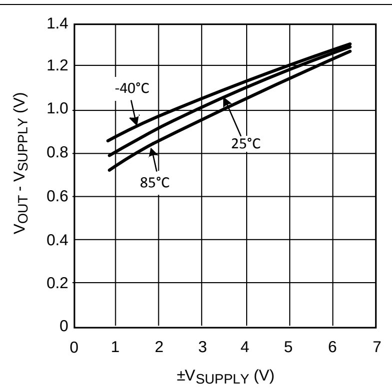


Figure 5. Negative Output Swing into 25Ω

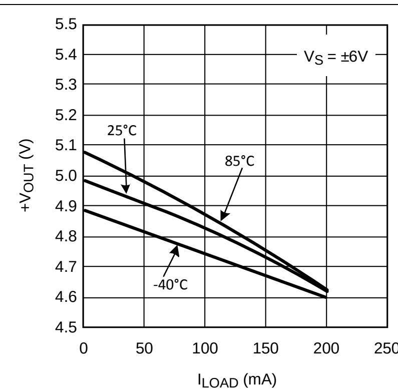


Figure 6. $+V_{OUT}$ vs. I_{LOAD}

Typical Performance Characteristics (continued)

Av = + 2V/V

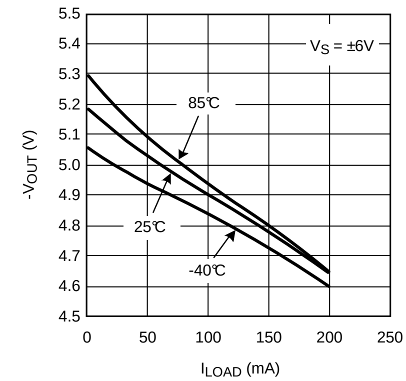


Figure 7. −V_{OUT} vs. I_{LOAD}

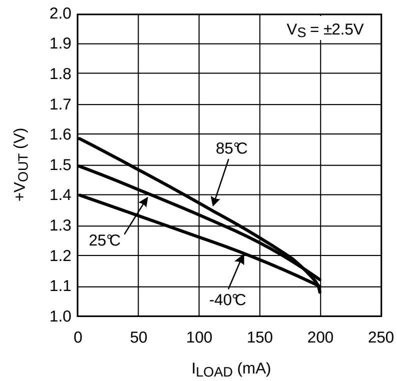


Figure 8. +V_{OUT} vs. I_{LOAD}

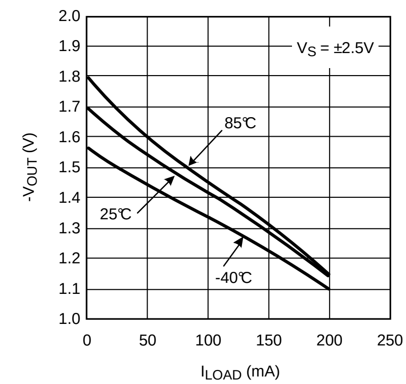


Figure 9. −V_{OUT} vs. I_{LOAD}

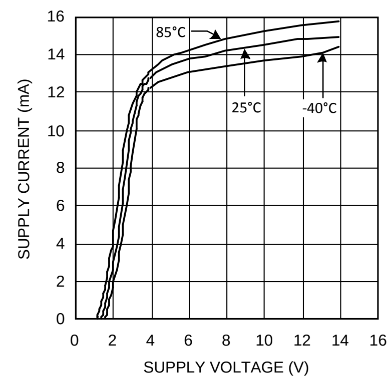


Figure 10. Supply Current vs. Supply Voltage

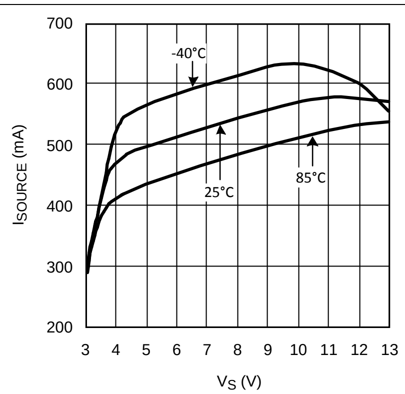


Figure 11. Sourcing Current vs. Supply Voltage

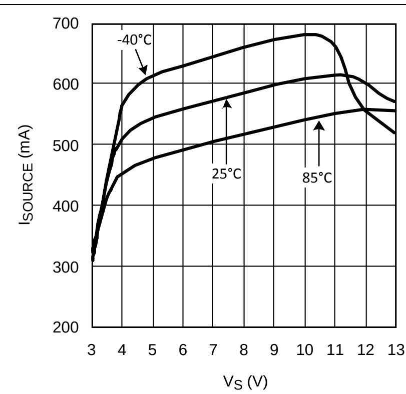


Figure 12. Sinking Current vs. Supply Voltage

Typical Performance Characteristics (continued)

Av = + 2V/V

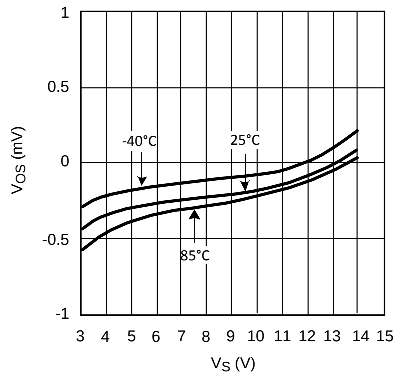


Figure 13. V_{OS} vs. V_S

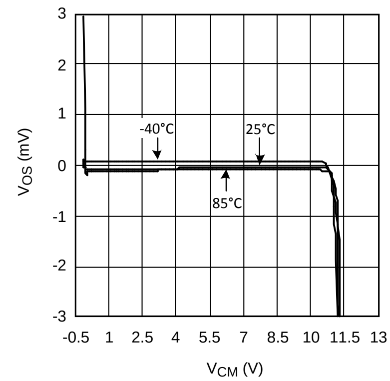


Figure 14. V_{OS} vs. V_{CM}, V_S = 12V

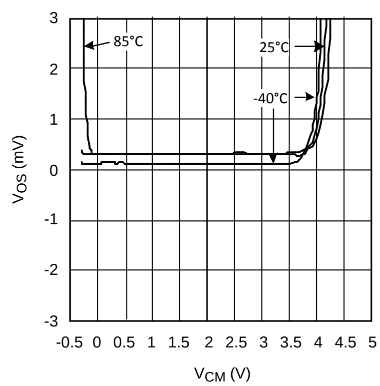


Figure 15. V_{OS} vs. V_{CM}, V_S = 5V

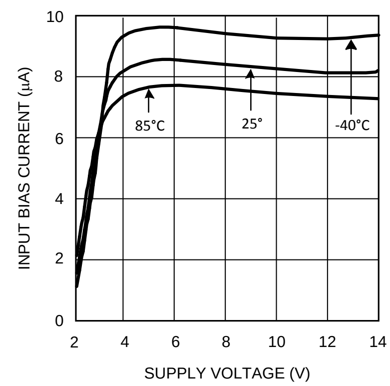


Figure 16. Bias Current vs. V_{SUPPLY}

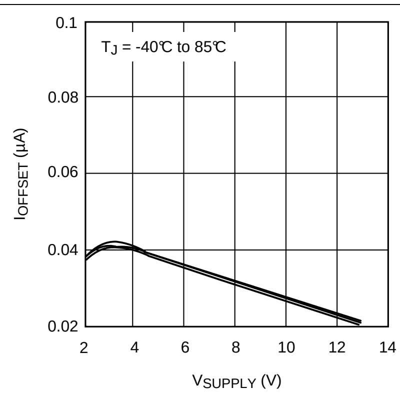


Figure 17. Offset Current vs. V_{SUPPLY}

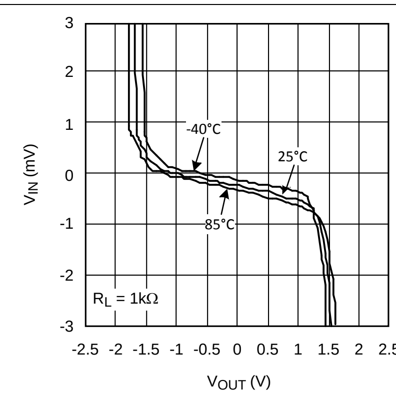


Figure 18. V_{OUT} vs. V_{IN}

Typical Performance Characteristics (continued)

Av = + 2V/V

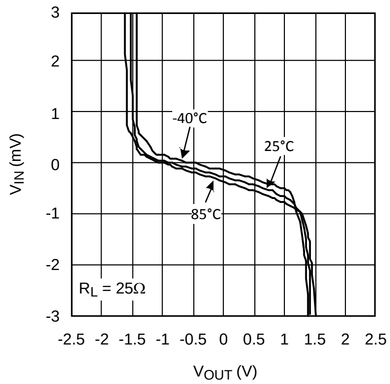


Figure 19. V_{OUT} vs. V_{IN}

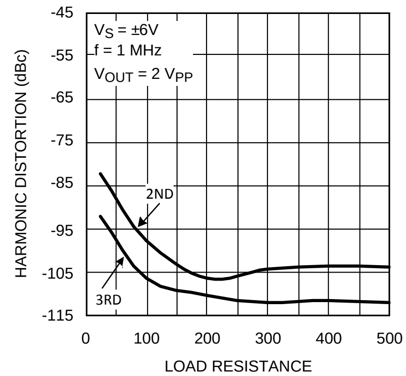


Figure 20. Harmonic Distortion vs. Load

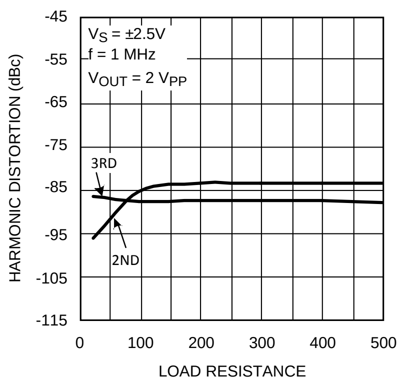


Figure 21. Harmonic Distortion vs. Load

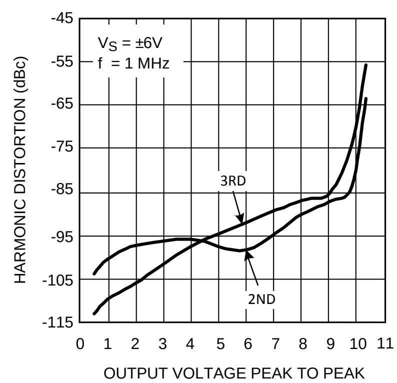


Figure 22. Harmonic Distortion vs. Output Voltage

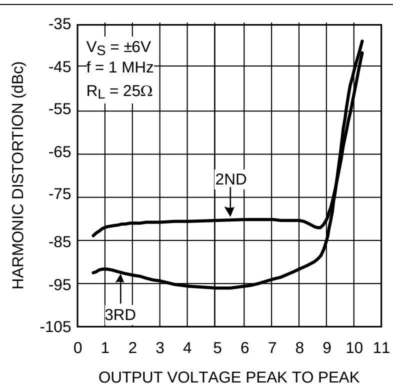


Figure 23. Harmonic Distortion vs. Output Voltage

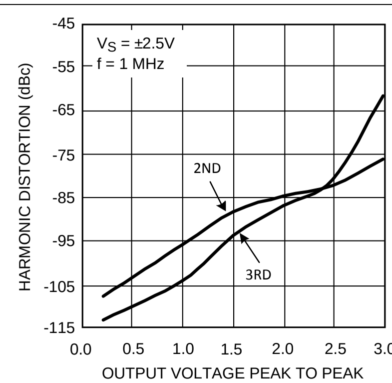


Figure 24. Harmonic Distortion vs. Output Voltage

Typical Performance Characteristics (continued)

Av = + 2V/V

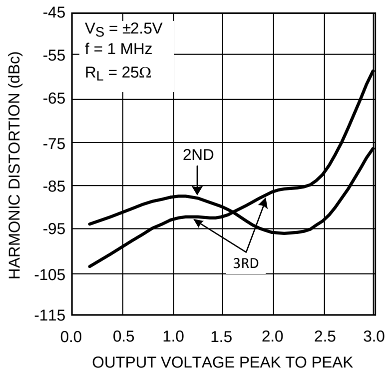


Figure 25. Harmonic Distortion vs. Output Voltage

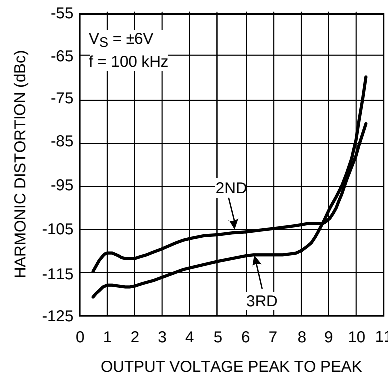


Figure 26. Harmonic Distortion vs. Output Voltage

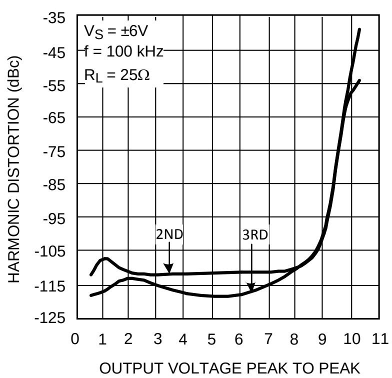


Figure 27. Harmonic Distortion vs. Output Voltage

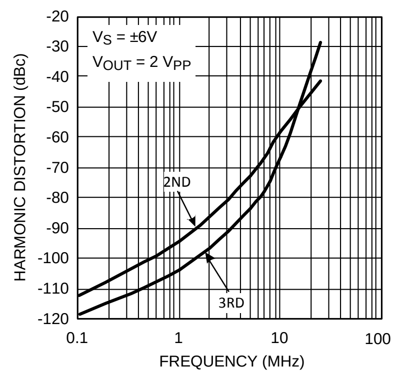


Figure 28. Harmonic Distortion vs. Frequency

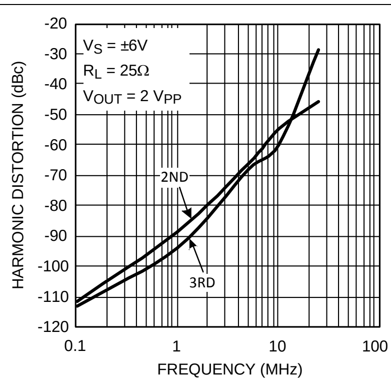


Figure 29. Harmonic Distortion vs. Frequency

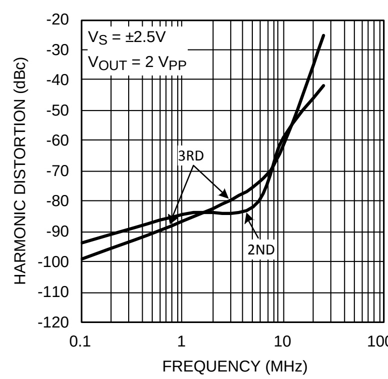


Figure 30. Harmonic Distortion vs. Frequency

Typical Performance Characteristics (continued)

Av = + 2V/V

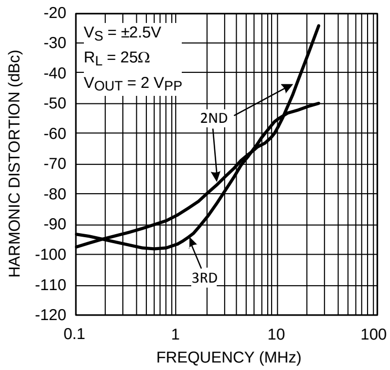


Figure 31. Harmonic Distortion vs. Frequency

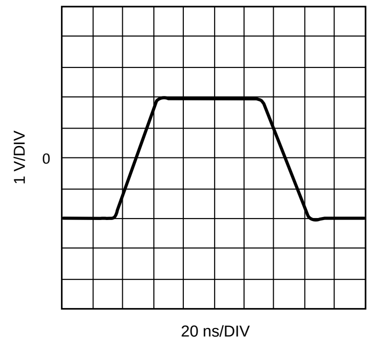


Figure 32. Pulse Response, V_S= ±6V

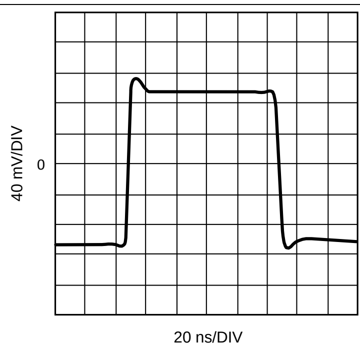


Figure 33. Pulse Response, V_S= ±2.5V, ±6V

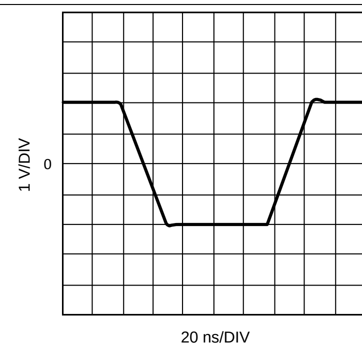


Figure 34. Pulse Response, A_{VCL} = −1, V_S= ±6V

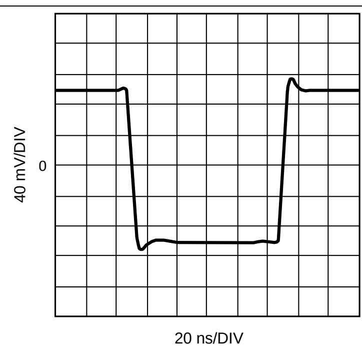


Figure 35. Pulse Response, A_{VCL} = −1, V_S= ±2.5V, ±6V

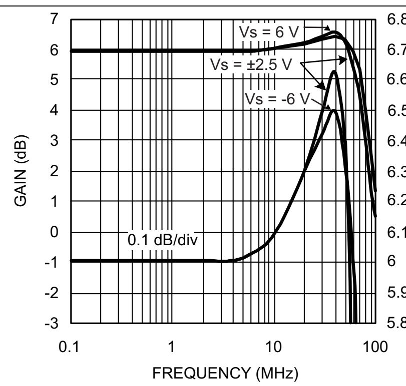


Figure 36. Frequency Response

Typical Performance Characteristics (continued)

Av = + 2V/V

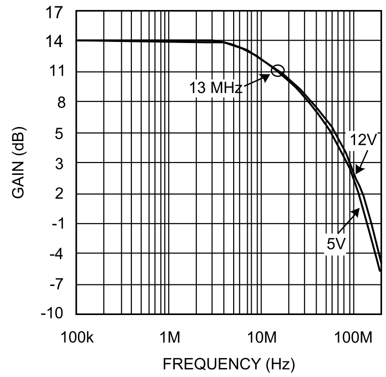


Figure 37. Frequency Response, A_{VCL} = +5V/V

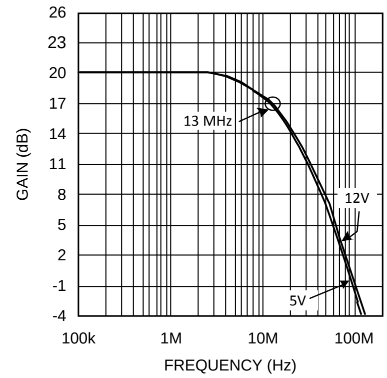


Figure 38. Frequency Response, A_{VCL} = +10V/V

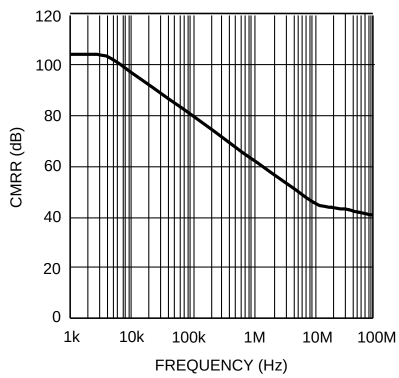


Figure 39. CMRR vs. Frequency, Vs = 12V

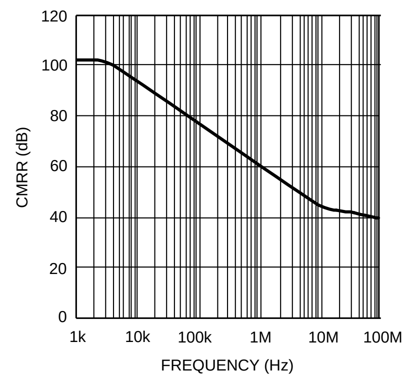


Figure 40. CMRR vs. Frequency, Vs = 5V

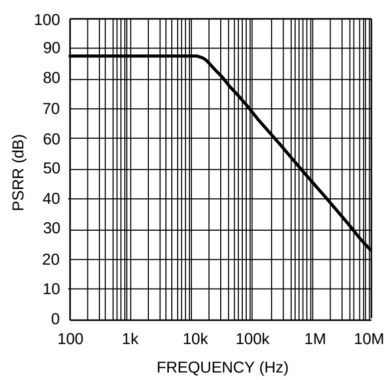


Figure 41. PSRR+ vs. Frequency, V_S = 5V and 12V

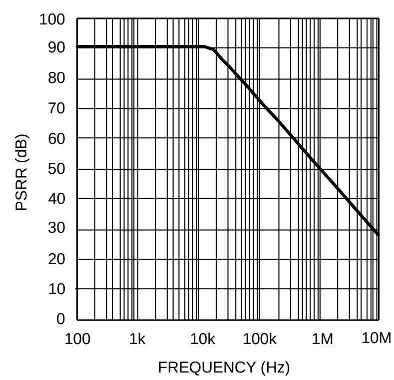


Figure 42. PSRR− vs. Frequency V_S = 5V and 12V

Typical Performance Characteristics (continued)

Av = + 2V/V

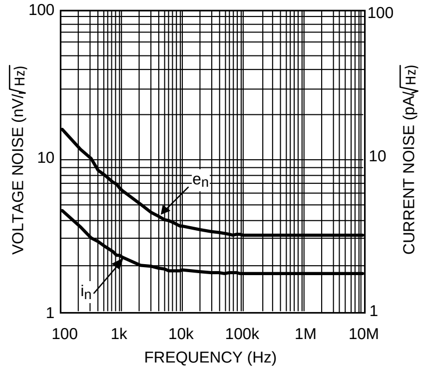


Figure 43. e_n & i_n vs. Frequency, V_S = 5V and 12V

7 Detailed Description

7.1 Functional Block Diagram

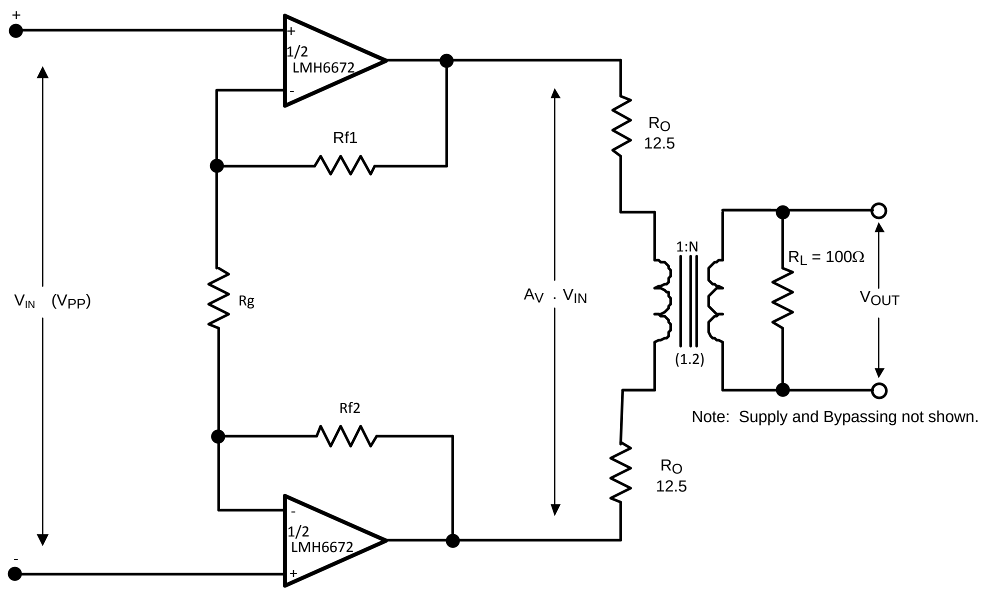


Figure 44. LMH6672 Block Diagram

8 Power Supply Recommendations

8.1 Thermal Management

The LMH6672 is a high-speed, high power, dual operational amplifier with a very high slew rate and very low distortion. For ease of use, it uses conventional voltage feedback. These characteristics make the LMH6672 ideal for applications where driving low impedances of 25 to 100 Ω such as xDSL and active filters.

A class AB output stage allows the LMH6672 to deliver high currents to low impedance loads with low distortion while consuming low quiescent supply current. For most op-amps, class AB topology means that internal power dissipation is rarely an issue, even with the trend to smaller surface mount packages. However, the LMH6672 has been designed for applications where high levels of power dissipation may be encountered.

Several factors contribute to power dissipation and consequently higher junction temperatures. These factors need to be well understood if the LMH6672 is to perform to specifications in all applications. This section will examine the typical application shown in Figure 44 as an example. Because both amplifiers are in a single package, the calculations are for the total power dissipated by both amplifiers.

There are two separate contributors to the internal power dissipation:

1. The product of the supply voltage and the quiescent current when no signal is being delivered to the external load.
2. The additional power dissipated while delivering power to the external load.

The first of these components appears easy to calculate simply by inspecting the data sheet. The typical quiescent supply current for this part is 7.2 mA per amplifier. Therefore, with a ±6 volt supply, the total power dissipation is:

$$P_D = V_S \times 2 \times I_Q = 12 \times (14.4 \times 10^{-3}) = 173 \text{ mW}$$

where

- $(V_S = V_{CC} + V_{EE})$ (1)

With a thermal resistance of 172°C/W for the SOIC package, this level of internal power dissipation will result in a junction temperature (T_J) of 30°C above ambient.

Using the worst-case maximum supply current of 18 mA and an ambient of 85°C, a similar calculation results in a power dissipation of 216 mW, or a T_J of 122°C.

This is approaching the maximum allowed T_J of 150°C before a signal is applied. Fortunately, in normal operation, this term is reduced, for reasons that will soon be explained.

The second contributor to high T_J is the power dissipated internally when power is delivered to the external load. This cause of temperature rise is more difficult to calculate, even when the actual operating conditions are known.

To maintain low distortion, in a Class AB output stage, an idle current, I_Q, is maintained through the output transistors when there is little or no output signal. In the LMH6672, about 4.8 mA of the total quiescent supply current of 14.4 mA flows through the output stages.

Under normal large signal conditions, as the output voltage swings positive, one transistor of the output pair will conduct the load current, while the other transistor shuts off, and dissipates no power. During the negative signal swing this situation is reversed, with the lower transistor sinking the load current while the upper transistor is cut off. The current in each transistor will approximate a half wave rectified version of the total load current.

Because the output stage idle current is now routed into the load, 4.8 mA can be subtracted from the quiescent supply current when calculating the quiescent power when the output is driving a load.

Thermal Management (continued)

The power dissipation caused by driving a load in a DSL application, using a 1:2 turns ratio transformer driving 20 mW into the subscriber line and 20 mW into the back termination resistors, can be calculated as follows:

$P_{DRIVER} = P_{TOT} – (P_{TERM} + P_{LINE})$

Where

- P_{DRIVER} is the LMH6672 power dissipation
- P_{TOT} is the total power drawn from the power supply
- P_{TERM} is the power dissipated in the back termination resistors
- P_{LINE} is the power sent into the subscriber line
- At full specified power, $P_{TERM} = P_{LINE} = 20$ mW, $P_{TOT} = V_S \times I_S$ (2)

In this application, $V_S = 12V$.

$I_S = I_Q + A_{VG} |I_{OUT}|$ (3)

I_Q = the LMH6672 quiescent current minus the output stage idle current. (4)

$I_Q = 14.4 – 4.8 = 9.6$ mA (5)

Average (A_{VG}) $|I_{OUT}|$ for a full-rate ADSL CPE application, using a 1:2 turns ratio transformer, is $\sqrt{(40\text{ mW}/50\Omega)}$ = 28.28 mA RMS.

For a Gaussian signal, which the DMT ADSL signal approximates, $A_{VG} |I_{OUT}| = \sqrt{2/\pi} \times I_{RMS}$ = 22.6 mA. Therefore, P_{TOT} = (22.6 mA + 9.6 mA) × 12V = 386 mW and P_{DRIVER} is 40 mW lower or 346 mW.

In the SOIC package, with a θ_{JA} of 172°C/W, this causes a temperature rise of 60°C. With an ambient temperature at the maximum recommended 85°C, the T_J is at 145°C, which is below the specified 150°C maximum.

Even if it is assumed that the absolute maximum I_S over temperature of 18 mA, when the I_Q is scaled up proportionally to 7 mA, the P_{DRIVER} only goes up by 17 mW causing a 62°C rise from ambient to 147°C.

Although very few CPE applications will ever operate in an environment as hot as 85°C, if a lower T_J is desired or the LMH6672 is to be used in an application where the power dissipation is higher, the SO PowerPAD (DDA) package provides a much lower $R_{\theta JA}$ of only 58.6° C/W. Using the same P_{DRIVER} as above, we find that the temperature rise is only about 21°C, resulting in T_J of 106°C with 85°C ambient.

NOTE

Since the exposed PAD (or DAP) of the SO PowerPAD (DDA) package is internally floating, the footprint for DAP could be connected to ground plane in PCB for better heat dissipation.

9 Device and Documentation Support

9.1 Trademarks

All trademarks are the property of their respective owners.

9.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6672MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	LMH66 72MA
LMH6672MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	LMH66 72MA
LMH6672MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	LMH66 72MA
LMH6672MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	LMH66 72MA
LMH6672MR/NOPB	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 150	LMH66 72MR
LMH6672MR/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 150	LMH66 72MR
LMH6672MRX/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	LMH66 72MR
LMH6672MRX/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	LMH66 72MR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

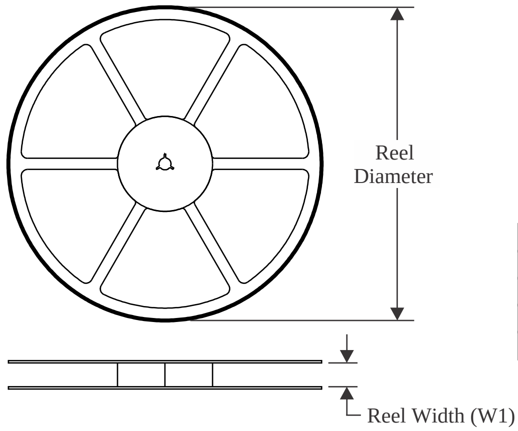
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

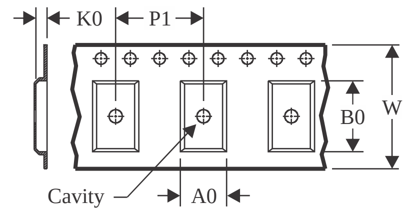
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

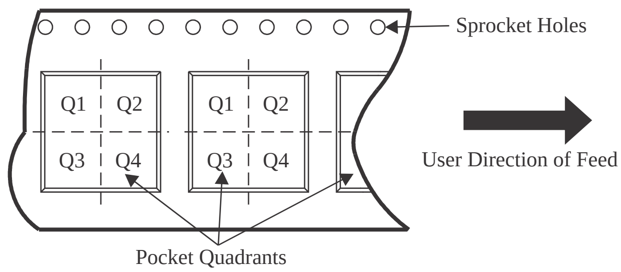


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

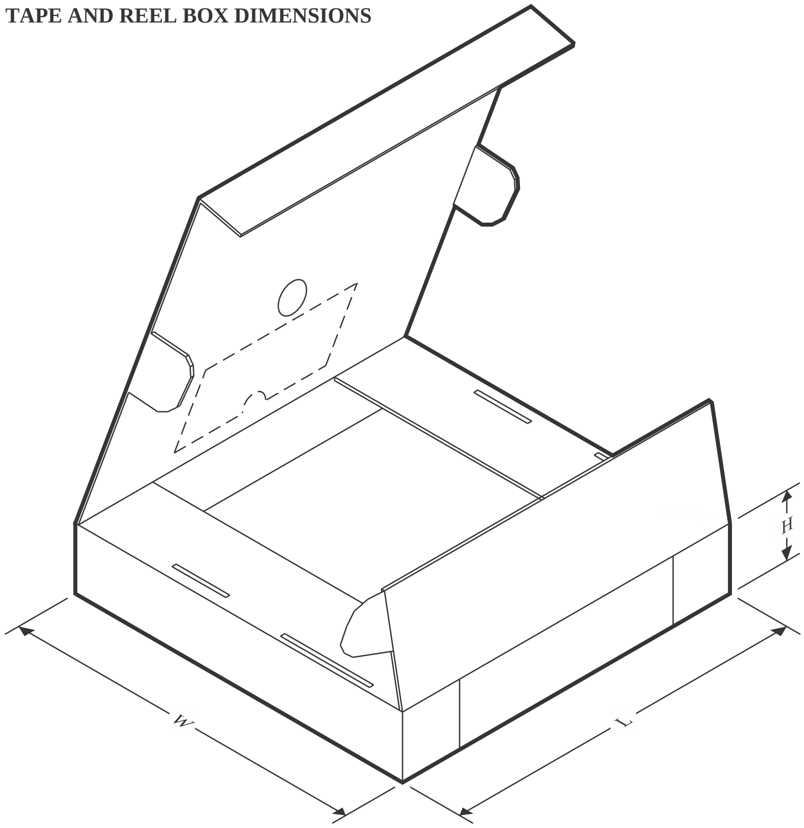
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6672MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6672MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

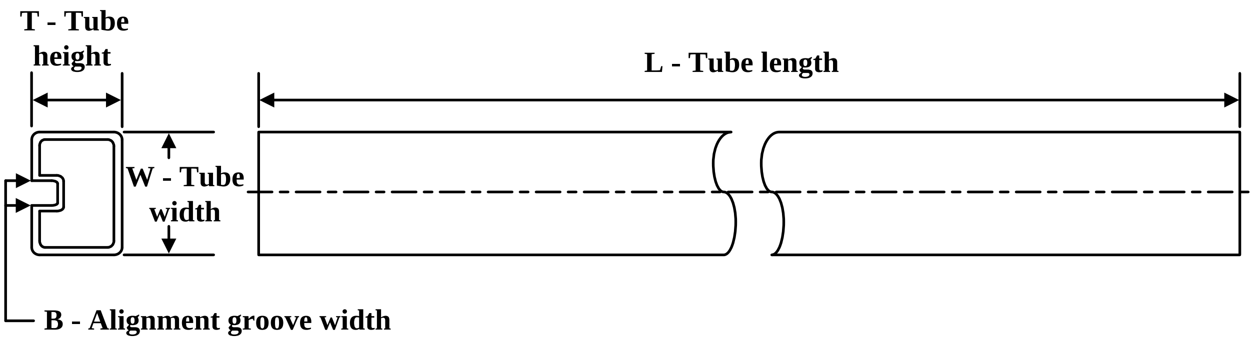
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

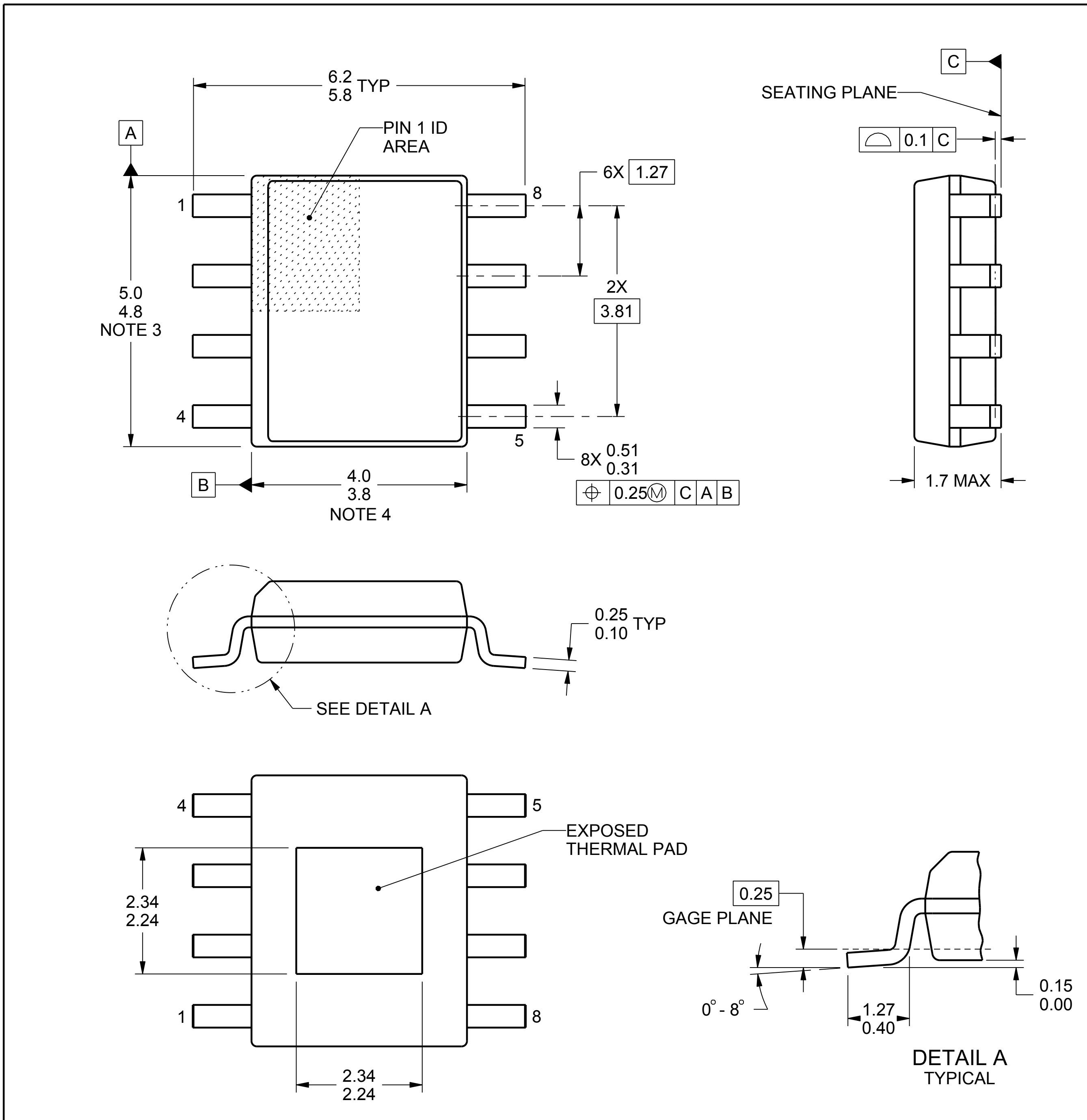
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6672MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6672MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6672MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6672MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMH6672MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LMH6672MR/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05

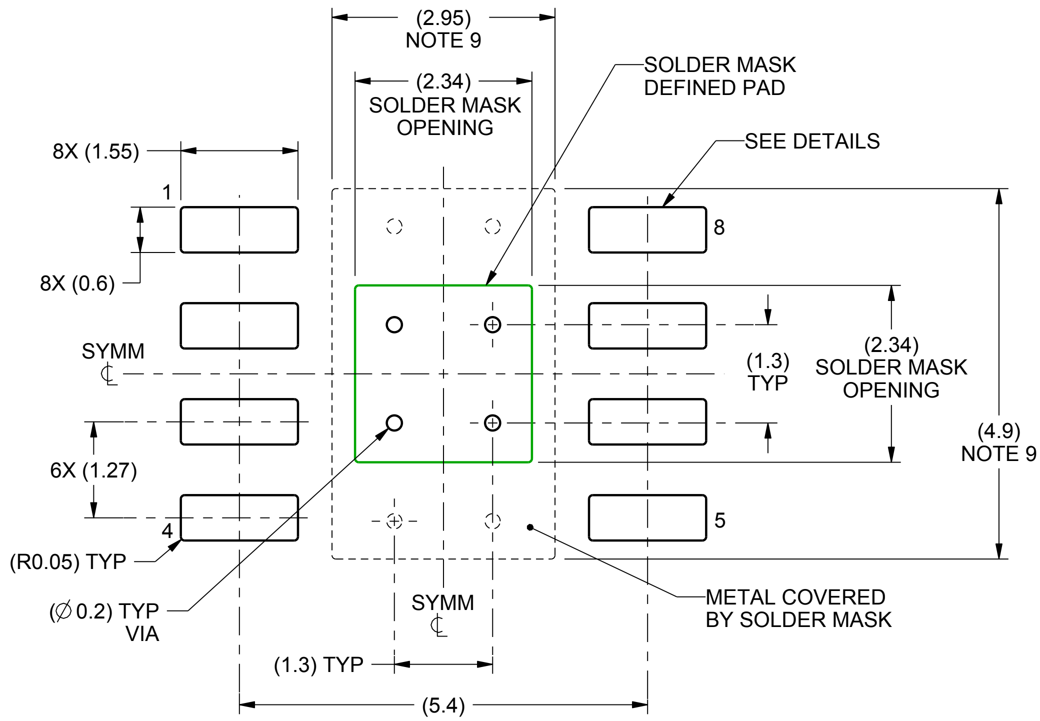


4218825/A 05/2016

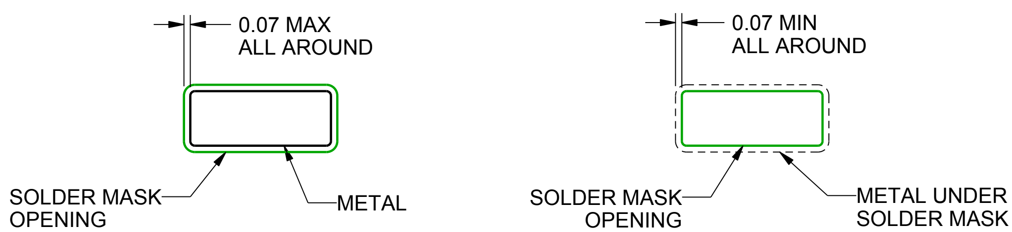
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

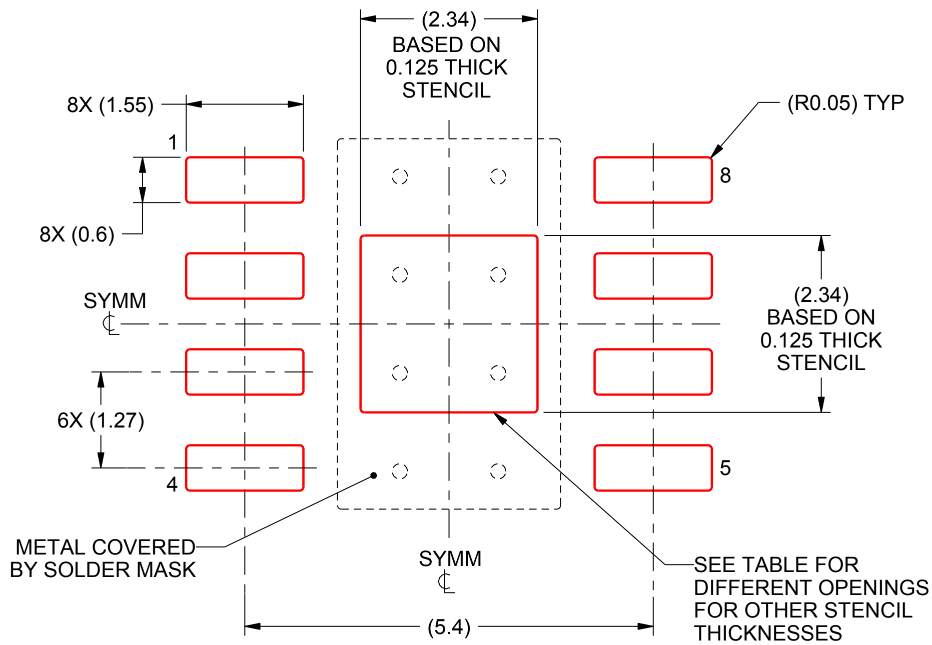
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



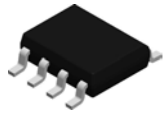
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

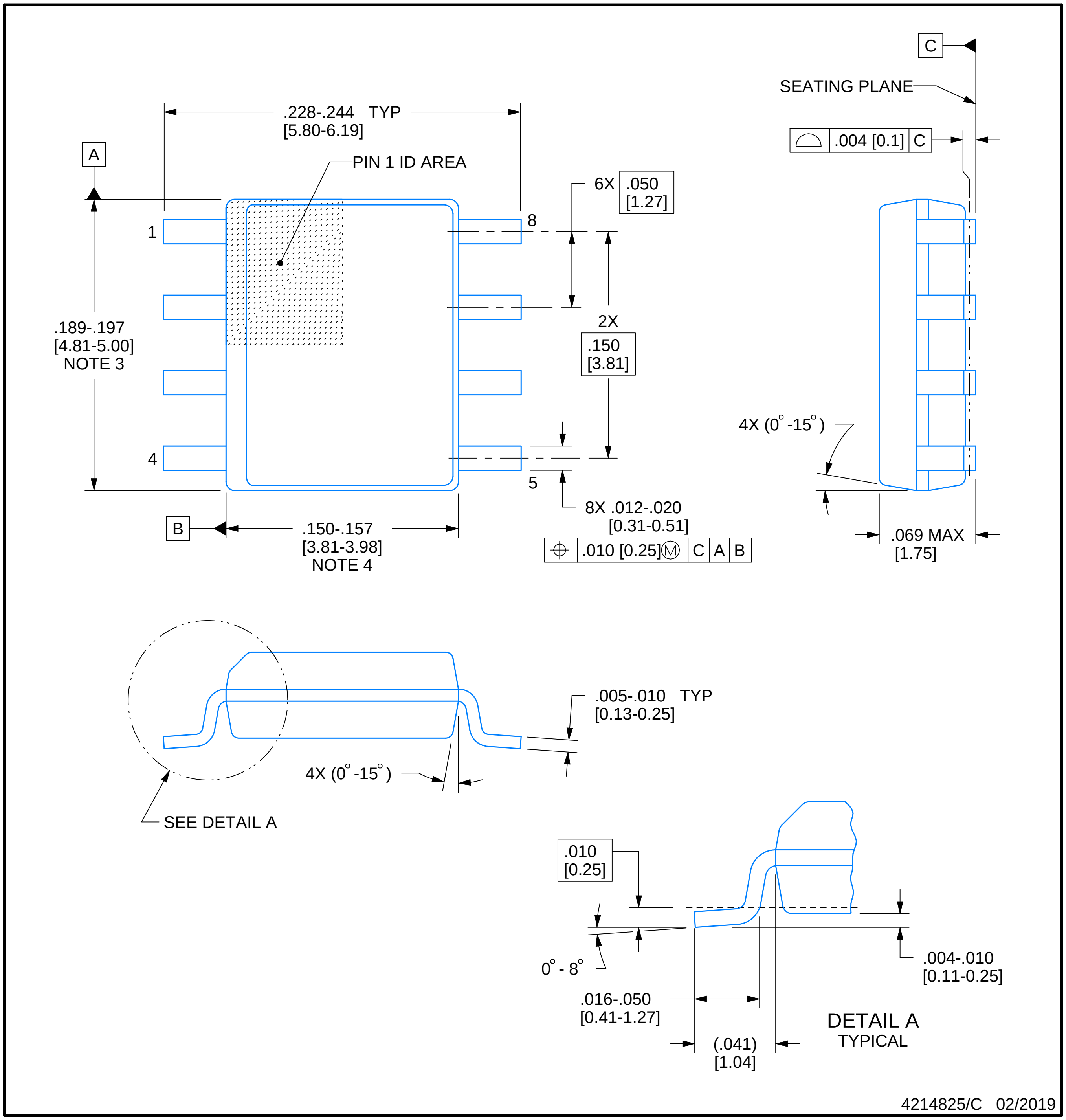


PACKAGE OUTLINE

D0008A

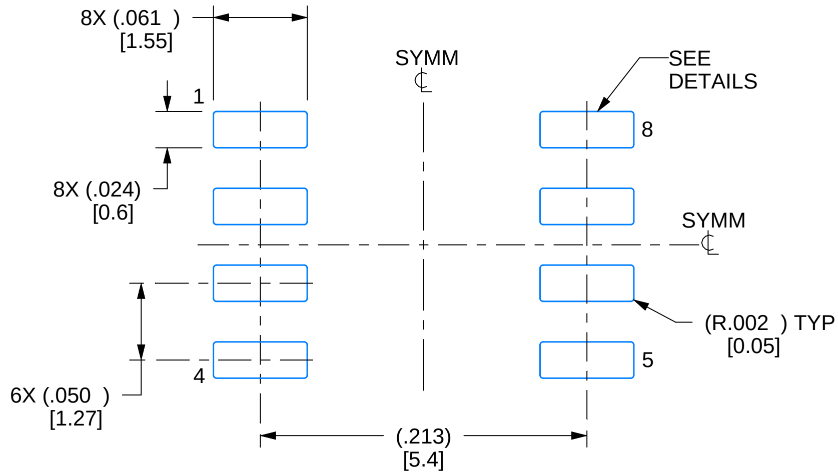
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

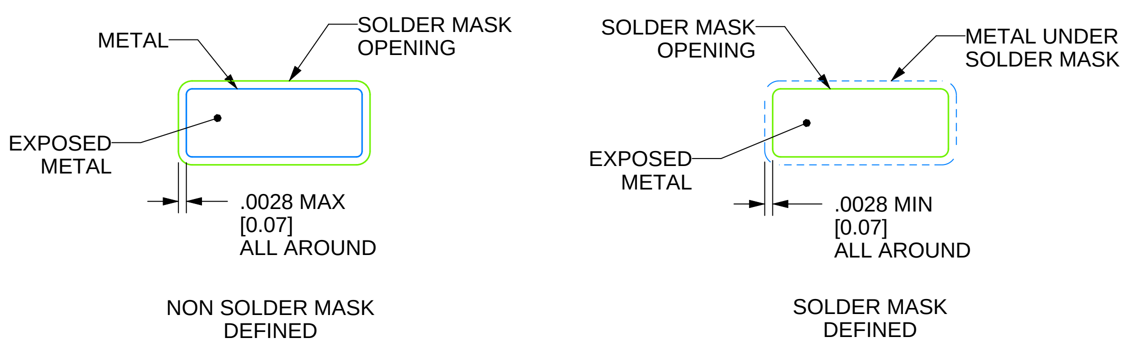


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

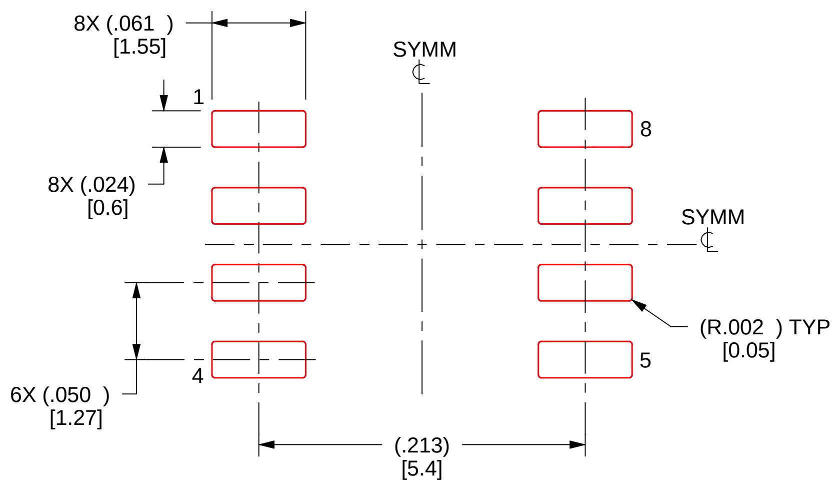


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.