

## ***iDiskOnChip (iDOC)***

### ***Flash Disk with IDE Interface***

Data Sheet, January 2006

#### **Highlights**

iDiskOnChip (iDOC) combines advanced and proven DiskOnChip technology with a standard IDE interface to complement the DiskOnChip product line.

iDiskOnChip provides:

- NAND flash-based technology
- High performance
- Platform independence
- Fast time to market - no driver required
- Reed-Solomon code-based EDC/ECC (2 bits/page)
- Wear-leveling mechanism that enables 2 million write/erase cycles for reliable data storage over an extended period
- Fast ATA host transfer rates supporting PIO-4 mode and DMA-2
- IDE master/slave modes of operation
- 40-pin or 44-pin IDE connector
- Vertical and horizontal alignments

#### **IDE Modes**

- PIO modes 0 through 4
- DMA modes 0 through 2

#### **Performance**

- Host data transfer rate:
  - Read: 5 MB/sec
  - Write: 4 MB/sec

#### **Power Requirements**

- Single power supply: 5V ( $\pm 10\%$ ) or 3.3V ( $\pm 5\%$ )
- Current
  - Active mode (typ.): 20 mA
  - Idle mode (max): 5 mA



#### **Operating Temperature**

- Temperature range: 0°C to +70°C

#### **Environmental Conditions**

- Storage temperature: -40°C to +70°C
- Sinusoidal vibration: 5g, 7-2000 Hz, 3 axes
- Shock: 50 G, 3 axes

#### **System Compatibility**

- Compatible with devices that support the ATA-4 Attachment for Disk Drive Standard

#### **Capacity and Packaging**

- Available in capacities of 16MB to 1536MB
- Alignments:
  - Vertical with or without shell
  - Horizontal, left-oriented
  - Horizontal, right-oriented

#### **Mechanical Dimensions**

- Vertical version with shell (LxWxH):
  - 40-pin: 56.5 x 6.0 x 28.70 (mm)
  - 44-pin: 53.2 x 6.5 x 27.85 (mm)
- Vertical version without shell (LxWxH):
  - 40-pin: 50.5 x 6.2 x 27.2 (mm)
  - 44-pin: 46.1 x 4.6 x 26.61 (mm)
- Horizontal version with shell (LxWxH):
  - 40-pin: 55.0 x 30.4 x 9.1 (mm)
  - 44-pin: 48.0 x 32.6 x 5.9 (mm)

## REVISION HISTORY

| Revision | Date          | Change Description                                                                                                                   | Reference                             |
|----------|---------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|
| 1.4      | October 2004  | Updated power consumption parameters<br>Added DMA support<br>Added list of supported IDE commands                                    | Section 6.4.2<br>--<br>Section 6.5    |
| 1.5      | December 2004 | Updated number of write/erase cycles<br>Updated ordering information                                                                 | Sections 3.4, 6.2.5<br>Section 7      |
| 1.6      | March 2005    | Added vertical shell-less configuration                                                                                              | Sections 6.3.3.2, 6.3.4.2             |
| 1.7      | May 2005      | Added new shell for vertical configuration<br>Added new capacity – 384MB                                                             | Section 6.3<br>Section 7              |
| 1.8      | August 2005   | Updated CHS parameters                                                                                                               | Section 6.6                           |
| 1.9      | January 2006  | Updated write performance parameters<br>Updated the ordering information for RoHS-compliant products<br>Updated storage temperatures | Highlights<br>Section 7<br>Section 15 |

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## 1. INTRODUCTION

This data sheet includes the following sections:

- Section 1:** Overview of data sheet contents
- Section 2:** Product overview, including brief product description, pin assignment and description
- Section 3:** Theory of operation
- Section 4:** Installation requirements, including electrical cabling and master/slave configurations
- Section 5:** Power management for the various iDiskOnChip operational modes
- Section 6:** Product specifications, including mechanical and electrical
- Section 7:** Product ordering information and available product configurations

For additional information on M-Systems' flash disk products, please contact one of the offices listed on the back page.

## **2. PRODUCT OVERVIEW**

### **2.1 Product Description**

iDiskOnChip complements the DiskOnChip product line, offering full IDE capabilities, high performance, a built-in ECC system and flexible design options. It can be used in any system with an IDE bus and can work with any operating system, since the driver is handled at the BIOS level.

iDiskOnChip is based on NAND flash technology. This technology is superior in its data storage characteristics, featuring the industry's highest write and erase performance, as well as the highest burst read/write transfer rate. Additionally, NAND flash technology is known for its high density and small die size, with the related cost and real estate benefits. Data integrity is guaranteed through embedded error detection and error correction code (EDC/ECC) that automatically detects and corrects data errors. An on-chip ECC unit generates the required code bytes for error detection and correction of up to 2 bits per 512-byte data sector. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without performance degradation.

iDiskOnChip is ergonomically designed for easy installation and ready-to-run operation. Available in 40-pin and 44-pin connector packages, iDiskOnChip fits easily into any platform with an IDE connector.

The horizontal version is provided in both left and right orientations, giving maximum flexibility for insertion to the host platform.

iDiskOnChip is available in capacities ranging from 16MB to 1536MB, making the upgrade path simple and fast.

## 2.2 Pin Assignment

iDiskOnChip uses a standard IDE pinout. See Table 1 for iDiskOnChip pin assignments.

Table 1: iDiskOnChip Pin Assignment

| Pin No.         | Signal | Function                         | Pin No.         | Signal   | Function            |
|-----------------|--------|----------------------------------|-----------------|----------|---------------------|
| 1               | RESET# | Host Reset                       | 2               | GND      | Ground              |
| 3               | HD7    | Host Data Bit 7                  | 4               | HD8      | Host Data Bit 8     |
| 5               | HD6    | Host Data Bit 6                  | 6               | HD9      | Host Data Bit 9     |
| 7               | HD5    | Host Data Bit 5                  | 8               | HD10     | Host Data Bit 10    |
| 9               | HD4    | Host Data Bit 4                  | 10              | HD11     | Host Data Bit 11    |
| 11              | HD3    | Host Data Bit 3                  | 12              | HD12     | Host Data Bit 12    |
| 13              | HD2    | Host Data Bit 1                  | 14              | HD13     | Host Data Bit 13    |
| 15              | HD1    | Host Data Bit 1                  | 16              | HD14     | Host Data Bit 14    |
| 17              | HD0    | Host Data Bit 0                  | 18              | HD15     | Host Data Bit 15    |
| 19              | GND    | Ground                           | 20              | 40-pin   | VCC <sup>1</sup>    |
|                 |        |                                  |                 | 44-pin   | KEY                 |
|                 |        |                                  |                 |          | Supply Voltage      |
|                 |        |                                  |                 |          | Cut pin             |
| 21              | DMARQ  | DMA Request                      | 22              | GND      | Ground              |
| 23              | HIOW#  | Host I/O Write                   | 24              | GND      | Ground              |
| 25              | HIOR#  | Host I/O Read                    | 26              | GND      | Ground              |
| 27              | IORDY  | I/O Ready                        | 28              | CSEL     | Master/Slave Select |
| 29              | DMACK  | DMA Acknowledge                  | 30              | GND      | Ground              |
| 31              | INTRQ  | Interrupt Request                | 32              | IOIS16#  | CS I/O 16-Bit       |
| 33              | HA1    | Host Address Bit 1               | 34              | PDIAG#   | Passed Diagnostics  |
| 35              | HA0    | Host Address Bit 0               | 36              | HA2      | Host Address Bit 2  |
| 37              | CS0#   | Chip Select 0                    | 38              | CS1#     | Chip Select 1       |
| 39              | DASP#  | Drive Active/<br>Drive 1 Present | 40              | GND      | Ground              |
| 41 <sup>2</sup> | NC     | Not Connected                    | 42 <sup>2</sup> | VCC      | Supply Voltage      |
| 43 <sup>2</sup> | GND    | Ground                           | 44 <sup>2</sup> | RESERVED | Reserved            |

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.

NC = These pins are not connected internally.

RESERVED = All reserved signals must be left floating.

## 2.3 Pin Description

Table 2 describes the pin descriptions for iDiskOnChip.

*Table 2: iDiskOnChip Pin Description*

| Signal                  | Pin No.  | Description                                                                                                                                                                                                                                                                                                                    | Signal Type |
|-------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <b>System Interface</b> |          |                                                                                                                                                                                                                                                                                                                                |             |
| HD15-HD0                | 3-18     | Host Data bus [15:0]. 16-bit bi-directional data input/output bus. HD15 is the most significant bit, while HD0 is the least significant bit. This bus carries data, commands and status information between the host and iDiskOnChip. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16 bits wide. | I/O         |
| HA2-HA0                 | 33,35,36 | Host Address bus HA[2:0]: Select the registers in the iDiskOnChip controller.                                                                                                                                                                                                                                                  | Input       |
| <b>Configuration</b>    |          |                                                                                                                                                                                                                                                                                                                                |             |
| DIOW#                   | 23       | Device I/O Write: Active low. Gates the data from the bus to iDiskOnChip. The clocking occurs on the rising edge of the signal.                                                                                                                                                                                                | Input       |
| DIOR#                   | 25       | Device I/O Read: Active low. Gates the data to the bus from iDiskOnChip. The clocking occurs on the falling edge of the signal.                                                                                                                                                                                                | Input       |
| CSEL                    | 28       | Configuration Select: Determines the device configuration as either Master or Slave. If CSEL is negated, then the device address is Master; if CSEL is asserted, then the device address is Slave.                                                                                                                             | Input       |
| CS0#                    | 37       | Host Chip Select 0: Active low. Selects the Command Block registers.                                                                                                                                                                                                                                                           | Input       |
| CS1#                    | 38       | Host Chip Select 1: Active low. Selects the Command Block registers.                                                                                                                                                                                                                                                           | Input       |
| <b>Control</b>          |          |                                                                                                                                                                                                                                                                                                                                |             |
| RESET#                  | 1        | Host reset: Active low.                                                                                                                                                                                                                                                                                                        | Input       |
| IORDY                   | 27       | I/O Ready: Negated by iDiskOnChip to extend the host transfer cycle (read or write) when the device is not ready to respond to a data transfer request.                                                                                                                                                                        | Output      |



| Signal        | Pin No.                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Signal Type |
|---------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| DMARQ         | 21                     | <p>DMA Request: This signal, used for DMA data transfers between the host and iDiskOnChip, is asserted by iDiskOnChip when it is ready to transfer data to or from the host.</p> <p>The direction of data transfer is controlled by DIOR# and DIOW#. This signal is used in a handshake manner with DMACK#, meaning iDiskOnChip waits until the host asserts DMACK# before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.</p> <p>This line is released (high impedance state) whenever iDiskOnChip is not selected, or is selected and no DMA command is in progress.</p> <p>When enabled by DMA transfer, DMARQ is driven high and low by the device.</p> <p>When a DMA operation is enabled, CS0# and CS1# are asserted and transfers are 16 bits wide.</p> | Output      |
| DMACK         | 29                     | DMA Acknowledge: This signal shall be used by the host in response to DMARQ to initiate DMA transfers                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Input       |
| INTRQ         | 31                     | Interrupt Request: Interrupt request from iDiskOnChip to the host. The output of this signal is tri-stated if the host disables the interrupt. When asserted, this signal is negated by the device within 400 nsec of the negation of the DIOR# signal that reads the Status register. When asserted, this signal is negated by the device within 400 nsec of the negation of the DIOW# signal that writes the Command register.                                                                                                                                                                                                                                                                                                                                                         | Output      |
| IOIS16#       | 32                     | I/O IS I6-Bit: Active low. Asserted (low) by iDiskOnChip to indicate to the host that the current cycle is a 16-bit (word) data transfer. When the signal is negated (high), an 8-bit data transfer is performed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Output      |
| <b>Status</b> |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |
| PDIAG#        | 34                     | Passed Diagnostics: Active low. Informs the Master drive that the self-diagnostic of the Slave drive has ended.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | I/O         |
| DASP#         | 39                     | Drive Active/Drive1 Present: Active low. This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | I/O         |
| <b>Power</b>  |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |
| GND           | 2,19,22,24,26,30,40,43 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Ground      |
| VCC           | 42                     | Power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Supply      |
| <b>Other</b>  |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |
| NC            | 41, 44                 | Not connected                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | N/A         |

### 3. THEORY OF OPERATION

#### 3.1 Overview

Figure 1 shows iDiskOnChip operation from the system level, including the major hardware blocks.

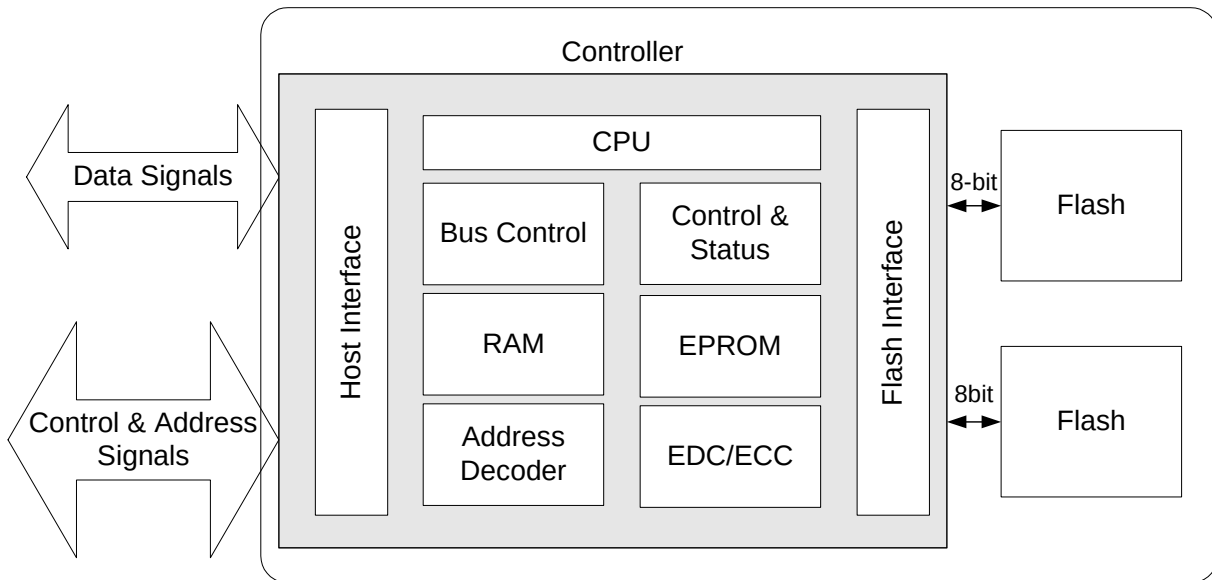


Figure 1: iDiskOnChip Block Diagram

iDiskOnChip integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

#### 3.2 Controller

The controller is equipped with 16KB of internal memory that is used for storing code and data. The internal memory can also be used as an intermediate memory for storing data blocks during a wear-leveling procedure.

An 8KB internal boot ROM includes basic routines for accessing the flash memories and for loading the main code into the internal memory.

The host interface provides all required signals, is fully compliant with the PC Card standard, and supports True-IDE mode operation requirements.

#### 3.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a Reed-Solomon algorithm that can correct two bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

### 3.4 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

iDiskOnChip uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

iDiskOnChip sustains more than two million write/erase cycles and an unlimited number of read cycles.

## 4. INSTALLATION REQUIREMENTS

### 4.1 iDiskOnChip Pin Directions

Figure 2 and Figure 3 illustrate the iDiskOnChip pin directions in the vertical version.

As the horizontal version uses the same connector, the same pin directions can be used for the horizontal models.

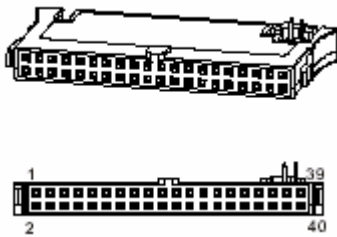


Figure 2: 40-Pin (Vertical with Shell) iDiskOnChip Connector Layout

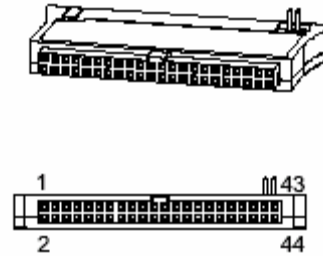


Figure 3: 44-Pin (Vertical with Shell) iDiskOnChip Connector Layout

### 4.2 iDiskOnChip Left/Right Orientation, Horizontal Version

The right-oriented iDiskOnChip, when held as shown in Figure 4, has pin 1 on the right side. The left-oriented iDiskOnChip, when held as shown in Figure 5, has pin 1 on the left side.

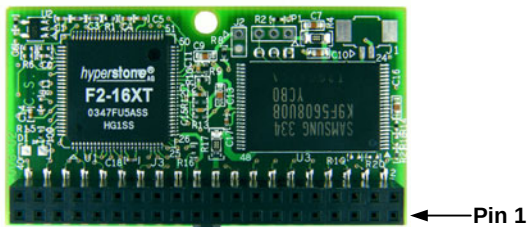


Figure 4: iDiskOnChip Horizontal Version 40 pin, Right-Oriented

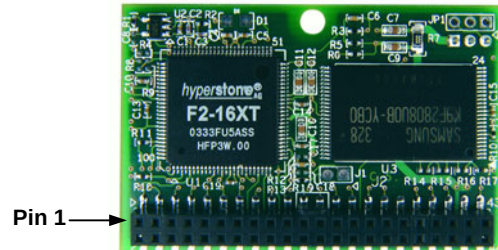


Figure 5: iDiskOnChip Horizontal Version 44 pin, Left-Oriented

### 4.3 Electrical Connections for iDiskOnChip

iDiskOnChip can be connected to the host by placing it directly on the on-board socket. If a cable is used, it should be no longer than 18 inches, and should be aligned as follows:

- For 44-pin iDiskOnChip:
  - o Pin 1 of the cable must be aligned with pin 1 of the iDiskOnChip connector.
  - o Pin 44 of the cable must be aligned with pin 44 of the iDiskOnChip connector.
- For 40-pin iDiskOnChip:
  - o Pin 1 of the cable must be aligned with pin 1 of the iDiskOnChip connector.
  - o Pin 40 of the cable must be aligned with pin 40 of the iDiskOnChip connector.

The 40-pin iDiskOnChip version has a separate connector for the power supply, to which a power supply cable can be connected. In addition, pin 20 can also be used for power supply connections. Please refer to the pin description for further details.

Note: For a list of recommended connectors, contact an M-Systems representative.

### 4.4 Installing iDiskOnChip in a Two-Drive Configuration (Master/Slave)

If iDiskOnChip is being installed as an additional IDE drive using the same IDE I/O port, jumper J1 must be set to indicate that this drive is a slave. The default is master with no jumpers. Table 3 shows the J1 jumper settings for iDiskOnChip operation in Master and Slave mode.

Table 3: Jumper Settings for Master/Slave Mode

| J1 Jumper Settings            | Operation Mode |
|-------------------------------|----------------|
| No jumper is installed (open) | Master         |
| Jumper is installed (short)   | Slave          |

#### 4.4.1 Vertical Configuration

The vertical configuration can operate in either Master or Slave mode. The following figures show the jumper settings for the iDiskOnChip vertical configuration.



Figure 6: Slave Setting for Vertical iDiskOnChip  
44-Pin Connector



Figure 7: Slave Setting for Vertical iDiskOnChip  
40-Pin Connector



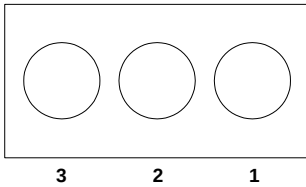
Figure 8: Master Setting for Vertical iDiskOnChip  
44-Pin Connector



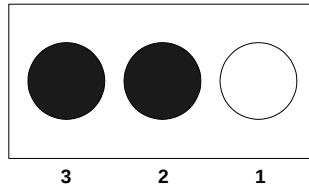
Figure 9: Master Setting for Vertical iDiskOnChip  
40-Pin Connector

#### 4.4.2 Horizontal Configuration

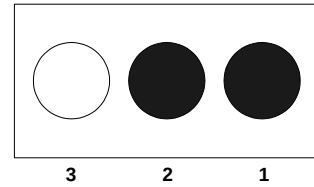
The horizontal configuration can operate in either Master or Slave mode. The mode can be set via the device jumper settings. In addition, the jumpers can be set to cable select. The following figures show the jumper settings for iDiskOnChip horizontal configuration.



*Figure 10: Jumper Not Installed, iDiskOnChip Configured as Master*



*Figure 11: Jumper Installed on Pins 2-3, iDiskOnChip Configured According to Cable Select*



*Figure 12: Jumper Installed on Pins 1-2, iDiskOnChip Configured as Slave*

## 5. POWER MANAGEMENT

iDiskOnChip has three operational modes, listed below. Idle and Sleep modes provide automatic power management.

- **Active:** If the iDiskOnChip controller receives any Command In or Soft Reset, it enters Active mode. In Active mode, iDiskOnChip can execute any supported ATA command. The power consumption level is the highest in this mode.
- **Idle:** After the iDiskOnChip controller executes any ATA command or Soft Reset, it automatically enters Idle mode. Power consumption is reduced as compared with Active mode.
- **Sleep:** The iDiskOnChip controller automatically transfers the device from Idle into Sleep mode if there is no Command In or Soft Reset from the host for about 16 ms. This time interval can be modified by firmware if necessary. In Sleep mode, iDiskOnChip power consumption is at its lowest level. During Sleep mode, the system main clock is stopped. This mode can be released through a hardware reset, software reset, or when any ATA command is asserted.

## 6. SPECIFICATIONS

### 6.1 CE and FCC Compatibility

iDiskOnChip conforms to CE requirements and FCC standards.

### 6.2 Environmental Specifications

#### 6.2.1 Temperature Ranges

Temperature Range 0°C to +70°C

Storage Temperature: -40°C to +70°C

#### 6.2.2 Humidity

Relative Humidity: 10-95%, non-condensing

#### 6.2.3 Shock and Vibration

Table 4: Shock/Vibration Testing for iDiskOnChip

| Reliability Tests | Test Conditions               | Reference Standards |
|-------------------|-------------------------------|---------------------|
| Vibration         | 7 Hz to 2000 Hz, 5 g, 3 axes  | IEC 68-2-6          |
| Mechanical Shock  | Duration: 10 ms, 50 g, 3 axes | IEC 68-2-27         |
| Drop Unit         | From a height of 1.5 m        | IEC 68-2-32         |

#### 6.2.4 Mean Time between Failures (MTBF)

Table 5 summarizes the MTBF prediction results for various iDiskOnChip configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- Mean Time Between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 5: iDiskOnChip MTBF

| Product           | Condition                 | MTBF (Hours) | Failure Rate per Million Hours |
|-------------------|---------------------------|--------------|--------------------------------|
| Vertical 40-pin   | Telcordia SR-332 GB, 25°C | 5,267,540    | 0.1898                         |
| Horizontal 40-pin |                           | 4,650,009    | 0.2151                         |
| Vertical 44-pin   |                           | 6,188,875    | 0.1616                         |
| Horizontal 44-pin |                           | 6,102,525    | 0.1639                         |



## 6.2.5 Endurance

iDiskOnChip sustains more than two million write/erase cycles and an unlimited number of read cycles. Performance is enhanced by the following features:

## 6.3 Mechanical Dimensions

### 6.3.1 40-Pin Horizontal Version

Figure 13 shows the mechanical dimensions of both left- and right-oriented iDiskOnChip, 40-pin horizontal version.

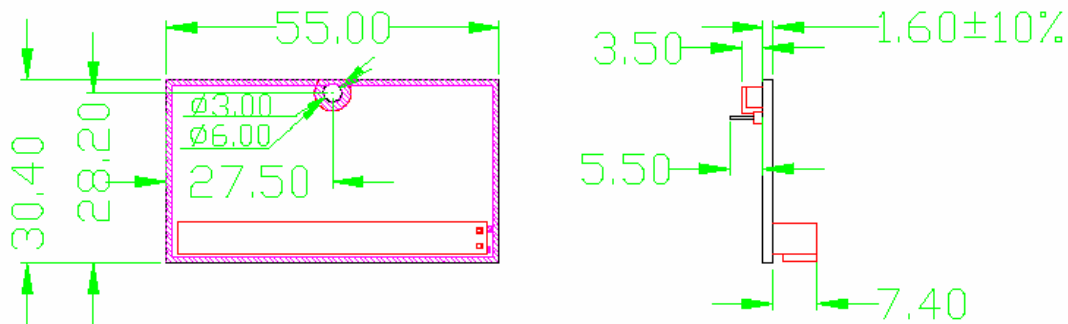


Figure 13: Mechanical Dimensions of iDiskOnChip, 40-Pin Horizontal Version

### 6.3.2 44-Pin Horizontal Version

Figure 14 shows the mechanical dimensions of left-oriented iDiskOnChip, 44-pin horizontal version.

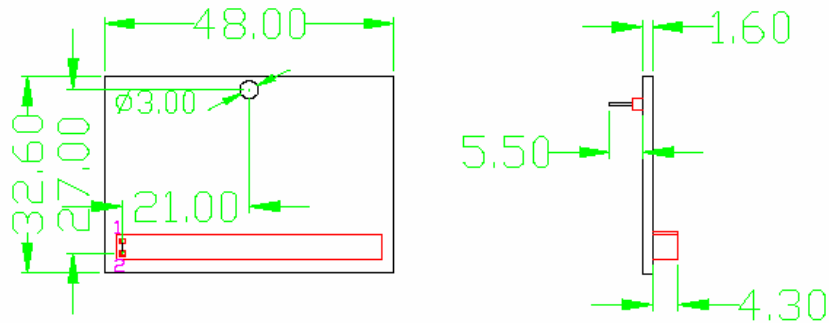


Figure 14: Mechanical Dimensions of iDiskOnChip, 44-Pin Horizontal Version

### 6.3.3 40-Pin Vertical Version

#### 6.3.3.1 With Shell

Figure 15 shows the mechanical dimensions of iDiskOnChip, 40-pin vertical version with a shell.

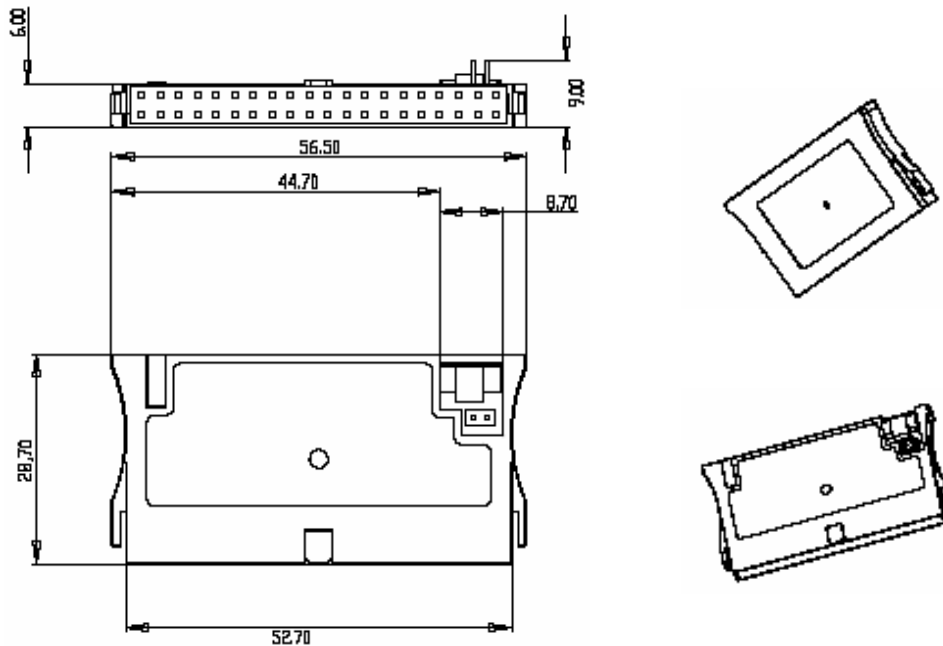


Figure 15: Dimensions of iDiskOnChip, 40-Pin Vertical Version with Shell

#### 6.3.3.2 Without Shell

Figure 16 shows the mechanical dimensions of iDiskOnChip, 40-pin vertical version without a shell.

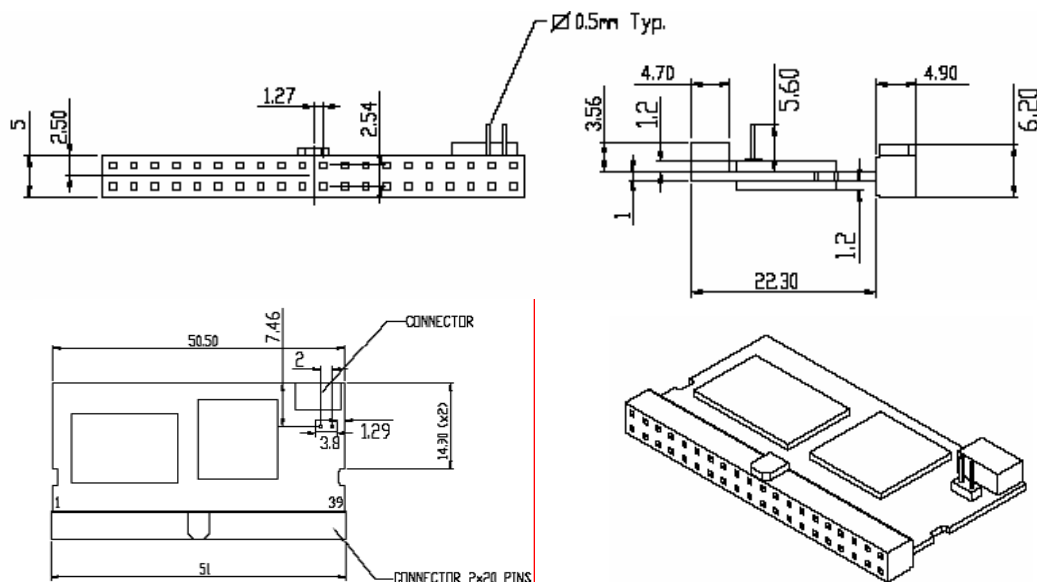


Figure 16: Dimensions of iDiskOnChip, 40-Pin Vertical Version Without Shell

### 6.3.4 44-Pin Vertical Version

#### 6.3.4.1 With Shell

Figure 17 shows the mechanical dimensions of iDiskOnChip, 44-pin vertical version with a shell.

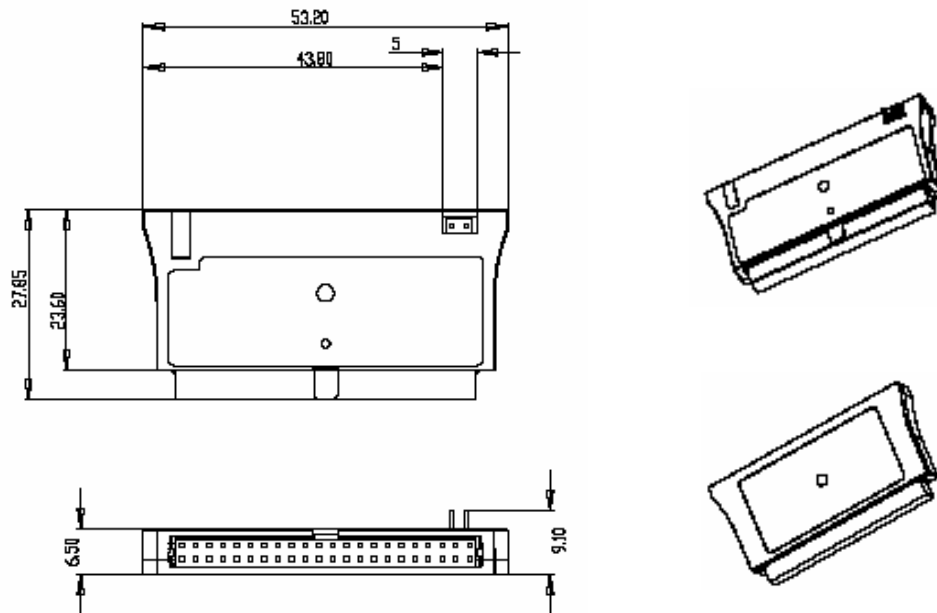


Figure 17: Dimensions of iDiskOnChip, 44-Pin Vertical Version with Shell

#### 6.3.4.2 Without Shell

Figure 18 shows the mechanical dimensions of iDiskOnChip, 44-pin vertical version without a shell.

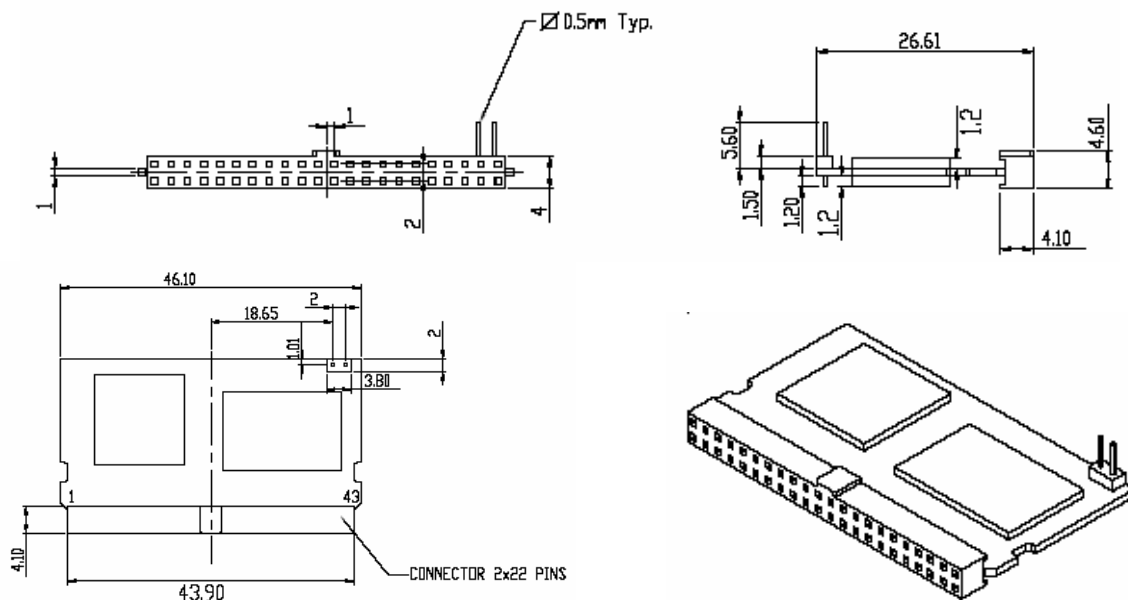


Figure 18: Dimensions of iDiskOnChip, 44-Pin Vertical Version

## 6.4 Electrical Specifications

### 6.4.1 Absolute Maximum Ratings

Table 6: iDiskOnChip Absolute Maximum Ratings

| Symbol          | Parameter             | Min  | Max  | Unit |
|-----------------|-----------------------|------|------|------|
| V <sub>IN</sub> | Input Voltage (5v)    | 4.5  | 5.5  | V    |
| V <sub>IN</sub> | Input Voltage (3.3v)  | 3.13 | 3.43 | V    |
| T <sub>a</sub>  | Operating Temperature | 0    | +70  | °C   |
| T <sub>st</sub> | Storage Temperature   | -40  | +80  | °C   |

### 6.4.2 DC Characteristics

Table 7: iDiskOnChip DC Characteristics

| Symbol           | Parameter                | Min  | Max                     | Unit |
|------------------|--------------------------|------|-------------------------|------|
| V <sub>IH</sub>  | Input High voltage       | 2.5  | V <sub>CC</sub> +0.3    | V    |
| V <sub>IL</sub>  | Input Low voltage        | -0.3 | 0.8                     | V    |
| V <sub>OH</sub>  | Output High voltage      | 2.4  | -                       | V    |
| V <sub>OL</sub>  | Output Low voltage       | -    | 0.45                    | V    |
| I <sub>CC</sub>  | Operating current        |      | 60 mA (max); 20mA (typ) | mA   |
| I <sub>CCS</sub> | Standby mode current (*) | -    | 5 mA (max)              | mA   |
| I <sub>LI</sub>  | Input leakage current    | -    | ±20                     | μA   |
| I <sub>LO</sub>  | Output leakage current   | -    | ±20                     | μA   |

T<sub>a</sub>=0°C to +70°C, V<sub>CC</sub>=5.0V ± 10

\*Measured with flash memory and host interface

### 6.4.3 AC Characteristics

Table 8: Timing Specifications, PIO Mode 4

| Symbol                  | Parameter                        | Min | Max | Unit |
|-------------------------|----------------------------------|-----|-----|------|
| t <sub>cR</sub>         | Cycle time                       | 120 |     | ns   |
| t <sub>suA</sub>        | Address setup time for IORD/IOWR | 25  |     | ns   |
| t <sub>hA</sub>         | Address hold time from IORD/IOWR | 10  |     | ns   |
| t <sub>w</sub>          | IORD/IOWR pulse width            | 70  |     | ns   |
| t <sub>rec</sub>        | IORD/IOWR recovery time          | 25  |     | ns   |
| t <sub>suD</sub> (IORD) | Data setup time for IORD         | 20  |     | ns   |
| t <sub>hD</sub> (IORD)  | Data hold following IORD         | 5   |     | ns   |
| t <sub>dis</sub> (IORD) | Output disable time from IORD    |     | 30  | ns   |
| t <sub>suD</sub> (IOWR) | Data setup time for IOWR         | 20  |     | ns   |
| t <sub>hD</sub> (IOWR)  | Data hold following IOWR         | 10  |     | ns   |

## 6.5 Supported IDE Commands

iDiskOnChip supports the commands listed in Table 9.

Table 9: IDE Commands

| Command Name                          | Command Code |
|---------------------------------------|--------------|
| CHECK POWER MODE                      | 98h E5h      |
| EXECUTE DEVICE DIAGNOSTIC             | 90h          |
| FORMAT TRACK                          | 50h          |
| IDENTIFY DEVICE                       | Ech          |
| IDLE                                  | 97h E3h      |
| IDLE IMMEDIATE                        | 95h E1h      |
| INITIALIZE DEVICE PARAMETERS          | 91h          |
| READ BUFFER                           | E4h          |
| READ DMA (with retry)                 | C8h          |
| READ DMA (without retry)              | C9h          |
| READ MULTIPLE                         | C4h          |
| READ SECTOR(S) (with retry)           | 20h          |
| READ SECTOR(S) (without retry)        | 21h          |
| READ LONG                             | 22h 23h      |
| READ VERIFY SECTOR(S) (with retry)    | 40h          |
| READ VERIFY SECTOR(S) (without retry) | 41h          |
| RECALIBRATE                           | 10h          |
| SEEK                                  | 70h          |
| SET FEATURES                          | Efh          |
| SET MULTIPLE MODE                     | C6h          |
| SLEEP                                 | 99h E6h      |
| STANDBY                               | 96h E2h      |
| STANDBY IMMEDIATE                     | 94h E0h      |
| WRITE BUFFER                          | E8h          |
| WRITE DMA (with retry)                | CAh          |
| WRITE DMA (without retry)             | CBh          |
| WRITE MULTIPLE                        | C5h          |
| WRITE SECTOR(S) (with retry)          | 30h          |
| WRITE SECTOR(S) (without retry)       | 31h          |
| WRITE LONG                            | 32h 33h      |

## 6.6 Cylinder Head Sector (CHS) Parameters

Table 10: CHS Parameters for iDiskOnChip

| iDiskOnChip Capacity (MB) | CHS Parameters |      |        |
|---------------------------|----------------|------|--------|
|                           | Cylinder       | Head | Sector |
| 16                        | 490            | 2    | 32     |
| 32                        | 500            | 8    | 16     |
| 64                        | 500            | 8    | 32     |
| 128                       | 500            | 16   | 32     |
| 192                       | 750            | 16   | 32     |
| 256                       | 1000           | 16   | 32     |
| 384                       | 745            | 16   | 63     |
| 512                       | 1015           | 16   | 63     |
| 768                       | 1522           | 16   | 63     |
| 1024                      | 2044           | 16   | 63     |
| 1536                      | 3067           | 16   | 63     |

## 7. ORDERING INFORMATION

### MD11AC-DXXXX-W-P

Where:

- MD11** M-Systems' iDiskOnChip product
- A** 5: Vertical alignment  
6: Horizontal alignment, left oriented  
7: Horizontal alignment, right oriented
- C** 0: 40-pin IDE connector  
1: 44-pin IDE connector
- W** W (vertical configuration only): Without shell  
Blank (vertical configuration only): With shell
- P** P: RoHS-compliant version  
Blank: Non-ROHS-compliant version

**DXXXX** Capacity (MB): 16, 32, 64, 128, 192, 256, 384, 512, 768, 1024, 1536

Refer to Table 11 for the combinations currently available and the associated ordering information.

*Table 11: Available Combinations*

| Capacity (MB) | IDE Connector | Alignment                | Ordering Code  |
|---------------|---------------|--------------------------|----------------|
| 16            | 40-pin        | Vertical                 | MD1150-D16-P   |
|               |               | Vertical (without shell) | MD1150-D16-W-P |
|               |               | Horizontal (left)        | MD1160-D16-P   |
|               |               | Horizontal (right)       | MD1170-D16-P   |
|               | 44-pin        | Vertical                 | MD1151-D16-P   |
|               |               | Vertical (without shell) | MD1151-D16-W-P |
|               |               | Horizontal (left)        | MD1161-D16-P   |
|               |               | Horizontal (right)       | MD1171-D16-P   |
| 32            | 40-pin        | Vertical                 | MD1150-D32-P   |
|               |               | Vertical (without shell) | MD1150-D32-W-P |
|               |               | Horizontal (left)        | MD1160-D32-P   |
|               |               | Horizontal (right)       | MD1170-D32-P   |
|               | 44-pin        | Vertical                 | MD1151-D32-P   |
|               |               | Vertical (without shell) | MD1151-D32-W-P |
|               |               | Horizontal (left)        | MD1161-D32-P   |
|               |               | Horizontal (right)       | MD1171-D32-P   |

| Capacity (MB) | IDE Connector | Alignment                | Ordering Code   |
|---------------|---------------|--------------------------|-----------------|
| 64            | 40-pin        | Vertical                 | MD1150-D64-P    |
|               |               | Vertical (without shell) | MD1150-D64-W-P  |
|               |               | Horizontal (left)        | MD1160-D64-P    |
|               |               | Horizontal (right)       | MD1170-D64-P    |
|               | 44-pin        | Vertical                 | MD1151-D64-P    |
|               |               | Vertical (without shell) | MD1151-D64-W-P  |
|               |               | Horizontal (left)        | MD1161-D64-P    |
|               |               | Horizontal (right)       | MD1171-D64-P    |
| 128           | 40-pin        | Vertical                 | MD1150-D128-P   |
|               |               | Vertical (without shell) | MD1150-D128-W-P |
|               |               | Horizontal (left)        | MD1160-D128-P   |
|               |               | Horizontal (right)       | MD1170-D128-P   |
|               | 44-pin        | Vertical                 | MD1151-D128-P   |
|               |               | Vertical (without shell) | MD1151-D128-W-P |
|               |               | Horizontal (left)        | MD1161-D128-P   |
|               |               | Horizontal (right)       | MD1171-D128-P   |
| 192           | 40-pin        | Vertical                 | MD1150-D192-P   |
|               |               | Vertical (without shell) | MD1150-D192-W-P |
|               |               | Horizontal (left)        | MD1160-D192-P   |
|               |               | Horizontal (right)       | MD1170-D192-P   |
|               | 44-pin        | Vertical                 | MD1151-D192-P   |
|               |               | Vertical (without shell) | MD1151-D192-W-P |
|               |               | Horizontal (left)        | MD1161-D192-P   |
|               |               | Horizontal (right)       | MD1171-D192-P   |
| 256           | 40-pin        | Vertical                 | MD1150-D256-P   |
|               |               | Vertical (without shell) | MD1150-D256-W-P |
|               |               | Horizontal (left)        | MD1160-D256-P   |
|               |               | Horizontal (right)       | MD1170-D256-P   |
|               | 44-pin        | Vertical                 | MD1151-D256-P   |
|               |               | Vertical (without shell) | MD1151-D256-W-P |
|               |               | Horizontal (left)        | MD1161-D256-P   |
|               |               | Horizontal (right)       | MD1171-D256-P   |



| Capacity (MB) | IDE Connector | Alignment                | Ordering Code    |
|---------------|---------------|--------------------------|------------------|
| 384           | 40-pin        | Vertical                 | MD1150-D384-P    |
|               |               | Vertical (without shell) | MD1150-D384-W-P  |
|               |               | Horizontal (left)        | MD1160-D384-P    |
|               |               | Horizontal (right)       | MD1170-D384-P    |
|               | 44-pin        | Vertical                 | MD1151-D384-P    |
|               |               | Vertical (without shell) | MD1151-D384-W-P  |
|               |               | Horizontal (left)        | MD1161-D384-P    |
|               |               | Horizontal (right)       | MD1171-D384-P    |
| 512           | 40-pin        | Vertical                 | MD1150-D512-P    |
|               |               | Vertical (without shell) | MD1150-D512-W-P  |
|               |               | Horizontal (left)        | MD1160-D512-P    |
|               |               | Horizontal (right)       | MD1170-D512-P    |
|               | 44-pin        | Vertical                 | MD1151-D512-P    |
|               |               | Vertical (without shell) | MD1151-D512-W-P  |
|               |               | Horizontal (left)        | MD1161-D512-P    |
|               |               | Horizontal (right)       | MD1171-D512-P    |
| 768           | 40-pin        | Vertical                 | MD1150-D768-P    |
|               |               | Vertical (without shell) | MD1150-D768-W-P  |
|               |               | Horizontal (left)        | MD1160-D768-P    |
|               |               | Horizontal (right)       | MD1170-D768-P    |
|               | 44-pin        | Vertical                 | MD1151-D768-P    |
|               |               | Vertical (without shell) | MD1151-D768-W-P  |
|               |               | Horizontal (left)        | MD1161-D768-P    |
|               |               | Horizontal (right)       | MD1171-D768-P    |
| 1024          | 40-pin        | Vertical                 | MD1150-D1024-P   |
|               |               | Vertical (without shell) | MD1150-D1024-W-P |
|               |               | Horizontal (left)        | MD1160-D1024-P   |
|               |               | Horizontal (right)       | MD1170-D1024-P   |
|               | 44-pin        | Vertical                 | MD1151-D1024-P   |
|               |               | Vertical (without shell) | MD1151-D1024-W-P |
|               |               | Horizontal (left)        | MD1161-D1024-P   |
|               |               | Horizontal (right)       | MD1171-D1024-P   |

| Capacity (MB) | IDE Connector | Alignment                | Ordering Code    |
|---------------|---------------|--------------------------|------------------|
| 1536          | 40-pin        | Vertical                 | MD1150-D1536-P   |
|               |               | Vertical (without shell) | MD1150-D1536-W-P |
|               |               | Horizontal (left)        | MD1160-D1536-P   |
|               |               | Horizontal (right)       | MD1170-D1536-P   |
|               | 44-pin        | Vertical                 | MD1151-D1536-P   |
|               |               | Vertical (without shell) | MD1151-D1536-W-P |
|               |               | Horizontal (left)        | MD1161-D1536-P   |
|               |               | Horizontal (right)       | MD1171-D1536-P   |

Note: The 40-pin iDiskOnChip requires an additional cable for the power supply. The ordering information is: DOC-IDE40-CABLE

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