Switch-mode Series NPN Silicon Power Transistor

BUV22

This device is designed for high speed, high current, high power applications.

Features

- High DC Current Gain:
  h_{FE} min = 20 at I_C = 10 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$
  max = 1.0 V at I_C = 10 A
- Very Fast Switching Times:
  TF max = 0.35 μs at I_C = 20 A
- Pb−Free Package is Available*

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{CEO(SUS)}$	Collector−Emitter Voltage	250	Vdc
V_{CBO}	Collector−Base Voltage	300	Vdc
V_{EBO}	Emitter−Base Voltage	7	Vdc
V_{CEX}	Collector−Emitter Voltage (V_{BE} = −1.5 V)	300	Vdc
V_{CER}	Collector−Emitter Voltage (R_{BE} = 100 Ω)	290	Vdc
I_C I_{CM}	Collector−Current − Continuous − Peak (PW ≤ 10 ms)	40 50	Adc Apk
I_B	Base−Current Continuous	8	Adc
P_D	Total Device Dissipation @ T_C = 25°C	250	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−65 to 200	°C

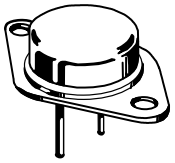
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristics	Max	Unit
θ_{JC}	Thermal Resistance, Junction−to−Case	0.7	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

40 AMPERES
NPN SILICON POWER
METAL TRANSISTOR
250 VOLTS − 250 WATTS



TO−204AE (TO−3)
CASE 197A

MARKING DIAGRAM

BUV22 = Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
BUV22G	TO−204 (Pb−Free)	100 Units / Tray

DISCONTINUED (Note 1)

BUV22	TO−204	100 Units / Tray

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
OFF CHARACTERISTICS (Note 2)				
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	250	–	Vdc
I_{CEX}	Collector Cutoff Current at Reverse Bias (V_{CE} = 300 V, V_{BE} = −1.5 V) (V_{CE} = 300 V, V_{BE} = −1.5 V, T_C = 125°C)		3.0 12.0	mAdc
I_{CEO}	Collector−Emitter Cutoff Current (V_{CE} = 200 V)	–	3.0	mAdc
V_{EBO}	Emitter−Base Reverse Voltage (I_E = 50 mA)	7	–	V
I_{EBO}	Emitter−Cutoff Current (V_{EB} = 5 V)	–	1.0	mAdc
SECOND BREAKDOWN				
$I_{S/b}$	Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	12 0.15		Adc
ON CHARACTERISTICS (Note 2)				
h_{FE}	DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)	20 10	60	
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 20 A, I_B = 2.5 A)		1.0 1.5	Vdc
$V_{BE(sat)}$	Base−Emitter Saturation Voltage (I_C = 40 A, I_B = 4 A)		1.5	Vdc
DYNAMIC CHARACTERISTICS				
f_T	Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
t_{on}	Turn−on Time	(I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CC} = 100 V, R_C = 5 Ω)		0.8	μs
t_s	Storage Time			2.0	
t_f	Fall Time			0.35	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

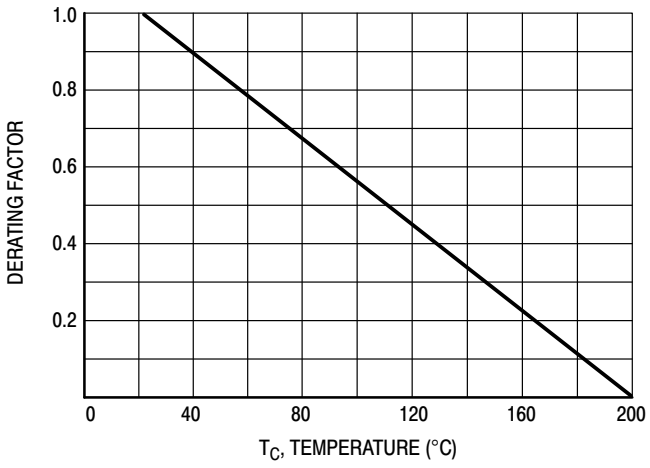


Figure 1. Power Derating

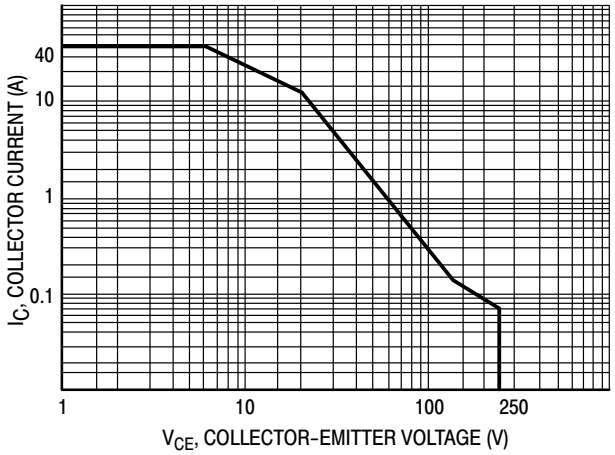


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

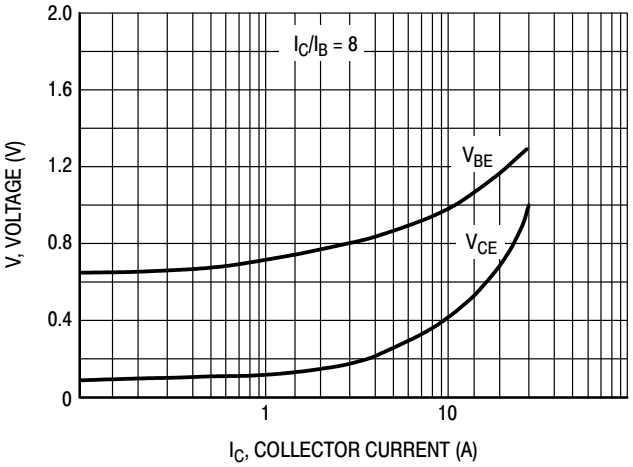


Figure 3. “On” Voltages

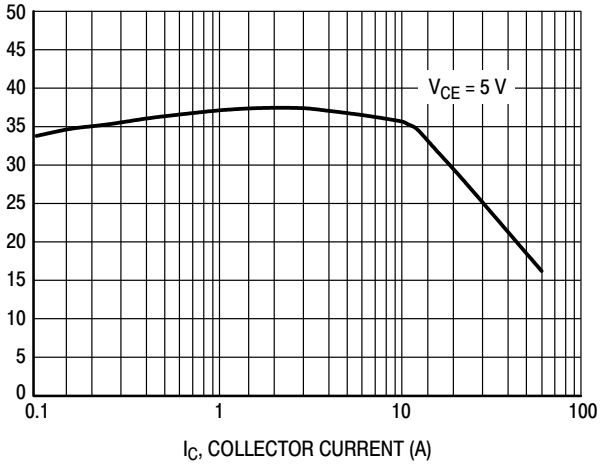


Figure 4. DC Current Gain

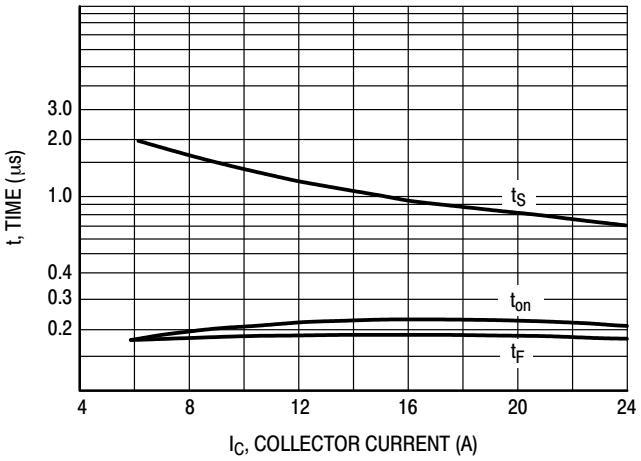


Figure 5. Resistive Switching Performance

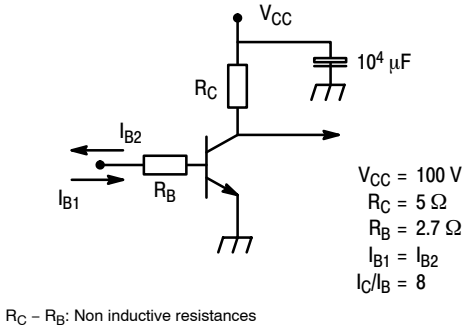
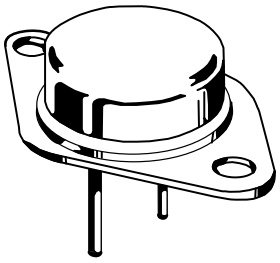


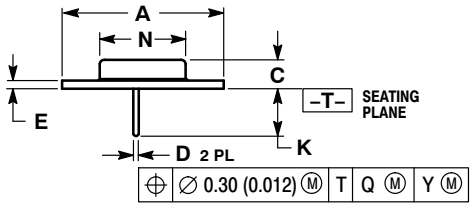
Figure 6. Switching Times Test Circuit

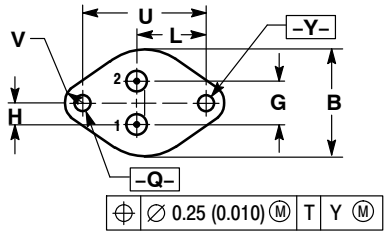


SCALE 1:1

TO−204 (TO−3)
CASE 197A−05
ISSUE K

DATE 21 FEB 2000





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

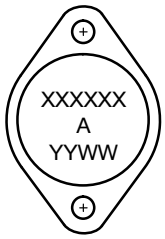
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. ANODE = 1
2. ANODE = 2
CASE: CATHODES

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Locationa
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42129B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−204 (TO−3)**	**PAGE 1 OF 1**

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