

# MMDF2C02E

## Power MOSFET 2.5 Amps, 25 Volts Complementary SO-8, Dual

These miniature surface mount MOSFETs feature ultra low  $R_{DS(on)}$  and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low  $R_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	25	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current – Continuous	N-Channel P-Channel	$I_D$	3.6
			2.5
	N-Channel P-Channel	$I_{DM}$	18
			13
– Pulsed	N-Channel		
	P-Channel		
Operating and Storage Temperature Range	$T_J$ and $T_{stg}$	– 55 to 150	$^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	2.0	Watts
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 20\text{ V}$ , $V_{GS} = 10\text{ V}$ , Peak $I_L = 9.0\text{ A}$ , $L = 6.0\text{ mH}$ , $R_G = 25\ \Omega$ )	N-Channel		
			245
	P-Channel		
			245
Thermal Resistance – Junction to Ambient (Note 2)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering, 0.0625" from case. Time in Solder Bath is 10 seconds.	$T_L$	260	$^\circ\text{C}$

1. Negative signs for P-Channel device omitted for clarity.
2. Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

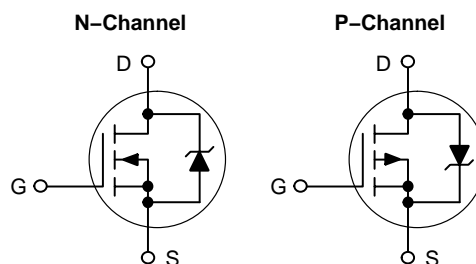


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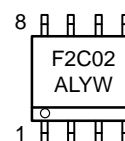
### 2.5 AMPERES 25 VOLTS

$R_{DS(on)} = 100\text{ m}\Omega$  (N-Channel)  
 $R_{DS(on)} = 250\text{ m}\Omega$  (P-Channel)



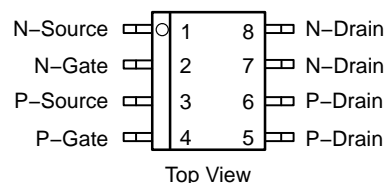
**SO-8  
CASE 751  
STYLE 14**

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

### PIN ASSIGNMENT



Top View

### ORDERING INFORMATION

Device	Package	Shipping†
MMDF2C02ER2	SO-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MMDF2C02E

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 3)

Characteristic	Symbol	Polarity	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain–Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\text{ }\mu\text{Adc}$ )	$V_{(BR)DSS}$	–	25	–	–	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	(N) (P)	– –	– –	1.0 1.0	$\mu\text{Adc}$
Gate–Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0$ )	$I_{GSS}$	–	–	–	100	nAdc

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{Adc}$ )	$V_{GS(th)}$	–	1.0	2.0	3.0	Vdc
Drain–to–Source On–Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.2\text{ Adc}$ ) ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ )	$R_{DS(on)}$	(N) (P)	– –	– –	0.100 0.250	Ohm
Drain–to–Source On–Resistance ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ ) ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ )	$R_{DS(on)}$	(N) (P)	– –	– –	0.200 0.400	Ohm
On–State Drain Current ( $V_{DS} = 5.0\text{ Vdc}$ , $V_{GS} = 4.5\text{ Vdc}$ )	$I_{D(on)}$	(N) (P)	2.0 2.0	– –	– –	Adc
Forward Transconductance ( $V_{DS} = 3.0\text{ Vdc}$ , $I_D = 1.5\text{ Adc}$ ) ( $V_{DS} = 3.0\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ )	$g_{FS}$	(N) (P)	1.0 1.0	2.6 2.8	– –	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	(N) (P)	– –	380 340	532 475	pF
Output Capacitance		$C_{oss}$	(N) (P)	– –	235 220	329 300	
Transfer Capacitance		$C_{rss}$	(N) (P)	– –	55 75	110 150	

### SWITCHING CHARACTERISTICS (Note 5)

Turn–On Delay Time	$(V_{DD} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $R_G = 9.1\text{ }\Omega$ )	$t_{d(on)}$	(N) (P)	– –	10 20	30 40	ns
Rise Time		$t_r$	(N) (P)	– –	35 40	70 80	
Turn–Off Delay Time	$(V_{DD} = 10\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ , $V_{GS} = 5.0\text{ Vdc}$ , $R_G = 25\text{ }\Omega$ )	$t_{d(off)}$	(N) (P)	– –	19 53	38 106	
Fall Time		$t_f$	(N) (P)	– –	25 41	50 82	
Turn–On Delay Time	$(V_{DD} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ , $V_{GS} = 10\text{ Vdc}$ , $R_G = 6.0\text{ }\Omega$ )	$t_{d(on)}$	(N) (P)	– –	7.0 13	21 26	
Rise Time		$t_r$	(N) (P)	– –	17 29	30 58	
Turn–Off Delay Time	$(V_{DD} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ , $V_{GS} = 10\text{ Vdc}$ , $R_G = 6.0\text{ }\Omega$ )	$t_{d(off)}$	(N) (P)	– –	27 30	48 60	
Fall Time		$t_f$	(N) (P)	– –	18 28	30 56	

3. Negative signs for P–Channel device omitted for clarity.

4. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperature.

# MMDF2C02E

## ELECTRICAL CHARACTERISTICS – continued ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 6)

Characteristic	Symbol	Polarity	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS – continued (Note 8)

Total Gate Charge	(V <sub>DS</sub> = 16 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	(N) (P)	– –	10.6 10	30 15	nC
Gate–Source Charge		Q <sub>1</sub>	(N) (P)	– –	1.3 1.0	– –	
Gate–Drain Charge		Q <sub>2</sub>	(N) (P)	– –	2.9 3.5	– –	
		Q <sub>3</sub>	(N) (P)	– –	2.7 3.0	– –	

### SOURCE–DRAIN DIODE CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ )

Forward Voltage (Note 7)	$(I_S = 2.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = 2.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$	$V_{SD}$	(N) (P)	– –	1.0 1.5	1.4 2.0	Vdc
Reverse Recovery Time see Figure 7	$(I_F = I_S,$ $dI_S/dt = 100 \text{ A}/\mu\text{s})$	$t_{rr}$	(N) (P)	– –	34 32	66 64	ns
		$t_a$	(N) (P)	– –	17 19	– –	
		$t_b$	(N) (P)	– –	17 12	– –	
		$Q_{RR}$	(N) (P)	– –	0.025 0.035	– –	$\mu\text{C}$

6. Negative signs for P–Channel device omitted for clarity.

7. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

8. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

TYPICAL ELECTRICAL CHARACTERISTICS

N-Channel

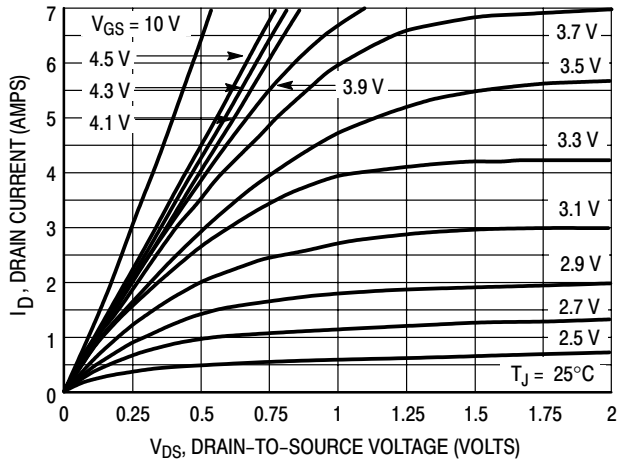


Figure 1. On-Region Characteristics

P-Channel

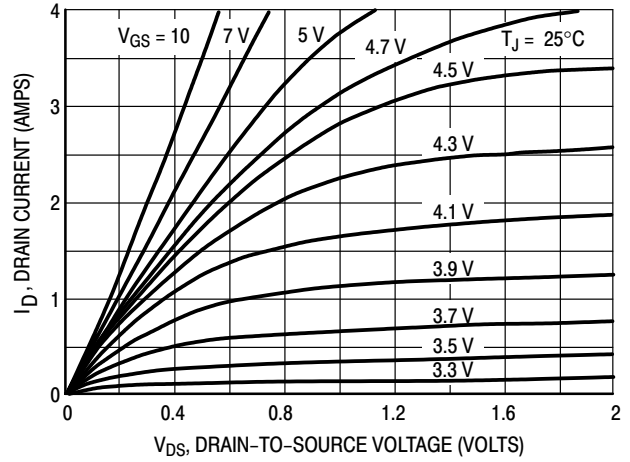


Figure 1. On-Region Characteristics

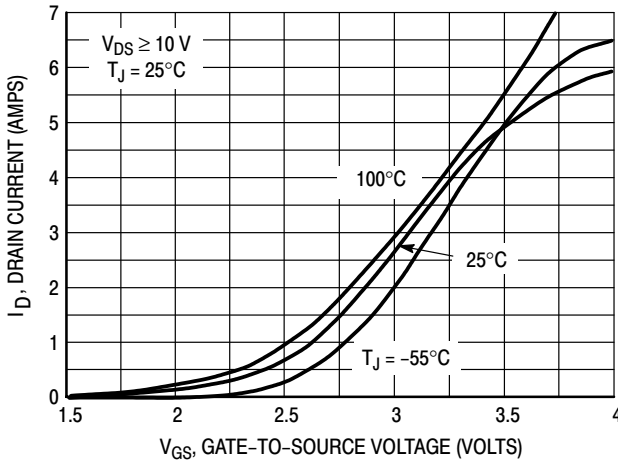


Figure 2. Transfer Characteristics

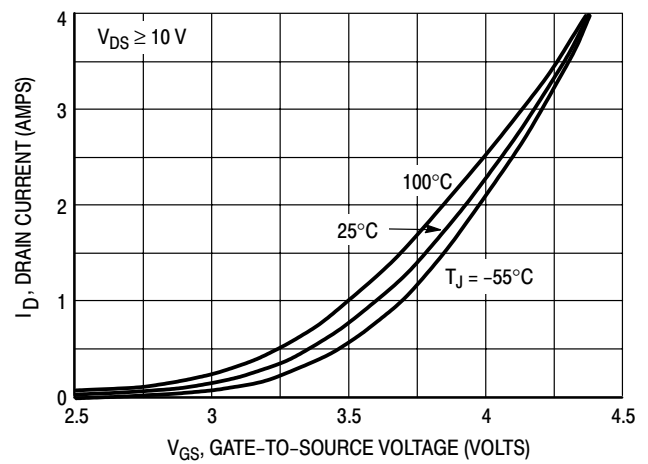


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N-Channel

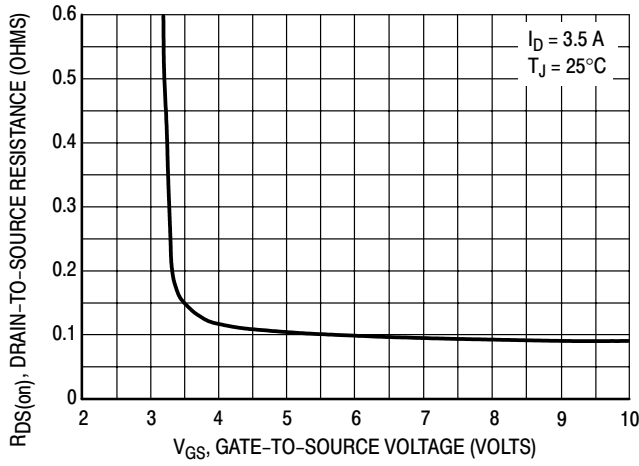


Figure 3. On-Resistance versus Gate-to-Source Voltage

P-Channel

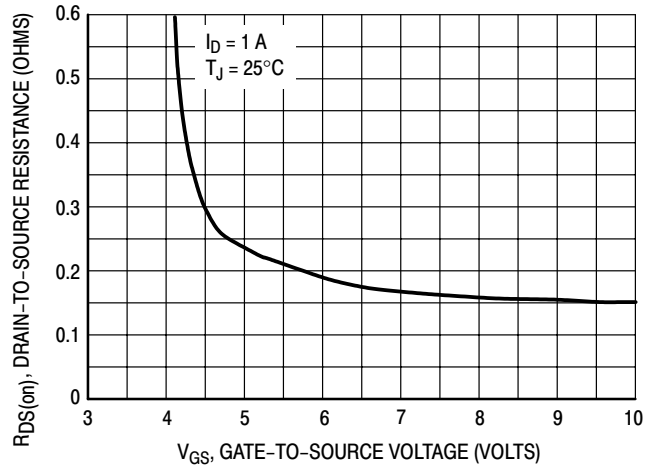


Figure 3. On-Resistance versus Gate-to-Source Voltage

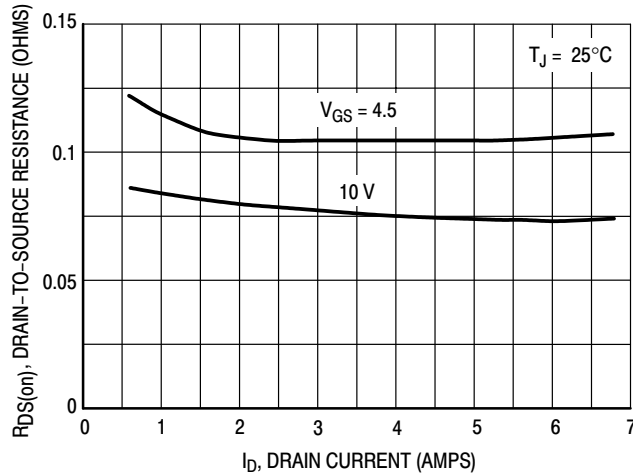


Figure 4. On-Resistance versus Drain Current and Gate Voltage

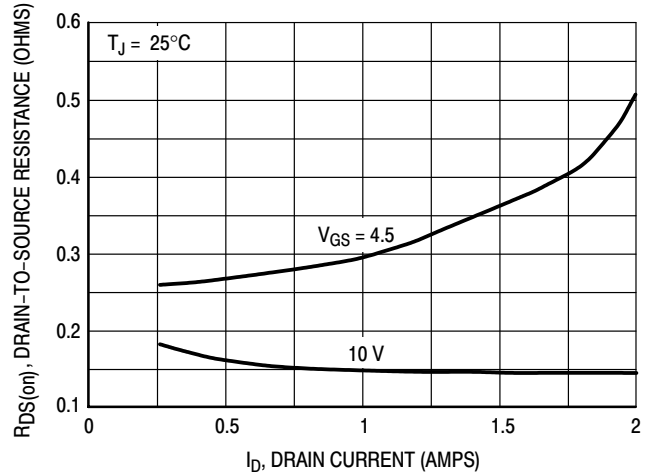


Figure 4. On-Resistance versus Drain Current and Gate Voltage

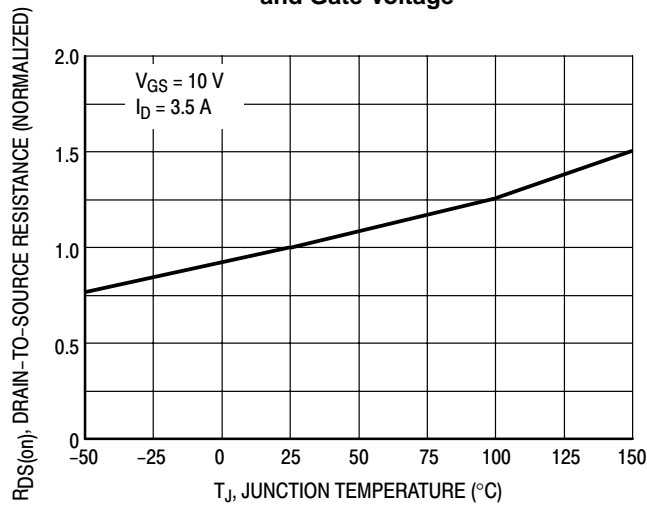


Figure 5. On-Resistance Variation with Temperature

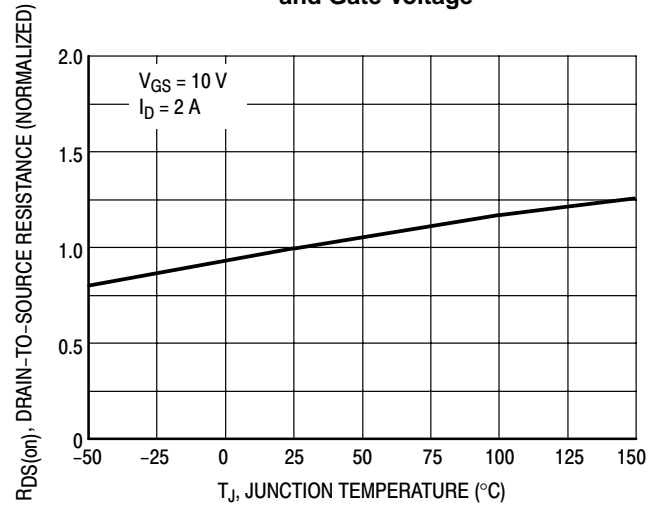


Figure 5. On-Resistance Variation with Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

N-Channel

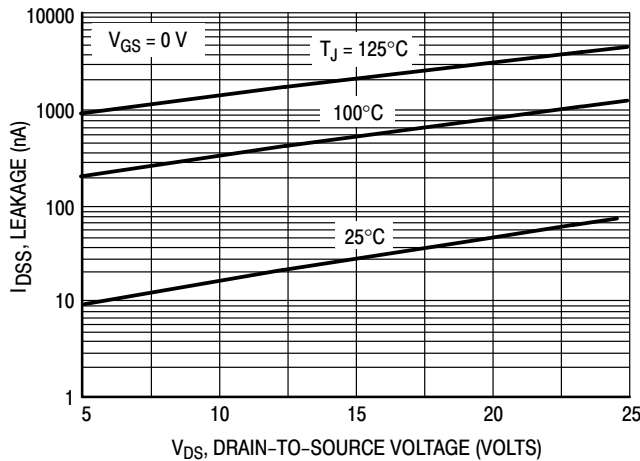


Figure 6. Drain-to-Source Leakage Current versus Voltage

P-Channel

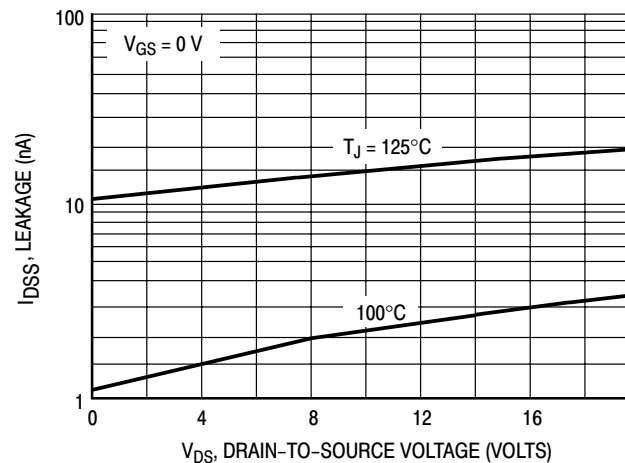


Figure 6. Drain-to-Source Leakage Current versus Voltage

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{SGP}$  are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{SGP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on-state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time,  $t_{rr}$ , due to the storage of minority carrier charge,  $Q_{RR}$ , as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short  $t_{rr}$  and low  $Q_{RR}$  specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by

high  $di/dt$ s. The diode's negative  $di/dt$  during  $t_a$  is directly controlled by the device clearing the stored charge. However, the positive  $di/dt$  during  $t_b$  is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of  $t_b/t_a$  serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter  $t_{rr}$ ), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher  $di/dt$  than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

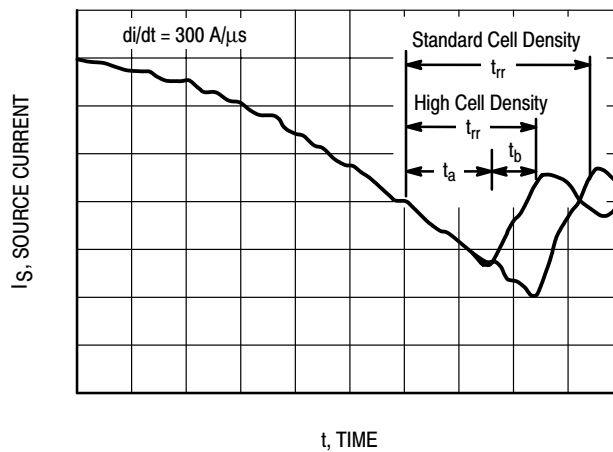


Figure 7. Reverse Recovery Time ( $t_{rr}$ )

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded, and that the transition time ( $t_r$ ,  $t_f$ ) does not exceed 10  $\mu$ s. In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

A power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

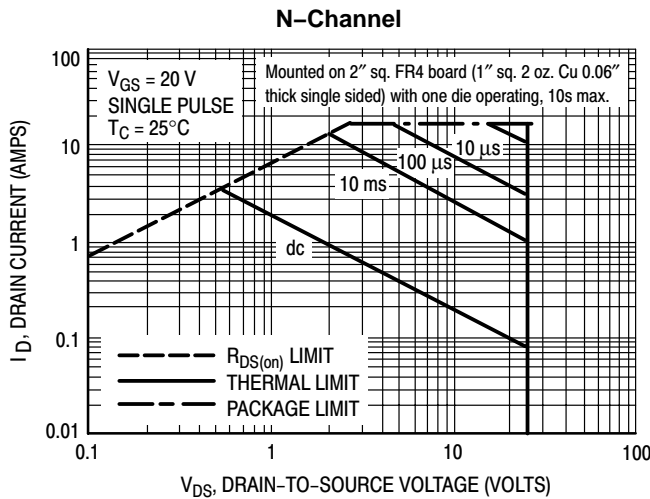


Figure 8. Maximum Rated Forward Biased Safe Operating Area

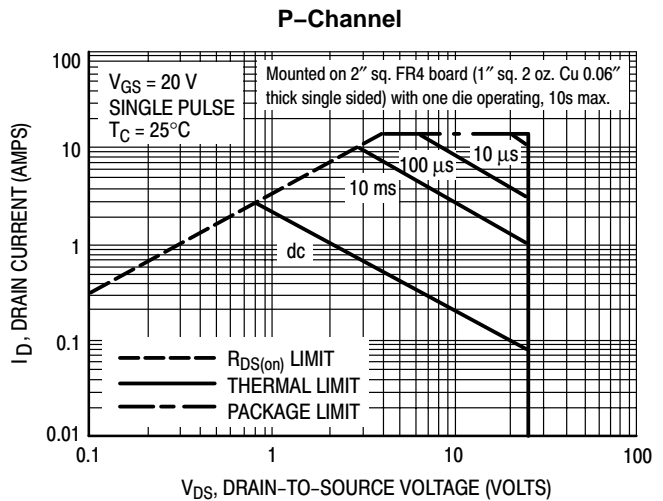


Figure 8. Maximum Rated Forward Biased Safe Operating Area

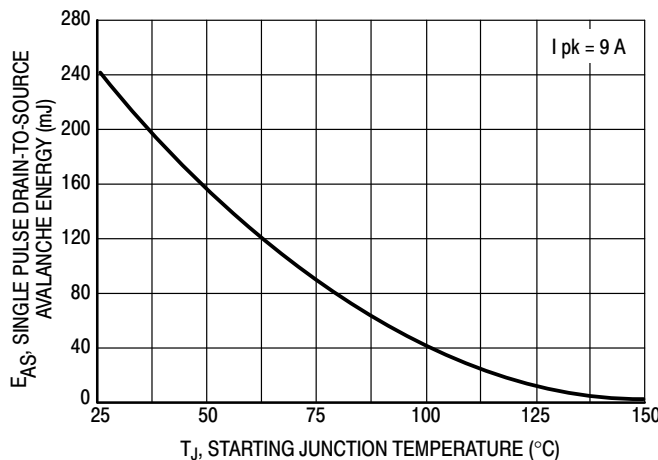


Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature

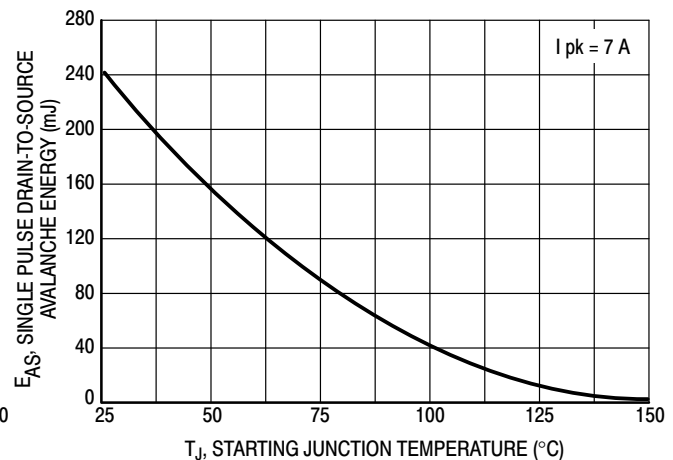


Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature



# MMDF2C02E

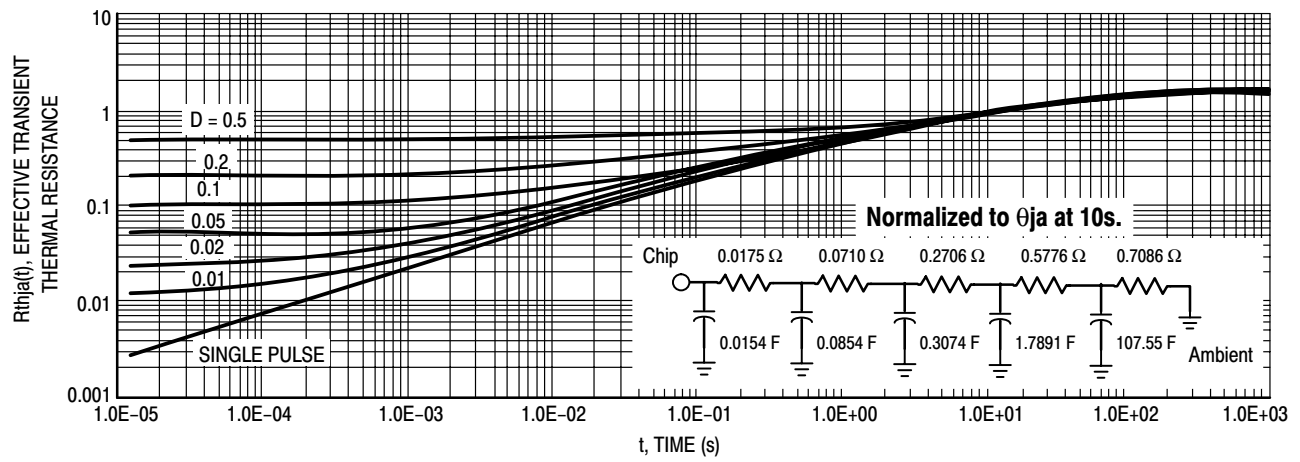


Figure 10. Thermal Response

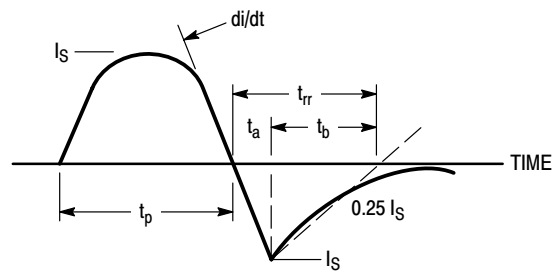
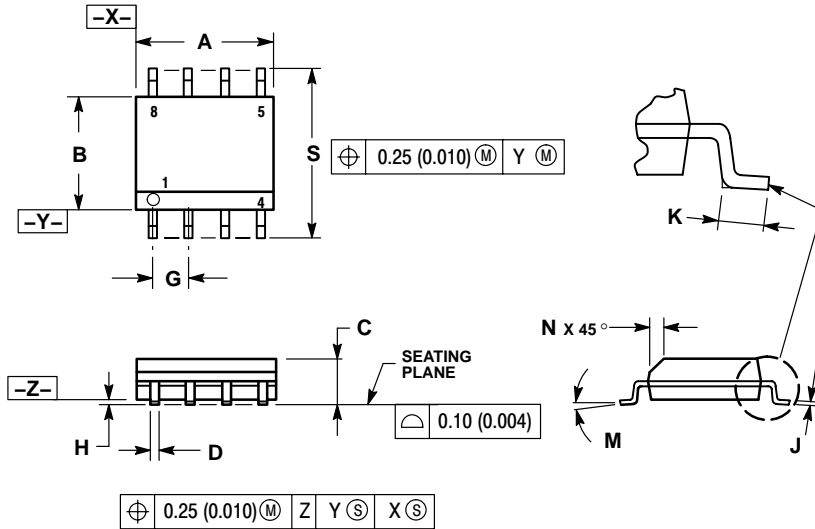


Figure 11. Diode Reverse Recovery Waveform

# M MDF2C02E

## PACKAGE DIMENSIONS

SO-8  
CASE 751-07  
ISSUE AB



### NOTES:

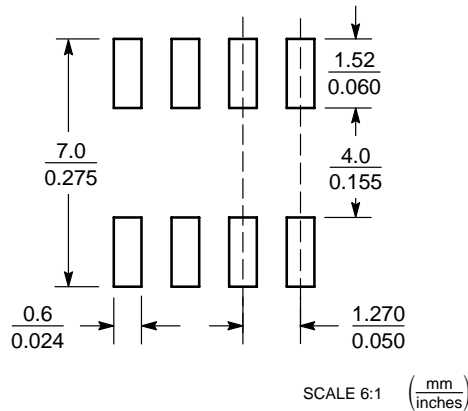
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27	BSC	0.050	BSC
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 14:

- PIN 1: N-SOURCE  
2: N-GATE  
3: P-SOURCE  
4: P-GATE  
5: P-DRAIN  
6: P-DRAIN  
7: N-DRAIN  
8: N-DRAIN

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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