Quad Supply and Line Monitor

FEATURES

- **Inputs for Monitoring up to Four Separate Supply Voltage Levels**
- **Internal Inverter for Sensing a Negative Supply Voltage**
- **Line/Switch Sense Input for Early Power Source Failure Warning**
- **Programmable Under- and Over-Voltage Fault Thresholds with Proportional Hysteresis**
- **A Precision 2.5-V Reference**
- **General Purpose Op-Amp for Auxiliary Use**
- **Three High Current, >3 0mA, Open-Collector Outputs Indicate Over-Voltage, Under-Voltage and Power OK Conditions**
- **8-V to 40-V Supply Operation with 7-mA Stand-By Current**

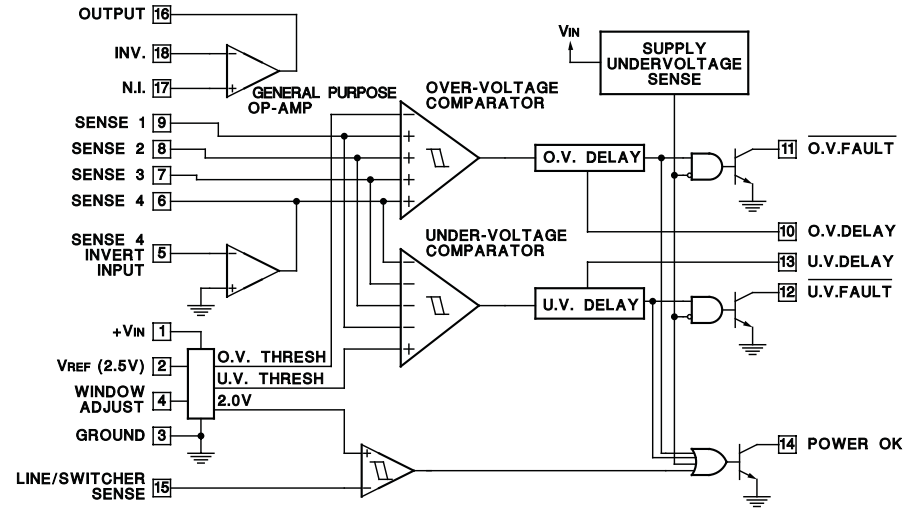
DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5-V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices sink in excess of 30 mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and DW packages.

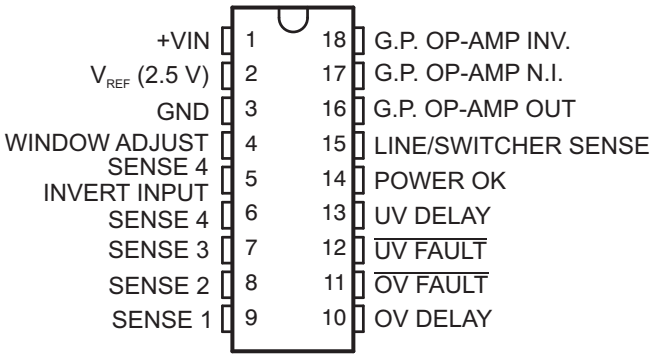
DESCRIPTION (CONT.)

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20 mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5-V output is used as a system reference.

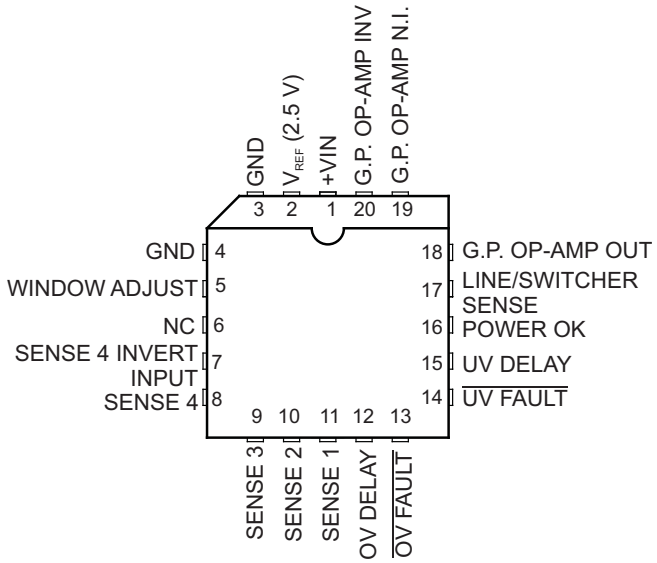
These parts operate over an 8-V to 40-V input supply range and require a typical stand-by current of only 7 mA.

CONNECTION DIAGRAMS

DIL-18, SOIC-18
J or N, DW PACKAGE
(TOP VIEW)



PLCC-20, LCC-20
Q, L PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
+VIN	Supply Voltage	+40	V
	Open Collector Output Voltages.	+40	V
	Open Collector Output Currents.	50	mA
	Sense 1-4 Input Voltages	–0.3 to +20	V
	Line/Switcher Sense Input Voltage	–0.3 to +40	V
	Op-Amp and Inverter Input Voltages	–0.3 to +40	V
	Op-Amp and Inverter Output Currents .	–40	mA
	Window Adjust Voltage.	0.0 to +10	V
	Delay Pin Voltages	0.0 to +5	V
	Reference Output Current	–40	mA
	Power Dissipation at T_A = 25°C(1)	1000	mW
	Power Dissipation at T_C = 25°C(1)	2000	mW
	Operating Junction Temperature	–55 to +150	°C
	Storage Temperature	–65 to +150	C
	Lead Temperature (Soldering, 10 Seconds)	300	°C

(1) Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; V_{PIN} 4 = 1.0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY								
Input Supply Current	No Faults		7	9		7	11	mA
	UV, OV and Line Fault		10	15		10	18	mA
Supply Under Voltage Threshold (V_{SUV})	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output			3.0	4.0		3.0	4.0	V
REFERENCE								
Output Voltage (V_{REF})	T_J = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465		2.535	2.465		2.535	V
Load Regulation	IL = 0 to 10mA		1	10		1	15	mV
Line Regulation	$+V_{IN}$ = 8 to 40V		1	4		1	8	mV
Short Circuit Current	TJ = 25°C		40			40		mA
FAULT THRESHOLDS(1)								
OV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN} 4 Input = Low to High, 0.5V ≤ V_{PIN} 4 ≤ 2.5V	0.230	0.25	0.270	0.230	0.25	0.270	V/V
UV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN} 4 Input = High to Low, 0.5V ≤ V_{PIN} 4 ≤ 2.5V	–0.270	–0.25	–0.230	–0.270	–0.25	–0.270	V/V
OV & UV Threshold Hyst.	0.5V ≤ V_{PIN} 4 ≤ 2.5V	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = 8V to 40V		0.002	0.01		0.002	0.02	%/V
Adjust Pin (Pin 4) Input Bias Current	0.5V ≤ VP_{IN} 4 ≤ 2.5V		±1	±10		±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV
SENSE INPUTS								
Sense 1-4 Input Bias Current	Input = 2.8V(2)		1	3		1	6	µA
	Input = 2.2(2)		–1	–3		–1	-6	µA
Line Sense Input Bias Current	Input = 2.3V(2)		1	3		1	6	µA
OV AND UV FAULT DELAY								
Charging Current			60			60		µA
Threshold Voltage	Delay Pin = Low to High		1.8			1.8		V
Threshold Hysteresis	T_J = 25°C		250			250		mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/µF

(1) Reference to pin numbers in this specification pertain to 18 pin DIL N and J packages and 18 pin SOIC DW package.
(2) These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

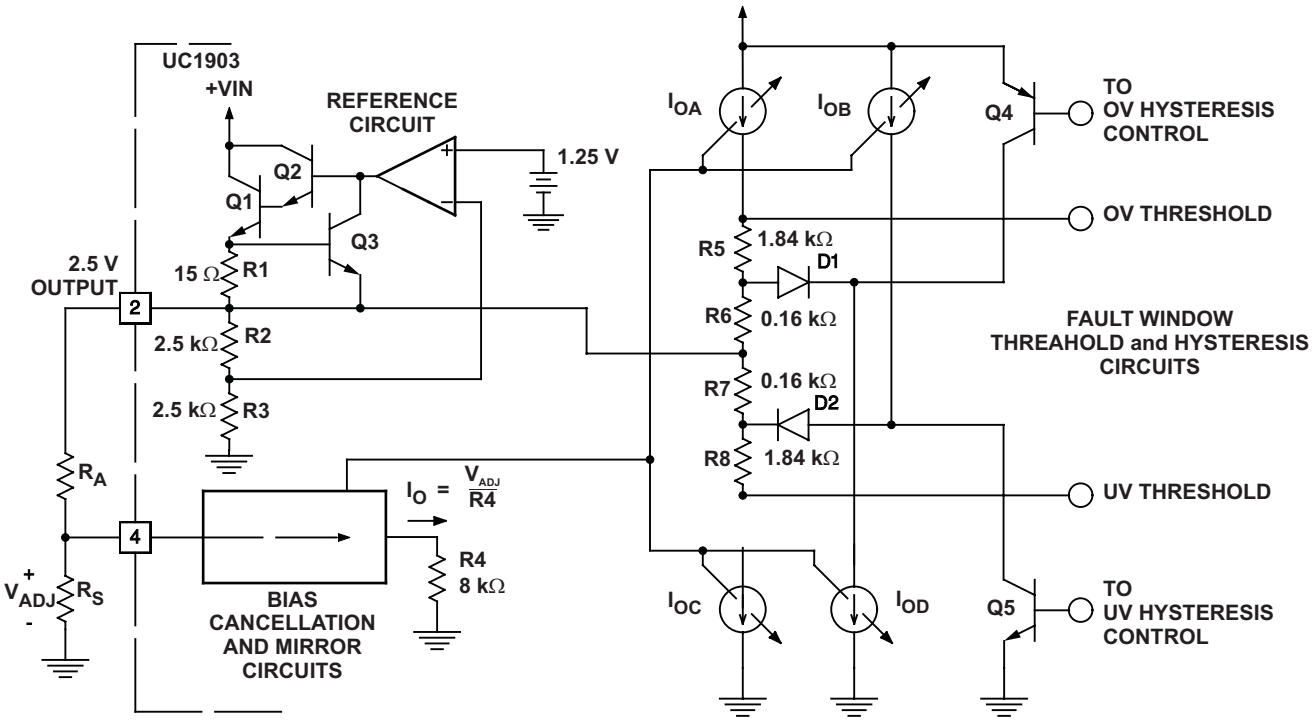
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; V_{PIN} 4 = 1.0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
FAULT OUTPUTS ($\overline{OV}$, $\overline{UV}$, AND POWER 0K)								
Maximum Current	V_{OUT} = 2V	30	70		30	70		mA
Saturation Voltage	I_{OUT} = 12mA		0.25	0.40		0.25	0.40	V
Leakage Current	V_{OUT} = 40 V		3	25		3	25	µA
SENSE 4 INVERTER(3)								
Input Offset Voltage			2	8		2	10	mV
Input Bias Current			0.1	2		0.1	4	µA
Open Loop Gain		65	80		65	80		dB
PSRR	+VIN = 8 to 40 V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			0.4			0.4		V/µs
Short Circuit Current	T_J = 2°C		40			40		mA
G.P. OP-AMP(3)								
Input Offset Voltage			1	5		1	8	mV
Input Bias Voltage			0.1	2		0.1	4	µA
Input Offset Current			0.01	.5		0.01	1.0	µA
Open Loop Gain		65	120		65	120		dB
CMRR	V_{CM} = 0 to $+V_{IN}$ = 2.0V	65	100		65	100		dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			0.4			0.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA

(3) When either the G.P. OP-Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.

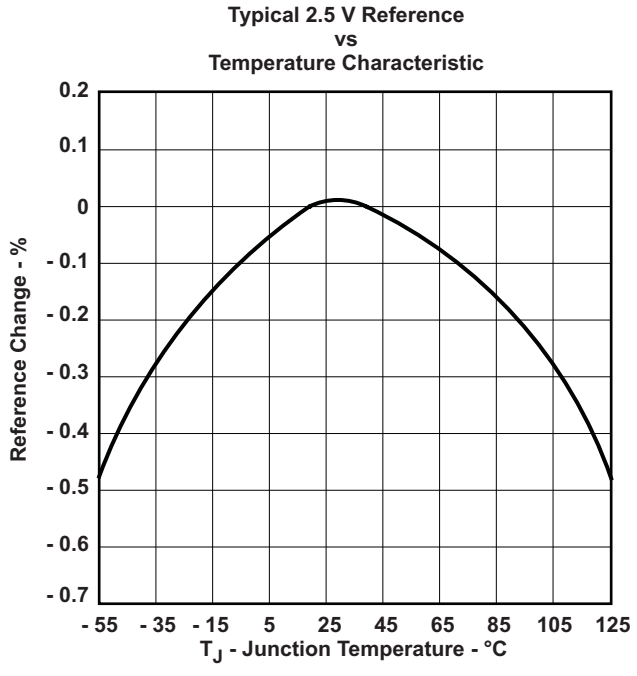
Block Diagram

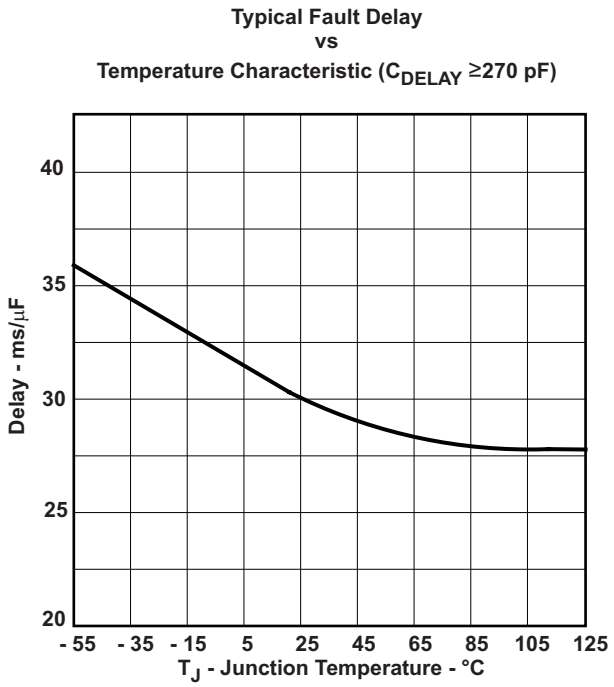


A. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5-V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

Figure 1. Operation and Application Information

Typical Characteristics





OPERATION AND APPLICATION INFORMATION

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5-V reference. The resulting fault window is centered around 2.5 V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 along with the Typical Characteristics diagrams. The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R4, and an 8-kΩ resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q4 and Q5 are turned on. In combination with D1 and D2 this prevents L_{OB} and L_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R5 + R6)$ and $V_{REF} – I_{OC}(R7 + R8)$ respectively. The fault window can be expressed as:

$$2.5\ V \pm \frac{V_{ADJ}}{4} \tag{1}$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

$$V_S \pm (10 \times V_{ADJ})\% \tag{2}$$

When a sense input moves outside the fault window given in Equation 1, the appropriate hysteresis control signal turns off Q4 or Q5. For the under-voltage case, Q5 is disabled and current source I_{OB} flows through D2. The net current through R7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The overvoltage case is the same, with Q4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

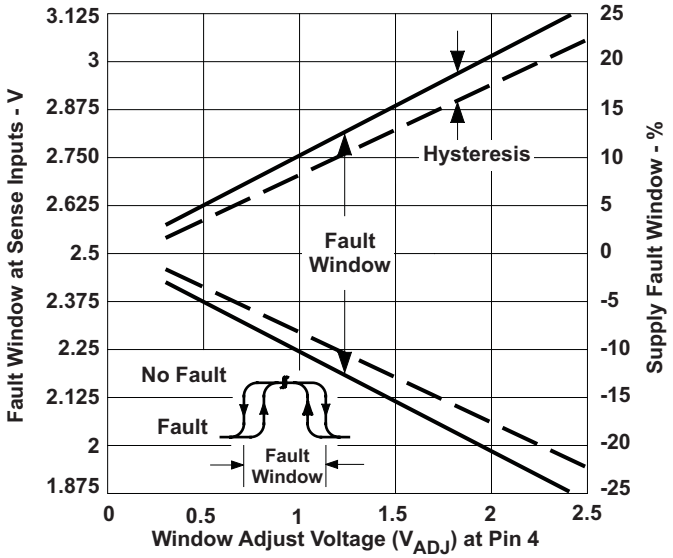
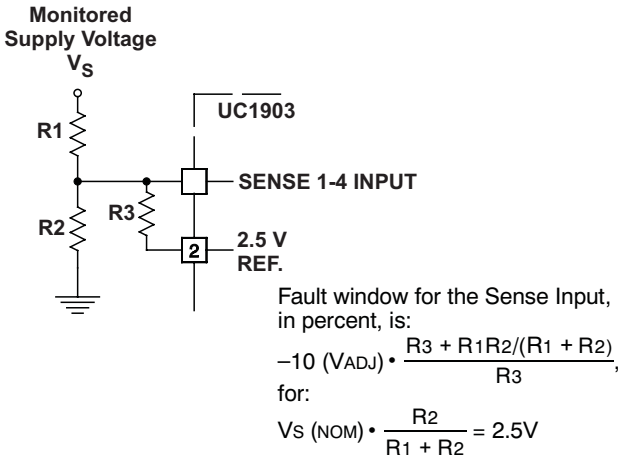


Figure 2. Fault Window and Threshold Hysteresis Scale as a Function of the Voltage Applied at Pin 4

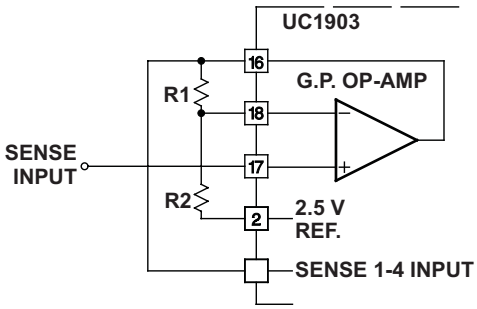
Fault Windows Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figure 3 and Figure 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.



A. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

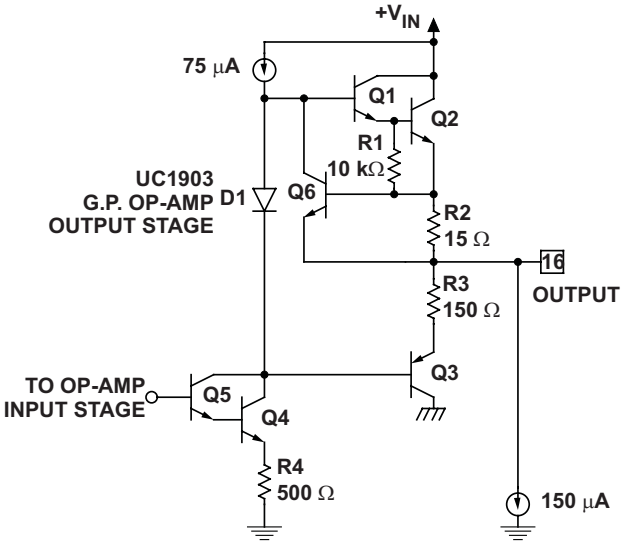
Figure 3. UC1903 Sense Input with an Independently Wider Fault Window



A. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4. UC1903 Sense Input with an Independently Tighter Fault Window

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5-V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability. ≥20 mA while the substrate device, Q3, provides good transient sinking capability.

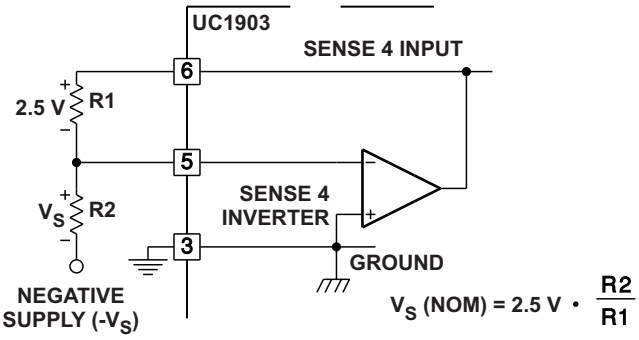


A. The G.P. op-amp on the UC1903 has a high source current (20 mA) capability and enhanced transient sinking capability through substrate device Q3.

Figure 5. The G.P. Op-Amp on the UC1903

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of the inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.



Note: A similar scheme w/the G.P. op-amp will allow a second negative supply to be monitored.

Figure 6. Inverting the Sense 4 Input for Monitoring a Negative Supply, Accommodated with the Dedicated Inverter

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0 V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0 V. The line sense comparator has approximately 175 mV of hysteresis requiring the line/switcher input to reach 2.175 V before the POWER OK output device can be turned off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

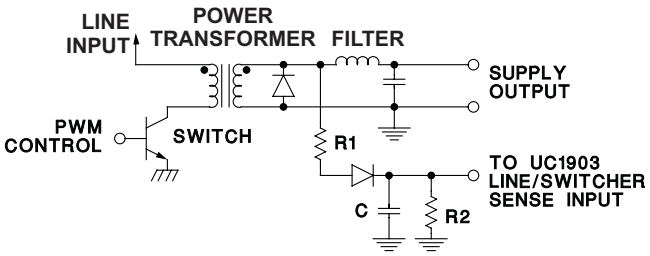
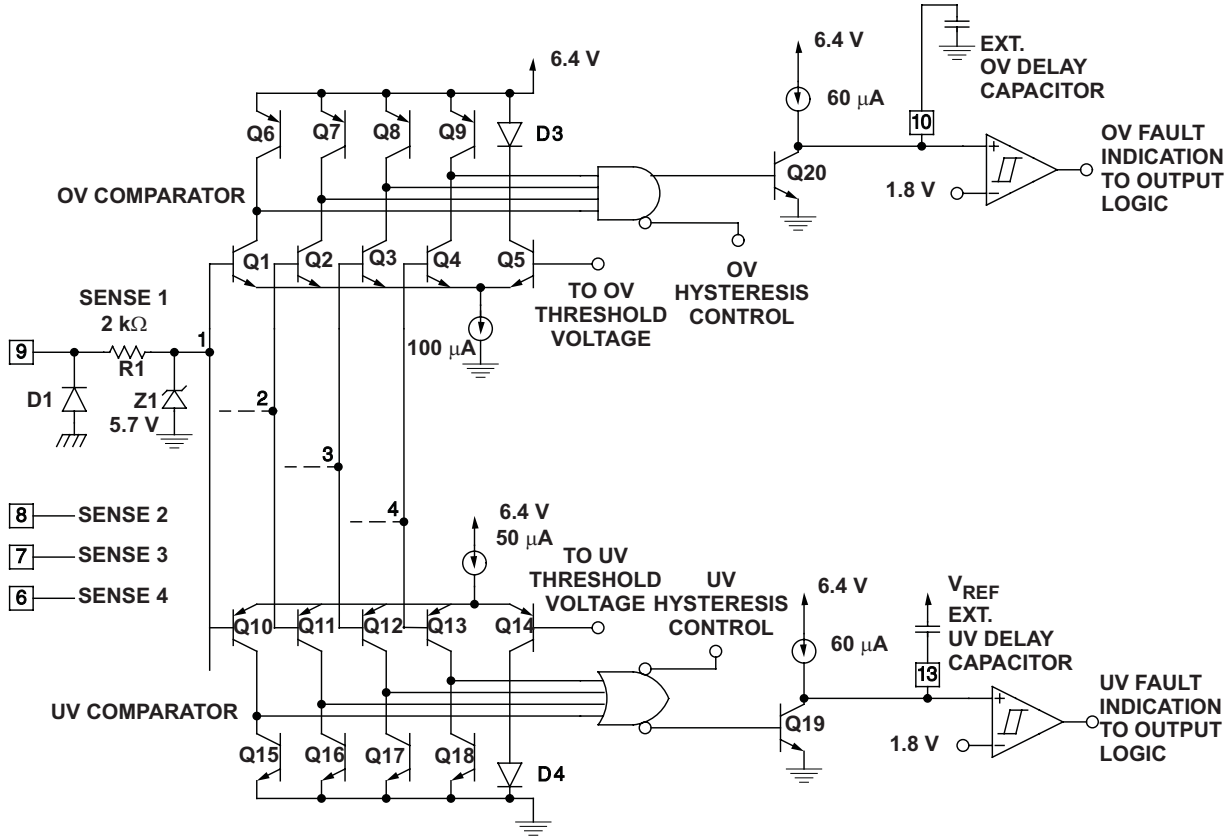


Figure 7. Line/Switcher Sense Input Used for Early Line or Switcher Fault Indication

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5-V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2-kΩ resistor, R1, and zener diode Z1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above –0.3 V. The same type of input protection exists at the line sense input, Pin 15, except a 5-kΩ series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q20 is turned off, allowing the internal 60-mA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8 V, the OV and POWER OK outputs become active low. When the fault condition goes away Q20 is turned back on, rapidly discharging the delay capacitor. Operation of the under- voltage delay is, with appropriate substitutions, the same.



A. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions. Terminating the UV delay capacitor to VREF assures correct logic at power up.

Figure 8. OV and UV Comparators on the UC1903

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

At power-Up, while the $+V_{IN}$ input supply is below 3 V, all open collector outputs are off. With $+V_{IN}$ greater than 3 V the POWER OK output will be driven low and the UV OV FAULT outputs are disabled. Once $+V_{IN}$ rises above the V_{SUV} threshold of 7 V the fault outputs will be enabled. As would be expected, the SENSE 1-4 voltages at power up may be below the UVFAULT window and the UVFAULT output may be driven low.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88697012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88697012A UC1903L/ 883B	Samples
5962-8869701VA	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8869701VA UC1903J/883B	Samples
UC1903J	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1903J	Samples
UC1903J883B	ACTIVE	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8869701VA UC1903J/883B	Samples
UC1903L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1903L	Samples
UC1903L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88697012A UC1903L/ 883B	Samples
UC2903DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2903DW	Samples
UC2903DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2903DW	Samples
UC2903DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2903DW	Samples
UC2903DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2903DW	Samples
UC2903J	LIFEBUY	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	-40 to 85	UC2903J	
UC2903N	LIFEBUY	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2903N	
UC2903NG4	ACTIVE	PDIP	N	18		TBD	Call TI	Call TI	-40 to 85		Samples
UC2903Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	UC2903Q	Samples
UC3903DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3903DW	Samples
UC3903DWG4	ACTIVE	SOIC	DW	18		TBD	Call TI	Call TI	0 to 70		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3903DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3903DW	Samples
UC3903DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3903DW	Samples
UC3903J	LIFEBUY	CDIP	J	18	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3903J	
UC3903N	LIFEBUY	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3903N	
UC3903NG4	LIFEBUY	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3903N	
UC3903Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	UC3903Q	Samples
UC3903QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	UC3903Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1903, UC2903, UC2903M, UC3903, UC3903M :

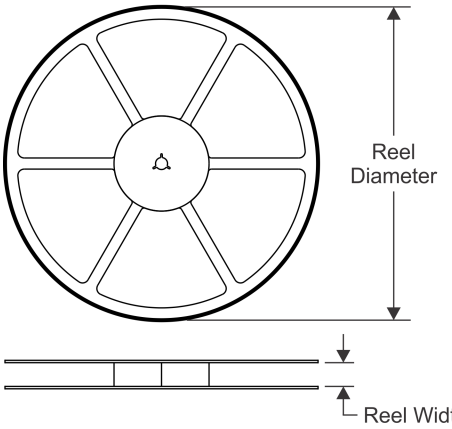
- Catalog: UC3903, UC2903, UC3903M, UC3903
- Military: UC2903M, UC1903, UC1903

NOTE: Qualified Version Definitions:

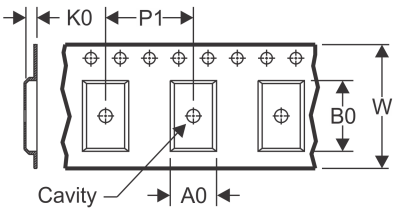
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

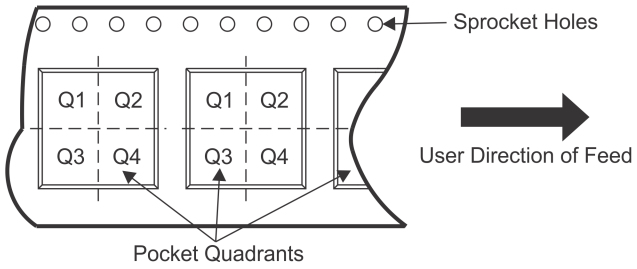


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

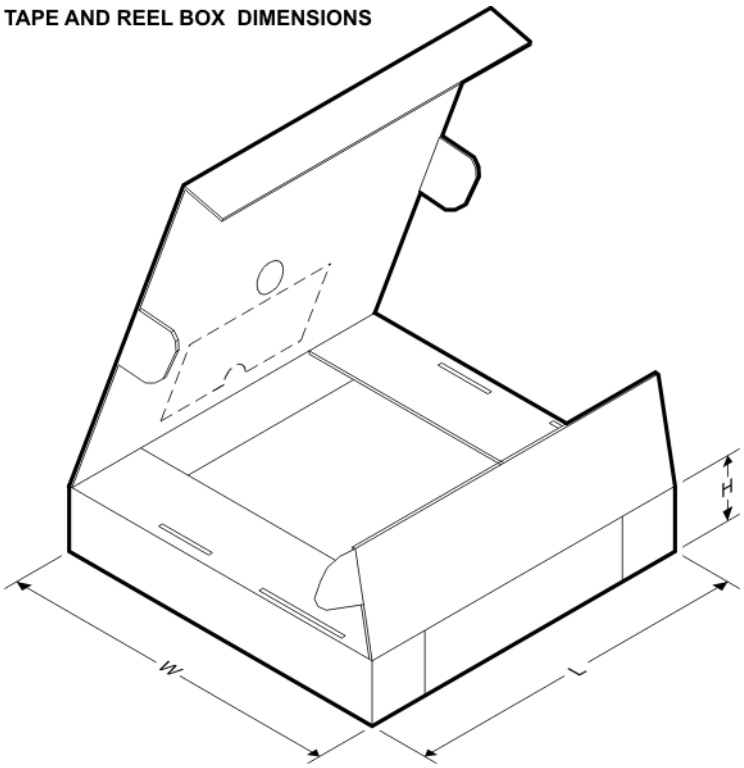
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2903DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
UC3903DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2903DWTR	SOIC	DW	18	2000	367.0	367.0	45.0
UC3903DWTR	SOIC	DW	18	2000	367.0	367.0	45.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265