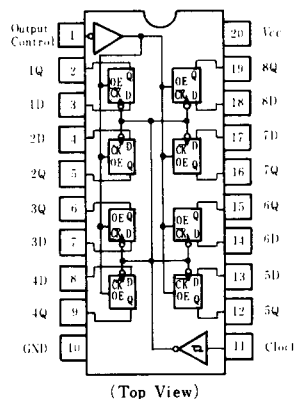


HD74LS374 ● Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

PIN ARRANGEMENT

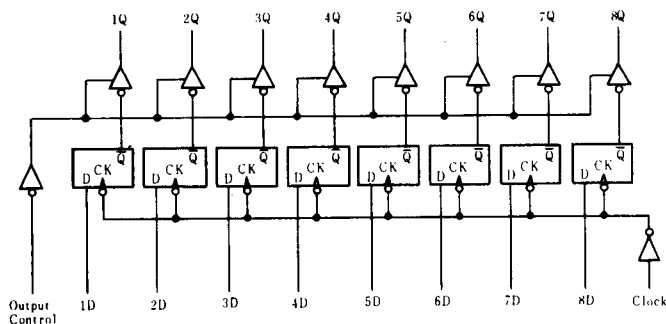


FUNCTION TABLE

Inputs			Output
Output control	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

Notes: H = high level, L = low level,
X = irrelevant
↑ = transition from low to high level
Q₀ = level of Q before the indicated steady-state input conditions were established
Z = off (high-impedance) state of a three-state output

BLOCK DIAGRAM



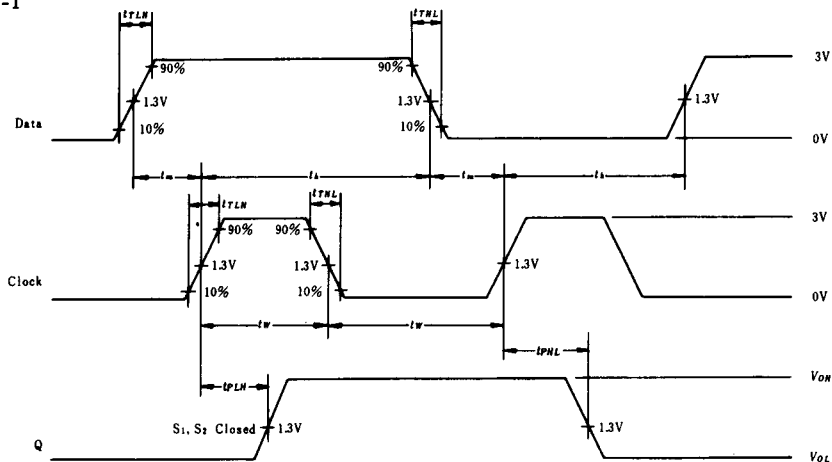
RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output voltage	V _{OH}	—	—	5.5	V
Output current	I _{OH}	—	—	-2.6	mA
	I _{OL}	—	—	24	mA
Clock pulse width	t _w	15	—	—	ns
		15	—	—	ns
Data setup time	t _{su}	20 ↑	—	—	ns
Data hold time	t _h	3 ↑	—	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.

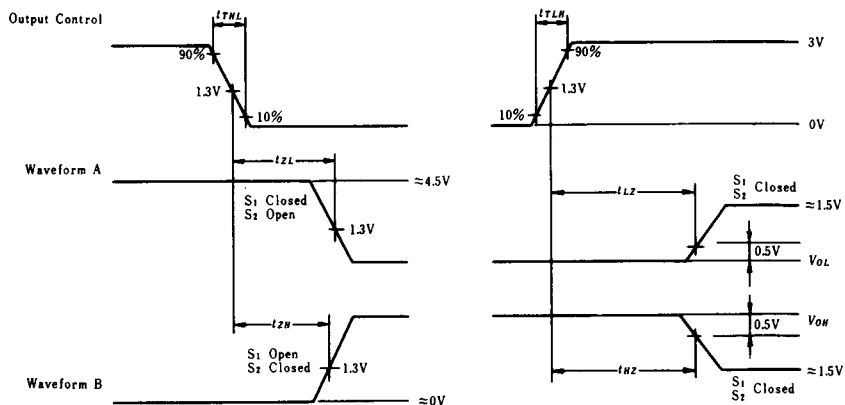
HD74LS374

Waveform-1



- Notes:
1. Input pulse; $t_{TLH} = 15\text{ns}$, $t_{THL} = 6\text{ns}$
Clock input; $PRR = 1\text{MHz}$, duty cycle 50%
Data input; $PRR = 500\text{kHz}$, duty cycle 50%
 2. f_{max} ; $t_{TLH} = 2.5\text{ns}$, $t_{THL} = 2.5\text{ns}$

Waveform-2



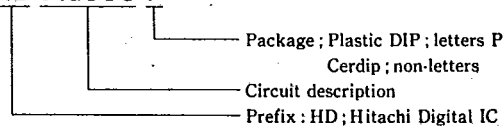
- Notes:
1. Input pulse; $t_{TLH} = 15\text{ns}$, $t_{THL} = 6\text{ns}$, $PRR = 1\text{MHz}$, duty cycle 50%
 2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

PACKAGING INFORMATION

T-90-20

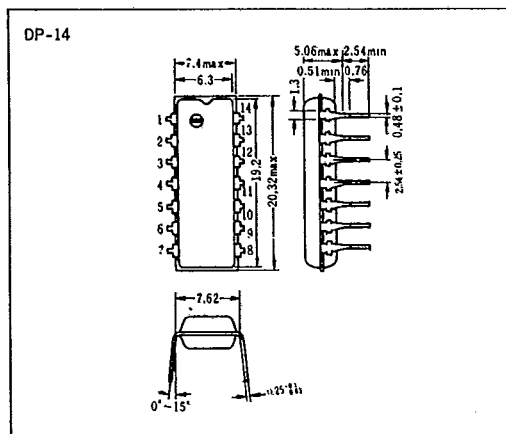
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

HD 74LS00 P

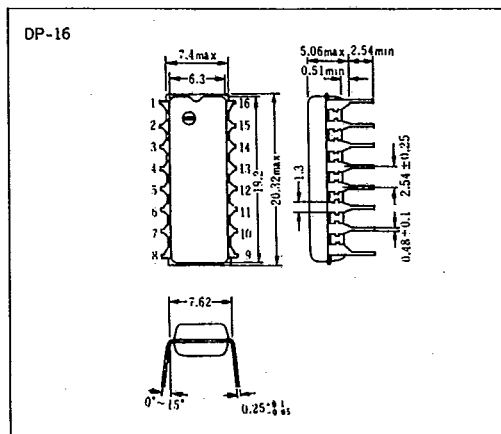


■ Plastic DIP

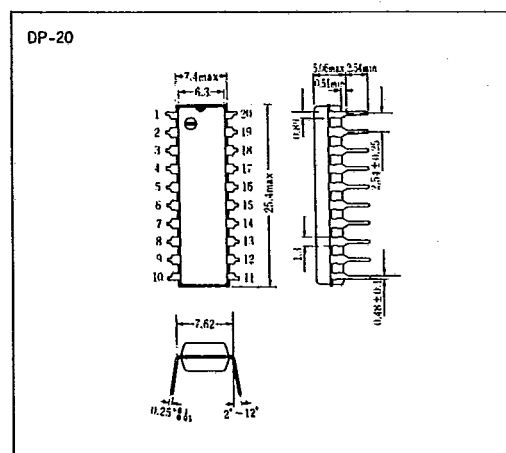
● 14 Pin



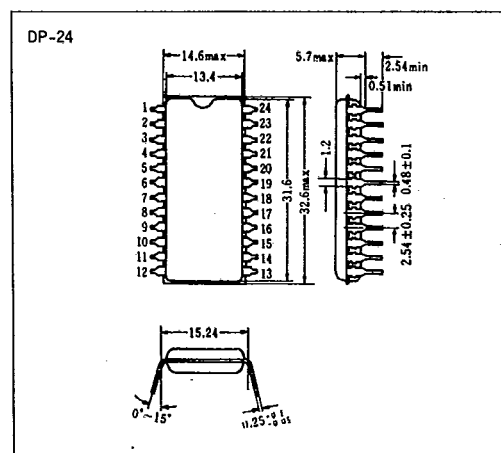
● 16 Pin



● 20 Pin



● 24 Pin



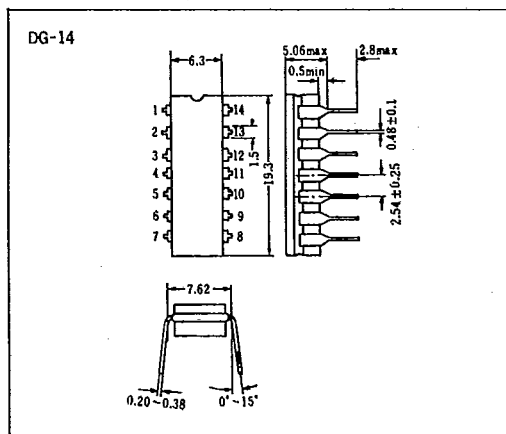
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T-90-20

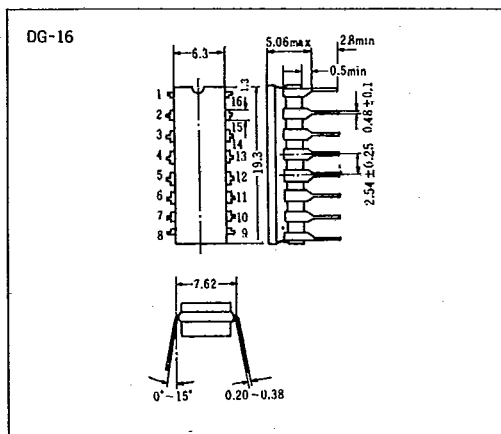
PACKAGING INFORMATION

■Cerdip

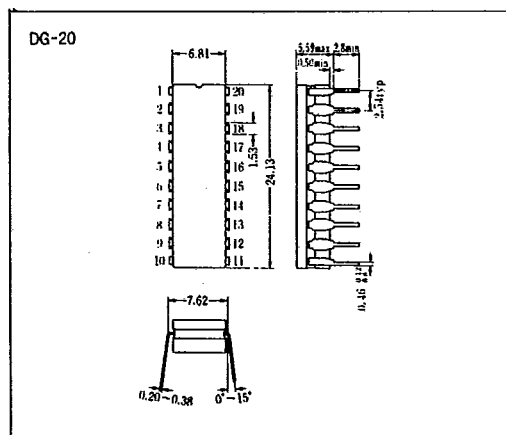
●14 Pin



●16 Pin



●20 Pin



●24 Pin

