

# AS3525

## Advanced Audio Processor System

### 1 Description

This highly flexible and fully integrated audio processor system (AS3525) combines strong calculating power, high performance audio features with system power management options for battery powered devices.

Using advanced 0.13µm process technology and large on chip RAM leads to outstanding low power consumption of as low as 58mW for a complete flash-player during MP3 playback.

Based on a powerful ARM9TDMI capable of performing up to 200MIPS it is suited to run MP3, AAC, WMA, OGG... decoders and encoders and, in addition, it can perform extensive user interfaces, motion graphics support, video playback and much more.

The AS3525 SOC (system-on-a-Chip) features dedicated high speed interfaces for ATA IDE, USB2.0 HS-OTG and SDRAM ensuring maximum performance for download, upload, and playback.

Furthermore interfaces for NAND flashes, MMC/SD cards and Memory Stick ensure most flexible system design possibilities. Hardware support for parallel interfaces lower the CPU load serving complex and/or colour user interfaces.

Additional serial high-speed data and control interfaces guarantee the connection to other peripherals and/or processors in the system.

Two independently programmable PLLs generate the required frequencies for audio playback/recording, for the processor core and for the USB interface at the same time. An additional external clock input eliminates the use of external crystals when used in multi-processor systems like mobile phones.

It has a variety of audio inputs and outputs to directly connect electret microphones, and auxiliary signal sources via a 10-channel mixer to a 16Ω/32Ω headset, 4Ω speaker or auxiliary audio peripherals.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player with flash or hard-disk memory are supplied by the AS3525. The different regulated supply voltages are fully programmable. The power management block generates 10 different supply voltages out of a single battery supply. CPU, NAND flash, SRAM, memory cards, LCD, LCD backlight and USB-OTG can be powered. When operating from a single cell (AA or AAA) battery the AS3525 can use a DCDC booster to generate the needed system supply.

The AS3525 has an independent 32kHz real time clock (RTC) on chip, which allows a complete power down of the system CPU and peripherals.

AS3525 also contains a charger for Li-Io battery supply

The single supply voltage may vary from 1.0V to 5.5V.

### 2 Key Features

#### 2.1 Digital Core

##### Embedded 32-Bit RISC Controller



- ARM922TDMI RISC CPU
- 2.5Mbit on-chip RAM
- 1Mbit on chip ROM
- Clock speed max. 250MHz (200MIPS)
- Standard JTAG interface

##### USB 2.0 HS & OTG Interface

- Up to 480Mbit/s transfer speed
- USB 2.0 HS/FS physical including OTG support
- USB 2.0 HS/FS digital core including OTG host
- Dedicated dual port buffer RAM
- DMA bus master functionality

##### IDE Host Controller

- Supporting Ultra ATA 33/66/100/133 modes
- Programmable IO and Multi-word DMA capability
- Dedicated dual port buffer RAM
- DMA bus master functionality

##### External Memory Controller

- Dynamic memory interface
- Asynchronous static memory
- DMA bus master functionality

##### DMA Controller

- Single Master DMA controller
- 2 DMA channels possible at the same time
- 16 DMA requests supported

##### Interrupt Controller

- Support for 32 standard interrupts
- Support for 16 vectored IRQ interrupts

##### Audio Subsystem Interface

- Dedicated 2 wire serial control master
- I2S input and output with dual port buffer RAM

##### Nand Flash Interface

- 8 and 16bit flash support
- 3, 4 & 5 byte address support
- hardware ECC

##### MMC/SD Interface

- MMC/SD Card host for multiple card support
- 4 data line support for SD cards

MS / MS Pro Interface

- Dedicated dual port buffer RAM

Display Interface

- Serial and parallel controller supported
- On chip hardware acceleration

Synchronous Serial Interface

- Master and slave operation
- 8 and 16 bit support
- Several protocol standards supported

I2S Interface

- Input multiplexed with audio subsystem
- selectable SPDIF input conversion
- Dedicated dual port buffer RAM

2 Wire Serial Control Interface

- Master and slave operation
- Standard and fast mode support

General Purpose IO Interface

- 4x 8-bit ports

## 2.2 Audio

Multi-bit Sigma Delta Converters

- DAC: 18bit with 94dB SNR ('A' weighted)
- ADC: 14bit with 82dB SNR ('A' weighted)
- Sampling Frequency: 8-48kHz
- 32 gain steps @ 1.5dB and MUTE

2 Line Inputs

- stereo, 2x mono or mono differential inputs
- 32 gain steps @ 1.5dB and MUTE

2 Microphone Inputs

- differential inputs
- 3 gain pre-sets (28/34/40 dB) and OFF with AGC
- 32 gain steps @ 1.5dB and MUTE
- microphone detection with about 50uA
- supply for electret microphone max 1mA
- remote control by switch

Line Output

- max 1Vp @ 10kΩ in single ended stereo mode
- >32Ω in mono differential mode to drive ear-pieces
- 32 gain steps @ 1.5dB and MUTE

Stereo Headphone Audio Amplifier

- 2x 60mW @ 16Ω driver capacity
- 32 gain steps @ 1.5dB and MUTE
- Click- and pop-less start-up and power down
- Headphone and over-current detection
- Phantom ground eliminates large capacitors

Stereo Speaker Audio Amplifier

- 2x 500mW @ 4Ω driver capacity
- 32 gain steps @ 1.5dB and MUTE
- Click- and pop-less start-up and power down
- Over-current detection

10 Channel Audio Mixer

- mixes Line inputs, Mic inputs and DAC output
- separate selectable source for right and left channel
- possibility to select AGC to prevent clipping

## 2.3 Power Management

Voltage Generation

- step up for system supply (3.0V-3.6V, 150mA)
- charge-pump for CPUcore (1.05V-1.2V, 50mA)
- charge pump for USB OTG (5V, 10mA)
- LDO for digital supply (2.9V, 200mA)
- LDO for analog supply (2.9V, 200mA)
- LDO for IO supply (2.94 or 3.11V, 200mA)
- LDO for peripherals (1.7V-3.3V, 200mA)
- LDO for USB Transceiver (3.26V, 200mA)
- LDO for RTC (1.0V-2.5V, 2mA)

15V Back-light step up converter

- for driving up to 6 white LEDs in series to achieve a uniform illumination
- current programmable up to 40mA (1.25mA steps)

Li-Io Battery Charger

- automatic 50mA trickle charging
- prog. constant current charging (50 – 400mA)
- prog. constant voltage charging (3.9 - 4.25V)

## 2.4 System

RTC

- ultra low power 32kHz oscillator
- 32bit RTC second counter
- selectable alarm (seconds or minutes)
- trim able oscillator

Oscillator

- low power 12-24MHz Oscillator
- generating main system clock

Supervisor

- automatic battery monitoring with interrupt generation and selectable warning level
- automatic temperature supervision with interrupt generation and selectable warning and shutdown levels

General Purpose ADC

- 10bit resolution
- 16 inputs analog multiplexer

UID

- Unique Identification Number in OTP ROM for DRM support

General

- Reset pin, watchdog
- 10sec emergency shut-down
- Wide battery supply range 1V – 5.5V
- MP3 playback with 58mW

Packages:

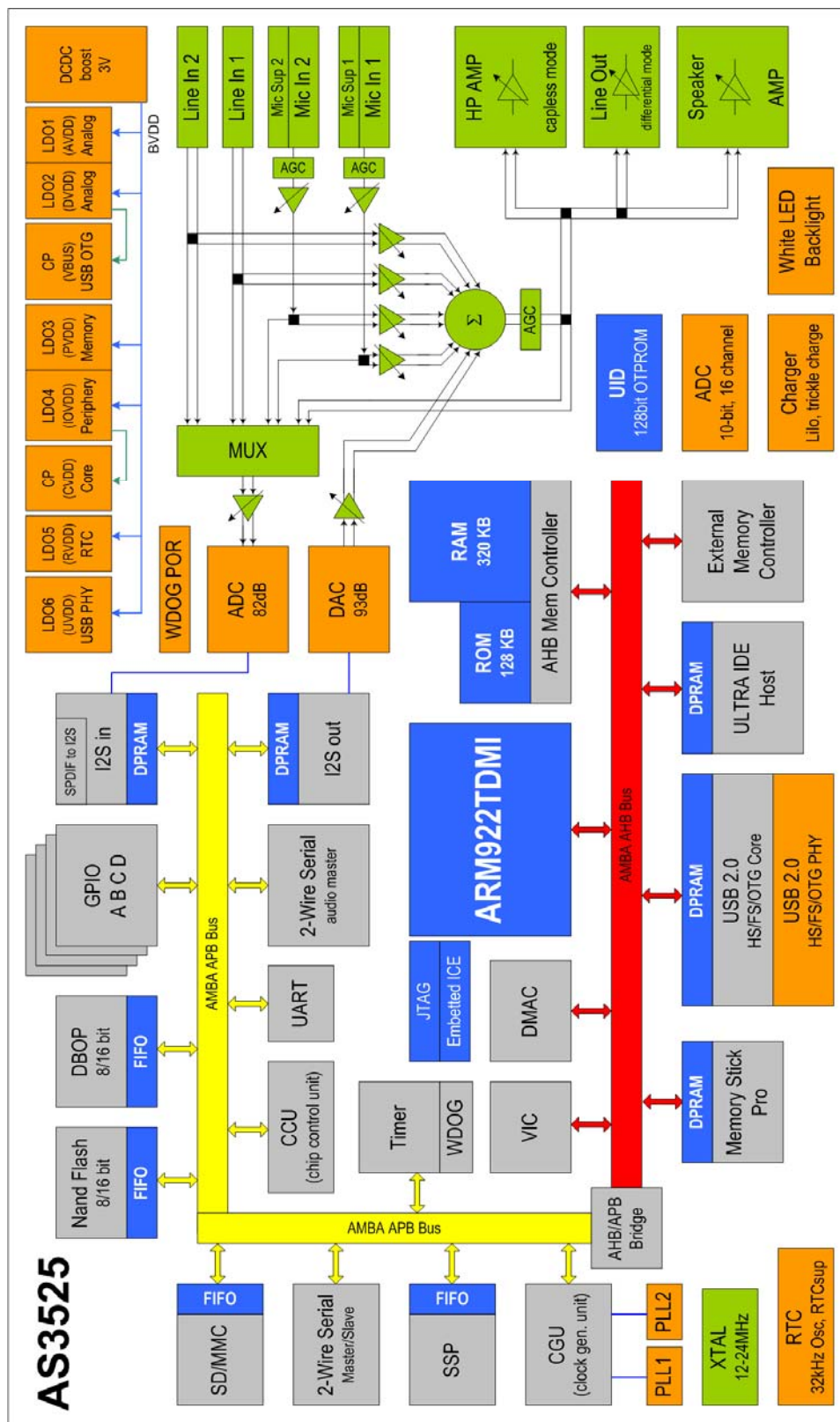
- AS3525-A: CTBGA224 13x13mm, 0.8mm pitch
- AS3525-B: CTBGA144 10x10mm, 0.8mm pitch

## 3 Application

- Portable Digital Audio Player and Recorder
- Portable Digital Media Player
- PDA
- Smartphone

## 4 Block Diagram

Figure 1 AS3525 Block Diagram



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## Document Revisions

| Revision | Chapter    | Date       | Owner   | Description                                                                                                                                                                                                                                                            |
|----------|------------|------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0.1      | all        | 9.12.2004  | mma     | first preliminary version                                                                                                                                                                                                                                              |
| 0.2      | 4,6.6      | 19.12.2004 | mma     | application figures, register base address                                                                                                                                                                                                                             |
| 0.3      | 7.6, 7.7   | 28.1.2005  | mma     | CTBGA144 ball-out added                                                                                                                                                                                                                                                |
| 0.4      | 6.2        | 7.3.2005   | mma     | changes in boot-concept                                                                                                                                                                                                                                                |
| 0.5      | 6.4.14     | 24.3.2005  | mma     | CGU frequency settings updated                                                                                                                                                                                                                                         |
| 0.6      | 6.2, 7.4   | 1.4.2005   | mma     | correct IntBootSel                                                                                                                                                                                                                                                     |
| 0.6      | 7.7        | 1.4.2005   | mma     | Package Code and Marking added                                                                                                                                                                                                                                         |
| 0.7      | 6.7 – 6.28 | 2.5.2005   | mma     | Parameters updated                                                                                                                                                                                                                                                     |
| 0.7      | 5.1.2.     | 2.5.2005   | mma     | Supply Currents added                                                                                                                                                                                                                                                  |
| 0.7      | 6.15       | 5.5.2005   | mma     | Audio Specification added                                                                                                                                                                                                                                              |
| 0.8      | 7.4, 7.7   | 21.6.2005  | mma     | tmsel PAD-type is pull down                                                                                                                                                                                                                                            |
| 0.8      | 5          | 28.7.2005  | mma     | Lead temperature corrected for lead-free package                                                                                                                                                                                                                       |
| 0.8      | 5.0, 5.1   | 5.8.2005   | wsg     | Added conditions for absolute max rating of vdd_peri, vdd_mem, vdd_core, usb_vdda_33t, usb_vdda_33c. Changed operating condition for vdd_core max limit.                                                                                                               |
| 0.82     | 7.8        | 6.10.2005  | pkm     | added pad cell description                                                                                                                                                                                                                                             |
| 0.82     | 7          | 13.10.2005 | pkm     | correct pin list pad types (JTAG_trst_n, jtag_tdi, mpmc_fbclk_in, naf_bsy_n, ide_ha[0..2], ide_reset_n, id_dig)                                                                                                                                                        |
| 0.83     | 5.1.1      | 22.10.2005 | wsg     | Added Note on VDD_CORE supply voltage scaling                                                                                                                                                                                                                          |
| 1.00     | all        |            | wsg/pkm | Major revision                                                                                                                                                                                                                                                         |
| 1.1      |            | 25.9.2006  | wsg     | added description for modified C22 bootloader                                                                                                                                                                                                                          |
|          |            | 16.2.2007  | wsg     | added UART description<br>corrected NAFmode register description<br>added C22O22 version in order information<br>corrected header in table "CGU frequency settings"                                                                                                    |
|          |            | 22.3.2007  | pkm     | updated ESD and soldering conditions, change ADC_10 source for C22O22 from BVDD to CHG_OUT                                                                                                                                                                             |
| 1.11     |            | 17.4.2007  | wsg     | update of PINOUT for AS3525A: test pins at K2, K4 and L2 are only used during production test and must stay unconnected for normal operation mode. Pins are now marked with NC. Added Note for AS3525B package that CVDD and vdd_core have to be connected externally! |
| 1.12     | 7.4.7.2    | 6.7.2007   | wsg     | added application circuit with schottky diodes for speaker output protection.                                                                                                                                                                                          |
|          | 7.1.6      | 6.7.2007   | wsg     | deleted description of C21O20 bootloader (this chip version is not available any more)                                                                                                                                                                                 |
| 1.13     | 6.2.3      | 24.2.2009  | wsg     | Added definition of Power Management Output Voltages                                                                                                                                                                                                                   |

## Related Documents

|                                                                            |                        |                                                               |
|----------------------------------------------------------------------------|------------------------|---------------------------------------------------------------|
| ARM922T Technical Reference Manual                                         | DDI0184B_922T_TRM.pdf  | <a href="http://www.arm.com">http://www.arm.com</a>           |
| ARM9TDMI Technical Reference Manual                                        | DDI0180A_9tdmi_trm.pdf | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ MultiPort Memory Controller; PL172 Technical Reference Manual   |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| AMBA Specification (Rev 2.0)                                               | IHI0011A_AMBA_SPEC.pdf | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ Synchronous Serial Port; PL022 Technical Reference Manual       |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ General Purpose Input/Output; PL061 Technical Reference Manual  |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ Single Master DMA Controller; PL081 Technical Reference Manual  |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ Multimedia Card Interface; PL180 Technical Reference Manual     |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| PrimeCell™ Vectored Interrupt Controller; PL190 Technical Reference Manual |                        | <a href="http://www.arm.com">http://www.arm.com</a>           |
| CWda03 - SPDIF-AES/EBU TO I2S CONVERTER                                    |                        | <a href="http://www.coreworks.pt">http://www.coreworks.pt</a> |
| TSMC TPZ013G3 Standard I/O Library Databook                                |                        | <a href="http://www.tsmc.com">http://www.tsmc.com</a>         |
| DesignWare USB 2.0 HI-SPEED ON-THE-GO Controller Subsystem                 |                        | <a href="http://www.synopsys.com">http://www.synopsys.com</a> |
| DesignWare USB 2 PHY Hardmacro                                             |                        | <a href="http://www.synopsys.com">http://www.synopsys.com</a> |
| SMS2IP mem stick host controller                                           |                        | <a href="http://www.sony.com">http://www.sony.com</a>         |
| ICON mem stick host con interface                                          |                        | <a href="http://www.sony.com">http://www.sony.com</a>         |
| IDE host controller BK3710S                                                |                        | <a href="http://www.palmchip.com">http://www.palmchip.com</a> |

## 5 Typical Applications

AS3525 is an advanced audio system-on-a-chip for flash-players, hard-disk players, mobile phones and PDAs powered by single Li+, AA or AAA batteries.

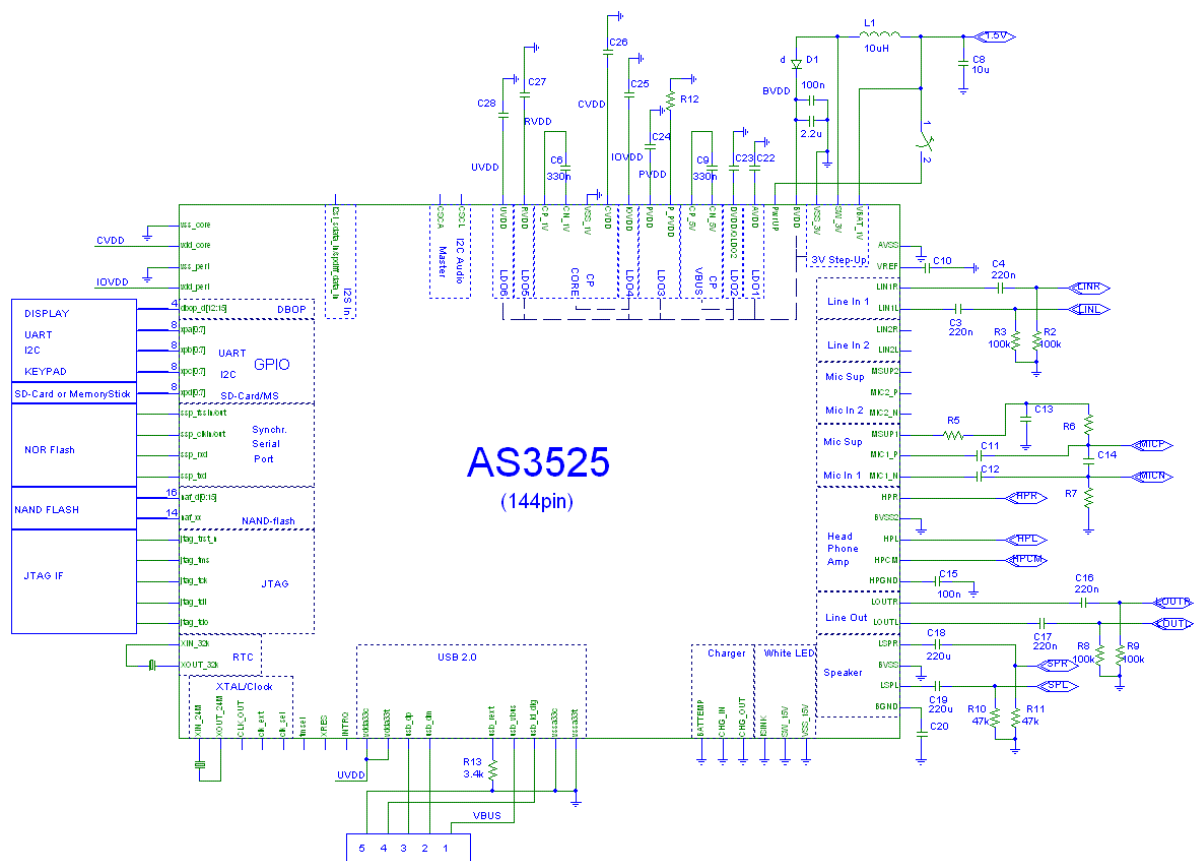
AS3525-A is the package variant with 224 balls intended for full-featured harddisk players, AS3525-B is the package variant with 144 balls for flash players with reduced feature set and no need for an external SDRAM.

Two versions are available for the chips: C22022 which is the newest version with additional boot loader features, and C21020 which is outdated and must not be used for new design starts.

### 5.1 Flash-Player

The following schematic shows a typical flash-player application of the AS3525-B in the CTBGA144 package. A single AAA or AA battery powers the complete system. The on-chip DC/DC converter generates a supply voltage of 3.25V (BVDD) with a maximum output load current of 150mA. Linear regulators, which are connected to this BVDD, provide the supply voltages for the analog functions, the USB-2.0-Phy, the digital periphery and external components. A highly efficient Charge-Pump Step-Down-Converter supplies the digital core. All analog features are available in this package variant. Also, the digital interfaces to NAND-flash, MMC/SD card, Memory-Stick-Pro, USB-2.0 HS&OTG, Synchronous Serial Interface, General Purpose IOs and different displays are provided.

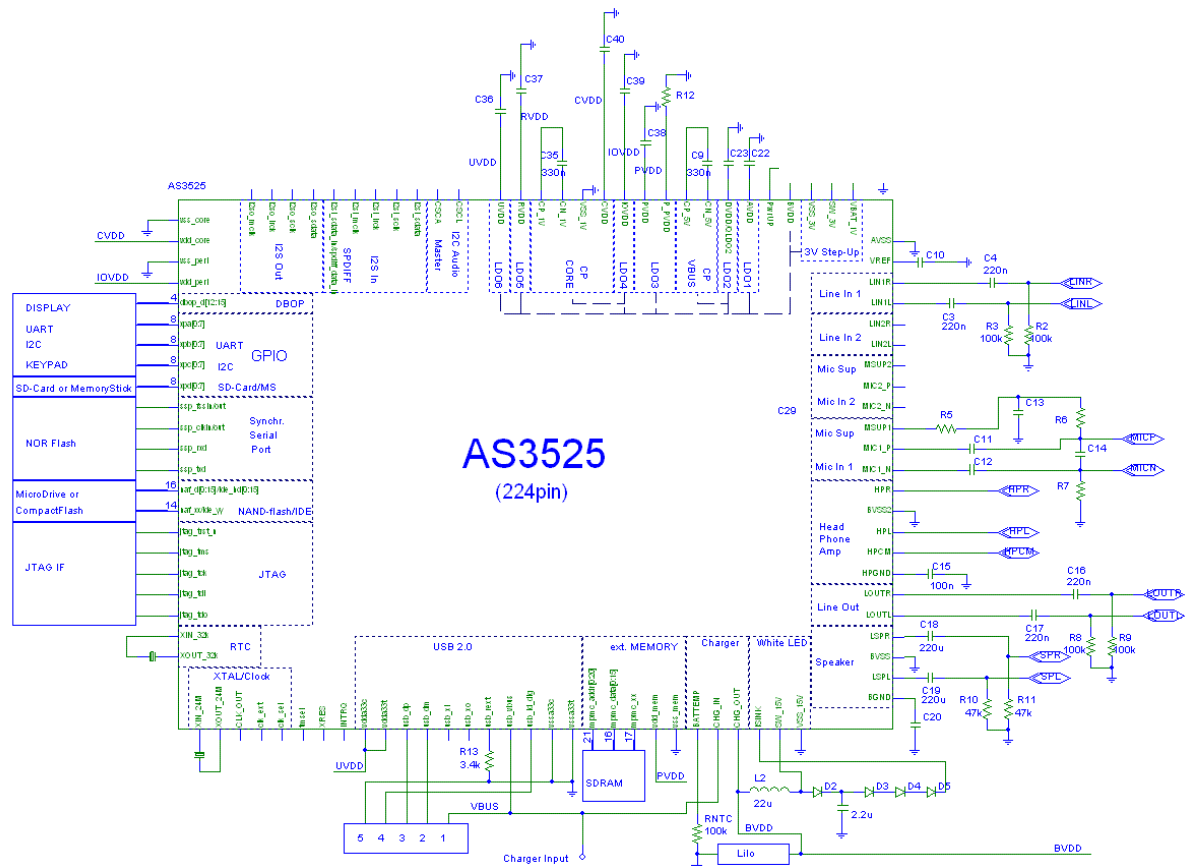
Figure 2 Flash Player Application



## 5.2 Hard-Disk-Player

The following schematic shows a typical hard-disk-player application of the AS3525-A using the CTBGA224 package. A single Li+ battery powers the complete system. The Li+ cell can be charged either from a DC-supply or the USB connector. Linear regulators, which are connected to this battery voltage (BVDD), provide the supply voltages for the analog functions, the USB-2.0-Phy, the digital periphery and the SDRAM interface. A highly efficient Charge-Pump Step-Down-Converter supplies the digital core. All chip functions are available in this package variant. For lowest power consumption, it is recommended to use low voltage external SDRAMs (PVDD=1.8V).

Figure 3 Hard Disk Player



## 6 Electrical Specifications

### 6.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 1 Absolute Maximum Ratings

| Symbol                | Parameter                                          | Min  | Max             | Unit | Note                                                                                                                                      |
|-----------------------|----------------------------------------------------|------|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>IN_SUP</sub>   | digital supply pins                                | -0.5 | 3.7             | V    | Applicable for pins vdd_peri, vdd_mem, usb_vdda33t1, usb_vdda33t2, usb_vdda33t3, usb_vdda33c                                              |
| V <sub>IN_CORE</sub>  | digital core supply pins                           | -0.5 | 1.68            | V    | Applicable for pins vdd_core                                                                                                              |
| V <sub>IN_VB1V</sub>  | single cell supply voltage                         | -0.5 | 5.0             | V    | Applicable for pin VBAT_1V                                                                                                                |
| V <sub>IN_5V</sub>    | 5V pins                                            | -0.5 | 7.0             | V    | Applicable for pins BVDD, CHG_IN, VBUS                                                                                                    |
| V <sub>IN_SW15</sub>  | 15V pin                                            | -0.5 | 17              | V    | Applicable for pins SW15                                                                                                                  |
| V <sub>IN_VSS</sub>   | Voltage difference at VSS terminals                | -0.5 | 0.5             | V    | Applicable for pins VSS3, VSS15, VSSCP, BVSS, BVSS2, AVSS, DVSS, vss_core, vss_peri, vss_mem, usb_vssa33t, usb_vssa33c                    |
| V <sub>IN_DVDD</sub>  | 3.3V pins with diode to DVDD                       | -0.5 | 5.0<br>DVDD+0.5 | V    | Applicable for pins MCLK, LRCK, SCLK, SDI, P_PVDD, BATTEMP, ISINK, XIN_32K, XOUT_32K, XIN_24M, XOUT_24M, INTRQ, XRES, CP_1V, CN_1V, CN_5V |
| V <sub>IN_XDVDD</sub> | pins with no diode to DVDD                         | -0.5 | 7.0V            | V    | Applicable for pins CSCL, CSDA, PWR_UP, CP_5V                                                                                             |
| V <sub>IN_AVDD</sub>  | 3.3V pins with diode to AVDD                       | -0.5 | 5.0<br>AVDD+0.5 | V    | Applicable for pins BGND, HPH_CM, HPGD, LOU1L/R, VREF, AGND, LIN1L/R, LIN2L/R, MIC1_P/N, MIC2_P/N, MSUP1, MSUP2                           |
| V <sub>IN_REG</sub>   | voltage regulator pins with diodes to BVDD         | -0.5 | 5.0<br>BVDD+0.5 | V    | Applicable for pins AVDD, QLDO2, DVDD, PVDD, CPVDD, CVDD, UVDD                                                                            |
| V <sub>IN_RVDD</sub>  | voltage regulator pin with diode to BVDD           | -0.5 | 3.6<br>BVDD+0.5 | V    | Applicable for pins RVDD                                                                                                                  |
| V <sub>IN_BVDD</sub>  | pins with diode to BVDD                            | -0.5 | 7.0<br>BVDD+0.5 | V    | Applicable for pins LSPR/L, HPR/L, CHG_OUT, SW3                                                                                           |
| I <sub>scr</sub>      | Input Current (latchup immunity)                   | -100 | 100             | mA   | Norm: JEDEC 17                                                                                                                            |
| ESD                   | Electrostatic Discharge HBM                        |      | +/-1            | kV   | Norm: JEDEC JESD22-A114C (1)                                                                                                              |
| ESD_USB               | Electrostatic Discharge HBM for USB Pins           |      | +/-2            | kV   | Norm: JEDEC JESD22-A114C (Pins: usb_dp, usb_dm, usb_vbus)                                                                                 |
| P <sub>t</sub>        | Total Power Dissipation (all supplies and outputs) |      | 1000            | mW   | Valid for CTBGA144 package                                                                                                                |
| H                     | Humidity non-condensing                            | 5    | 85              | %    |                                                                                                                                           |

(1) Electrostatic discharge of XIN24 and XOUT24 pin is +/-600V for C21020

Table 2 Soldering Conditions

| Symbol            | Parameter                | Min | Max | Unit | Note                                                                |
|-------------------|--------------------------|-----|-----|------|---------------------------------------------------------------------|
| T <sub>body</sub> | Package Body Temperature |     | 260 | °C   | Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only |
| T <sub>peak</sub> | Solder Profile*          | 235 | 245 | °C   |                                                                     |
| D <sub>well</sub> |                          | 30  | 45  | s    | above 217 °C                                                        |

\* austriamicrosystems AG strongly recommends to use underfill.

## 6.2 Operating Conditions

### 6.2.1 Supply Voltages

Table 3 Operating conditions for supply input voltages

| Symbol | Parameter                                                                               | Min  | Max | Unit | Note                                                                                                          |
|--------|-----------------------------------------------------------------------------------------|------|-----|------|---------------------------------------------------------------------------------------------------------------|
| VB1V   | DCDC Supply Voltage                                                                     | 1.0  | 3.6 | V    |                                                                                                               |
| BVDD   | Battery Supply Voltage                                                                  | 3.2  | 5.5 | V    |                                                                                                               |
| VBUS   | USB VBUS Voltage                                                                        | 4.0  | 5.5 | V    |                                                                                                               |
| CHGIN  | Charger Supply Voltage                                                                  | 4.5  | 5.5 | V    |                                                                                                               |
|        | Difference of Negative Supplies<br>VSS3, VSS1, VSS15, BVSS,<br>BVSS2, AVSS, DVSS, VSSCP | -0.1 | 0.1 | V    | To achieve good performance, the negative supply terminals should be connected to low impedance ground plane. |

### 6.2.2 Internal Supply Voltages

Following supply voltages for the digital system are generated by the integrated power management

Table 4 Operating conditions for internal internal supply voltages

| Symbol              | Parameter                                                                                   | Min  | Max  | Unit | Note                                                                                                          |
|---------------------|---------------------------------------------------------------------------------------------|------|------|------|---------------------------------------------------------------------------------------------------------------|
| VDD <sub>peri</sub> |                                                                                             | 3.0  | 3.6  | V    | digital periphery supply voltage to be connected to IOVDD                                                     |
| VDD <sub>mem</sub>  |                                                                                             | 1.7  | 3.6  | V    | digital IO supply for MPMC PADs to be connected to PVDD                                                       |
| VDD <sub>core</sub> |                                                                                             | 1.08 | 1.26 | V    | digital core supply voltage to be connected to CVDD; <b>see Note (1)</b>                                      |
| USBVDDA33T          |                                                                                             | 3.15 | 3.45 | V    | USB analog supply transmit block to be connected to UVDD                                                      |
| USBVDDA33C          |                                                                                             | 3.15 | 3.45 | V    | USB analog supply common block to be connected to UVDD                                                        |
| DVDD                | Digital Supply Voltage                                                                      | 2.8  | 3.6  | V    | Digital Audio Supply Voltage (LDO2)                                                                           |
| AVDD                | Analogue Supply Voltage                                                                     | 2.8  | 3.6  | V    | Analog Audio Supply Voltage (LDO1)                                                                            |
|                     | Difference of Negative Supplies<br>vss_peri, vss_core, vss_mem,<br>usb_vssa33c, usb_vssa33t | -0.1 | 0.1  | V    | To achieve good performance, the negative supply terminals should be connected to low impedance ground plane. |

**Note(s)** (1) For the VDD\_CORE supply, voltage scaling should be applied to optimize power consumption and CPU speed performance. For normal operation with fclk (CPU ARM-922T clock) frequencies below 200 MHz, CVDD (supply of VDD\_CORE) can be set to a lower value of 1.10 V. Only for setting fclk of the CPU to clock frequencies above 200 MHz, the VDD\_CORE supply voltage must be set to 1.20 V typical conditions.

## 6.2.3 Power Management Output Voltages

Following voltages are generated by the integrated power management blocks.

Table 5 Power Management – Output Voltages

| Symbol                 | Parameter                                | Condition                          | min. | typ. | max. | Unit |
|------------------------|------------------------------------------|------------------------------------|------|------|------|------|
| CVDD Regulator         |                                          |                                    |      |      |      |      |
| CVDDP                  | Core Supply Voltage                      | bits CVDDp[1:0]=00                 | 1.16 | 1.20 | 1.24 | V    |
|                        |                                          | bits CVDDp[1:0]=01                 | 1.10 | 1.15 | 1.30 | V    |
|                        |                                          | bits CVDDp[1:0]=10<br>see Note (1) | 1.06 | 1.10 | 1.14 | V    |
|                        |                                          | bits CVDDp[1:0]=11<br>see Note (1) | 1.01 | 1.05 | 1.09 | V    |
| Low Dropout Regulators |                                          |                                    |      |      |      |      |
| AVDD                   | Output Voltage LDO1                      |                                    | 2.85 | 2.90 | 2.95 | V    |
| DVDD                   | Output Voltage LDO2                      |                                    | 2.85 | 2.90 | 2.95 | V    |
| PVDDP                  | Output Voltage LDO3                      | bit PVDDp=0                        | 1.65 | 1.70 | 1.75 | V    |
|                        |                                          | bit PVDDp=1                        | 1.75 | 1.80 | 1.85 | V    |
|                        |                                          | bit PVDDp=0                        | 2.69 | 2.74 | 2.80 | V    |
|                        |                                          | bit PVDDp=1                        | 2.84 | 2.90 | 2.96 | V    |
|                        |                                          | bit PVDDp=0                        | 3.10 | 3.15 | 3.20 | V    |
|                        |                                          | bit PVDDp=1                        | 3.27 | 3.30 | 3.39 | V    |
|                        |                                          | bit PVDDp=0                        | 2.45 | 2.50 | 2.55 | V    |
|                        |                                          | bit PVDDp=1                        | 2.30 | 2.36 | 2.42 | V    |
| IOVDD                  | Output Voltage LDO4                      | bit IOVDDp=0                       | 3.06 | 3.11 | 3.16 | V    |
|                        |                                          | bit IOVDDp=1                       | 2.89 | 2.94 | 2.99 | V    |
| 3V Step-Up Converter   |                                          |                                    |      |      |      |      |
| BVDD                   | Output Voltage of DCDC Step Up Converter | bits DCDC3p=11                     | 1.95 | 3.00 | 3.05 | V    |
|                        |                                          | bits DCDC3p=10                     | 3.05 | 3.10 | 3.15 | V    |
|                        |                                          | bits DCDC3p=01                     | 3.15 | 3.20 | 3.25 | V    |
|                        |                                          | bits DCDC3p=00                     | 3.55 | 3.60 | 3.65 | V    |

Notes:

(1) This setting must not be used for AS3525 core supply because the lower voltage limit is out of core supply specification limits.

## 6.2.4 Operating Currents

Table 6 Supply currents

| Symbol         | Parameter                                                      | Typ | Max | Unit | Note          |
|----------------|----------------------------------------------------------------|-----|-----|------|---------------|
| I_BVDD         | Total current consumption at BVDD                              | 22  | 340 | mA   | (1), (2), (3) |
| IDD_PERI_OP    | Peripheral current                                             | 2   | 20  | mA   |               |
| IDD_MEM_OP     | External memory interface current                              | -   | 20  | mA   | (2)           |
| IDD_CORE_OP    | Digital core current                                           | 20  | 145 | mA   | (1), (2), (3) |
| IDD_USBA33T_OP | USB transmitter current                                        |     | 30  | mA   |               |
| IDD_USBA33C_OP | USB common blocks current                                      |     | 30  | mA   |               |
| I_Headphone    | Headphone current from BVDD                                    | 2   | 40  | mA   | (3)           |
| I_Audio        | Analog audio frontend current from DVDD (2.9V) and AVDD (2.9V) | 8   | 15  | mA   | (1), (3)      |

- Notes
- (1) Typical condition for playback of MP3 music with 44.1 KHz / 128 kbit with 32Ω headphones. The internal charge pump generates VDD\_CORE. No external SDRAM connected. USB2.0 in standby.
  - (2) Maximum condition for ARM running at 250 MHz, AHB/APB bus and memory at 64 MHz, USB 2.0 in HS operation. For high current mode, the charge pump is disabled and IDD\_CORE\_OP is added to the total current consumption at BVDD.
  - (3) For maximum value: assuming maximum output power of 2x40 mW sine-wave into headphones (16Ω). Internal loss of headphone AB amplifier is included.

In the case of standby mode or in the case of configuring the device to stopped clock, following current consumption is measured.

Table 7 Leakage currents

| Symbol        | Parameter | Typ | Max  | Unit | Note                       |
|---------------|-----------|-----|------|------|----------------------------|
| IDD_PERI_LEAK |           |     | 1500 | μA   | Including USBA33T, USBA33C |
| IDD_MEM_LEAK  |           |     | 500  | μA   |                            |
| IDD_CORE_LEAK |           |     | 1000 | μA   |                            |

## 6.2.5 Temperature Range

Table 8 Temperature Range

| Symbol          | Parameter                   | Min | Typ | Max | Unit | Note                 |
|-----------------|-----------------------------|-----|-----|-----|------|----------------------|
| T <sub>op</sub> | Operating temperature range | 0   | 25  | 85  | °C   |                      |
| T <sub>j</sub>  | Junction temperature range  | 0   |     | 110 | °C   |                      |
| R <sub>th</sub> | Thermal Resistance          |     | 29  |     | °C/W | For CTBGA144 package |

## 6.2.6 Audio Specification

Table 9 Audio Parameters

| Symbol                           | Parameter                 | Notes                                                            | Min | Typ   | Max | Unit             |
|----------------------------------|---------------------------|------------------------------------------------------------------|-----|-------|-----|------------------|
| <b>DAC Input to Line Output</b>  |                           |                                                                  |     |       |     |                  |
| FS                               | Full Scale Output         | 1kHz FS input                                                    |     | 0.985 |     | V <sub>RMS</sub> |
| SNR                              | Signal to Noise Ratio     | A-weighted, no load, silence input                               |     | 92    |     | dB               |
| DR                               | Dynamic Range             | A-weighted, no load, -60dB FS 1kHz input                         |     | 89    |     | dB               |
| THD                              | Total Harmonic Distortion | 1kHz FS input                                                    |     | -90   |     | dB               |
| <b>Line Input to Line Output</b> |                           |                                                                  |     |       |     |                  |
| FS                               | Full Scale Output         | 1kHz 1V <sub>RMS</sub> (FS) input                                |     | 0.95  |     | V <sub>RMS</sub> |
| SNR                              | Signal to Noise Ratio     | A-weighted, no load, silence input                               |     | 93    |     | dB               |
| THD                              | Total Harmonic Distortion | 1kHz 1V <sub>RMS</sub> (FS) input                                |     | -85   |     | dB               |
| CS                               | Channel Separation        |                                                                  |     | 89    |     | dB               |
| <b>DAC Input to HP Output</b>    |                           |                                                                  |     |       |     |                  |
| FS                               | Full Scale Output         | R <sub>L</sub> = 32Ω                                             |     | 0.950 |     | V <sub>RMS</sub> |
|                                  |                           | R <sub>L</sub> = 16Ω                                             |     | 0.944 |     | V <sub>RMS</sub> |
| SNR                              | Signal to Noise Ratio     | A-weighted, no load, silence input                               |     | 94    |     | dB               |
| DR                               | Dynamic Range             | A-weighted, no load, -60dB FS 1kHz input                         |     | 90    |     | dB               |
| THD                              | Total Harmonic Distortion | no load, 1kHz FS input                                           |     | -90   |     | dB               |
|                                  |                           | P <sub>out</sub> =20mW, R <sub>L</sub> = 32Ω, f=1kHz FS input    |     | -73   |     | dB               |
|                                  |                           | P <sub>out</sub> =40mW, R <sub>L</sub> = 16Ω, f=1kHz FS input    |     | -66   |     | dB               |
| CS                               | Channel Separation        | R <sub>L</sub> = 32Ω                                             |     | 73    |     | dB               |
|                                  |                           | R <sub>L</sub> = 16Ω                                             |     | 66    |     | dB               |
| <b>Line Input to HP Output</b>   |                           |                                                                  |     |       |     |                  |
| FS                               | Full Scale Output         | R <sub>L</sub> = 32Ω, 1kHz 1V <sub>RMS</sub> (FS) input          |     | 0.930 |     | V <sub>RMS</sub> |
|                                  |                           | R <sub>L</sub> = 16Ω, 1kHz 1V <sub>RMS</sub> (FS) input          |     | 0.936 |     | V <sub>RMS</sub> |
| SNR                              | Signal to Noise Ratio     | A-weighted, no load, silence input                               |     | 96    |     | dB               |
| DR                               | Dynamic Range             | A-weighted, no load, -60dB FS 1kHz (FS) input                    |     | 95    |     | dB               |
| THD                              | Total Harmonic Distortion | no load, 1kHz 1V <sub>RMS</sub> input                            |     | -86   |     | dB               |
|                                  |                           | P <sub>out</sub> =20mW, R=32Ω, 1kHz 1V <sub>RMS</sub> (FS) input |     | -75   |     | dB               |
|                                  |                           | P <sub>out</sub> =40mW, R=16Ω, 1kHz 1V <sub>RMS</sub> (FS) input |     | -69   | -60 | dB               |
| CS                               | Channel Separation        | R <sub>L</sub> = 32Ω                                             |     | 70    |     | dB               |
|                                  |                           | R <sub>L</sub> = 16Ω                                             |     | 62    |     | dB               |
| <b>Line Input to SP Output</b>   |                           |                                                                  |     |       |     |                  |
| FS                               | Full Scale Output         | R <sub>L</sub> = 32Ω, 1kHz 1V <sub>RMS</sub> (FS) input          |     | 1.708 |     | V <sub>RMS</sub> |
|                                  |                           | R <sub>L</sub> = 16Ω, 1kHz 1V <sub>RMS</sub> (FS) input          |     | 1.690 |     | V <sub>RMS</sub> |
|                                  |                           | R <sub>L</sub> = 4Ω, 1kHz 1V <sub>RMS</sub> (FS) input           |     | 1.524 |     | V <sub>RMS</sub> |
| SNR                              | Signal to Noise Ratio     | A-weighted, no load, silence input                               |     | 94    |     | dB               |
| THD                              | Total Harmonic Distortion | no load, 1kHz 1V <sub>RMS</sub> (FS) input                       |     | -86   |     | dB               |
| CS                               | Channel Separation        | R <sub>L</sub> = 32Ω                                             |     | 70    |     | dB               |

| Symbol                          | Parameter                 | Notes                                    | Min | Typ | Max | Unit |
|---------------------------------|---------------------------|------------------------------------------|-----|-----|-----|------|
| <b>MIC Input to ADC Output</b>  |                           |                                          |     |     |     |      |
| SNR                             | Signal to Noise Ratio     | A-weighted, no load, silence input       |     | 74  |     | dB   |
| DR                              | Dynamic Range             | A-weighted, no load, -60dB FS 1kHz input |     | 73  |     | dB   |
| THD                             | Total Harmonic Distortion | 1kHz 53mV <sub>RMS</sub> (FS) input      |     | -61 |     | dB   |
| <b>Line Input to ADC Output</b> |                           |                                          |     |     |     |      |
| SNR                             | Signal to Noise Ratio     | A-weighted, no load, silence input       |     | 83  |     | dB   |
| DR                              | Dynamic Range             | A-weighted, no load, -60dB FS 1kHz input |     | 82  |     | dB   |
| THD                             | Total Harmonic Distortion | 1kHz, 1V <sub>RMS</sub> , -3dB FS input  |     | -62 |     | dB   |

BVDD = 3.3V, T<sub>A</sub> = 25°C, f<sub>s</sub> = 48kHz, R<sub>L</sub> = 10kΩ unless otherwise mentioned

## 7 Detailed Functional Descriptions

This chapter contains detailed functional descriptions of all modules of the chip. Central microcontroller is an ARM-9, all peripherals are connected to the AMBA bus which is divided into a AHB (advanced high speed bus) and APB (advanced peripheral bus) part. All audio, power management and system monitoring functions are controlled via an I2C interface (I2C audio master). This chapter includes also all detailed descriptions and performance values for these parts.

### 7.1 ARM922-T Processor Core

#### 7.1.1 General

The ARM922T macrocell is a high-performance 32-bit RISC integer processor combining an ARM9TDMI™ processor core with:

- 8KB instruction cache and 8 KB data cache
- Instruction and data Memory Management Unit (MMU)
- Write buffer with 16 data words and 4 addresses
- Advanced Microprocessor Bus Architecture (AMBA™) AHB interface

The ARM922T provides a high-performance processor solution for open systems requiring full virtual memory management and sophisticated memory protection. The ARM922T processor core is capable of running at 250 MHz. The ARM922T hard macrocell has a very low power consumption. The integrated cache helps to significantly reduce memory bandwidth demands, improving performance and minimizing power consumption.

At 250 MHz the ARM922T consumes as little as 65 mW, making it ideal for high-performance battery operated audio or video applications.

The ARM core and associated bus structures are configured for little endian byte order (compatible with Windows CE™ and Symbian™ OS).

Table 10 ARM 922T characteristics

| Cache (I/D) | MMU | AHB | Thumb | mW/MHz       | MHz |
|-------------|-----|-----|-------|--------------|-----|
| 8KB / 8KB   | yes | yes | yes   | 0.25 @ 1.2 V | 250 |

#### Features

- 32-bit RISC architecture (ARMv4T)
- Harvard architecture with separated instruction (I) and data (D) caches with 8 KB each and 8-word line length
- Five stage pipeline (fetch, decode, execute, memory, write back) enabling high master clock speeds
- 32-bit ARM instruction set for maximum performance and flexibility
- 16-bit Thumb instruction set for increased code density
- Enhanced ARM architecture V4 MMU to provide translation and access permission checks for instruction and data addresses. With this MMU different operating systems (Windows CE, Symbian ...) can be implemented.
- Industry standard AMBA bus interface (AHB and APB)
- Hard-macro implementation
- The processor core clock frequency (FCLK) is programmable up to 250MHz and the ARM922 power consumption is directly proportional to this clock frequency FCLK

### 7.1.2 Block Diagrams

Figure 4 ARM 922T Functional Block Diagram

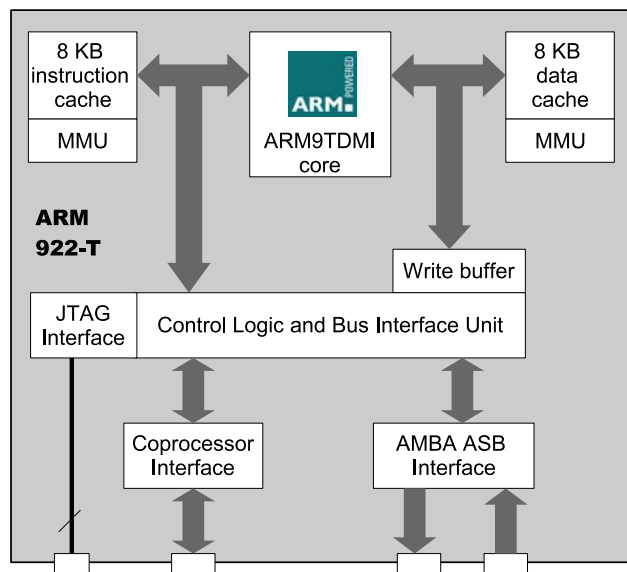
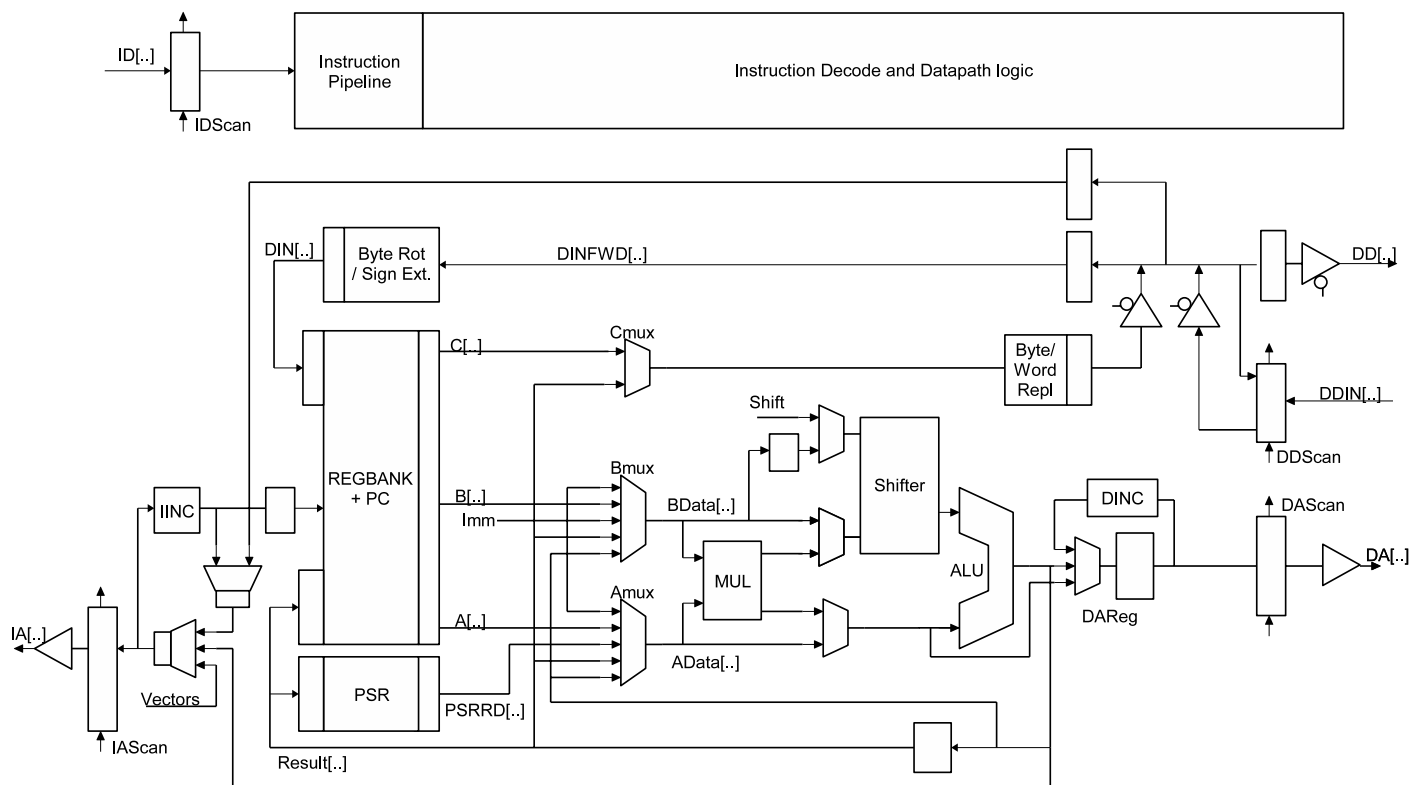


Figure 5 ARM9TDMI Functional Block Diagram



### 7.1.3 ARM922T Details

The ARM922T macrocell is based on the ARM9TDMI Harvards architecture processor core with an efficient five-stage pipeline. To reduce the effect of memory bandwidth and latency on performance, the ARM922T macrocell includes separate caches and MMUs for both instructions and data. It also has a write buffer and physical address TAG RAM.

#### Caches

Two 8KB caches are implemented, one for instructions, the other for data, both with an 8-word line size. Separate buses connect each cache to the ARM9TDMI core permitting a 32 bit instruction to be fetched and fed into the Decode stage of the pipeline at the same time as a 32 bit data access for the memory stage of the pipeline.

Cache lock-down is provided to permit critical code sequences to be locked into the cache to ensure predictability for real-time code. The cache replacement algorithm can be selected by the operating system as either pseudo-random or round-robin. Both caches are 64-way set-associative. Lock-down operates on a per-way basis.

#### Write Buffer

The ARM922T macrocell also incorporates a 16-data, 4-address write buffer to avoid stalling the processor when writes to external memory are performed.

#### PA TAG RAM

The ARM922T macrocell implements a physical address TAG RAM (PA TAG RAM) to perform write-backs from the data cache.

The physical addresses of all the lines held in the data cache are stored by the PA TAG memory, removing the requirement for address translation when evicting a line from the cache.

#### MMU

The ARM922T macrocell implements an enhanced ARMv4 MMU to provide translation and access permission checks for the instruction and data address ports of the ARM9TDMI core.

The MMU features are:

- Standard ARMv4 MMU mapping sizes, domains, and access protection scheme
- Mapping sizes are 1 MB sections, 64 KB large pages, 4 KB small pages, and new 1KB tiny pages
- Access permissions for sections
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpages)
- Access permissions for tiny pages
- 16 domains implemented in hardware
- 64-entry instruction Translation-Lookaside-Buffer (TLB) and 64-entry data TLB
- Hardware page table walks
- Round-robin replacement algorithm (also called cyclic)

### Control Coprocessor (CP15)

The control coprocessor is provided for configuration of the caches, the write buffer, and other ARM922T options.

Eleven registers are available for program control:

- Register 1 controls system operation parameters including endianness, cache, and MMU enable
- Register 2 and 3 configure and control MMU functions
- Register 5 and 6 provide MMU status information
- Register 7 and 9 are used for cache maintenance operations
- Register 8 and 10 are used for MMU maintenance operations
- Register 13 is used for fast context switching
- Register 15 is used for test.

#### Debug Features

The ARM9TDMI processor core incorporates an EmbeddedICE unit and EmbeddedICE-RT logic permitting both software tasks and external debug hardware to

- Set hardware and software breakpoints
- Perform single-stepping
- Enable access to registers and memory

This functionality is implemented as a coprocessor and is accessible from hardware through the JTAG port.

Full-speed, real-time execution of the processor is maintained until a breakpoint is hit.

At this point control is passed either to a software handler or to JTAG control.

### 7.1.4 ARM V4T Architecture

The ARM9TDMI processor core implements the ARMv4T Instruction Set Architecture (ISA). The ARMv4T ISA is a superset of the ARMv4 ISA with additional support for the Thumb 16-bit compressed instruction set.

#### Performance and Code Density

The ARM9TDMI core executes two instruction sets

- 32-bit ARM instruction set
- 16-bit Thumb instruction set

The ARM instruction set is designed so that a program can achieve maximum performance with the minimum number of instructions. Most ARM9TDMI instructions are executed in a single cycle.

The simpler Thumb instruction set offers much increased code density deducing code size and memory requirement.

Code can switch between the ARM and Thumb instruction sets on any procedure call.

#### ARM9TDMI Integer Pipeline Stages

The integer pipeline consists of five stages to maximize instruction throughput in the ARM9TDMI core:

- Fetch
- Decode and register read
- Execute shift and ALU operation, or address calculate, or multiply
- Memory access and multiply
- Write register

By using a five-stage pipeline, the ARM922T delivers a throughput approaching one instruction per cycle.

## Registers

The ARM9TDMI processor core consists of a 32-bit datapath and associated control logic. This datapath contains 31 general-purpose registers, coupled to a full shifter, Arithmetic Logic Unit, and a multiplier. At any one time 16 registers are visible to the user. The remainder are mode-specific replacement registers (banked registers) used to speed up execution processing, and make nested exceptions possible.

Register 15 is the Program Counter (PC) that can be used in all instructions to reference data relative to the current instruction. R14 holds the return address after a subroutine call. R13 is used (by software convention) as a stack pointer.

## Exception Types/Modes

The ARM9TDMI core supports five types of exception, and a privileged processing mode for each type. The types of exceptions are:

- Fast interrupt (FIQ)
- Normal interrupt (IRQ)
- Memory aborts (used to implement memory protection or virtual memory)
- Attempted execution of an undefined instruction
- Software interrupts (SWIs)

All exceptions have banked registers for R14 and R13. After an exception, R14 holds the return address for exception processing. This address is used both to return after the exception is processed and to address the instruction that caused the exception.

R13 is banked across exception modes to provide each exception handler with a private stack pointer. The fast interrupt mode also banks registers 8 to 12 so that interrupt processing can begin without the need to save or restore these registers.

A seventh processing mode, System mode, uses the User mode registers. System mode runs tasks that require a privileged processor mode and enables them to invoke all classes of exceptions.

## Status Registers

All other processor states are held in status registers. The current operating processor status is in the Current Program Status Register (CPSR). The CPSR holds:

- Four ALU flags (Negative, Zero, Carry, Overflow)
- An interrupt disable bit for each of the IRQ and FIQ interrupts
- A bit to indicate ARM or Thumb execution state
- Five bits to encode the current processor mode

All five exception modes also have a Saved Program Status Register (SPSR) that holds the CPSR of the task immediately before the exception occurred.

## Conditional Execution

All ARM instructions can be executed conditionally and can optionally update the four condition code flags (Negative, Zero, Carry, and Overflow) according to their result. Fifteen conditions are implemented.

## Classes of Instructions

The ARM and Thumb instruction sets can be divided into four broad classes of instruction:

- Data processing instructions
- Load and store instructions
- Branch instructions
- Coprocessor instructions

## Data Processing Instructions

The data processing instructions operate on data held in general-purpose registers. Of the two source operands, one is always a register. The other has two basic forms:

- An immediate value
- A register value optionally shifted

If the operand is a shifted register, the shift can be an immediate value or the value of another register. Four types of shift can be specified. Most data processing instructions can perform a shift followed by a logical or arithmetic operation.

There are two classes of multiply instructions:

- Normal, 32 bit result
- Long, 64 bit result variants.

Both types of multiply instruction can optionally perform an accumulate operation

## Load and Store Instructions

There are two main types of load and store instructions:

- Load or store the value of a single register
- Load or store multiple register values

Load and store single register instructions can transfer a 32-bit word, a 16-bit halfword, or an 8-bit byte between memory and a register. Byte and halfword loads can be automatically zero extended or sign extended as they are loaded. These instructions have three primary addressing modes:

- Offset
- Pre-indexed
- Post-indexed

The address is formed by adding an immediate, or register-based, positive, or negative offset to a base register. Register-based offsets can also be scaled with shift operations. Pre-indexed and post-indexed addressing modes update the base registers with the base plus offset calculation.

As the PC is a general-purpose register, a 32-bit value can be loaded directly into the PC to perform a jump to any address in the 4GB memory space.

Load and store multiple instructions perform a block transfer of any number of the general purpose registers to, or from, memory. Four addressing modes are provided:

- Pre-increment addressing
- Post-increment addressing
- Pre-decrement addressing
- Post-decrement addressing

The base address is specified by a register value (that can be optionally updated after the transfer). As the subroutine return address and the PC values are in general-purpose registers, very efficient subroutine calls can be constructed.

## Branch Instructions

As well as letting data processing or load instructions change control flow (by writing the PC) a standard branch instruction is provided with 24-bit signed offset, providing for forward and backward branches of up to 32 MB.

A branch with link (BL) instruction enables efficient subroutine calls. BL preserves the address of the instruction after the branch in R14 (Link register or LR). This lets a move instruction put the LR in to the PC and return to the instruction after the branch.

The branch and exchange (BX) instruction switches between ARM and Thumb instruction sets with the return address optionally preserving the operating mode of the calling subroutine.

## Coprocessor Instructions

There are three types of coprocessor instructions:

- Coprocessor data processing instructions
- Coprocessor register transfer instructions
- Coprocessor data transfer instructions

## 7.1.5 JTAG Interface

The ARM933T debug interface is based on IEEE Std. 1149.1- 1990, standard test access port. The ARM922T contains hardware extensions for advanced debugging features. These are intended to ease the development of application software.

The debug extensions allow the core to be stopped by one of the following:

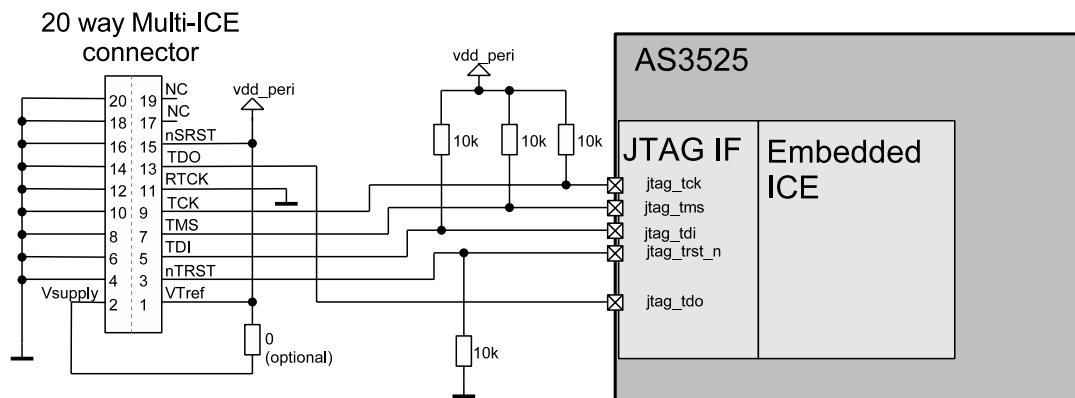
- A given instruction fetch (breakpoint)
- A data access (watchpoint)
- Asynchronously by a debug request

When this happens, the ARM922T is said to be in debug state. At this point, you can examine the internal state of the core and the external state of the system. When examination is complete, you can restore the core and system state and resume program execution.

Normally, all control for debugging is done by running a debugger software (ARM AXD or ARM Realview Debugger) on a debug host PC. Connection to the chip is done by an ARM Multi-ICE interface, which connects either to the parallel port or the USB port of the debug host PC.

The connection to the multi-ICE interface is done via a 20 way connector and ribbon cable. Following diagram shows the signals connections of the AS3525 to this ICE connector.

Figure 6 Interface connector to multi-ICE



## 7.1.6 Boot Concept

It can be selected if the system should boot either using the internal ROM (internal boot loader) or an external ROM/Flash (connected to the MPMC interface). XPC[0] is read within global chip reset to do the selection of either internal or external boot.

Table 11 Boot definitions for internal/external boot selection

| XPC[0] | Booting Option     |
|--------|--------------------|
| 1      | Internal ROM       |
| 0      | External ROM/Flash |

### 7.1.6.1 Internal Bootloader Version C22

Within the internal ROM boot loader several options for booting can be selected:

- SSP IF - SPI master for ST serial flash types
- SSP IF - SPI slave
- NandFlash
- Debug UART diagnostics
- IDE boot: direct boot from harddisk
- USB boot promer. In the case that a USB connection is present and either an update button is pressed or there is no bootable device, the USB promer is started (see Figure 7 Boot decision between normal boot and USB boot promer" for details). The USB boot promer allows update of the firmware by using an USB mass storage class device. This update can be used either for initial programming (factory programming) or as mechanism for an in-field firmware update.

All boot loader options of the internal bootloader are configured by XPC[3:1] pins. External pull-up or pull-down resistors should be used to configure the boot options.

Table 12 Boot definitions Chip version C22

| XPC[3:1] | Boot Device                                       |
|----------|---------------------------------------------------|
| 0 000    | SPI master ST M25Pxx serial Nor Flash             |
| 1 001    | SPI master Atmel AT45DB011B serial Nor Flash      |
| 2 010    | SPI slave                                         |
| 3 011    | NandFlash                                         |
| 4 100    | IDE                                               |
| 5 101    | reserved for developers mode                      |
| 6 110    | UART / Command Line Interface without diagnostics |
| 7 111    | UART / Command Line Interface with diagnostics    |

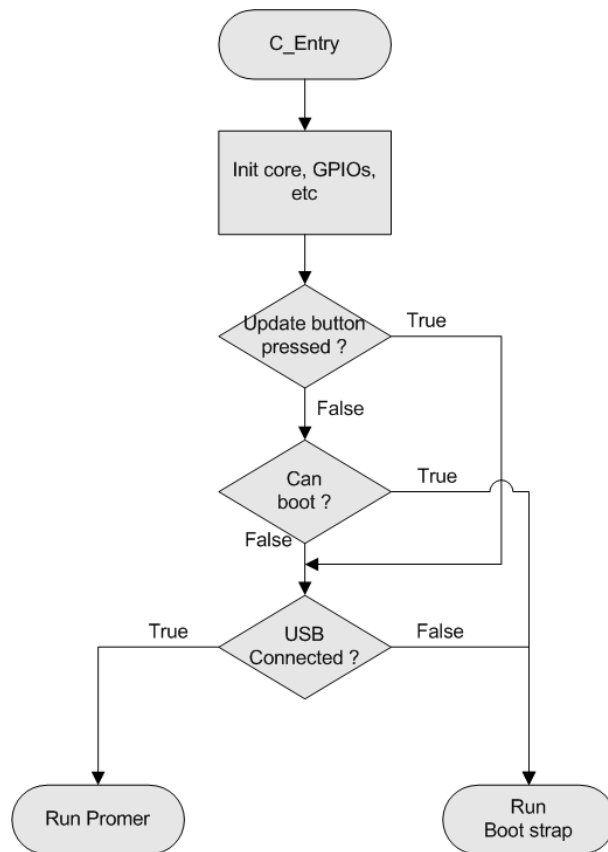
The update button is located between xpa[4] and xpa[0]. Within the key scan routine, xpa[4] is driven shortly to each logic level "0" and "1" and the value of xpa[0] is read back to sense a keypress of the update button.

For the USB promer, it is necessary that frequency settings defining the quartz crystal frequency are defined by the pins xpa[6:4]. For details refer to "Table 13 USB promer frequency settings". These settings are read at the beginning in the initialisation routine of the bootloader.

Table 13 USB promer frequency settings

| XPA[6:4] | USB promer frequency settings |
|----------|-------------------------------|
| 000      | 24 MHz                        |
| 001      | 20 MHz                        |
| 010      | 13 MHz                        |
| 011      | 12 MHz                        |
| 100      | 10 MHz                        |
| others   | reserved / defaults to 24 MHz |

Figure 7 Boot decision between normal boot and USB boot promoter



## 7.2 AHB Peripheral Blocks

ARM AHB ("advanced high-performance bus") is the new generation of AMBA bus, which is intended to address the requirements of high-performance synthesizable designs. AMBA AHB implements the features required for high performance, high clock frequency systems including:

- burst transfers
- split transactions
- single cycle bus master handover
- non-tristate implementation
- 32 bit bus width
- the clock frequency of the AHB can set by software up to 65MHz

### 7.2.1 2.5 MBIT RAM Main Memory

The memory subsystem consists of a RAM part and a ROM part.

Within the RAM memory subsystem, following functions are included:

- 1-TRAM controller with AHB bus slave interface
- 1-TRAM memory macros

#### 7.2.1.1 1-TRAM Controller

The 1T RAM Controller is a slave interface connected to the AMBA AHB bus.

- slave AHB interface
- supports byte(8 bit), half-word(16 bit) and word(32 bit) read/write accesses
- 128-bit Line Buffer as temporary storage to reduce the number of memory accesses and optimise power consumption
- controls 5TSMC 1T-RAM instances

#### 7.2.1.2 On-Chip 1T-RAM macro blocks

TSMC Emb1tRAM™ technology is a special kind of DRAM, which is implemented in a logic CMOS process. This innovative concept and design guarantees lowest power, high density, high performance and high yield advantages.

ECC (Error Correction Code) technique is applied in the macro to dynamically correct errors caused by hard defects or soft errors. No fuses are needed because the conventional redundancy scheme is replaced with ECC design in the macro.

The macro can be operated at clock rate from 20 MHz up to maximum AHB bus clock frequency in flow through random access mode. In the product, one idle cycle for refresh is needed in every 32 clock cycles.

Total 5 macros with organisation of 4Kx128 = 64 KByte each are implemented. For the refresh, one master macro is generating the refresh clock (T1F4Kx128\_PIFE) and four macros are connected serially in slave mode to the refresh clock (T1F4Kx128PIFES).

#### Features

- 20 Mhz to 65 Mhz operation speed
- Flow through random access
- Built-in error correction (ECC)
- 128-bit wide data bus
- Separated data in/out bus
- SRAM-style interface operation
- Built-in refresh controller with refresh clock generator



### 7.2.3.2 VIC Interrupt Sources

Table 14 VIC Interrupt Sources

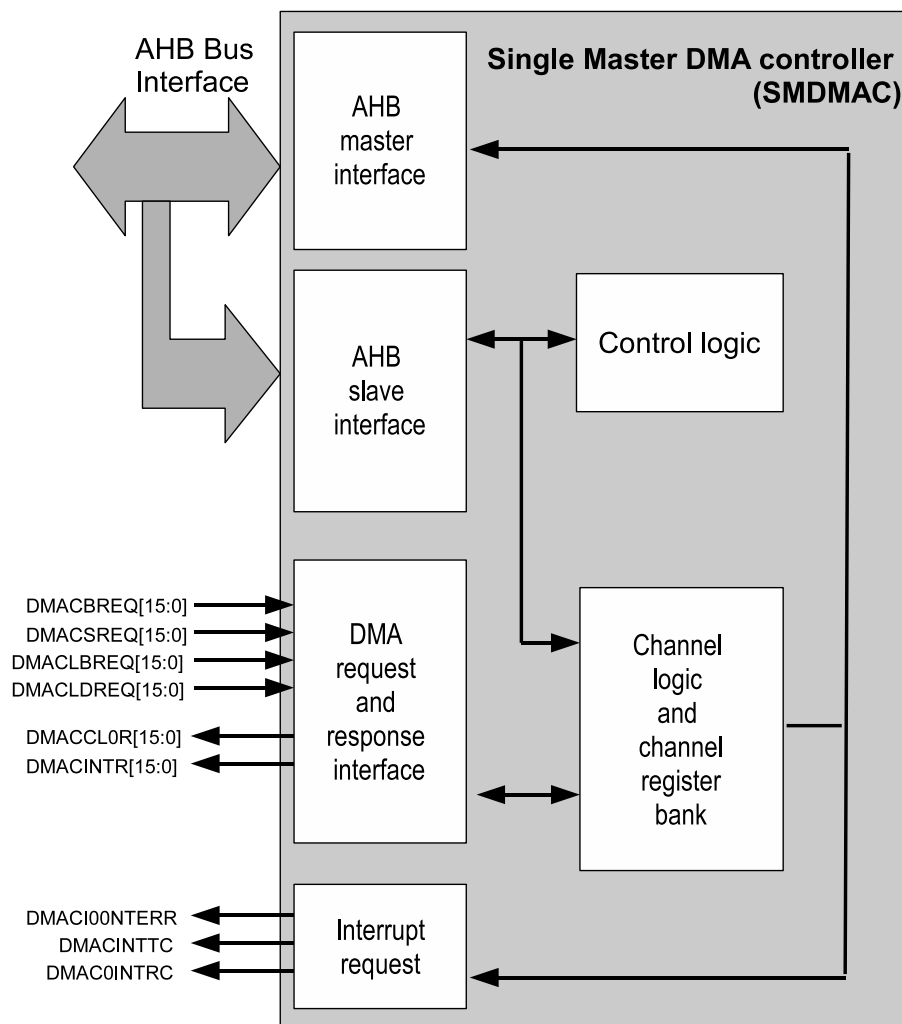
| IRQ Source | Module     | IRQ Source | Module       |
|------------|------------|------------|--------------|
| 0          | Watchdog   | 16         | GPIO4 (XPD)  |
| 1          | Timer 1    | 17         | -            |
| 2          | Timer 2    | 18         | CGU          |
| 3          | USB        | 19         | Memory Stick |
| 4          | DMAC       | 20         | DBOP         |
| 5          | Nand Flash | 21         | -            |
| 6          | IDE        | 22         | -            |
| 7          | MCI INTR0  | 23         | -            |
| 8          | MCI INTR1  | 24         | -            |
| 9          | AUDIO IRQ  | 25         | -            |
| 10         | SSP        | 26         | -            |
| 11         | I2C MS     | 27         | -            |
| 12         | I2C Audio  | 28         | -            |
| 13         | I2SIN      | 29         | GPIO1 (XPA)  |
| 14         | I2SOUT     | 30         | GPIO2 (XPB)  |
| 15         | UART       | 31         | GPIO3 (XPC)  |

## 7.2.4 SMDMAC - Single master DMAC

The ARM PrimeCell™ PL081 “SMDMAC single master DMA controller” is included in the AHB system.

- AMBA specification Rev 2.0 compliant
- two DMA channels. Each channel can support a unidirectional transfer
- provides 16 peripheral DMA request lines
- single DMA and burst DMA request signals. Each peripheral connected to the PrimeCell™ SMDMAC can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the PrimeCell™ SMDMAC
- Memory-to-Memory, memory-to-peripheral, peripheral-to-memory and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not need to occupy contiguous areas of memory
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The PrimeCell™ SMDMAC is programmed by writing to the DMA control registers over the AHB slave interface
- One AHB bus master for transferring data. This interface is used to transfer data when a DMA request goes active.

Figure 9 SMDMAC Block Diagram



## 7.2.4.1 DMAC Registers

Table 15 DMAC Registers

| Register Name          | Base Address    | Offset | Note                                         |
|------------------------|-----------------|--------|----------------------------------------------|
| DMAC_IntStatus         | AS3525_DMACHASE | 0x000  | Interrupt status register                    |
| DMAC_IntTCStatus       | AS3525_DMACHASE | 0x004  | Interrupt terminal count status register     |
| DMAC_IntTCClear        | AS3525_DMACHASE | 0x008  | Interrupt terminal count clear register      |
| DMAC_IntErrorStatus    | AS3525_DMACHASE | 0x00C  | Interrupt error status register              |
| DMAC_IntErrorClear     | AS3525_DMACHASE | 0x010  | Interrupt error clear register               |
| DMAC_RawIntTCStatus    | AS3525_DMACHASE | 0x014  | Raw interrupt terminal count status register |
| DMAC_RawIntErrorStatus | AS3525_DMACHASE | 0x018  | Raw interrupt error status register          |
| DMAC_SoftBReq          | AS3525_DMACHASE | 0x020  | Software burst request register              |
| DMAC_SoftSReq          | AS3525_DMACHASE | 0x024  | Software single request register             |
| DMAC_SoftLBReq         | AS3525_DMACHASE | 0x028  | Software last burst request register         |
| DMAC_SoftSBReq         | AS3525_DMACHASE | 0x02C  | Software last single request register        |
| DMAC_Configuration     | AS3525_DMACHASE | 0x030  | Configuration register                       |
| DMAC_Sync              | AS3525_DMACHASE | 0x034  | Synchronisation register                     |
| DMAC_C0SrcAddr         | AS3525_DMACHASE | 0x100  | Channel 0 source address                     |
| DMAC_C0DestAddr        | AS3525_DMACHASE | 0x104  | Channel 0 destination address                |
| DMAC_C0LLI             | AS3525_DMACHASE | 0x108  | Channel 0 linked list item register          |
| DMAC_C0Control         | AS3525_DMACHASE | 0x10C  | Channel 0 control register                   |
| DMAC_C0Configuration   | AS3525_DMACHASE | 0x110  | Channel 0 configuration register             |
| DMAC_C1SrcAddr         | AS3525_DMACHASE | 0x120  | Channel 1 source address                     |
| DMAC_C1DestAddr        | AS3525_DMACHASE | 0x124  | Channel 1 destination address                |
| DMAC_C1LLI             | AS3525_DMACHASE | 0x128  | Channel 1 linked list item register          |
| DMAC_C1Control         | AS3525_DMACHASE | 0x12C  | Channel 1 control register                   |
| DMAC_C1Configuration   | AS3525_DMACHASE | 0x130  | Channel 1 configuration register             |
| DMAC_PeripheralId0     | AS3525_DMACHASE | 0xFE0  | peripheral ID0 register                      |
| DMAC_PeripheralId1     | AS3525_DMACHASE | 0xFE4  | peripheral ID1 register                      |
| DMAC_PeripheralId2     | AS3525_DMACHASE | 0xFE8  | peripheral ID2 register                      |
| DMAC_PeripheralId3     | AS3525_DMACHASE | 0xFEC  | peripheral ID3 register                      |
| DMAC_CellId0           | AS3525_DMACHASE | 0xFF0  | peripheral cell ID0 register                 |
| DMAC_CellId1           | AS3525_DMACHASE | 0xFF4  | peripheral cell ID1 register                 |
| DMAC_CellId2           | AS3525_DMACHASE | 0xFF8  | peripheral cell ID2 register                 |
| DMAC_CellId3           | AS3525_DMACHASE | 0xFFC  | peripheral cell ID3 register                 |

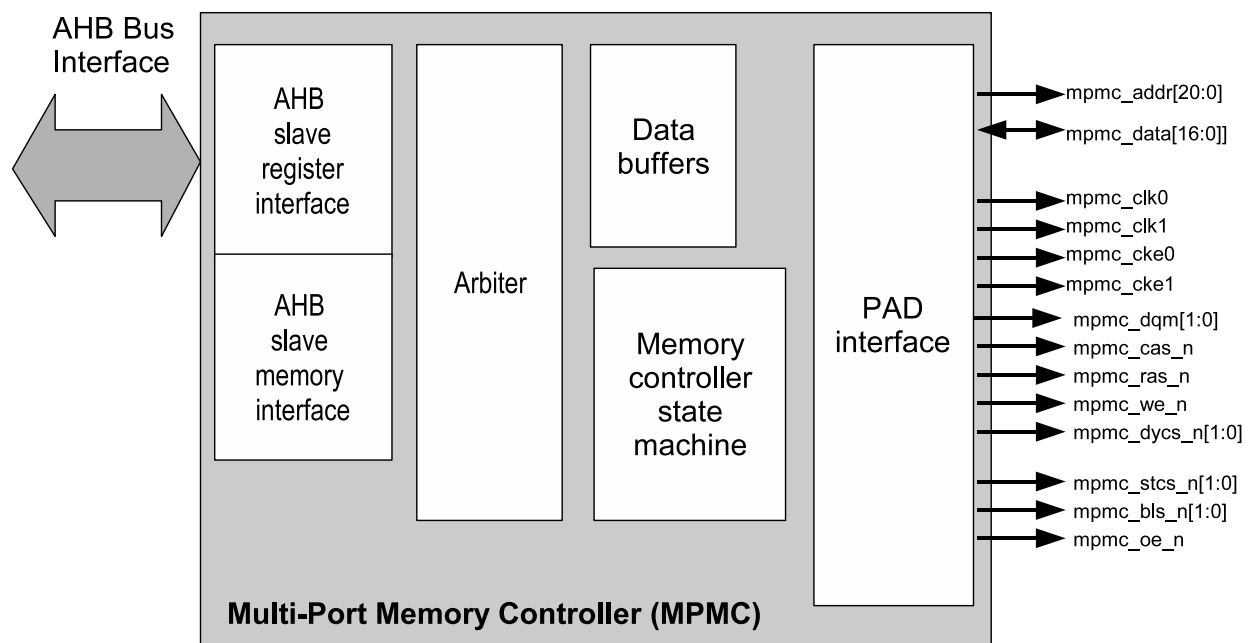
## 7.2.5 Multi Port Memory Controller (MPMC)

The MPMC block is integrated into the AMBA system through AHB slave port.

The PrimeCell™ MPMC offers:

- AMBA 32-bit AHB compliance.
- Dynamic memory interface support including SDRAM and JEDEC low-power SDRAM
- Asynchronous static memory device support including RAM, ROM, and Flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- Single AHB interface for accessing external memory.
- 8-bit and 16-bit wide static memory support.
- 16-bit wide chip select SDRAM memory support.
- Static memory features include:
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround delay
  - output enable, and write enable delays
  - extended wait
- Two chip selects for synchronous memory and two chip selects for static memory devices.
- Software controllable HCLK to MPMCCLKOUT ratio.
- Power-saving modes dynamically control SDRAM MPMCCKEOUT and MPMCCLKOUT.
- Dynamic memory self-refresh mode supported by software.
- Controller supports 2K, 4K, and 8K row address synchronous memory parts. That is typical 512MB, 256MB, 128MB, and 16Mb parts, with 8, 16 bits per device.
- Two reset domains enable dynamic memory contents to be preserved over a soft reset.
- A separate AHB interface to program the MPMC. This enables the PrimeCell™ MPMC registers to be situated in memory with other system peripheral registers.
- Locked AHB transactions supported.
- Support for all AHB burst types.

Figure 10 Multi Port Memory Controller Block Diagram



## 7.2.6 IDE Interface

**Note:** The IDE interface is only available on AS3525-A, not for AS3525-B because some of the IDE PINs are not bonded within the AS3525-B package variant.

The IDE host interface core provides an efficient and easy-to-use interface to IDE and ATAPI devices. The core implements programmable I/O, Multi-word DMA, and Ultra ATA-33, -66, -100 and -133 modes of operation and supports up to two devices. The core interface to the system-on-chip provides PIO access and DMA capability to optimise data transfers to and from the IDE devices. For ease of integration, this interface includes a register set compatible with the Intel chip set, including a descriptor-based scatter-gather DMA core. This core is compatible with ATA-4 with Ultra ATA-33, -66, -100 and -133 extensions. Single-word DMA is not supported.

The licensed SpeedSelect™ technology allows the core to be reconfigured to support any timing mode for PIO, Multi-Word DMA, and Ultra ATA transfers (-33, -66, -100 or -133) while running at any clock frequency. Interface to the host processor is the AMBA AHB bus architecture.

There are two AHB interfaces on the core: an AHB master and an AHB slave.

### 7.2.6.1 AHB Master Interface

The AHB Master implements a subset of the AHB protocol. The following features are supported:

- Single transfer, unspecified-length, 4-beat incrementing and optionally 8-beat incrementing bursts (HBURST will be '000', '001', '011', or optionally '101')
- Accesses that cross a 1kB boundary will be unspecified-length incrementing (HBURST will be '001')
- 16-bit and 32-bit transfers only (HSIZE will only be '001' or '010')
- BUSY cycles are not issued (HTRANS will not be '01')
- HPROT is not implemented
- OKAY, SPLIT and RETRY responses accepted (HRESP may be '00', '10' or '11')
- HLOCK asserted during fixed-length bursts
- The AHB master may be granted by default

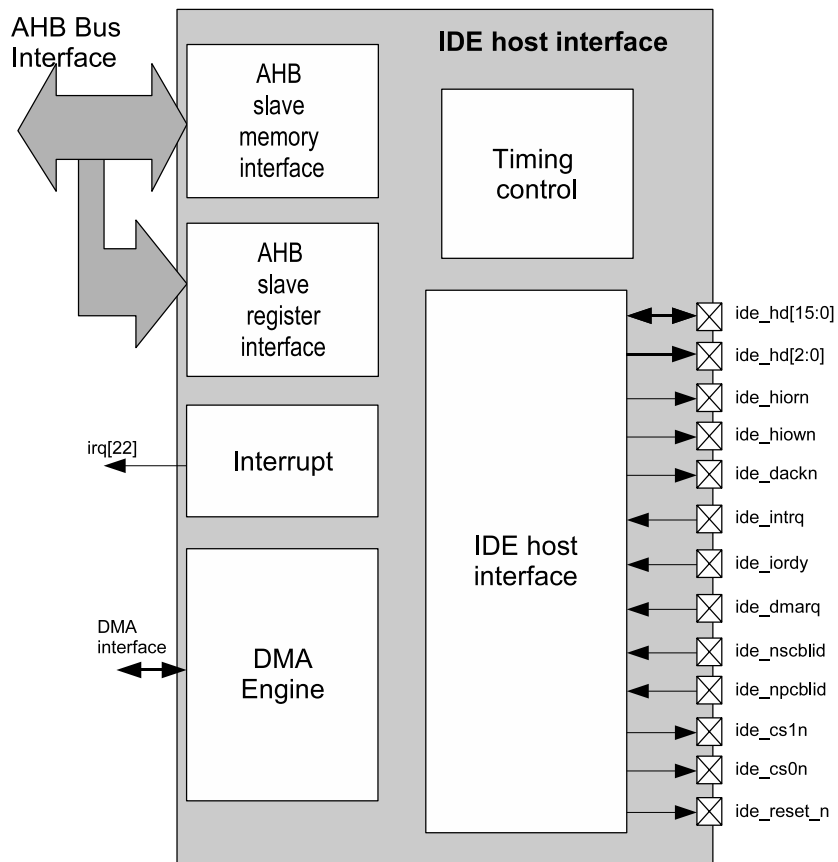
### 7.2.6.2 AHB Slave Interface

The AHB Slave implements a subset of the AHB protocol. The following features are supported:

- Non-burst only (HBURST must be '000')
- 8-, 16-, or 32-bit transfers only (HSIZE must be '000', '001' or '010')
- No advantage is gained by issuing a SEQ cycle over a NONSEQ cycle (HTRANS values of '10' and '11' are interpreted identically)
- HPROT is ignored
- HRESP is '00' (OKAY)
- HREADY is issued no sooner than 2 clock cycles after a valid SEQ or NONSEQ cycle
- The AHB slave may be selected by default

### 7.2.6.3 IDE Block diagram

Figure 11 IDE Block Diagram



## 7.2.6.4 IDE Interface Registers

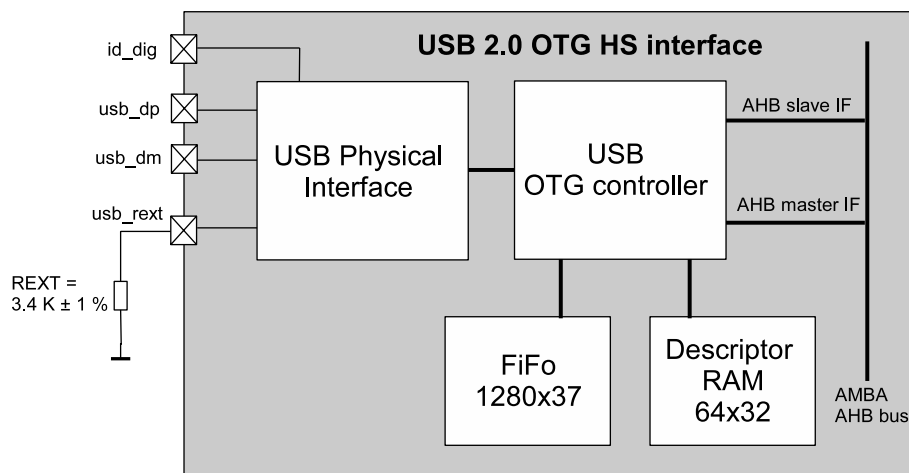
Table 16 IDE Interface Registers

| Register Name              | Base Address       | Offset | Note                                        |
|----------------------------|--------------------|--------|---------------------------------------------|
| IdeReg_BMICP               | AS3525_CF_IDE_BASE | 0x00   | primary channel bus master command          |
| IdeReg_BMISP               | AS3525_CF_IDE_BASE | 0x02   | primary channel bus master status           |
| IdeReg_BMIDTPP_LO          | AS3525_CF_IDE_BASE | 0x04   | primary channel bus master table pointer    |
| IdeReg_BMIDTPP_HI          | AS3525_CF_IDE_BASE | 0x06   |                                             |
| IdeReg_IDETIMP_LO          | AS3525_CF_IDE_BASE | 0x40   | primary channel timing register             |
| IdeReg_IDETIMP_HI          | AS3525_CF_IDE_BASE | 0x41   |                                             |
| IdeReg_IDETIMS_LO          | AS3525_CF_IDE_BASE | 0x42   | secondary channel timing register           |
| IdeReg_IDETIMS_HI          | AS3525_CF_IDE_BASE | 0x43   |                                             |
| IdeReg_SIDETIM             | AS3525_CF_IDE_BASE | 0x44   | slave IDE timing register                   |
| IdeReg_SLEWCTL_LO          | AS3525_CF_IDE_BASE | 0x45   | slew rate control register                  |
| IdeReg_SLEWCTL_HI          | AS3525_CF_IDE_BASE | 0x46   |                                             |
| IdeReg_IDESTAT             | AS3525_CF_IDE_BASE | 0x47   | IDE status register                         |
| IdeReg_UDMACTL             | AS3525_CF_IDE_BASE | 0x48   | ultra DMA control register                  |
| IdeReg_UDMATIM_LO          | AS3525_CF_IDE_BASE | 0x4A   | ultra DMA timing register                   |
| IdeReg_UDMATIM_HI          | AS3525_CF_IDE_BASE | 0x4B   |                                             |
| IdeReg_MISCCTL             | AS3525_CF_IDE_BASE | 0x50   | miscellaneous control register              |
| IdeReg_REGSTB              | AS3525_CF_IDE_BASE | 0x54   | task file register strobe timing register   |
| IdeReg_REGRCVR             | AS3525_CF_IDE_BASE | 0x58   | task file register recovery timing register |
| IdeReg_DATSTB              | AS3525_CF_IDE_BASE | 0x5C   | data register PIO strobe timing register    |
| IdeReg_DATRCVR             | AS3525_CF_IDE_BASE | 0x60   | data register PIO recovery timing register  |
| IdeReg_DMASTB              | AS3525_CF_IDE_BASE | 0x64   | DMA strobe timing register                  |
| IdeReg_DMARCVR             | AS3525_CF_IDE_BASE | 0x68   | DMA recovery timing register                |
| IdeReg_UDMASTB             | AS3525_CF_IDE_BASE | 0x6C   | ultra DMA strobe timing register            |
| IdeReg_UDMATRP             | AS3525_CF_IDE_BASE | 0x70   | ultra DMA ready-to-stop timing register     |
| IdeReg_UDMATENV            | AS3525_CF_IDE_BASE | 0x74   | ultra DMA timing envelope register          |
| IdeReg_IORDYTMP            | AS3525_CF_IDE_BASE | 0x78   | primary IO ready timer configuration reg    |
| IdeReg_IORDYTMS            | AS3525_CF_IDE_BASE | 0x7C   | secondary IO ready timer configuration reg  |
| IdeTaskF_DATA              | AS3525_CF_IDE_BASE | 0x1F0  |                                             |
| IdeTaskF_ERR_FEAT          | AS3525_CF_IDE_BASE | 0x1F1  |                                             |
| IdeTaskF_SECT_CNT          | AS3525_CF_IDE_BASE | 0x1F2  |                                             |
| IdeTaskF_SECT_NUM          | AS3525_CF_IDE_BASE | 0x1F3  |                                             |
| IdeTaskF_CYL_LO            | AS3525_CF_IDE_BASE | 0x1F4  |                                             |
| IdeTaskF_CYL_HI            | AS3525_CF_IDE_BASE | 0x1F5  |                                             |
| IdeTaskF_DEV_HEAD          | AS3525_CF_IDE_BASE | 0x1F6  |                                             |
| IdeTaskF_STAT_CMD          | AS3525_CF_IDE_BASE | 0x1F7  |                                             |
| IdeTaskF_ALT_STAT_DEV_CTRL | AS3525_CF_IDE_BASE | 0x3F6  |                                             |
| IdeTaskF_DEV_ADDR          | AS3525_CF_IDE_BASE | 0x3F7  |                                             |

## 7.2.7 USB 2.0 HS OTG interface

The USB 2.0 on-chip interface includes the USB 2.0 On-The-Go Physical Interface and the HS OTG controller.

Figure 12 USB 2.0 Interface



### 7.2.7.1 HS OTG controller subsystem

The Synopsys HS OTG subsystem is a configurable design. The HS OTG subsystem is fully compliant with the On-The-Go supplement to the USB 2.0 specification, Revision 1.0a. The subsystem supports high speed (480-Mbps) and full-speed transfers. It is designed to interface to the AMBA AHB bus, shielding the application from the complexities of the HS OTG subsystem-native protocols and simplifying the system interface.

The OTG subsystem can be configured using application software as follows:

- OTG dual-role device (DRD)
- OTG device only
- OTG mini host only
- USB High-Speed (HS) device
- USB HS mini host
- USB Full-Speed (FS) device

The HS OTG subsystem has the following interfaces

- the UTMI+, which connect the on-chip PHY to the HS OTG core
- the AHB slave interface, which provides the microcontroller with read and write access to the core's control and status register (CSRs)
- the AHB master interface, which enables the core to act as a master on the AHB to transfer data to and from the core's DMA controller
- the descriptor prefetch buffer RAM interface, which connects to an single-port RAM for DMA descriptor prefetch buffer storage
- the data RAM interface, which connects to and dual-port RAM (FIFO memory) for transaction data storage

#### General features

- handles all clock synchronisation within the core
- uses a descriptor prefetch buffer for optimal AHB use in host mode
- supports adaptive buffering for dynamic FIFO memory allocation, avoiding gaps in RAM utilisation
- SOFs are supported in high/full speed modes
- includes built-in DMA
- includes hardware transaction scheduling for enhanced performance
- supports memory mapped address space for the CSRs

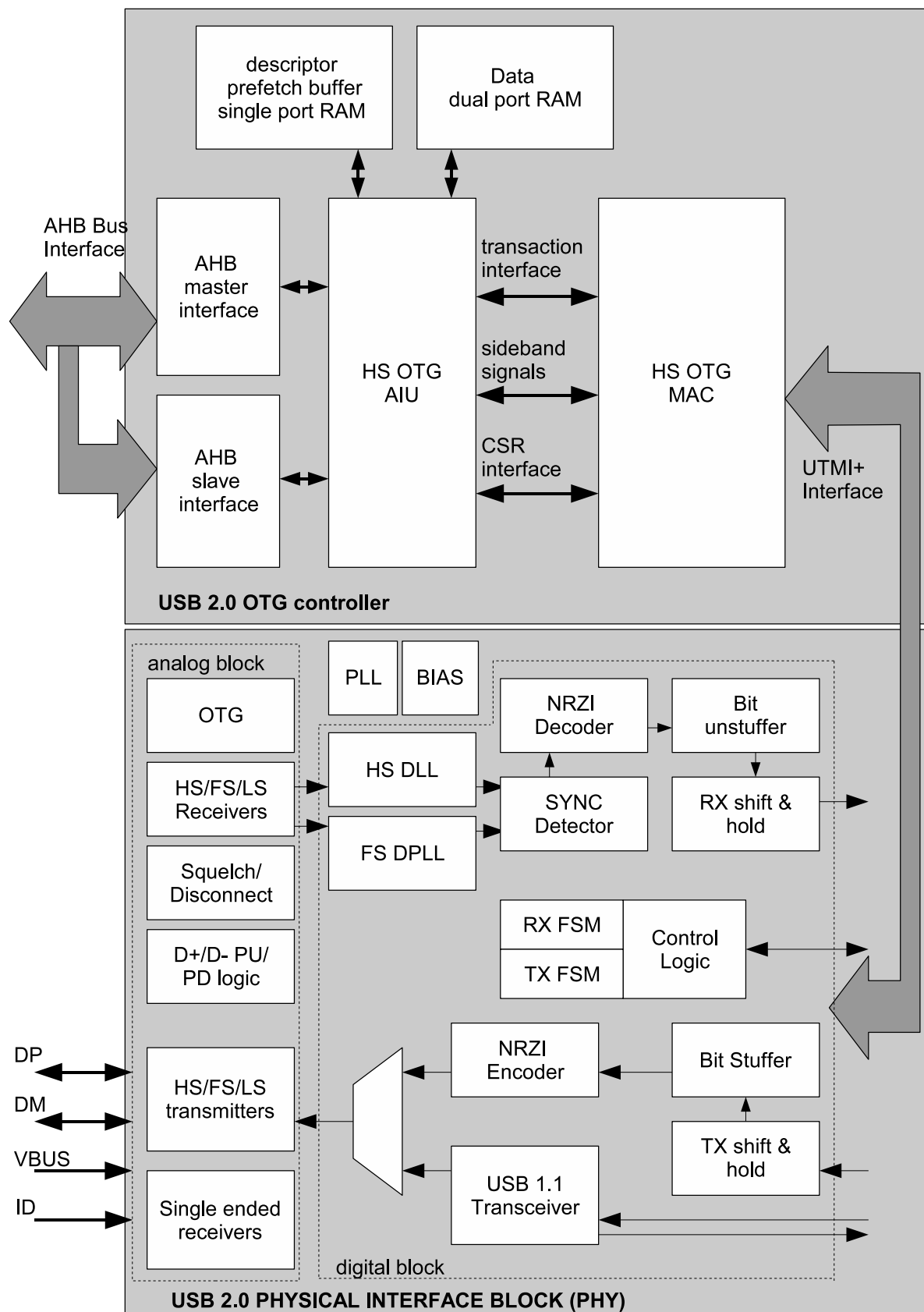
#### USB 2.0 supported features

- supports up to 15 configurations in Device mode
  - each configuration supports 15 interfaces
  - each interface handles up to 15 alternate settings
- supports session request protocol (SRP)
- supports session request protocol (SRP)
- supports Host Negotiation Protocol (HNP)
- recovers clock and data from the USB
- supports a generic root hub
- includes auto ping/split completion capabilities
- complies with UTMI+ level 3 interface

Implemented Controller configurations are:

- configured with 4 host channels and 3 bidirectional- plus 1 in-endpoints in device mode
- dynamic alternate configuration selection (for different bandwidths of isochronous endpoints)

Figure 13 USB 2.0 OTG Controller Block Diagram



### 7.2.7.2 USB 2.0 OTG PHY

- Complete PHY for USB2.0 On-The-Go
- USB 2.0 UTMI+ specification compliant
- Supports high speed (480 Mbit/s), full speed (12 Mbit/s) and low speed (1.5 Mbit/s) data transmission
- Supports OT supplement features: VBUS state detecting SRP request by “data-line pulsing” method
- Low jitter clock from either on-chip PLL (48MHz) or optional additional crystal (12MHz, 24MHz or 48MHz) which is available with the 224 pin package, only
- 16 bit parallel datain/out interface
- Typical current consumption on vdda33c and vdd33t:
  - 12 mA in FS RX mode
  - 30 mA in FS TX mode
  - 30 mA in HS RX mode
  - 40 mA in HS TX mode
  - < 100 uA in suspend mode
- Rext = 3.4kOhm (+/- 1%) must be connected between pads “rxt” and “vssa33c” to set the bias current.

### 7.2.7.3 USB 2.0 OTG Interface Registers

Table 17 USB Interface Registers

| Register Name     | Base Address    | Offset  | Note                            |
|-------------------|-----------------|---------|---------------------------------|
| USB_IEP0_CTRL     | AS3525_USB_BASE | 0x00000 | Control Register                |
| USB_IEP0_STS      | AS3525_USB_BASE | 0x00004 | Status Register                 |
| USB_IEP0_TXFSIZE  | AS3525_USB_BASE | 0x00008 | TxFIFO Size                     |
| USB_IEP0_MPS      | AS3525_USB_BASE | 0x0000c | Maximum Packet Size             |
| USB_IEP0_DESC_PTR | AS3525_USB_BASE | 0x00014 | Data Descriptor Pointer         |
| USB_IEP0_STS_MASK | AS3525_USB_BASE | 0x00018 | Status Mask Register            |
| USB_IEP1_CTRL     | AS3525_USB_BASE | 0x00020 | Control Register                |
| USB_IEP1_STS      | AS3525_USB_BASE | 0x00024 | Status Register                 |
| USB_IEP1_TXFSIZE  | AS3525_USB_BASE | 0x00028 | TxFIFO Size                     |
| USB_IEP1_MPS      | AS3525_USB_BASE | 0x0002c | Maximum Packet Size             |
| USB_IEP1_DESC_PTR | AS3525_USB_BASE | 0x00034 | Data Descriptor Pointer         |
| USB_IEP1_STS_MASK | AS3525_USB_BASE | 0x00038 | Status Mask Register            |
| USB_IEP2_CTRL     | AS3525_USB_BASE | 0x00040 | Control Register                |
| USB_IEP2_STS      | AS3525_USB_BASE | 0x00044 | Status Register                 |
| USB_IEP2_TXFSIZE  | AS3525_USB_BASE | 0x00048 | TxFIFO Size                     |
| USB_IEP2_MPS      | AS3525_USB_BASE | 0x0004c | Maximum Packet Size             |
| USB_IEP2_DESC_PTR | AS3525_USB_BASE | 0x00054 | Data Descriptor Pointer         |
| USB_IEP2_STS_MASK | AS3525_USB_BASE | 0x00058 | Status Mask Register            |
| USB_IEP3_CTRL     | AS3525_USB_BASE | 0x00060 | Control Register                |
| USB_IEP3_STS      | AS3525_USB_BASE | 0x00064 | Status Register                 |
| USB_IEP3_TXFSIZE  | AS3525_USB_BASE | 0x00068 | TxFIFO Size                     |
| USB_IEP3_MPS      | AS3525_USB_BASE | 0x0006c | Maximum Packet Size             |
| USB_IEP3_DESC_PTR | AS3525_USB_BASE | 0x00074 | Data Descriptor Pointer         |
| USB_IEP3_STS_MASK | AS3525_USB_BASE | 0x00078 | Status Mask Register            |
| USB_OEP0_CTRL     | AS3525_USB_BASE | 0x00200 | Control                         |
| USB_OEP0_STS      | AS3525_USB_BASE | 0x00204 | Status Register                 |
| USB_OEP0_RXFR     | AS3525_USB_BASE | 0x00208 | Rx Packet Frame Number Register |
| USB_OEP0_MPS      | AS3525_USB_BASE | 0x0020c | RxFIFO Size/Maximum Packet Size |
| USB_OEP0_SUP_PTR  | AS3525_USB_BASE | 0x00210 | Setup buffer Pointer Register   |
| USB_OEP0_DESC_PTR | AS3525_USB_BASE | 0x00214 | Data Descriptor Pointer         |
| USB_OEP0_STS_MASK | AS3525_USB_BASE | 0x00218 | Status Mask Register            |
| USB_OEP1_CTRL     | AS3525_USB_BASE | 0x00220 | Control Register                |
| USB_OEP1_STS      | AS3525_USB_BASE | 0x00224 | Status Register                 |
| USB_OEP1_RXFR     | AS3525_USB_BASE | 0x00228 | Rx Packet Frame Number Register |

| Register Name         | Base Address    | Offset  | Note                                            |
|-----------------------|-----------------|---------|-------------------------------------------------|
| USB_OEP1_MPS          | AS3525_USB_BASE | 0x0022c | RxFIFO Size/Maximum Packet Size                 |
| USB_OEP1_SUP_PTR      | AS3525_USB_BASE | 0x00230 | Setup buffer Pointer Register                   |
| USB_OEP1_DESC_PTR     | AS3525_USB_BASE | 0x00234 | Data Descriptor Pointer                         |
| USB_OEP1_STS_MASK     | AS3525_USB_BASE | 0x00238 | Status Mask Register                            |
| USB_OEP2_CTRL         | AS3525_USB_BASE | 0x00240 | Control Register                                |
| USB_OEP2_STS          | AS3525_USB_BASE | 0x00244 | Status Register                                 |
| USB_OEP2_RXFR         | AS3525_USB_BASE | 0x00248 | Rx Packet Frame Number Register                 |
| USB_OEP2_MPS          | AS3525_USB_BASE | 0x0024c | RxFIFO Size/Maximum Packet Size                 |
| USB_OEP2_SUP_PTR      | AS3525_USB_BASE | 0x00250 | Setup buffer Pointer Register                   |
| USB_OEP2_DESC_PTR     | AS3525_USB_BASE | 0x00254 | Data Descriptor Pointer                         |
| USB_OEP2_STS_MASK     | AS3525_USB_BASE | 0x00258 | Status Mask Register                            |
| USB_OEP3_CTRL         | AS3525_USB_BASE | 0x00260 | Control Register                                |
| USB_OEP3_STS          | AS3525_USB_BASE | 0x00264 | Status Register                                 |
| USB_OEP3_RXFR         | AS3525_USB_BASE | 0x00268 | Rx Packet Frame Number Register                 |
| USB_OEP3_MPS          | AS3525_USB_BASE | 0x0026c | RxFIFO Size/Maximum Packet Size                 |
| USB_OEP3_SUP_PTR      | AS3525_USB_BASE | 0x00270 | Setup buffer Pointer Register                   |
| USB_OEP3_DESC_PTR     | AS3525_USB_BASE | 0x00274 | Data Descriptor Pointer                         |
| USB_OEP3_STS_MASK     | AS3525_USB_BASE | 0x00278 | Status Mask Register                            |
| USB_DEV_CFG           | AS3525_USB_BASE | 0x00400 | Device Configuration Register                   |
| USB_DEV_CTRL          | AS3525_USB_BASE | 0x00404 | Device Control Register                         |
| USB_DEV_STS           | AS3525_USB_BASE | 0x00408 | Device Status Register                          |
| USB_DEV_INTR          | AS3525_USB_BASE | 0x0040c | Device Interrupt Register                       |
| USB_DEV_INTR_MASK     | AS3525_USB_BASE | 0x00410 | Device Interrupt Mask Register                  |
| USB_DEV_EP_INTR       | AS3525_USB_BASE | 0x00414 | Device Endpoint Interrupt                       |
| USB_DEV_EP_INTR_MASK  | AS3525_USB_BASE | 0x00418 | Device Endpoint Interrupt Mask                  |
| USB_PHY_EP0_INFO      | AS3525_USB_BASE | 0x00504 | Information Register                            |
| USB_PHY_EP1_INFO      | AS3525_USB_BASE | 0x00508 | Information Register                            |
| USB_PHY_EP2_INFO      | AS3525_USB_BASE | 0x0050c | Information Register                            |
| USB_PHY_EP3_INFO      | AS3525_USB_BASE | 0x00510 | Information Register                            |
| USB_PHY_EP4_INFO      | AS3525_USB_BASE | 0x00514 | Information Register                            |
| USB_PHY_EP5_INFO      | AS3525_USB_BASE | 0x00518 | Information Register                            |
| USB_HOST_CH0_SPLT     | AS3525_USB_BASE | 0x01000 | Split Information Register                      |
| USB_HOST_CH0_STS      | AS3525_USB_BASE | 0x01004 | Status Register                                 |
| USB_HOST_CH0_TXFSIZE  | AS3525_USB_BASE | 0x01008 | TxFIFO Register                                 |
| USB_HOST_CH0_REQ      | AS3525_USB_BASE | 0x0100c | Request Register                                |
| USB_HOST_CH0_PER_INFO | AS3525_USB_BASE | 0x01010 | Periodic/Split Transaction Information Register |
| USB_HOST_CH0_DESC_PTR | AS3525_USB_BASE | 0x01014 | Data Descriptor Pointer                         |
| USB_HOST_CH0_STS_MASK | AS3525_USB_BASE | 0x01018 | Status Mask Register                            |
| USB_HOST_CH1_SPLT     | AS3525_USB_BASE | 0x01020 | Split Information Register                      |
| USB_HOST_CH1_STS      | AS3525_USB_BASE | 0x01024 | Status Register                                 |
| USB_HOST_CH1_TXFSIZE  | AS3525_USB_BASE | 0x01028 | TxFIFO Register                                 |
| USB_HOST_CH1_REQ      | AS3525_USB_BASE | 0x0102c | Request Register                                |
| USB_HOST_CH1_PER_INFO | AS3525_USB_BASE | 0x01030 | Periodic/Split Transaction Information Register |
| USB_HOST_CH1_DESC_PTR | AS3525_USB_BASE | 0x01034 | Data Descriptor Pointer                         |
| USB_HOST_CH1_STS_MASK | AS3525_USB_BASE | 0x01038 | Status Mask Register                            |
| USB_HOST_CH2_SPLT     | AS3525_USB_BASE | 0x01040 | Split Information Register                      |
| USB_HOST_CH2_STS      | AS3525_USB_BASE | 0x01044 | Status Register                                 |
| USB_HOST_CH2_TXFSIZE  | AS3525_USB_BASE | 0x01048 | TxFIFO Register                                 |
| USB_HOST_CH2_REQ      | AS3525_USB_BASE | 0x0104c | Request Register                                |
| USB_HOST_CH2_PER_INFO | AS3525_USB_BASE | 0x01050 | Periodic/Split Transaction Information          |

| Register Name           | Base Address    | Offset  | Note                                            |
|-------------------------|-----------------|---------|-------------------------------------------------|
|                         |                 |         | Register                                        |
| USB_HOST_CH2_DESC_PTR   | AS3525_USB_BASE | 0x01054 | Data Descriptor Pointer                         |
| USB_HOST_CH2_STS_MASK   | AS3525_USB_BASE | 0x01058 | Status Mask Register                            |
| USB_HOST_CH3_SPLT       | AS3525_USB_BASE | 0x01060 | Split Information Register                      |
| USB_HOST_CH3_STS        | AS3525_USB_BASE | 0x01064 | Status Register                                 |
| USB_HOST_CH3_TXFSIZE    | AS3525_USB_BASE | 0x01068 | TxFIFO Register                                 |
| USB_HOST_CH3_REQ        | AS3525_USB_BASE | 0x0106c | Request Register                                |
| USB_HOST_CH3_PER_INFO   | AS3525_USB_BASE | 0x01070 | Periodic/Split Transaction Information Register |
| USB_HOST_CH3_DESC_PTR   | AS3525_USB_BASE | 0x01074 | Data Descriptor Pointer                         |
| USB_HOST_CH3_STS_MASK   | AS3525_USB_BASE | 0x01078 | Status Mask Register                            |
| USB_HOST_CFG            | AS3525_USB_BASE | 0x01400 | Host Configuration Register                     |
| USB_HOST_CTRL           | AS3525_USB_BASE | 0x01404 | Host Control Register                           |
| USB_HOST_INTR           | AS3525_USB_BASE | 0x0140c | Host Interrupt Register                         |
| USB_HOST_INTR_MASK      | AS3525_USB_BASE | 0x01410 | Host Interrupt Mask Register                    |
| USB_HOST_CH_INTR        | AS3525_USB_BASE | 0x01414 | Host Channel Interrupt Register                 |
| USB_HOST_CH_INTR_MASK   | AS3525_USB_BASE | 0x01418 | Host Channel Interrupt Mask Register            |
| USB_HOST_FRAME_INT      | AS3525_USB_BASE | 0x0141c | Host Frame Interval Register                    |
| USB_HOST_FRAME_REM      | AS3525_USB_BASE | 0x01420 | Host Frame Remaining Register                   |
| USB_HOST_FRAME_NUM      | AS3525_USB_BASE | 0x01424 | Host Frame Number Register                      |
| USB_HOST_PORT0_CTRL_STS | AS3525_USB_BASE | 0x01500 | Host Port and Status Register                   |
| USB_OTG_CSR             | AS3525_USB_BASE | 0x02000 | OTG Control and Status Register                 |
| USB_I2C_CSR             | AS3525_USB_BASE | 0x02004 | I2C Access Register                             |
| USB_GPIO_CSR            | AS3525_USB_BASE | 0x02008 | General Purpose Input/Output Register           |
| USB_SNPSID_CSR          | AS3525_USB_BASE | 0x0200c | Synopsys ID Register                            |
| USB_USERID_CSR          | AS3525_USB_BASE | 0x02010 | User ID Register                                |
| USB_USER_CONF1          | AS3525_USB_BASE | 0x02014 | User Config1 Register                           |
| USB_USER_CONF2          | AS3525_USB_BASE | 0x02018 | User Config2 Register                           |
| USB_USER_CONF3          | AS3525_USB_BASE | 0x0201c | User Config3 Register                           |
| USB_USER_CONF4          | AS3525_USB_BASE | 0x02020 | User Config4 Register                           |
| USB_USER_CONF5          | AS3525_USB_BASE | 0x02024 | User Config5 Register                           |

## 7.2.8 Memory Stick / Memory Stick Pro Interface

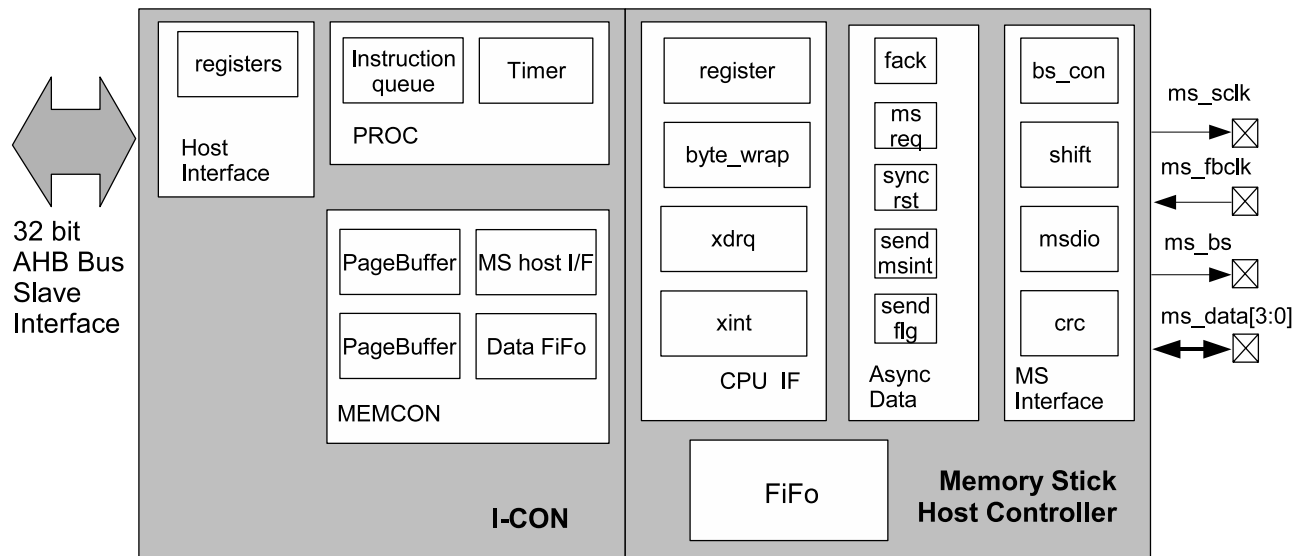
The Sony memory stick interface is an AHB bus slave device. This interface conforms to following standards:

- Memory Stick Standard Format Specifications version 1.4-00
- Memory Stick PRO Format Specifications version 1.00-01

### 7.2.8.1 Block Diagram

The memory stick interface contains two main blocks, the ICON and the host controller.

Figure 14 SONY memory stick interface block diagram



### 7.2.8.2 I-CON

This IP is Memory Stick / Memory Stick PRO Host Controller automatic control IP with a 32-bit CPU interface. This IP automatically controls the series of TPC-based communication with the Memory Stick in place of the CPU, and aims to reduce the burden on the Host CPU.

The contents of communication with the Memory Stick are designated in this IP by micro codes.

#### Features

- 32-bit CPU interface
- Inside controller specified by microcodes
- Buffer for two-way data transmission loaded (256 byte x 2)
- 32/16 bit access available
- DMA support
- General-purpose data transmit/receive FIFO (12 Bytes)

### 7.2.8.3 Host Controller

#### Features

- Memory Stick and Memory Stick PRO support
- FiFo memory (64 bits x 4) for two-way data transmission
- Built-in CRC circuit
- Memory Stick serial clock (Serial: 20 MHz (max.), Parallel: 40 MHz (max.))
- DMA support
- 16/32/64-bit access possible

#### 7.2.8.4 Functional description

## Communication with the Memory Stick

The communication protocol with the Memory Stick is started by write from the CPU to the command register. When the protocol finishes, the CPU is notified that the protocol has ended by an interrupt request.

## Data transfer request

When the protocol is started and enters the data transfer state, data is requested by issuing a DMA transfer request or an interrupt request to the CPU. Data can also be requested to an external memory.

Memory Stick communication time out

The RDY time out time when the handshake state (read protocol: BS2, write protocol: BS3) is established in communication with the Memory Stick can be designated as the number of Memory Stick transfer clocks. When a time out occurs, the CPU is notified that the protocol has ended due to a time out error by an interrupt request.

CRC off

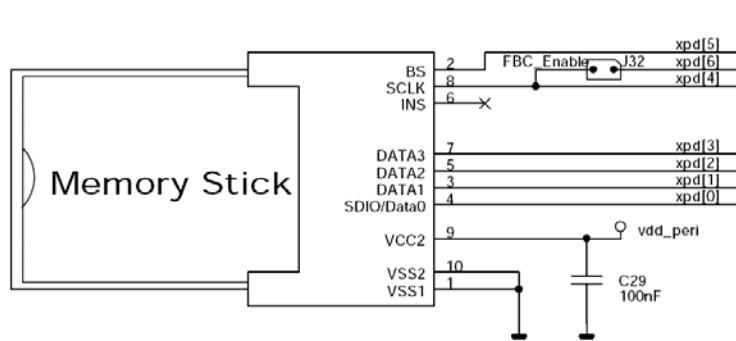
CRC off can be set as a test mode.

When CRC off is set, CRC is not added to the data transmitted to the Memory Stick.

PAD cells

The connections to the MemoryStick Interface are shared with the General Purpose I/O port-D (GPIO xpd[0:7]).

Figure 15 external memory stick connection



## 7.3 APB Peripheral Block

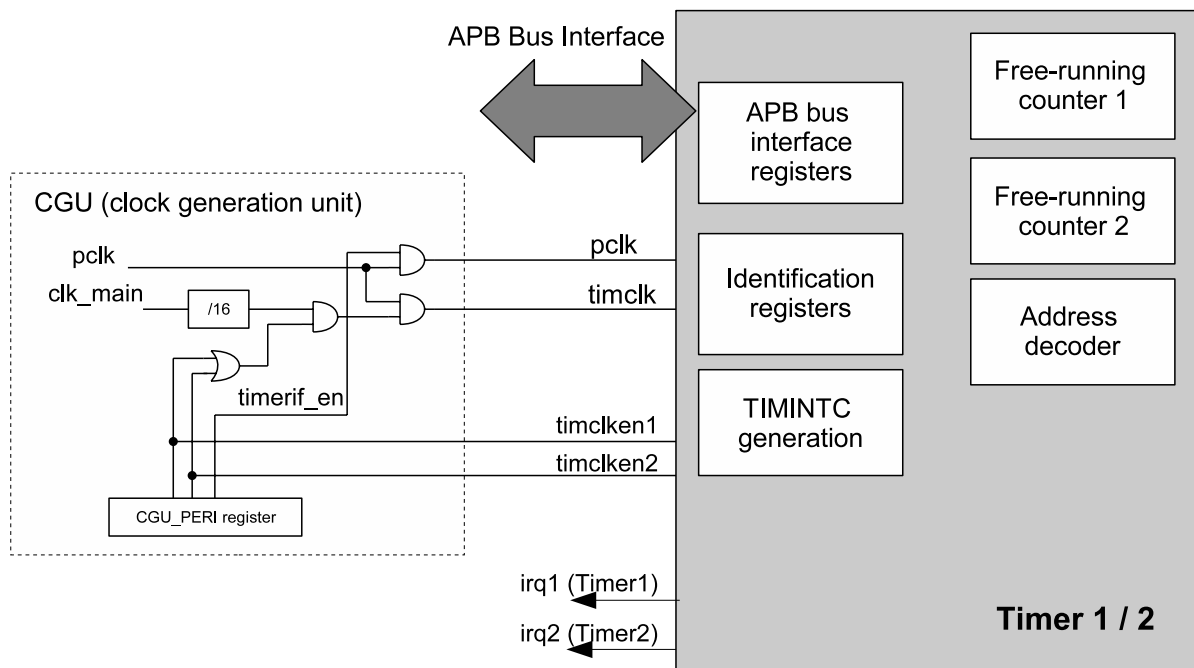
### 7.3.1 Timers

The Dual Input Timers module is an APB slave that provides access to two interrupt-generating, programmable 32-bit free-running decrementing counters (FRCs). The system clock (PCLK) is used to control the programmable registers, and the second clock input is used to drive the counter, enabling the counters to run from a much slower clock than the system clock. This input clock of the counters (TIMCLK) is connected to a clock derived (divided by 16) from the main clock (clk\_main) signal. That clock clk\_main is always running and is coming from the internal or external oscillator (set by clk\_sel pad).

#### 7.3.1.1 Timer modes

- Free-running mode: the counter wraps after zero and continues at the maximum value. This is the default mode.
- Periodic mode: reload of original value after wrapping past zero.
- One-shot mode - interrupt is generated once, counter halts after reaching zero

Figure 16 Timer Block Diagram



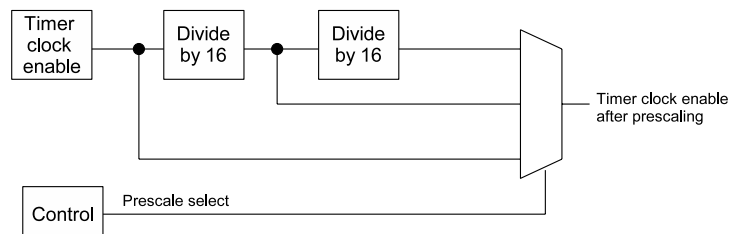
Each timer has an identical set of registers shown in table Table 18. The operation of each timer is identical. The timer is loaded by writing to the load register and, if enabled, counts down to zero. When a counter is already running, writing to the load register will cause the counter to immediately restart at the new value. Writing to the background load value has no effect on the current count. The counter continues to decrement to zero, and then recommences from the new load value (if in periodic mode, and one shot mode is not selected).

When zero is reached, an interrupt is generated. The interrupt can be cleared by writing to the clear register. If One Shot Mode is selected, the counter halts on reaching zero. One Shot Mode is deselected, or a new load value is written. Otherwise, after reaching a zero count, if the timer is operating in free-running mode it continues to decrement from its maximum value. If periodic timer mode is selected, the timer reloads the count value from the load register and continues to decrement. In this mode the counter effectively generates a periodic interrupt. The mode is selected by a bit in the timer control register. At any point, the current counter value can be read from the value register. The counter is enabled by a bit in the control register. At reset, the counter is disabled, the interrupt is cleared, and the load register is set to zero. The mode and prescale values are set to free-running, and clock divide of 1 respectively.

The timer clock enable is generated by a prescale unit. The enable is then used by the counter to create a clock with a timing of one of the following.

- The system clock
- The system clock divided by 16, generated by 4 bits of prescale
- The system clock divided by 256, generated by a total of 8 bits of prescale

Figure 17 - timer prescaler



### 7.3.1.2 Interrupt generation

An interrupt is generated when the full 32-bit counter reaches zero, and is only cleared when the TimerXClear location is written to. A register holds the value until the interrupt is cleared. The most significant carry bit of the counter detects the counter reaching zero.

Interrupts can be masked by writing 0 to the interrupt enable bit in the control register. Both the raw interrupt status (prior to masking) and the final interrupt status (after masking) can be read from status registers.

Timer 1 interrupt output is connected to interrupt input line irq1 (VIC input) and Timer 2 interrupt output is connected to interrupt line irq2.

### 7.3.1.3 Timer Register Descriptions

Table 18 – Timer 1 and 2 registers

| Register Name                     | Base Address      | Offset | Note                              |
|-----------------------------------|-------------------|--------|-----------------------------------|
| Timer1Load                        | AS3525_TIMER_BASE | 0x00   | load value for Timer 1            |
| Timer1Value                       | AS3525_TIMER_BASE | 0x04   | current value for Timer 1         |
| Timer1Control                     | AS3525_TIMER_BASE | 0x08   | Timer 1 control register          |
| Timer1IntClr                      | AS3525_TIMER_BASE | 0x0C   | Timer 1 interrupt clear           |
| Timer1RIS                         | AS3525_TIMER_BASE | 0x10   | Timer 1 raw interrupt status      |
| Timer1MIS                         | AS3525_TIMER_BASE | 0x14   | Timer 1 masked interrupt status   |
| Timer1BGLoad                      | AS3525_TIMER_BASE | 0x18   | Timer 1 background load value     |
| Timer2Load                        | AS3525_TIMER_BASE | 0x20   | load value for Timer 2            |
| Timer2Value                       | AS3525_TIMER_BASE | 0x24   | current value for Timer 2         |
| Timer2Control                     | AS3525_TIMER_BASE | 0x28   | Timer 2 control register          |
| Timer2IntClr                      | AS3525_TIMER_BASE | 0x2C   | Timer 2 interrupt clear           |
| Timer2RIS                         | AS3525_TIMER_BASE | 0x30   | Timer 2 raw interrupt status      |
| Timer2MIS                         | AS3525_TIMER_BASE | 0x34   | Timer 2 masked interrupt status   |
| Timer2BGLoad                      | AS3525_TIMER_BASE | 0x38   | Timer 2 background load value     |
| Peripheral ID register bits 7:0   | AS3525_TIMER_BASE | 0xFE0  | Peripheral ID register bits 7:0   |
| Peripheral ID register bits 15:8  | AS3525_TIMER_BASE | 0xFE4  | Peripheral ID register bits 15:8  |
| Peripheral ID register bits 23:16 | AS3525_TIMER_BASE | 0xFE8  | Peripheral ID register bits 23:16 |
| Peripheral ID register bits 31:24 | AS3525_TIMER_BASE | 0xFEC  | Peripheral ID register bits 31:24 |
| Primecell ID register bits 7:0    | AS3525_TIMER_BASE | 0xFF0  | Primecell ID register bits 7:0    |
| Primecell ID register bits 15:8   | AS3525_TIMER_BASE | 0xFF4  | Primecell ID register bits 15:8   |
| Primecell ID register bits 23:16  | AS3525_TIMER_BASE | 0xFF8  | Primecell ID register bits 23:16  |
| Primecell ID register bits 31:24  | AS3525_TIMER_BASE | 0xFFC  | Primecell ID register bits 31:24  |

## Load register, Timer1Load, Timer2Load

This is a 32-bit register containing the value from which the counter is to decrement. This is the value used to reload the counter when periodic mode is enabled, and the current count reaches zero.

When this register is written to directly, the current count is immediately reset to the new value at the next rising edge of TIMCLK which is enabled by TIMCLKEN.

The value in this register is also overwritten if the TimerXBGLoad register is written to, but the current count is not immediately affected.

If values are written to both the timerXLoad and TimerXBGLoad registers before an enabled rising edge on TIMCLK, the following occurs:

- On the next enabled TIMCLK edge the value written to the TimerXLoad value replaces the current count value
- Following this, each time the counter reaches zero, the current count value is reset to the value written to TimerXBGLoad.

Reading from the TimerXLoad register at any time after the two writes have occurred will retrieve the value written to TimerXBGLoad. That is, the value read from TimerXLoad is always the value which will take effect for periodic mode after the next time the counter reaches zero.

## Current value register, Timer1Value, Timer2Value

This register gives the current value of the decrementing counter.

## Timer control register

Table 19 Timer control register

| Name                         |                  | Base                                        |        | Default                                                                                                                                                                                                  |
|------------------------------|------------------|---------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer1Control, Timer2Control |                  | AS3525_TIMER_BASE                           |        | 0x20                                                                                                                                                                                                     |
| Offset: 0x08, 0x28           |                  | Timer Control Register                      |        |                                                                                                                                                                                                          |
|                              |                  | Contains control bits of the PLLA register. |        |                                                                                                                                                                                                          |
| Bit                          | Bit Name         | Default                                     | Access | Bit Description                                                                                                                                                                                          |
| 7                            | Timer Enable     | 0                                           | R/W    | Enable bit:<br>0: timer disabled (default)<br>1: timer enabled                                                                                                                                           |
| 6                            | Timer Mode       | 0                                           | R/W    | Mode bit<br>0: timer is in free-running mode (default)<br>1: timer is in periodic mode                                                                                                                   |
| 5                            | Interrupt Enable | 1                                           | R/W    | Interrupt enable bit<br>0: timer interrupt disabled<br>1: timer interrupt enabled (default)                                                                                                              |
| 4                            | RESERVED         |                                             |        | Reserved bit, do not modify, and ignore on read                                                                                                                                                          |
| 3:2                          | TimerPre         | 00                                          | R/W    | Prescale bits:<br>00: no prescale, clock is divided by 1 (default)<br>01: 4 stages of prescale, clock is divided by 16<br>10: 8 stages of prescale, clock is divided by 256<br>11: undefined, do not use |
| 1                            | Timer Size       | 0                                           | R/W    | Selects 16/32 bit counter operation<br>0: 16 bit counter (default)<br>1: 32 bit counter                                                                                                                  |
| 0                            | OneShotCount     | 0                                           | R/W    | Selects one-shot or wrapping counter mode<br>0: wrapping mode (default)<br>1: one-shot mode                                                                                                              |

## Interrupt clear register, Timer1IntClr, Timer2IntClr

Any write to this register will clear the interrupt output from the counter

## Raw Interrupt status register, Timer1RIS, Timer2RIS

This register indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the control register to create the masked interrupt, which is passed to the interrupt output pin.

Table 20 raw interrupt status register

| Name                 |                     | Base                                        |        | Default                               |
|----------------------|---------------------|---------------------------------------------|--------|---------------------------------------|
| Timer1RIS, Timer2RIS |                     | AS3525_TIMER_BASE                           |        |                                       |
| Offset: 0x10, 0x30   |                     | Timer raw interrupt status register         |        |                                       |
|                      |                     | Contains control bits of the PLLA register. |        |                                       |
| Bit                  | Bit Name            | Default                                     | Access | Bit Description                       |
| 0                    | Raw Timer Interrupt |                                             | R      | Raw interrupt status from the counter |

## Interrupt status register, TIMERXMIS

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the control register, and is the same value which is passed to the interrupt output pin.

Table 21 interrupt status register

| Name                 |                     | Base                                        |        | Default                               |
|----------------------|---------------------|---------------------------------------------|--------|---------------------------------------|
| Timer1MIS, Timer2MIS |                     | AS3525_TIMER_BASE                           |        |                                       |
| Offset: 0x10, 0x30   |                     | Timer raw interrupt status register         |        |                                       |
|                      |                     | Contains control bits of the PLLA register. |        |                                       |
| Bit                  | Bit Name            | Default                                     | Access | Bit Description                       |
| 0                    | Raw Timer Interrupt |                                             | R      | Raw interrupt status from the counter |

## Background load register, TimerXBGLoad

This is a 32 bit register containing the value from which the counter is to decrement. This is the value used to reload the counter when periodic mode is enabled, and the current count reaches zero.

This register provides an alternative method of accessing the TimerXLoad register. The difference is that writes to TimerXBGLoad will not cause the counter immediately to restart from the new value.

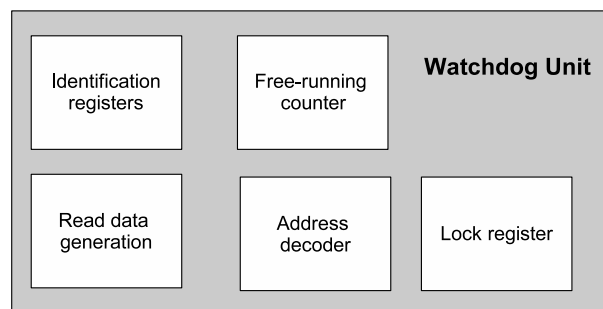
Reading from this register returns the same value returned from TimerXLoad.

## 7.3.2 Watchdog Unit

The watchdog unit provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value. The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserved for the entire programmed period. You can enable or disable the watchdog unit as required.

Clock reference for the watchdog is PCLK divided by 256.

Figure 18 watchdog unit



### 7.3.2.1 Watchdog register descriptions

Table 22 Watchdog Registers

| Register Name | Base Address    | Offset | Note                              |
|---------------|-----------------|--------|-----------------------------------|
| WDT_LOAD      | AS3525_WDT_BASE | 0x00   | load register                     |
| WDT_VALUE     | AS3525_WDT_BASE | 0x04   | counter current value             |
| WDT_CONTROL   | AS3525_WDT_BASE | 0x08   | control register                  |
| WDT_INTCLR    | AS3525_WDT_BASE | 0x0C   | Interrupt clear register          |
| WDT_RIS       | AS3525_WDT_BASE | 0x10   | Raw interrupt status register     |
| WDT_MIS       | AS3525_WDT_BASE | 0x14   | Masked interrupt status register  |
| WDT_LOCK      | AS3525_WDT_BASE | 0xC00  | Lock register                     |
| WDT_PERIPHID0 | AS3525_WDT_BASE | 0xFE0  | Watchdog peripheral ID 0 register |
| WDT_PERIPHID1 | AS3525_WDT_BASE | 0xFE4  | Watchdog peripheral ID 1 register |
| WDT_PERIPHID2 | AS3525_WDT_BASE | 0xFE8  | Watchdog peripheral ID 2 register |
| WDT_PERIPHID3 | AS3525_WDT_BASE | 0xFEC  | Watchdog peripheral ID 3 register |
| WDT_PCELLID0  | AS3525_WDT_BASE | 0xFF0  | Watchdog primecell ID 0 register  |
| WDT_PCELLID1  | AS3525_WDT_BASE | 0xFF4  | Watchdog primecell ID 1 register  |
| WDT_PCELLID2  | AS3525_WDT_BASE | 0xFF8  | Watchdog primecell ID 2 register  |
| WDT_PCELLID3  | AS3525_WDT_BASE | 0xFFC  | Watchdog primecell ID 3 register  |

#### Watchdog load register, WdogLoad

This is a 32-bit register containing the value from which the counter is to decrement. When this register is written to, the count is immediately restarted from the new value. The minimum valid value for WdogLoad is one.

## Watchdog control register, WdogControl

This is a read/write register that enables the software to control the watchdog unit.

Table 23 watchdog control register

| Name         |          | Base                      |        | Default                                                                                                                     |
|--------------|----------|---------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------|
| WdogControl  |          | AS3525_WDT_BASE           |        | 0x04                                                                                                                        |
| Offset: 0x08 |          | Watchdog Control Register |        |                                                                                                                             |
| Bit          | Bit Name | Default                   | Access | Bit Description                                                                                                             |
| 1            | RESEN    | 0                         | R/W    | Enable Watchdog reset output (WDOGRES). Acts as a mask for the reset output.<br>0: disable the reset<br>1: enable the reset |
| 0            | INTEN    | 0                         | R/W    | Enable the interrupt event (WDOGINT).<br>0: disable the counter and interrupt<br>1: enable the counter and interrupt        |

## Watchdog clear interrupt register, WdogIntClr

A write of any value to this location clears the watchdog interrupt, and reloads the counter from the value in WdogLoad.

## Raw interrupt status register, WdogRIS

This register indicates the raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt, which is passed to the interrupt output pin.

Table 24 watchdog raw interrupt status register

| Name         |                    | Base                               |        | Default                                   |
|--------------|--------------------|------------------------------------|--------|-------------------------------------------|
| WdogRIS      |                    | AS3525_WDT_BASE                    |        |                                           |
| Offset: 0x10 |                    | Watchdog interrupt status register |        |                                           |
| Bit          | Bit Name           | Default                            | Access | Bit Description                           |
| 0            | Watchdog Interrupt |                                    | R      | Enabled interrupt status from the counter |

## Interrupt status register, WdogMIS

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the INTEN bit from the control register, and is the same value which is passed to the interrupt output pin.

| Name         |                        | Base                                   |        | Default                               |
|--------------|------------------------|----------------------------------------|--------|---------------------------------------|
| WdogMIS      |                        | AS3525_WDT_BASE                        |        |                                       |
| Offset: 0x14 |                        | Watchdog raw interrupt status register |        |                                       |
| Bit          | Bit Name               | Default                                | Access | Bit Description                       |
| 0            | Raw Watchdog Interrupt |                                        | R      | Raw interrupt status from the counter |

Table 25 watchdog interrupt status register

## Watchdog lock register, WdogLock

Use of this register allows write-access to all other registers to be disabled. This is to prevent rogue software from disabling the watchdog functionality. Writing a value of 0x1ACCE551 will enable write access to all other registers. Writing any other value will disable write accesses. A read from this register will return only the bottom bit:

- 0 indicates that write access is enabled (not locked)
- 1 indicates that write access is disabled (locked)

Table 26 watchdog lock register

| Name          |                              | Base                                   |        | Default                                                                                                            |
|---------------|------------------------------|----------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------|
| WdogLock      |                              | AS3525_WDT_BASE                        |        | 0x00                                                                                                               |
| Offset: 0xC00 |                              | Watchdog raw interrupt status register |        |                                                                                                                    |
| Bit           | Bit Name                     | Default                                | Access | Bit Description                                                                                                    |
| 31:0          | Enable register writes       |                                        | W      | Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value. |
| 0             | Register write enable status | 0                                      | R      | 0: write access to all other registers is enabled (default)<br>1: write access to all other registers is disabled  |

### 7.3.3 SSP – Synchronous Serial Port

The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:

- a Motorola SPI-compatible interface
- a TI synchronous serial interface
- a National Semiconductor MicroWire interface

In both master and slave configurations the SSP performs

- parallel-to-serial conversion on data written to an internal 16-bit wide, 8-location deep transmit FIFO
- serial-to-parallel conversion on received data, buffering it in a similar 16-bit wide, 8 location-deep receive FIFO

Interrupts are generated to:

- request servicing of the transmit and receive FIFO
- inform the system that a receive FIFO overrun has occurred
- inform the system that data is present in the receive FIFO after an idle period has expired

SSP Features:

- compliant to AMBA Rev 2.0
- master or slave operation
- programmable clock bit rate and prescale
- separate receive and transmit memory buffers each 16 bits wide and 8 bits deep
- programmable data frame size from 4 to 16 bit
- independent masking of receive FIFO, transmit FIFO and receive overrun interrupts
- internal loopback testmode available
- support for DMA
- identification register uniquely identifying the PrimeCell™ itself (support for OS)

SPI features:

- full-duplex, four wire synchronous transfer
- programmable clock polarity and phase

MicroWire features:

- half duplex transfer using 8 bit control message

Texas Instruments SSI features:

- full-duplex, four wire synchronous transfer
- transmit data PIN tristateable when not transmitting

Programmable parameters:

- master or slave mode
- enabling of operation
- frame format
- communication baud rate
- clock phase and polarity
- data width from 4 to 16 bit
- interrupt masking

Figure 19 Serial Synchronous Port Block Diagram

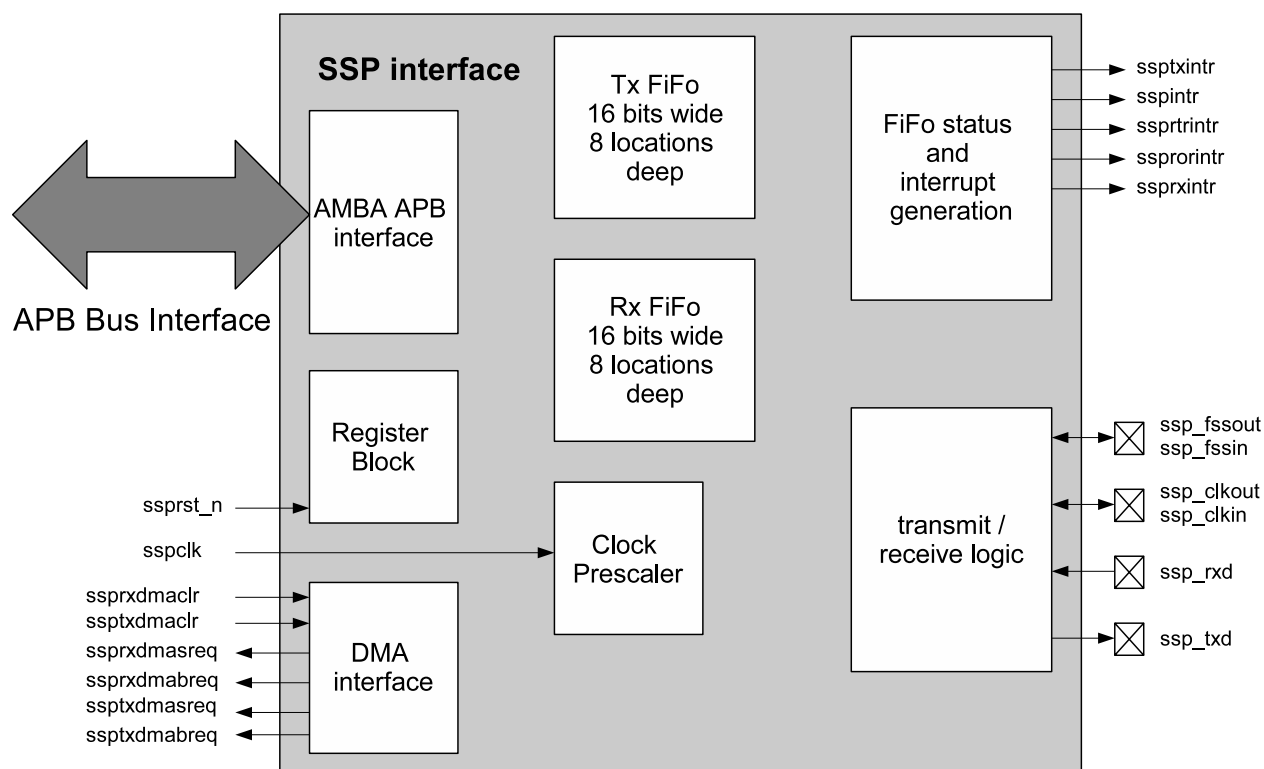


Table 27 SSP Registers

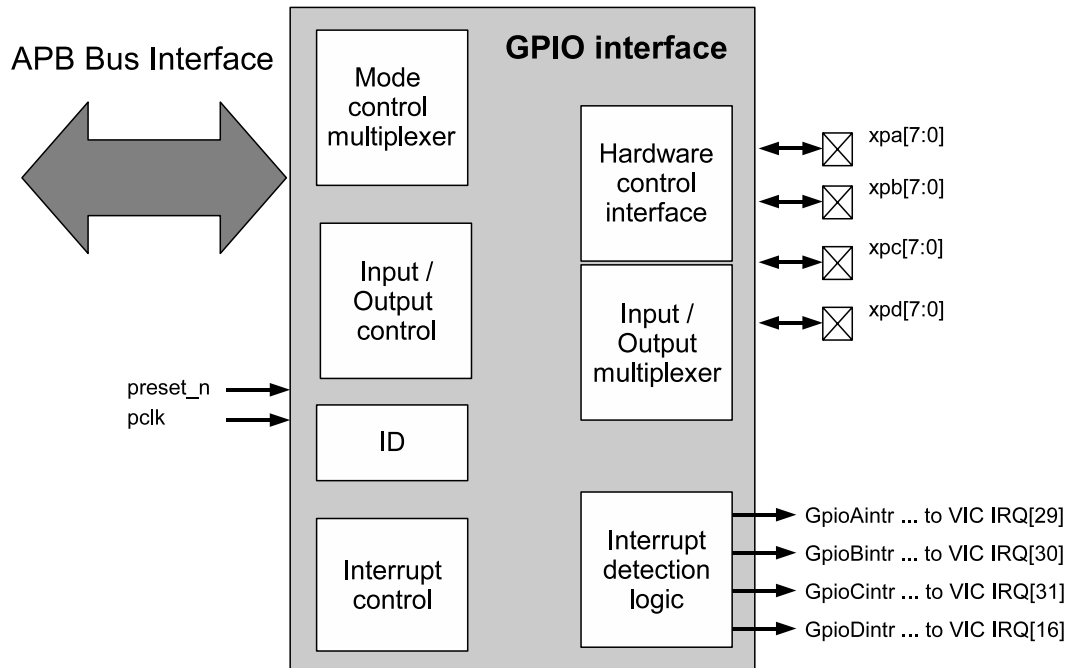
| Register Name | Base Address | Offset | Note                                  |
|---------------|--------------|--------|---------------------------------------|
| SPI_SSPCR0    | SSP_BASE     | 0x00   | CR0 control register                  |
| SPI_SSPCR1    | SSP_BASE     | 0x04   | CR1 control register                  |
| SPI_SSPRXD    | SSP_BASE     | 0x08   | Read Data Register                    |
| SPI_SSPTXD    | SSP_BASE     | 0x08   | Write Data register                   |
| SPI_SSPSR     | SSP_BASE     | 0x0C   | SSP status register                   |
| SPI_SSPCPSR   | SSP_BASE     | 0x10   | SSP Pre-scaler register               |
| SPI_SSIMISC   | SSP_BASE     | 0x14   | SSP Interrupt Mask and clear register |
| SPI_SSPIRS    | SSP_BASE     | 0x18   | SSP Raw interrupt status register     |
| SPI_SSPMIS    | SSP_BASE     | 0x1C   | SSP Masked interrupt status register  |
| SPI_SSPICR    | SSP_BASE     | 0x20   | SSP interrupt clear register          |
| SPI_SSPPMACR  | SSP_BASE     | 0x24   | SSP DMA control register              |

### 7.3.4 GPIO - General purpose input/output ports

The ARM PrimeCell™ PL061 “General Purpose Input/Output” is included in the APB system.

- compliant to AMBA Rev 2.0
- each port has eight individually programmable input/output pins, default to input at reset
- four ports A, B, C, D are included
- programmable interrupt generation capability, from a transition or level condition, on any number of PINs
- hardware control capability of GPIO's for different system configurations.
- bit masking in both read and write operations through address lines

Figure 20 GPIO Block Diagram



## 7.3.4.1 GPIO register descriptions

Table 28: GPIO Registers

| Register Name | Base Address      | Offset | Note                               |
|---------------|-------------------|--------|------------------------------------|
| GPIO1_DATA    | AS3525_GPIO1_BASE | 0x000  | GPIO data register                 |
| GPIO1_DIR     | AS3525_GPIO1_BASE | 0x400  | GPIO data direction register       |
| GPIO1_IS      | AS3525_GPIO1_BASE | 0x404  | GPIO interrupt sense register      |
| GPIO1_IBE     | AS3525_GPIO1_BASE | 0x408  | GPIO interrupt both edges register |
| GPIO1_IEV     | AS3525_GPIO1_BASE | 0x40C  | GPIO interrupt event register      |
| GPIO1_IE      | AS3525_GPIO1_BASE | 0x410  | GPIO interrupt mask register       |
| GPIO1_RIS     | AS3525_GPIO1_BASE | 0x414  | GPIO raw interrupt status          |
| GPIO1_MIS     | AS3525_GPIO1_BASE | 0x418  | GPIO masked interrupt status       |
| GPIO1_IC      | AS3525_GPIO1_BASE | 0x41C  | GPIO interrupt clear               |
| GPIO1_AFSEL   | AS3525_GPIO1_BASE | 0x420  | GPIO mode control select           |
| GPIO2_DATA    | AS3525_GPIO2_BASE | 0x000  | GPIO data register                 |
| GPIO2_DIR     | AS3525_GPIO2_BASE | 0x400  | GPIO data direction register       |
| GPIO2_IS      | AS3525_GPIO2_BASE | 0x404  | GPIO interrupt sense register      |
| GPIO2_IBE     | AS3525_GPIO2_BASE | 0x408  | GPIO interrupt both edges register |
| GPIO2_IEV     | AS3525_GPIO2_BASE | 0x40C  | GPIO interrupt event register      |
| GPIO2_IE      | AS3525_GPIO2_BASE | 0x410  | GPIO interrupt mask register       |
| GPIO2_RIS     | AS3525_GPIO2_BASE | 0x414  | GPIO raw interrupt status          |
| GPIO2_MIS     | AS3525_GPIO2_BASE | 0x418  | GPIO masked interrupt status       |
| GPIO2_IC      | AS3525_GPIO2_BASE | 0x41C  | GPIO interrupt clear               |
| GPIO2_AFSEL   | AS3525_GPIO2_BASE | 0x420  | GPIO mode control select           |
| GPIO3_DATA    | AS3525_GPIO3_BASE | 0x000  | GPIO data register                 |
| GPIO3_DIR     | AS3525_GPIO3_BASE | 0x400  | GPIO data direction register       |
| GPIO3_IS      | AS3525_GPIO3_BASE | 0x404  | GPIO interrupt sense register      |
| GPIO3_IBE     | AS3525_GPIO3_BASE | 0x408  | GPIO interrupt both edges register |
| GPIO3_IEV     | AS3525_GPIO3_BASE | 0x40C  | GPIO interrupt event register      |
| GPIO3_IE      | AS3525_GPIO3_BASE | 0x410  | GPIO interrupt mask register       |
| GPIO3_RIS     | AS3525_GPIO3_BASE | 0x414  | GPIO raw interrupt status          |
| GPIO3_MIS     | AS3525_GPIO3_BASE | 0x418  | GPIO masked interrupt status       |
| GPIO3_IC      | AS3525_GPIO3_BASE | 0x41C  | GPIO interrupt clear               |
| GPIO3_AFSEL   | AS3525_GPIO3_BASE | 0x420  | GPIO mode control select           |
| GPIO4_DATA    | AS3525_GPIO4_BASE | 0x000  | GPIO data register                 |
| GPIO4_DIR     | AS3525_GPIO4_BASE | 0x400  | GPIO data direction register       |
| GPIO4_IS      | AS3525_GPIO4_BASE | 0x404  | GPIO interrupt sense register      |
| GPIO4_IBE     | AS3525_GPIO4_BASE | 0x408  | GPIO interrupt both edges register |
| GPIO4_IEV     | AS3525_GPIO4_BASE | 0x40C  | GPIO interrupt event register      |
| GPIO4_IE      | AS3525_GPIO4_BASE | 0x410  | GPIO interrupt mask register       |
| GPIO4_RIS     | AS3525_GPIO4_BASE | 0x414  | GPIO raw interrupt status          |
| GPIO4_MIS     | AS3525_GPIO4_BASE | 0x418  | GPIO masked interrupt status       |
| GPIO4_IC      | AS3525_GPIO4_BASE | 0x41C  | GPIO interrupt clear               |
| GPIO4_AFSEL   | AS3525_GPIO4_BASE | 0x420  | GPIO mode control select           |

## GPIO data register

Table 29 GPIO data register

| Name          |                    | Base                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        | Default                  |
|---------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------|
| GPIO1_DATA    |                    | AS3525_GPIO1_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | 0xC80B0000               |
| GPIO2_DATA    |                    | AS3525_GPIO2_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | 0xC80C0000               |
| GPIO3_DATA    |                    | AS3525_GPIO3_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | 0xC80D0000               |
| GPIO4_DATA    |                    | AS3525_GPIO4_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | 0xC80E0000               |
| Offset: 0x000 |                    | GPIO data register                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |                          |
|               |                    | <p>In software control mode (GPIO1_AFSEL,...), values written in this register are transferred onto the GPOUT pins if the respective pins have been configured as outputs through the GPIO1_DIR, ...</p> <p>So that GPIO bits can be set without affect to other pins in a single write operation, the address bus is used as a mask on read/write operation. The data register covers 256 locations in the address space. The eight address lines used are PADDR[9:2]. During a write, only GPIO1_DATA,... bits corresponding to HIGH address bits are updated. During a read all data bits corresponding to HIGH address bits are read, the other bits are zero.</p> <p>A read from this register returns the last bit value written if the respective pins are configured as output, or it returns the value on the corresponding input GPIN bit when these are configured as inputs. All bits are cleared by a reset.</p> |        |                          |
| Bit           | Bit Name           | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Access | Bit Description          |
| 7:0           | GPIO data register | 00000000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | RW     | Input data, output data. |

## GPIO data direction register

Table 30 GPIO data direction register

| Name          |                              | Base                                                                                                                                                 |        | Default                         |
|---------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------|
| GPIO1_DIR     |                              | AS3525_GPIO1_BASE                                                                                                                                    |        | 0xC80B0000                      |
| GPIO2_DIR     |                              | AS3525_GPIO2_BASE                                                                                                                                    |        | 0xC80C0000                      |
| GPIO3_DIR     |                              | AS3525_GPIO3_BASE                                                                                                                                    |        | 0xC80D0000                      |
| GPIO4_DIR     |                              | AS3525_GPIO4_BASE                                                                                                                                    |        | 0xC80E0000                      |
| Offset: 0x400 |                              | GPIO data direction register                                                                                                                         |        |                                 |
|               |                              | <p>Bits set to HIGH configure corresponding pin to be an output. Clearing a bit configures the pin to be input. All bits are cleared by a reset.</p> |        |                                 |
| Bit           | Bit Name                     | Default                                                                                                                                              | Access | Bit Description                 |
| 7:0           | GPIO data direction register | 00000000                                                                                                                                             | RW     | 0: pins input<br>1: pins output |

## GPIO interrupt sense register

Table 31 GPIO interrupt sense register

| Name          |                               | Base                                                                                                                                                    |        | Default                                                                               |
|---------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------|
| GPIO1_IS      |                               | AS3525_GPIO1_BASE                                                                                                                                       |        | 0xC80B0000                                                                            |
| GPIO2_IS      |                               | AS3525_GPIO2_BASE                                                                                                                                       |        | 0xC80C0000                                                                            |
| GPIO3_IS      |                               | AS3525_GPIO3_BASE                                                                                                                                       |        | 0xC80D0000                                                                            |
| GPIO4_IS      |                               | AS3525_GPIO4_BASE                                                                                                                                       |        | 0xC80E0000                                                                            |
| Offset: 0x404 |                               | GPIO interrupt sense register                                                                                                                           |        |                                                                                       |
|               |                               | Bits set to HIGH configure the corresponding pins to detect levels. Clearing a bit configures the pin to detect edges. All bits are cleared by a reset. |        |                                                                                       |
| Bit           | Bit Name                      | Default                                                                                                                                                 | Access | Bit Description                                                                       |
| 7:0           | GPIO interrupt sense register | 00000000                                                                                                                                                | RW     | 0: edge on corresponding pin is detected<br>1: level on corresponding pin is detected |

## GPIO interrupt both edges register

Table 32 GPIO interrupt both edges register

| Name          |                               | Base                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        | Default                                                                                                                                                                                                                                                                           |
|---------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1_IBE     |                               | AS3525_GPIO1_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        | 0xC80B0000                                                                                                                                                                                                                                                                        |
| GPIO2_IBE     |                               | AS3525_GPIO2_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        | 0xC80C0000                                                                                                                                                                                                                                                                        |
| GPIO3_IBE     |                               | AS3525_GPIO3_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        | 0xC80D0000                                                                                                                                                                                                                                                                        |
| GPIO4_IBE     |                               | AS3525_GPIO4_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        | 0xC80E0000                                                                                                                                                                                                                                                                        |
| Offset: 0x408 |                               | GPIO interrupt both edges register                                                                                                                                                                                                                                                                                                                                                                                                                                                     |        |                                                                                                                                                                                                                                                                                   |
|               |                               | When the corresponding bit in GPIO interrupt sense register (GPIO1_IS, ...) is set to detect edges, bits set to HIGH in GPIO interrupt both edges register (GPIO1_IBE, ...) configure the corresponding pin to detect both rising and falling edges, regardless of the corresponding bit in the GPIO interrupt event register (GPIO1_IEV, ...). Clearing a bit configures the pin to be controlled by GPIO interrupt event register (GPIO1_IEV, ...). All bits are cleared by a reset. |        |                                                                                                                                                                                                                                                                                   |
| Bit           | Bit Name                      | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Access | Bit Description                                                                                                                                                                                                                                                                   |
| 7:0           | GPIO interrupt event register | 00000000                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | RW     | 0: on corresponding pin interrupt generation event is controlled by GPIO interrupt event register (GPIO1_IEV, ...).<br>1: both edges on corresponding pin trigger an interrupt.<br>Single edge determined by corresponding bit in GPIO interrupt event register (GPIO1_IEV, ...). |

## GPIO interrupt event register

Table 33 GPIO interrupt event register

| Name          |                               | Base                                                                                                                                                                                                                                                                                                                                                                                    |        | Default                                                                                                                                              |
|---------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1_I_EV    |                               | AS3525_GPIO1_BASE                                                                                                                                                                                                                                                                                                                                                                       |        | 0xC80B0000                                                                                                                                           |
| GPIO2_I_EV    |                               | AS3525_GPIO2_BASE                                                                                                                                                                                                                                                                                                                                                                       |        | 0xC80C0000                                                                                                                                           |
| GPIO3_I_EV    |                               | AS3525_GPIO3_BASE                                                                                                                                                                                                                                                                                                                                                                       |        | 0xC80D0000                                                                                                                                           |
| GPIO4_I_EV    |                               | AS3525_GPIO4_BASE                                                                                                                                                                                                                                                                                                                                                                       |        | 0xC80E0000                                                                                                                                           |
| Offset: 0x40C |                               | GPIO interrupt event register                                                                                                                                                                                                                                                                                                                                                           |        |                                                                                                                                                      |
|               |                               | Bits set to HIGH configure the corresponding pin to detect rising edges or high levels, depending on the corresponding bit value in GPIO interrupt sense register (GPIO1_IS, ...). Clearing a bit configures the pin to detect falling edges or low levels, depending on the corresponding bit value in GPIO interrupt sense register (GPIO1_IS, ...). All bits are cleared by a reset. |        |                                                                                                                                                      |
| Bit           | Bit Name                      | Default                                                                                                                                                                                                                                                                                                                                                                                 | Access | Bit Description                                                                                                                                      |
| 7:0           | GPIO interrupt event register | 00000000                                                                                                                                                                                                                                                                                                                                                                                | RW     | 0: falling edges, or low levels on corresponding pin trigger interrupts.<br>1: rising edges, or high levels on corresponding pin trigger interrupts. |

## GPIO interrupt mask register

Table 34 GPIO interrupt mask register

| Name          |                              | Base                                                                                                                                                                                                            |        | Default                                                                                    |
|---------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------|
| GPIO1_IE      |                              | AS3525_GPIO1_BASE                                                                                                                                                                                               |        | 0xC80B0000                                                                                 |
| GPIO2_IE      |                              | AS3525_GPIO2_BASE                                                                                                                                                                                               |        | 0xC80C0000                                                                                 |
| GPIO3_IE      |                              | AS3525_GPIO3_BASE                                                                                                                                                                                               |        | 0xC80D0000                                                                                 |
| GPIO4_IE      |                              | AS3525_GPIO4_BASE                                                                                                                                                                                               |        | 0xC80E0000                                                                                 |
| Offset: 0x410 |                              | GPIO interrupt mask register                                                                                                                                                                                    |        |                                                                                            |
|               |                              | Bits set to HIGH allow the corresponding pins to trigger their individual interrupts and the combined GPIOINTR line. Clearing a bit disables interrupt triggering on that pin. All bits are cleared by a reset. |        |                                                                                            |
| Bit           | Bit Name                     | Default                                                                                                                                                                                                         | Access | Bit Description                                                                            |
| 7:0           | GPIO interrupt mask register | 00000000                                                                                                                                                                                                        | RW     | 0: corresponding pin interrupt is masked.<br>1: corresponding pin interrupt is not masked. |

## GPIO raw interrupt status register

Table 35 GPIO raw interrupt status register

| Name          |                                    | Base                                                                                                                                                                                                                                                                                                                                                                                                       |        | Default                                                                                                                                                                                        |
|---------------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1_RIS     |                                    | AS3525_GPIO1_BASE                                                                                                                                                                                                                                                                                                                                                                                          |        | 0xC80B0000                                                                                                                                                                                     |
| GPIO2_RIS     |                                    | AS3525_GPIO2_BASE                                                                                                                                                                                                                                                                                                                                                                                          |        | 0xC80C0000                                                                                                                                                                                     |
| GPIO3_RIS     |                                    | AS3525_GPIO3_BASE                                                                                                                                                                                                                                                                                                                                                                                          |        | 0xC80D0000                                                                                                                                                                                     |
| GPIO4_RIS     |                                    | AS3525_GPIO4_BASE                                                                                                                                                                                                                                                                                                                                                                                          |        | 0xC80E0000                                                                                                                                                                                     |
| Offset: 0x414 |                                    | GPIO raw interrupt status register                                                                                                                                                                                                                                                                                                                                                                         |        |                                                                                                                                                                                                |
|               |                                    | Bits read HIGH reflect the status of interrupts trigger conditions detected (raw, prior to masking), indicating that all the requirements have been met, before they are finally allowed to trigger by GPIO interrupt mask register (GPIO1_IE, ...). Bits read as LOW indicate that corresponding input pins have not initiated an interrupt. This register is read only, its bits are cleared by a reset. |        |                                                                                                                                                                                                |
| Bit           | Bit Name                           | Default                                                                                                                                                                                                                                                                                                                                                                                                    | Access | Bit Description                                                                                                                                                                                |
| 7:0           | GPIO raw interrupt status register | 00000000                                                                                                                                                                                                                                                                                                                                                                                                   | R      | Reflect the status of interrupts trigger conditions detection on pins (raw, prior to masking).<br>0: requirements not met on corresponding pins.<br>1: requirements met by corresponding pins. |

## GPIO masked interrupt status register

Table 36 GPIO masked interrupt status register

| Name          |                                       | Base                                                                                                                                                                                                                                                                                                                                                                                                                            |        | Default                                                                                                                                            |
|---------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1_MIS     |                                       | AS3525_GPIO1_BASE                                                                                                                                                                                                                                                                                                                                                                                                               |        | 0xC80B0000                                                                                                                                         |
| GPIO2_MIS     |                                       | AS3525_GPIO2_BASE                                                                                                                                                                                                                                                                                                                                                                                                               |        | 0xC80C0000                                                                                                                                         |
| GPIO3_MIS     |                                       | AS3525_GPIO3_BASE                                                                                                                                                                                                                                                                                                                                                                                                               |        | 0xC80D0000                                                                                                                                         |
| GPIO4_MIS     |                                       | AS3525_GPIO4_BASE                                                                                                                                                                                                                                                                                                                                                                                                               |        | 0xC80E0000                                                                                                                                         |
| Offset: 0x418 |                                       | GPIO masked interrupt status register                                                                                                                                                                                                                                                                                                                                                                                           |        |                                                                                                                                                    |
|               |                                       | Bits read HIGH reflect the status of input lines triggering an interrupt. Bits read as LOW indicate that either no interrupt has been generated, or the interrupt is masked. This register shows the state of the interrupt after masking. This register is read-only. All bits are cleared by a reset. The contents of this register are made available externally through the intra-chip (or on-chip) GPIO1_MIS, ... signals. |        |                                                                                                                                                    |
| Bit           | Bit Name                              | Default                                                                                                                                                                                                                                                                                                                                                                                                                         | Access | Bit Description                                                                                                                                    |
| 7:0           | GPIO masked interrupt status register | 00000000                                                                                                                                                                                                                                                                                                                                                                                                                        | R      | Masked value of interrupt due to corresponding pin.<br>0: PrimeCell GPIO line interrupt not active.<br>1: PrimeCell GPIO line asserting interrupt. |

## GPIO interrupt clear register

Table 37 GPIO interrupt clear register

| Name          |                               | Base                                                                                                                                                                                                                        |        | Default                                              |
|---------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------|
| GPIO1_IC      |                               | AS3525_GPIO1_BASE                                                                                                                                                                                                           |        | 0xC80B0000                                           |
| GPIO2_IC      |                               | AS3525_GPIO2_BASE                                                                                                                                                                                                           |        | 0xC80C0000                                           |
| GPIO3_IC      |                               | AS3525_GPIO3_BASE                                                                                                                                                                                                           |        | 0xC80D0000                                           |
| GPIO4_IC      |                               | AS3525_GPIO4_BASE                                                                                                                                                                                                           |        | 0xC80E0000                                           |
| Offset: 0x41C |                               | GPIO interrupt clear register                                                                                                                                                                                               |        |                                                      |
|               |                               | Setting a bit to HIGH in this register clears the corresponding interrupt edge detection logic register. Setting a bit to LOW in this register has no effect. This register is write-only. All bits are cleared by a reset. |        |                                                      |
| Bit           | Bit Name                      | Default                                                                                                                                                                                                                     | Access | Bit Description                                      |
| 7:0           | GPIO interrupt clear register | 00000000                                                                                                                                                                                                                    | W      | 0: has no effect.<br>1: clears edge detection logic. |

## GPIO mode control select register

Table 38 GPIO2, GPIO3 mode control select register

| Name          |                                   | Base                                                                                                                                    |        | Default                                                                                                           |
|---------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------|
| GPIO2_AFSEL   |                                   | AS3525_GPIO2_BASE                                                                                                                       |        | 0xC80C0000                                                                                                        |
| GPIO3_AFSEL   |                                   | AS3525_GPIO3_BASE                                                                                                                       |        | 0xC80D0000                                                                                                        |
| Offset: 0x420 |                                   | GPIO mode control select register                                                                                                       |        |                                                                                                                   |
|               |                                   | Setting a bit to HIGH in this register selects DBOP control for the corresponding PrimeCell GPIO line. All bits are cleared by a reset. |        |                                                                                                                   |
| Bit           | Bit Name                          | Default                                                                                                                                 | Access | Bit Description                                                                                                   |
| 7:0           | GPIO mode control select register | 00000000                                                                                                                                | RW     | 0: enables software control mode on corresponding pin.<br>Bits 1: enables DBOP control mode on corresponding pin. |

Table 39 GPIO1, GPIO4 mode control select register

| Name          |                                   | Base                                                                  |        | Default                                                                                             |
|---------------|-----------------------------------|-----------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------|
| GPIO1_AFSEL   |                                   | AS3525_GPIO1_BASE                                                     |        | 0xC80B0000                                                                                          |
| GPIO4_AFSEL   |                                   | AS3525_GPIO4_BASE                                                     |        | 0xC80E0000                                                                                          |
| Offset: 0x420 |                                   | GPIO mode control select register                                     |        |                                                                                                     |
|               |                                   | Not used. If bit set to HIGH, the corresponding pin will be set to 1. |        |                                                                                                     |
| Bit           | Bit Name                          | Default                                                               | Access | Bit Description                                                                                     |
| 7:0           | GPIO mode control select register | 00000000                                                              | RW     | Bits 0: enables software control mode on corresponding pin.<br>Bits 1: corresponding pins set to 1. |

### 7.3.5 MCI – SD / MMC Card Interface

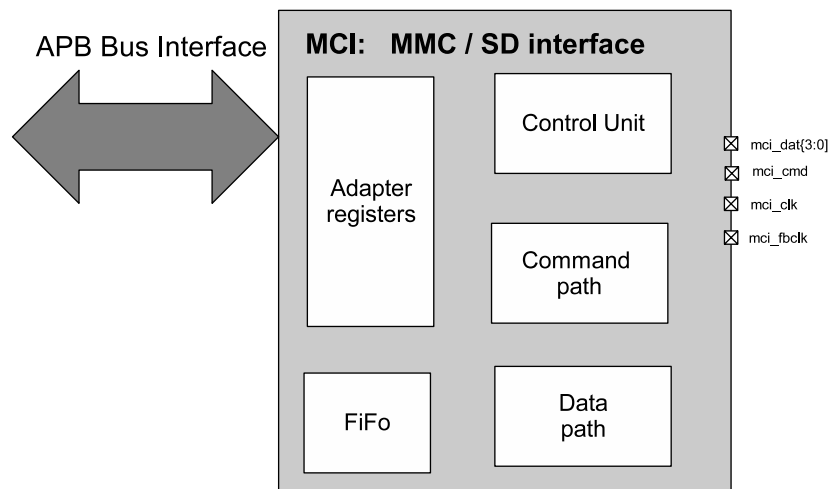
#### Features

- Conformance to Multimedia Card Specification v2.11
- Conformance to Secure Digital Memory Card Physical Layer Specification, v0.96
- uses multimedia card bus or SD card bus.

The PrimeCell™ MCI provides an interface between the APB system bus and multimedia and/or secure digital memory cards. It consists of two parts:

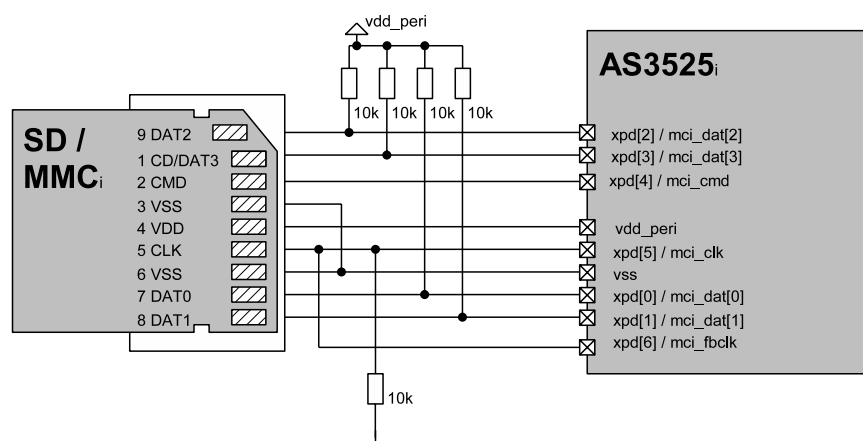
- The PrimeCell™ MCI adapter block includes the clock generation unit, the power management control, command and data transfer
- the APB interface provides access to the MCI adapter registers, and generates interrupt and DMA request signals.

Figure 21 Multimedia Card Interface Block Diagram



The connections to the Multimedia Card Interface are shared with the General Purpose I/O port-D (GPIO xpd[0:7]). Following diagram shows the external circuit elements for connection to a SD card adapter. Note that a feedback clock must be routed back to xpd[6]/mci\_fbclk.

Figure 22 Connecting SD / MC to GPIO-D



### 7.3.6 I2cAudMas - I2C audio master interface

This is the control interface between the digital and the audio-part. The corresponding signal lines are connected inside of the MCM on the BGA substrate. For test purposes of the audio chip only, the signals are available at dedicated balls.

- The key features of this interface block are:
- serial 2-wire I2C bus master
- supports standard (100 kbps) and fast speed (400kbps)
- 7-bit addressing
- sub-addressing
- programmable clock divider
- programmable transfer count
- soft reset bit
- interrupt generation (on RX Full, TX Empty, RX Overrun, no acknowledge received)
- status register
- test register

Figure 23 I2C Audio Master Interface Block Diagram

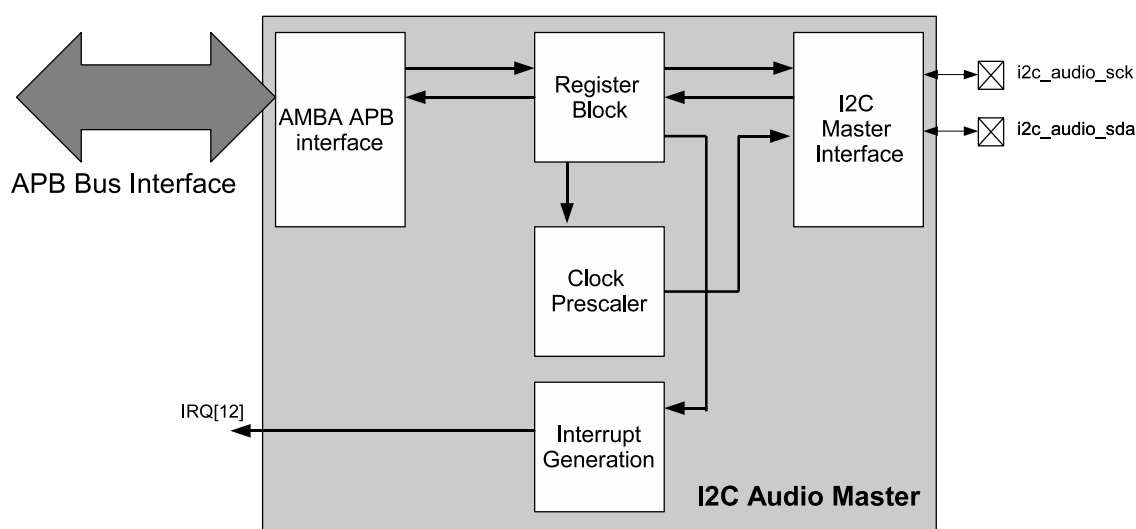


Table 40 I2C Audio Master Registers

| Register Name | Base Address          | Offset | Note                                                                     |
|---------------|-----------------------|--------|--------------------------------------------------------------------------|
| I2C2_DATA     | AS3525_I2C_AUDIO_BASE | 0x00   | transmit/receive FIFO data register                                      |
| I2C2_SLAD0    | AS3525_I2C_AUDIO_BASE | 0x04   | slave ID register                                                        |
| I2C2_CNTRL    | AS3525_I2C_AUDIO_BASE | 0x0C   | control register                                                         |
| I2C2_DACNT    | AS3525_I2C_AUDIO_BASE | 0x10   | master data count register                                               |
| I2C2_CPSR0    | AS3525_I2C_AUDIO_BASE | 0x1C   | clock prescale register 0                                                |
| I2C2_CPSR1    | AS3525_I2C_AUDIO_BASE | 0x20   | clock prescale register 1                                                |
| I2C2_IMR      | AS3525_I2C_AUDIO_BASE | 0x24   | interrupt mask register                                                  |
| I2C2_RIS      | AS3525_I2C_AUDIO_BASE | 0x28   | raw interrupt status register                                            |
| I2C2_MIS      | AS3525_I2C_AUDIO_BASE | 0x2C   | masked interrupt status register                                         |
| I2C2_SR       | AS3525_I2C_AUDIO_BASE | 0x30   | I2C status register                                                      |
| I2C2_INT_CLR  | AS3525_I2C_AUDIO_BASE | 0x40   | interrupt clear register                                                 |
| I2C2_SADDR    | AS3525_I2C_AUDIO_BASE | 0x44   | sub-address register                                                     |
| I2C2_TESTIN   | AS3525_I2C_AUDIO_BASE | 0x50   | test register (monitors state of SCL and SDA)                            |
| I2C2_TESTOUT1 | AS3525_I2C_AUDIO_BASE | 0x54   | test mode register for driving output interrupt                          |
| I2C2_TESTOUT2 | AS3525_I2C_AUDIO_BASE | 0x58   | test mode register for driving SCLout, SCLOEn, SDAOUT and SDAOEN signals |

### 7.3.7 I2CMSI - I2C master/slave interface

This is a general control interface for chip-to-chip communication. The corresponding IOs are either used by the general purpose port C (xpc[6:7]) or by this I2C interface.

The features of this interface block are:

- serial 2-wire I2C bus master
- supports standard (100 kbps) and fast speed (400kbps)
- supports multi-master system architecture
- programmable clock divider
- programmable transfer count
- programmable slave wait enable (for slave mode of operation, insertion of wait on the bus)
- soft reset bit
- interrupt generation (on RX Full, TX Empty, RX Overrun, no acknowledge received)
- status register
- test register

Figure 24: I2C Interface

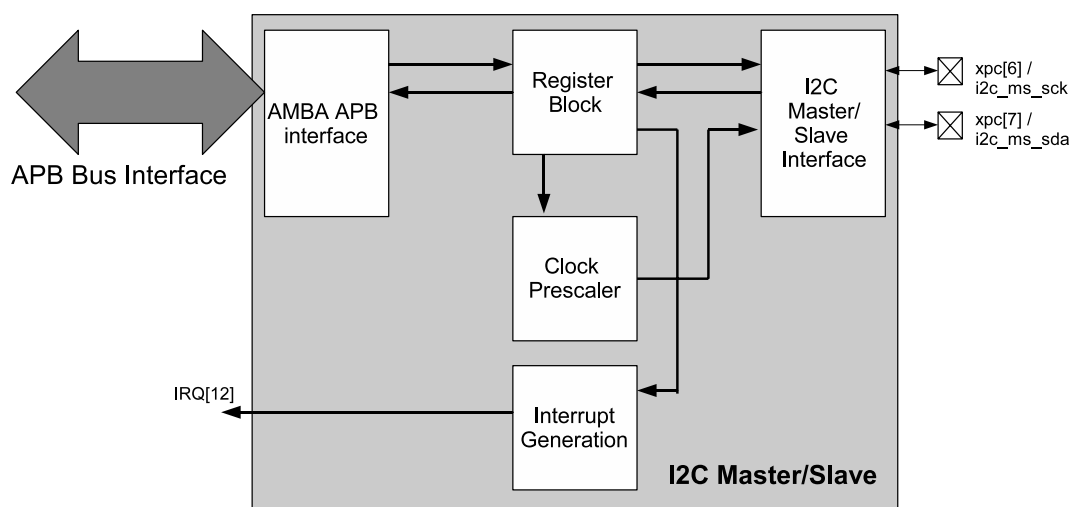


Table 41 I2C Interface Registers

| Register Name | Base Address       | Offset | Note                                                                     |
|---------------|--------------------|--------|--------------------------------------------------------------------------|
| I2C1_DATA     | AS3525_I2C_MS_BASE | 0x00   | transmit/receive FIFO data register                                      |
| I2C1_SLAD0    | AS3525_I2C_MS_BASE | 0x04   | slave ID register 0                                                      |
| I2C1_SLAD1    | AS3525_I2C_MS_BASE | 0x08   | slave ID register 1                                                      |
| I2C1_CNTRL    | AS3525_I2C_MS_BASE | 0x0C   | control register                                                         |
| I2C1_DACNT    | AS3525_I2C_MS_BASE | 0x10   | master data count register                                               |
| I2C1_SEAD0    | AS3525_I2C_MS_BASE | 0x14   | self ID of slave 0                                                       |
| I2C1_SEAD1    | AS3525_I2C_MS_BASE | 0x18   | self ID of slave 1                                                       |
| I2C1_CPSR0    | AS3525_I2C_MS_BASE | 0x1C   | clock prescale register 0                                                |
| I2C1_CPSR1    | AS3525_I2C_MS_BASE | 0x20   | clock prescale register 1                                                |
| I2C1_IMR      | AS3525_I2C_MS_BASE | 0x24   | interrupt mask register                                                  |
| I2C1_RIS      | AS3525_I2C_MS_BASE | 0x28   | raw interrupt status register                                            |
| I2C1_MIS      | AS3525_I2C_MS_BASE | 0x2C   | masked interrupt status register                                         |
| I2C1_SR       | AS3525_I2C_MS_BASE | 0x30   | I2C status register                                                      |
| I2C1_TXCNT    | AS3525_I2C_MS_BASE | 0x34   | transmit Fifo data count register                                        |
| I2C1_RXCNT    | AS3525_I2C_MS_BASE | 0x38   | receive Fifo data count register                                         |
| I2C1_TX_FLUSH | AS3525_I2C_MS_BASE | 0x3C   | TX Fifo flush register                                                   |
| I2C1_INT_CLR  | AS3525_I2C_MS_BASE | 0x40   | interrupt clear register                                                 |
| I2C1_TESTIN   | AS3525_I2C_MS_BASE | 0x50   | test register (monitors state of SCL and SDA)                            |
| I2C1_TESTOUT1 | AS3525_I2C_MS_BASE | 0x54   | test mode register for driving output interrupt                          |
| I2C1_TESTOUT2 | AS3525_I2C_MS_BASE | 0x58   | test mode register for driving SCLout, SCLOEn, SDAOUT and SDAOEN signals |

### 7.3.8 I2SIN - I2S input interface

The I2S input interface module (called I2SINIF module hereafter) is used to connect an external audio source to the processor system. The communication is based on the standardized I2S interface. The interface module connects to the processor system using the AMBA APB bus.

All the input left & right channel data are mapped to either 14 or 24 bit format, selectable within the control register. If the data word length is less than 24 bit, the unused lower bits are set to zero. To reduce the interrupt frequency for the processor, a FIFO buffer is provided. The buffer can hold up to 32 words of 48 bit length (left plus right channel).

Generation of interrupt request signal with several maskable interrupt sources (Pop Full, Pop Empty, Pop Error, Push Error, ...etc)

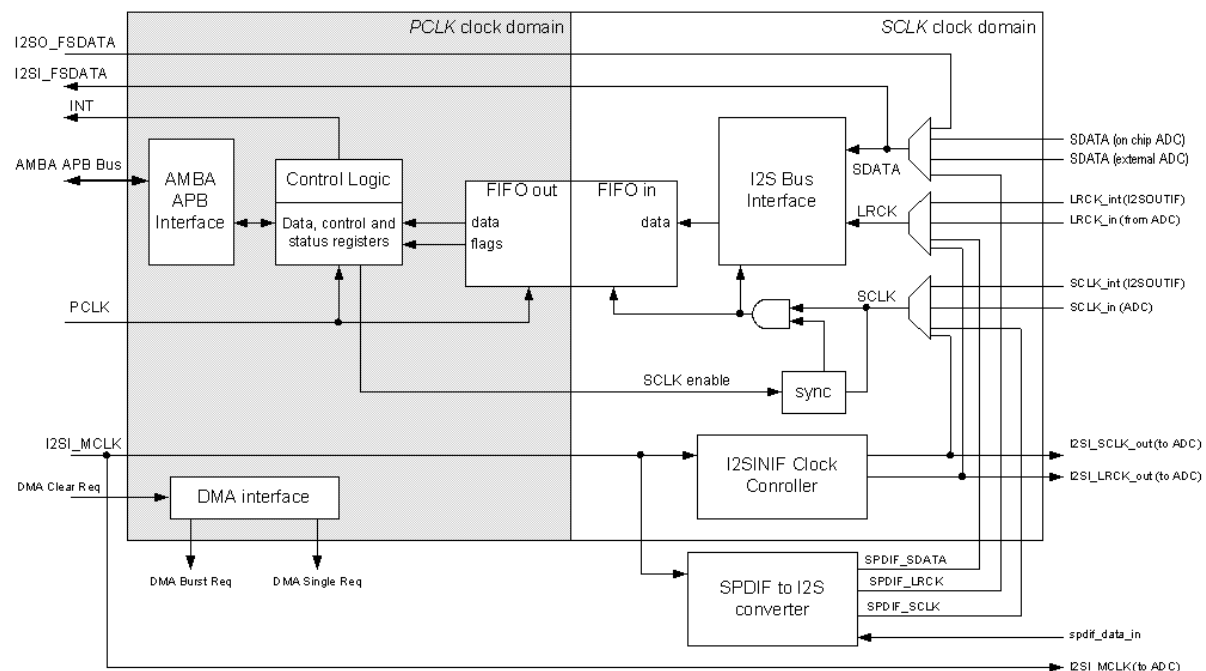
The I2SINIF provides the following features:

- two independent clock domains: AMBA APB clock PCLK, I2S input clock i2si\_sclk
- FIFO (32 words/48 bit) separating clock domains
- support of several oversampling rates: 128x, 256x, 512x
- interrupt support for FIFO data read
- DMA support for FIFO data transfer

The I2SINIF provides five different modes:

- input from on-chip audio ADC
- input from external audio ADC in master mode (SCLK, LRCK generated by external ADC)
- input from external audio ADC in slave mode (SCLK, LRCK, MCLK generated internally and fed to external ADC)
- input from SPDIF (SPDIF to I2S converter)
- feedback mode with input from I2S output interface: used for test purposes

Figure 25 I2S Input Interface



## 7.3.8.1 I2S Input Register Mapping

## I2S Input Interface Registers

Table 42 I2S Input Interface Registers

| Register Name      | Base Address      | Offset | Note                          |
|--------------------|-------------------|--------|-------------------------------|
| I2SIN_CONTROL      | AS3525_I2SIN_BASE | 0x0000 | Control register              |
| I2SIN_MASK         | AS3525_I2SIN_BASE | 0x0004 | Interrupt mask register       |
| I2SIN_RAW_STATUS   | AS3525_I2SIN_BASE | 0x0008 | Raw status register           |
| I2SIN_STATUS       | AS3525_I2SIN_BASE | 0x000C | Status register               |
| I2SIN_CLEAR        | AS3525_I2SIN_BASE | 0x0010 | Interrupt clear register      |
| I2SIN_DATA         | AS3525_I2SIN_BASE | 0x0014 | Audio data register           |
| I2SIN_SPDIF_STATUS | AS3525_I2SIN_BASE | 0x0018 | SPDIF status signals register |

Table 43 I2S Input Control Register

| Name           |                | Base                                                                        |        | Default                                                                                                                                                                                                                                                                  |
|----------------|----------------|-----------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I2SIN_CONTROL  |                | AS3525_I2SIN_BASE                                                           |        | 0x04                                                                                                                                                                                                                                                                     |
| Offset: 0x0000 |                | Control register                                                            |        |                                                                                                                                                                                                                                                                          |
|                |                | 12 bit wide read/write register containing the control bits of the I2SINIF. |        |                                                                                                                                                                                                                                                                          |
| Bit            | Bit Name       | Default                                                                     | Access | Bit Description                                                                                                                                                                                                                                                          |
| 11             | DMA_req_en     | 0                                                                           | R/W    | DMA request enable<br>0: disable<br>1: enable                                                                                                                                                                                                                            |
| 10             | mclk_invert    | 0                                                                           | R/W    | Invert MCLK<br>0: disable (SCLK changes at MCLK's falling edge)<br>1: enable (SCLK changes at MCLK's rising edge)                                                                                                                                                        |
| 9,8            | i2s_clk_source | 00                                                                          | R/W    | Define the source of SCLK and LRCK for I2SINIF<br>00: SCLK and LRCK from I2SOUTIF (used if AFE sends data)<br>01: SCLK and LRCK from external ADC device (outside AS3525)<br>10: SCLK and LRCK from SPDIF converter<br>11: SCLK and LRCK from I2SINIF's clock controller |
| 7,6            | sdata_source   | 00                                                                          | R/W    | Define the source of SDATA for I2SINIF<br>00: SDATA from AFE<br>01: SDATA from external ADC device (outside AS3525)<br>10: SDATA from SPDIF converter<br>11: loopback SDATA from I2SOUTIF (test purpose)                                                                 |
| 5              | 14bit_mode     | 0                                                                           | R/W    | 0: ADC data from FIFO transferred in two 32-bit words to I2SIN_DATA (first left and then right data as indicated by the stereo24_status bit)<br>1: ADC data from FIFO transferred in one 32-bit word to I2SIN_DATA                                                       |
| 4              | sclk_idle      | 0                                                                           | R/W    | Enable/disable SCLK for I2SINIF<br>0: SCLK enabled<br>1: SCLK disabled                                                                                                                                                                                                   |
| 3              | SDATA_valid    | 0                                                                           | R/W    | 0: SDATA ignored at first SCLK edge (I2S standard)<br>1: valid SDATA at first SCLK edge                                                                                                                                                                                  |
| 2              | sclk_edge      | 1                                                                           | R/W    | 0: data valid at negative edge of SCLK<br>1: data valid at positive edge of SCLK                                                                                                                                                                                         |
| 1,0            | osr            | 00                                                                          | R/W    | Oversampling rate (needed for generating sclk and lrck)<br>00: 128x<br>01: 256x<br>10: 512x<br>11: 128x                                                                                                                                                                  |

The following table shows the valid combinations for sdata\_source (bit 7 and 6) and i2s\_clk\_source (bit 9 and 8) of the I2SIN\_CONTROL register.

| sdata_source | i2s_clk_source | Description                         |
|--------------|----------------|-------------------------------------|
| 00           | 00             | default mode (AFE with AS3525)      |
| 01           | 00             | external data, external clock       |
| 01           | 11             | external data, internal clock       |
| 10           | 10             | data and clock from SPDIF converter |
| 11           | 00             | loopback, internal data and clock   |

Table 44 I2S Input mask register

| Name           |                 | Base                                                                                                                   |        | Default                                          |
|----------------|-----------------|------------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------|
| I2SIN_MASK     |                 | AS3525_I2SIN_BASE                                                                                                      |        | 0x00                                             |
| Offset: 0x0004 |                 | Interrupt mask register                                                                                                |        |                                                  |
|                |                 | The interrupt mask register determines which status flags generate an interrupt by setting the corresponding bit to 1. |        |                                                  |
| Bit            | Bit Name        | Default                                                                                                                | Access | Bit Description                                  |
| 7              | reserved        | 0                                                                                                                      | R/W    | stereo24_status cannot assert interrupt request  |
| 6              | I2SIN_MASK_PUER | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH error interrupt          |
| 5              | I2SIN_MASK_POE  | 0                                                                                                                      | R/W    | 1 enables the FIFO POP is empty interrupt        |
| 4              | I2SIN_MASK_POAE | 0                                                                                                                      | R/W    | 1 enables the FIFO POP is almost empty interrupt |
| 3              | I2SIN_MASK_POHF | 0                                                                                                                      | R/W    | 1 enables the FIFO POP is half full interrupt    |
| 2              | I2SIN_MASK_POAF | 0                                                                                                                      | R/W    | 1 enables the FIFO POP is almost full interrupt  |
| 1              | I2SIN_MASK_POF  | 0                                                                                                                      | R/W    | 1 enables the FIFO POP is full interrupt         |
| 0              | I2SIN_MASK_POER | 0                                                                                                                      | R/W    | 1 enables the FIFO POP error interrupt           |

Table 45 I2S Input raw status register

| Name             |                 | Base                                                                                                                                                                                                                                                                                                                                                                                                                                    |        | Default                                                                                                                                             |
|------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| I2SIN_RAW_STATUS |                 | AS3525_I2SIN_BASE                                                                                                                                                                                                                                                                                                                                                                                                                       |        | 0x00                                                                                                                                                |
| Offset: 0x0008   |                 | Raw status register                                                                                                                                                                                                                                                                                                                                                                                                                     |        |                                                                                                                                                     |
|                  |                 | The read-only raw status register contains the actual bit values as reflected by the FIFO controller status signals. I2SIN_PUER and I2SIN_POER are static bits, since FIFO controller gives the PUSH/POP error bit only for one clock. This means that these two bits remain asserted until they are cleared in the I2SIN_CLEAR register. All other bits change state depending on the underlying logic, i.e. state of FIFO controller. |        |                                                                                                                                                     |
| Bit              | Bit Name        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                 | Access | Bit Description                                                                                                                                     |
| 7                | stereo24_status | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | Status of write interface for 24 bit stereo mode<br>0: left audio sample will be transferred next<br>1: right audio sample will be transferred next |
| 6                | I2SIN_PUER      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO PUSH error                                                                                                                                |
| 5                | I2SIN_POE       | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP is empty                                                                                                                              |
| 4                | I2SIN_POAE      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP is almost empty                                                                                                                       |
| 3                | I2SIN_POHF      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP is half full                                                                                                                          |
| 2                | I2SIN_POAF      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP is almost full                                                                                                                        |
| 1                | I2SIN_POF       | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP is full                                                                                                                               |
| 0                | I2SIN_POER      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 1 if FIFO POP error                                                                                                                                 |

Table 46 I2S input status register

| Name           |                 | Base                                                                                                                                                                                      |        | Default                                                                                                                                             |
|----------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| I2SIN_STATUS   |                 | AS3525_I2SIN_BASE                                                                                                                                                                         |        | 0x00                                                                                                                                                |
| Offset: 0x000C |                 | Status register                                                                                                                                                                           |        |                                                                                                                                                     |
|                |                 | The status register is a read-only register. A read to this register returns the value of the raw status bits AND'ed with the corresponding mask of enable bits set in the mask register. |        |                                                                                                                                                     |
| Bit            | Bit Name        | Default                                                                                                                                                                                   | Access | Bit Description                                                                                                                                     |
| 7              | stereo24_status | 0                                                                                                                                                                                         | R      | Status of write interface for 24 bit stereo mode<br>0: left audio sample will be transferred next<br>1: right audio sample will be transferred next |
| 6              | I2SIN_PUER      | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH error                                                                                                                                |
| 5              | I2SIN_POE       | 0                                                                                                                                                                                         | R      | 1 if FIFO POP is empty                                                                                                                              |
| 4              | I2SIN_POAE      | 0                                                                                                                                                                                         | R      | 1 if FIFO POP is almost empty                                                                                                                       |
| 3              | I2SIN_POHF      | 0                                                                                                                                                                                         | R      | 1 if FIFO POP is half full                                                                                                                          |
| 2              | I2SIN_POAF      | 0                                                                                                                                                                                         | R      | 1 if FIFO POP is almost full                                                                                                                        |
| 1              | I2SIN_POF       | 0                                                                                                                                                                                         | R      | 1 if FIFO POP is full                                                                                                                               |
| 0              | I2SIN_POER      | 0                                                                                                                                                                                         | R      | 1 if FIFO POP error                                                                                                                                 |

Table 47 I2S Input interrupt clear register

| Name           |                  | Base                                                                                                                                                                                                                                                                                                                    |        | Default                         |
|----------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------|
| I2SIN_CLEAR    |                  | AS3525_I2SIN_BASE                                                                                                                                                                                                                                                                                                       |        | 0x00                            |
| Offset: 0x0010 |                  | Interrupt clear register                                                                                                                                                                                                                                                                                                |        |                                 |
|                |                  | The interrupt clear register is a write-only register. The corresponding static status bit can be cleared by writing a 1 to the corresponding bit in the clear register. All other interrupt flags are level interrupts depending on the status of the FIFO. The bits are de-asserted depending on the FIFO controller. |        |                                 |
| Bit            | Bit Name         | Default                                                                                                                                                                                                                                                                                                                 | Access | Bit Description                 |
| 7              | reserved         |                                                                                                                                                                                                                                                                                                                         | W      |                                 |
| 6              | I2SIN_clear_puer |                                                                                                                                                                                                                                                                                                                         | W      | Clear PUSH error interrupt flag |
| 5:1            | reserved         |                                                                                                                                                                                                                                                                                                                         | W      |                                 |
| 0              | I2SIN_clear_poer |                                                                                                                                                                                                                                                                                                                         | W      | Clear POP error interrupt flag  |

## I2SIN\_DATA

The I2SINIF provides a single 32 bit wide data register. The register is used to read the audio samples from FIFO. If 14 bit mode is selected, both the left and right data are made available in the same register. Otherwise in the 24 bit mode the left and right data are provided through the same register alternatively. The stereo24\_status bit in the I2SIN\_STATUS register provides information which channel's data will be provided next. The 14bit\_mode bit in the I2SIN\_CONTROL register defines how the values are read from the FIFO.

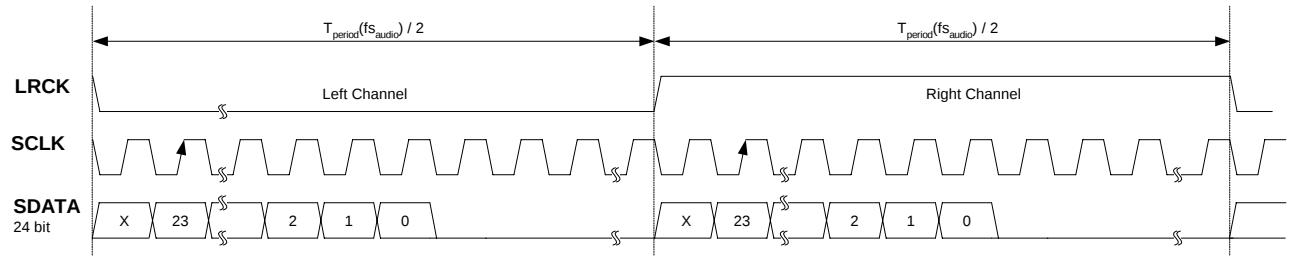
### 7.3.8.2 I2S Input Signals

The following specifications signals are given:

- Data are valid at rising/falling edge of SCLK (depending on I2SI\_CONTROL's setting).
- The left and right channels are indicated by the LRCK signal.

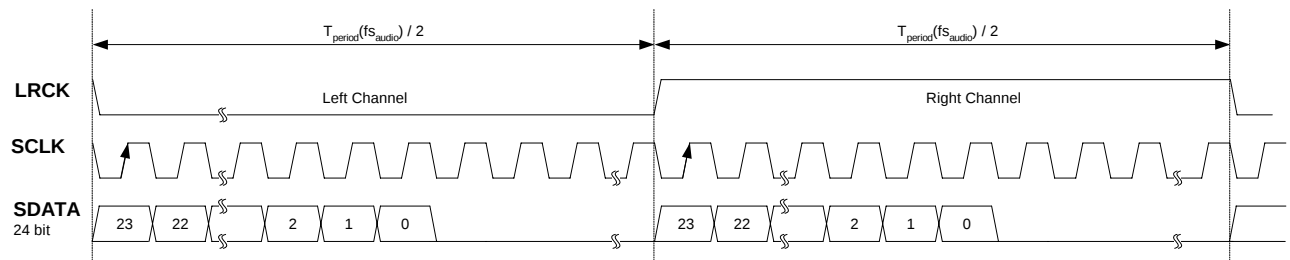
The timing diagram of the standard I2S interface signals from the ADC is shown below (Figure 29).

Figure 26 - I2S standard timing diagram



While the I2S standard states that the LRCK line changes one clock cycle before the MSB is transmitted. If the ADC sends the MSB directly after LRCK line changes, the *SDATA\_valid* bit in the I2SI\_CONTROL register must be set.

Figure 27 - I2S standard timing diagram with SDATA valid directly after LRC changes



Assumption: The LRCK toggles every 32 clocks of SCLK.

### 7.3.8.3 Power Modes

The I2SINIF contains two clock domains. The PCLK domain can be turned off in the clock controller. The SCLK clock domain can be turned off locally using the SCLK\_idle bit in the I2SIN\_CONTROL register. Note that the SCLK's clock gating signal has to be synchronized with the SCLK clock in order to guarantee correct operation.

If PCLK is turned off, no interrupt must be triggered by the I2SINIF module.

The I2SI\_MCLK clock can be turned on/off in the clock generation unit.

### 7.3.8.4 Loopback Feature

On the AS3525 are two I2S interfaces:

- I2SOUTIF is responsible to send values to the DAC of the audio chip via I2SO\_SDATA
- I2SINIF is responsible to receive audio values from ADC of the audio chip via I2SI\_SDATA

In the AS3525 both SDATA signals are provided as loopback signals (I2SO\_FSDATA, I2SI\_FSDATA):

- I2SO\_SDATA to I2SINIF: This loopback is mainly for testing the transmit and receive paths of both I2S interfaces. The loopback signal is called I2SO\_FSDATA.
- I2SI\_SDATA to I2SOUTIF: This loopback feature allows the application to echo the input audio samples directly to a loudspeaker. The signal provided by the I2SINIF is called I2SI\_FSDATA.

In normal mode the I2SINIF pushes audio values into the FIFO based on the I2SI\_SDATA signal. If the loopback feature is enabled, the *sddata\_source* bit in the control register must be set to 3. The FIFO content is filled with audio values send by the I2SOUTIF (signal I2SO\_FSDATA).

NOTE: This feature will only be available if SCLK is the same for I2S input and output interface. For implementation the I2SO\_FSDATA signal is simply routed through a multiplexer to the I2SI\_SDATA interface.

### 7.3.8.5 DMA Interface

The I2SINIF supports DMA transfers. The DMA controller supports incrementing and non-incrementing (single address) addressing for source and destination. For I2SINIF the single-address mode is used. The address of the I2SI\_DATA register is used as DMA source address.

### 7.3.8.6 The 24 bit Stereo DMA Mode

In 24 bit stereo mode, right and left audio samples must be read separately from the FIFO. In single-address DMA-mode both data must be read from the same address. The I2SINIF is responsible to split up the 48 bit FIFO entries into two 24 bit samples. The 24 bit value can then be transferred via the 32 bit wide AMBA bus.

The I2SINIF provides the data in a specific order: first the left value is sent, and afterwards the right value is provided. Then a left value follows, and so on. In the destination memory the words are stored incrementally as shown below.

| Address    | Value   |
|------------|---------|
| addr 0     | LDATA 0 |
| addr 1     | RDATA 0 |
| addr 2     | LDATA 1 |
| addr 3     | RDATA 1 |
| ...        | ...     |
| addr n*2   | LDATA n |
| addr n*2+1 | RDATA n |

### 7.3.9 SPDIF interface

As part of the I2SIN module also a SPDIF receiver interface is included. This SPDIF interface works as converter from SPDIF-AES/EBU to I2S.

The SPDIF-AES/EBU standard is a serial audio interface that conveys 2 time-multiplexed audio channels, the left and right channels, as is the case in audio stereo transmission. The two channels are encoded in a 64-bit frame. Each individual channel is encoded in a sub-frame that consists of a 4-bit preamble, followed by 24 bits of audio data and 4 control bits, in a total of 32 bits per sub-frame. The SPDIF-AES/EBU standard provides for LSB first, up to 24-bit audio samples. Samples of 20 bits or less may be used, in which case the 4 least significant bits may be used for a 12-bit monitoring channel, transmitted at 1/3 of the sample rate. Please refer to the SPDIF-AES/EBU, AES3 or IEC958 standard documentation for more information.

#### Features

- Feed-forward operation: extracts audio data from the SPDIF-AES/EBU input signal by sampling it with a fast clock signal which not necessarily related to the sample rate frequency
- Purely digital receiver solution, without need of an input PLL for synchronisation.
- The audio samples are output serially in I2S format.
- PLL interface to filter out the jitter and generate a jitter-free I2S output.
- Recognizes all common audio and video related sample frequencies and outputs a nibble code for each.

#### 7.3.9.1 SPDIF register description

Table 48 SPDIF status register

| Name               |                                | Base                                                                                                                                                                                                                                                                                                                                   |        | Default                                                                                                                                      |
|--------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------|
| I2SIN_SPDIF_STATUS |                                | AS3525_I2SIN_BASE                                                                                                                                                                                                                                                                                                                      |        | 0x00                                                                                                                                         |
| Offset: 0x0018     |                                | SPDIF status signals register                                                                                                                                                                                                                                                                                                          |        |                                                                                                                                              |
|                    |                                | This read-only register contains status information of the SPDIF interface. The <code>spdif_sample_freq</code> and <code>spdif_sync</code> status bits are directly derived from the SPDIF converter. In order to provide valid status bits, these signals must be synchronized with <code>pclk</code> , i.e. <code>clk_i2sin</code> . |        |                                                                                                                                              |
| Bit                | Bit Name                       | Default                                                                                                                                                                                                                                                                                                                                | Access | Bit Description                                                                                                                              |
| 4:1                | <code>spdif_sample_freq</code> |                                                                                                                                                                                                                                                                                                                                        | R      | Incoming sample frequency                                                                                                                    |
| 0                  | <code>spdif_sync</code>        |                                                                                                                                                                                                                                                                                                                                        | R      | Recognition of sub-frame preamble<br>0: first sub-frame preamble not recognized<br>1: successful recognition of the first sub-frame preamble |

The following table shows the input sample rate in KHz according to the `sample_freq_code` (bit 5 to 1) in the I2SIN\_SPDIF register.

| sample_freq_code | Input Sample Rate (KHz) |
|------------------|-------------------------|
| 0001             | 22.050                  |
| 0010             | 24.000                  |
| 0011             | 32.000                  |
| 0100             | 44.100                  |
| 0101             | 48.000                  |
| 0110             | 64.000                  |
| 0111             | 88.200                  |
| 1000             | 96.000                  |
| 1001             | 176.400                 |
| 1010             | 192.000                 |

### 7.3.10 I2SOUT - I2S output interface

The I2S output interface module (called I2SOUTIF module hereafter) is used to connect the processor system to an audio DAC. The communication is based on the standardized I2S interface. The audio samples are transferred from the processor to the I2SOUTIF module using the AMBA APB bus. A FIFO for 128 dual-channel audio samples is provided as a data buffer. Furthermore, the module provides a set of data, control and status registers.

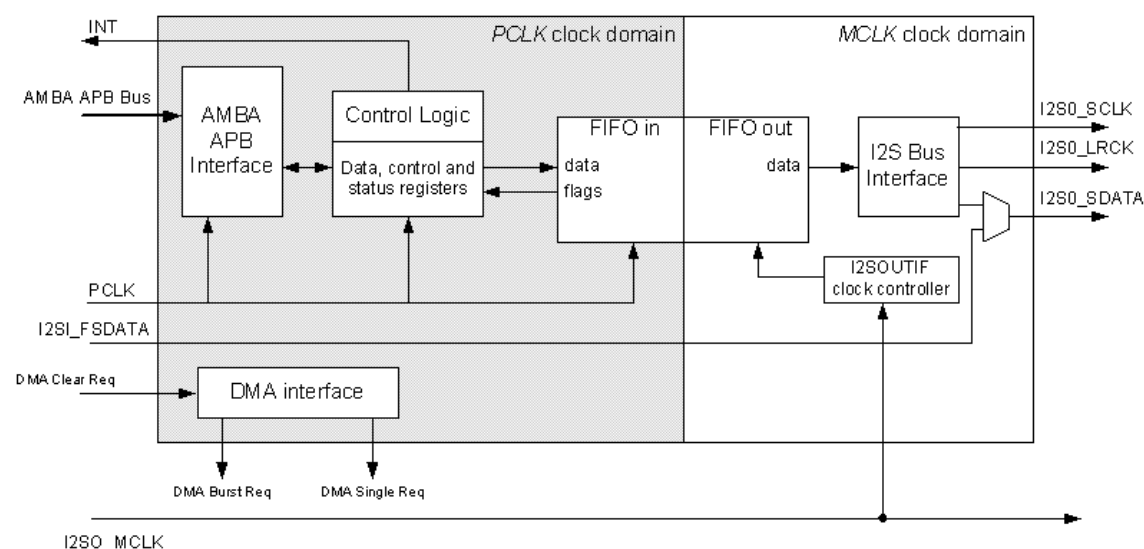
The I2SOUTIF provides the following features:

- two independent clock domains: AMBA APB clock PCLK, I2S output clock i2so\_mclk
- FIFO (128 words with 36 bit) separating clock domains
- support of 16 and 18 bit audio samples
- clock generator for I2S clocks (LCLK, I2SO\_SCLK)
- support of several oversampling rates: 128x, 256x, 512x
- interrupt support for FIFO data write
- DMA support for FIFO data transfer

For data output, following modes are implemented:

- two 18 bit audio samples, one for each channel (R,L). The values are written to I2SO\_DATA.
- two 16 bit audio samples, one for each channel (R,L). Both values are written to the 32-bit wide I2SO\_DATA register at the same time. This mode is highly efficient for 32-bit processor architectures.
- one 18 bit mono audio sample; the sample is used for both channels (R and L). The value is written to the I2SO\_DATA.
- one 16 bit mono audio sample; the sample is used for both channels (R and L). The value is written to the I2SO\_DATA.

Figure 28 I2SO Block Diagram



#### 7.3.10.1 I2S Output Interface Registers

Table 49 I2S Output Interface Registers

| Register Name     | Base Address       | Offset | Note                     |
|-------------------|--------------------|--------|--------------------------|
| I2SOUT_CONTROL    | AS3525_I2SOUT_BASE | 0x0000 | Control register         |
| I2SOUT_MASK       | AS3525_I2SOUT_BASE | 0x0004 | Interrupt mask register  |
| I2SOUT_RAW_STATUS | AS3525_I2SOUT_BASE | 0x0008 | Raw status register      |
| I2SOUT_STATUS     | AS3525_I2SOUT_BASE | 0x000C | Status register          |
| I2SOUT_CLEAR      | AS3525_I2SOUT_BASE | 0x0010 | Interrupt clear register |
| I2SOUT_DATA       | AS3525_I2SOUT_BASE | 0x0014 | Audio data register      |

Table 50 I2SOUT control register

| Name           |             | Base                                                                        |        | Default                                                                                                                                                  |
|----------------|-------------|-----------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| I2SOUT_CONTROL |             | AS3525_I2SOUT_BASE                                                          |        | 0x0C                                                                                                                                                     |
| Offset: 0x0000 |             | Control register                                                            |        |                                                                                                                                                          |
|                |             | 7 bit wide read/write register containing the control bits of the I2SOUTIF. |        |                                                                                                                                                          |
| Bit            | Bit Name    | Default                                                                     | Access | Bit Description                                                                                                                                          |
| 6              | DMA_req_en  | 0                                                                           | R/W    | DMA request enable<br>0: disable<br>1: enable                                                                                                            |
| 5              | sdata_lb    | 0                                                                           | R/W    | I2SDATA loopback from I2SINIF<br>0: I2SOUT_SDATA source is I2SOUTIF's FIFO<br>1: I2SOUT_SDATA source is loopback value from I2SINIF (signal I2SIN_FDATA) |
| 4              | mclk_invert | 0                                                                           | R/W    | Invert MCLK<br>0: disable (SCLK changes at MCLK's falling edge)<br>1: enable (SCLK changes at MCLK's rising edge)                                        |
| 3              | stereo_mode | 1                                                                           | R/W    | Audio samples provided by processor<br>0: mono<br>1: stereo                                                                                              |
| 2              | 18bit_mode  | 1                                                                           | R/W    | Bit width of audio samples provided by processor<br>0: 16 bit<br>1: 18 bit                                                                               |
| 1,0            | osr         | 00                                                                          | R/W    | Oversampling rate<br>00: 128x<br>01: 256x<br>10: 512x<br>11: 128x                                                                                        |

CAUTION: The control bit sdata\_lb can only be set, if the I2SIN\_FSDATA is synchronous to I2SOUT\_SCLK. This is the case if AFE is used together with the AS3525 (in this case the I2SINIF uses also I2SOUT\_CLK).

Table 51 I2S Output mask register

| Name           |                  | Base                                                                                                                   |        | Default                                           |
|----------------|------------------|------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------|
| I2SOUT_MASK    |                  | AS3525_I2SOUT_BASE                                                                                                     |        | 0x00                                              |
| Offset: 0x0004 |                  | Interrupt mask register                                                                                                |        |                                                   |
|                |                  | The interrupt mask register determines which status flags generate an interrupt by setting the corresponding bit to 1. |        |                                                   |
| Bit            | Bit Name         | Default                                                                                                                | Access | Bit Description                                   |
| 7              | reserved         | 0                                                                                                                      | R/W    | stereo18_status cannot assert interrupt request   |
| 6              | I2SOUT_MASK_POER | 0                                                                                                                      | R/W    | 1 enables the FIFO POP error interrupt            |
| 5              | I2SOUT_MASK_PUE  | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH is empty interrupt        |
| 4              | I2SOUT_MASK_PUAE | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH is almost empty interrupt |
| 3              | I2SOUT_MASK_PUHF | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH is half full interrupt    |
| 2              | I2SOUT_MASK_PUAF | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH is almost full interrupt  |
| 1              | I2SOUT_MASK_PUF  | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH is full interrupt         |
| 0              | I2SOUT_MASK_PUER | 0                                                                                                                      | R/W    | 1 enables the FIFO PUSH error interrupt           |

Table 52 I2S output raw status register

| Name              |                 | Base                                                                                                                                                                                                                                                                                                                                                                                                                                       |        | Default                                                                                                                             |
|-------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------|
| I2SOUT_RAW_STATUS |                 | AS3525_I2SOUT_BASE                                                                                                                                                                                                                                                                                                                                                                                                                         |        | 0x00                                                                                                                                |
| Offset: 0x0008    |                 | Raw status register                                                                                                                                                                                                                                                                                                                                                                                                                        |        |                                                                                                                                     |
|                   |                 | The read-only raw status register contains the actual bit values as reflected by the FIFO controller status signals. I2SOUT_POER and I2SOUT_PUER are static bits, since FIFO controller gives the PUSH/POP error bit only for one clock. This means that these two bits remain asserted until they are cleared in the I2SOUT_CLEAR register. All other bits change state depending on the underlying logic, i.e. state of FIFO controller. |        |                                                                                                                                     |
| Bit               | Bit Name        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                    | Access | Bit Description                                                                                                                     |
| 7                 | stereo18_status | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | Status of write interface for 18 bit stereo mode<br>0: left audio sample is expected next<br>1: right audio sample is expected next |
| 6                 | I2SOUT_POER     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO POP error                                                                                                                 |
| 5                 | I2SOUT_PUE      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH is empty                                                                                                             |
| 4                 | I2SOUT_PUAE     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH is almost empty                                                                                                      |
| 3                 | I2SOUT_PUHF     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH is half full                                                                                                         |
| 2                 | I2SOUT_PUAF     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH is almost full                                                                                                       |
| 1                 | I2SOUT_PUF      | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH is full                                                                                                              |
| 0                 | I2SOUT_PUER     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 1 if FIFO PUSH error                                                                                                                |

Table 53 I2S output status register

| Name           |                 | Base                                                                                                                                                                                      |        | Default                                                                                                                             |
|----------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------|
| I2SOUT_STATUS  |                 | AS3525_I2SOUT_BASE                                                                                                                                                                        |        | 0x00                                                                                                                                |
| Offset: 0x000C |                 | Status register                                                                                                                                                                           |        |                                                                                                                                     |
|                |                 | The status register is a read-only register. A read to this register returns the value of the raw status bits AND'ed with the corresponding mask of enable bits set in the mask register. |        |                                                                                                                                     |
| Bit            | Bit Name        | Default                                                                                                                                                                                   | Access | Bit Description                                                                                                                     |
| 7              | stereo18_status | 0                                                                                                                                                                                         | R      | Status of write interface for 18 bit stereo mode<br>0: left audio sample is expected next<br>1: right audio sample is expected next |
| 6              | I2SOUT_POER     | 0                                                                                                                                                                                         | R      | 1 if FIFO POP error                                                                                                                 |
| 5              | I2SOUT_PUE      | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH is empty                                                                                                             |
| 4              | I2SOUT_PUAE     | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH is almost empty                                                                                                      |
| 3              | I2SOUT_PUHF     | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH is half full                                                                                                         |
| 2              | I2SOUT_PUAF     | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH is almost full                                                                                                       |
| 1              | I2SOUT_PUF      | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH is full                                                                                                              |
| 0              | I2SOUT_PUER     | 0                                                                                                                                                                                         | R      | 1 if FIFO PUSH error                                                                                                                |

Table 54 I2S output interrupt clear register

| Name           |                   | Base                                                                                                                                                                                                                                                                                                                    |        | Default                         |
|----------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------|
| I2SOUT_CLEAR   |                   | AS3525_I2SOUT_BASE                                                                                                                                                                                                                                                                                                      |        | 0x00                            |
| Offset: 0x0010 |                   | Interrupt clear register                                                                                                                                                                                                                                                                                                |        |                                 |
|                |                   | The interrupt clear register is a write-only register. The corresponding static status bit can be cleared by writing a 1 to the corresponding bit in the clear register. All other interrupt flags are level interrupts depending on the status of the FIFO. The bits are de-asserted depending on the FIFO controller. |        |                                 |
| Bit            | Bit Name          | Default                                                                                                                                                                                                                                                                                                                 | Access | Bit Description                 |
| 7              | reserved          |                                                                                                                                                                                                                                                                                                                         | W      |                                 |
| 6              | I2SOUT_clear_poer |                                                                                                                                                                                                                                                                                                                         | W      | Clear POP error interrupt flag  |
| 5:1            | reserved          |                                                                                                                                                                                                                                                                                                                         | W      |                                 |
| 0              | I2SOUT_clear_puer |                                                                                                                                                                                                                                                                                                                         | W      | Clear PUSH error interrupt flag |

## I2SOUT\_DATA

The I2SOUTIF provides two 32 bit wide data registers. The registers are used to store the audio samples before they are written to the FIFO. The registers can be used in different modes depending on the setting of the I2SOUT\_CONTROL register.

Basically, there are four ways to fill the FIFO.

The processor can provide

- two 18 bit audio samples, one for each channel (R,L). The values are written to I2SOUT\_DATA.
- two 16 bit audio samples, one for each channel (R,L). Both values are written to the 32-bit wide I2SOUT\_DATA register at the same time. This mode is highly efficient for 32-bit processor architectures.
- one 18 bit mono audio sample; the sample is used for both channels (R and L). The value is written to the I2SOUT\_DATA.
- one 16 bit mono audio sample; the sample is used for both channels (R and L). The value is written to the I2SOUT\_DATA.

In 18 bit stereo mode the data in I2SOUT\_DATA is interpreted either as left or right audio value. The stereo18\_status bit in the I2SOUT\_STATUS register provides the information which channel's audio sample is expected next.

## The I2S Output Signals

The following specifications signals are given:

- Data are valid at the rising edge of I2SO\_SCLK.
- The MSB is left justified to the I2S frame identification (I2SO\_LRCK). According to standard I2S definition, a delay of one clock cycle between transition of I2SO\_LRCK and the data MSB is used.

The timing diagram of the I2S interface signals for 18bit and 16bit DAC is shown below.

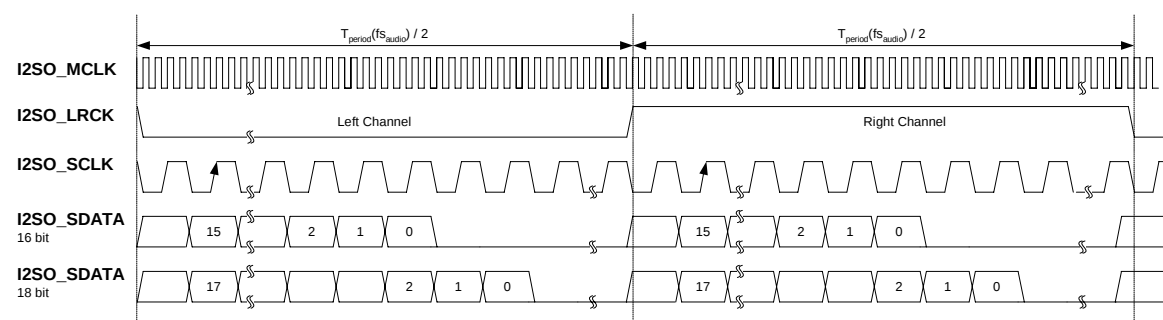
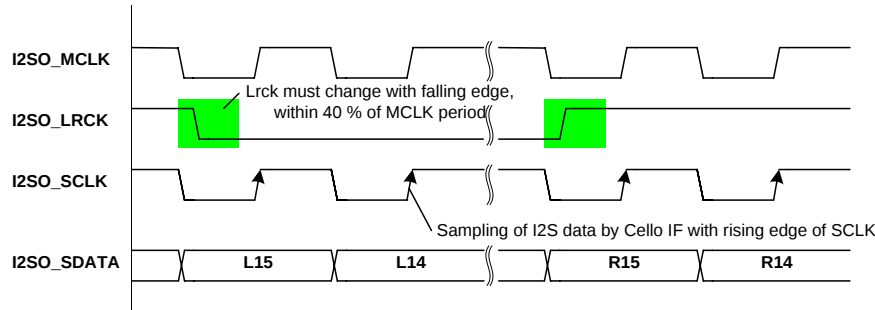


Figure 29 - I2S output timing diagram

For the relationship of the clocks following constraints must be met:

- LRCK must change with the falling edge of MCLK while MCLK is low (constrained should be set to 40 % of the MCLK period, see figure below).
- SDATA must change at the falling edge of SCLK. It will be read with the rising edge of SCLK.

Figure 30 Clock constraints



### 7.3.10.2 Power Modes

The I2SOUTIF contains two clock domains. Each clock domain can be turned off separately. The I2SO\_MCLK must be turned off in the global clock controller register. This is necessary, as the audio chip requires I2SO\_MCLK and I2SO\_SCLK not only for I2S output, but also I2S input (see I2SINIF).

#### PCLK Idle Mode

If the PCLK is turned off (by the clock controller) the I2SOUT\_STATUS register can hold invalid data. However, no interrupt should be triggered if the I2SOUTIF is in idle mode.

#### I2SO\_MCLK Idle Mode

If I2SO\_MCLK is disabled (by the clock controller) no audio samples are read from the FIFO. The output signals remain unchanged until the I2SO\_MCLK is enabled again.

### 7.3.10.3 Loopback Feature

On the AS3525 are two I2S interfaces:

- I2SOUTIF is responsible to send values to the DAC of the audio chip via I2SO\_SDATA
- I2SINIF is responsible to receive audio values from ADC of the audio chip via I2SI\_SDATA

In the AS3525 both SDATA signals are provided as loopback signals (I2SO\_FSDATA, I2SI\_FSDATA):

- I2SO\_SDATA to I2SINIF: This loopback is mainly for testing the transmission and reception paths of both I2S interfaces. The loopback signal is called I2SO\_FSDATA.
- I2SI\_SDATA to I2SOUTIF: This loopback feature allows the application to echo the input audio samples directly to a loudspeaker. The signal provided by the I2SINIF is called I2SI\_FSDATA.

In normal mode the I2SOUTIF generates the I2SO\_SDATA signal based on the contents of the FIFO. If the loop back feature is enabled, the SDATA\_LB bit in the I2SOUT\_CONTROL register must be set.

NOTE: This feature will only be available if SCLK is the same for I2S input and output interface. For implementation the I2SI\_FSDATA signal is simply routed through a multiplexer to the I2SO\_SDATA interface.

### 7.3.10.4 DMA Interface

The I2SOUTIF supports DMA transfers. The DMA controller supports incrementing and non-incrementing (single address) addressing for source and destination. For I2SOUTIF the single-address mode is used. The address of the I2SOUT\_DATA register is used as DMA destination address.

#### Stereo 18 bit DMA Mode

In 18 bit stereo mode, right and left audio samples must be transferred separately to the FIFO. In single-address DMA-mode both data must be written to the same address. The I2SOUTIF is responsible to put the two 18 bit samples together to a 36 bit word. This word is written into the 36 bit wide FIFO.

The I2SOUTIF requires a specific ordering of the samples written to the I2SOUT\_DATA register: first the left value must be written, and afterwards the DMA controller must write the right value. Then a left value can follow, a.s.o. The status bit *stereo18\_status* shows which audio sample is expected.

In order to set up a correct DMA transfer the values must be placed in the source memory as follows:

| Address    | Value   |
|------------|---------|
| addr 0     | LDATA 0 |
| addr 1     | RDATA 0 |
| addr 2     | LDATA 1 |
| addr 3     | RDATA 1 |
| ...        | ...     |
| addr n*2   | LDATA n |
| addr n*2+1 | RDATA n |

### 7.3.11 NAND Flash Interface

The NAND FLASH interface module enables control of NAND flash devices. The design follows the hardware reference implementation described in SMIL (SmartMedia™ Interface Library), Hardware Edition 1.00, TOSHIBA Corporation, but has extensions to support the latest generation of NAND flash devices.

Programming and Reading can be done either by direct access to/from data register (normal mode) or by using a FIFO (burst mode). NAF supports 8-bit and 16-bit transfers.

#### Features

- interface compliant to AMBA APB bus
- generation of interrupt request signal with several maskable interrupt sources (ready, empty, almost\_empty...)
- hardware error detection (2 detect, 1 correct per 256 bytes block) for up to 8 \* 256 bytes (up to 24 ECC bytes)
- 8-bit and 16-bit transfer Mode fore X8/X16 devices
- big endian / little endian support
- DMA Mode
- Normal Mode
- Data/Mode/Status Register
- write/read on/from data register automatically generates read/write strobes
- Burst Transfer
- 36 x 32 bit FIFO for DMA/burst support
- read- & write controller for automatic data resizing (32bit <=> 8/16bit) and read/write control
- configurable strobe (low and high time) for higher PCLK clocks / lower speed NAND Flash devices
- little endian/ big endian selectable
- load interrupts when FIFO is 'almost\_empty' & 'almost\_full' to ensure continuous data flow

Figure 31 Block Diagram of NAND Flash Interface

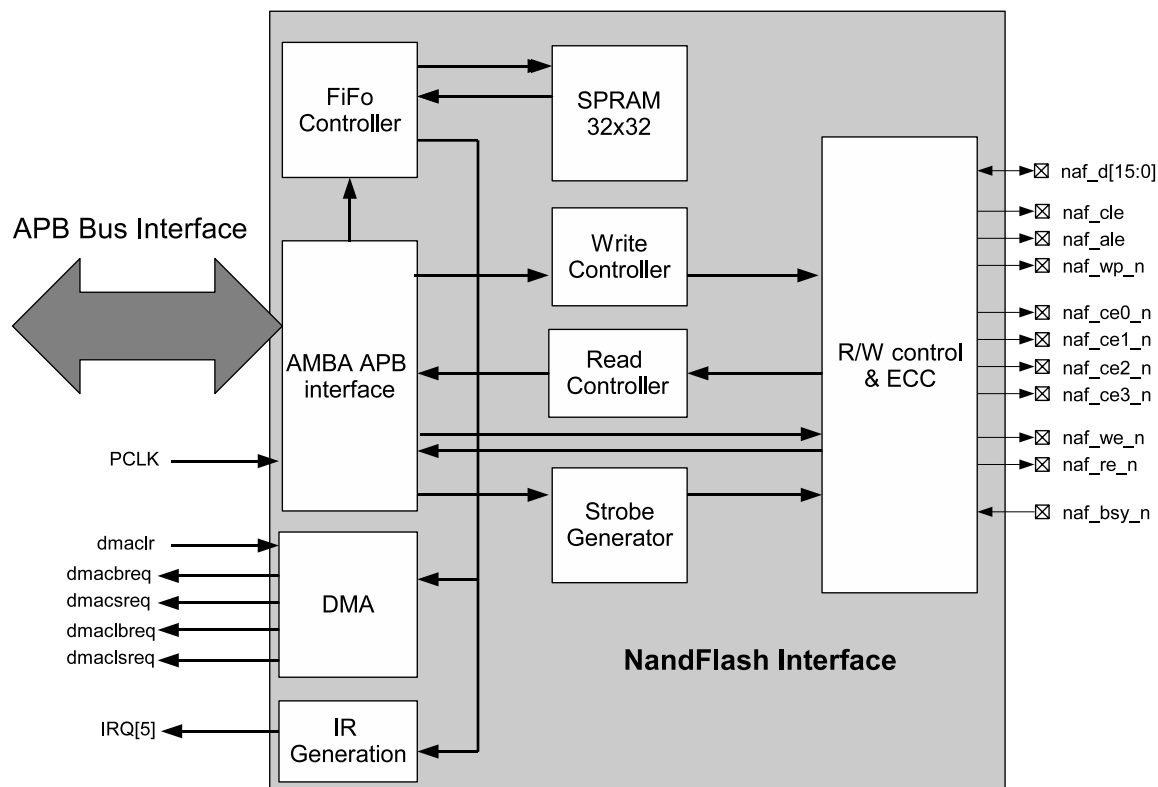
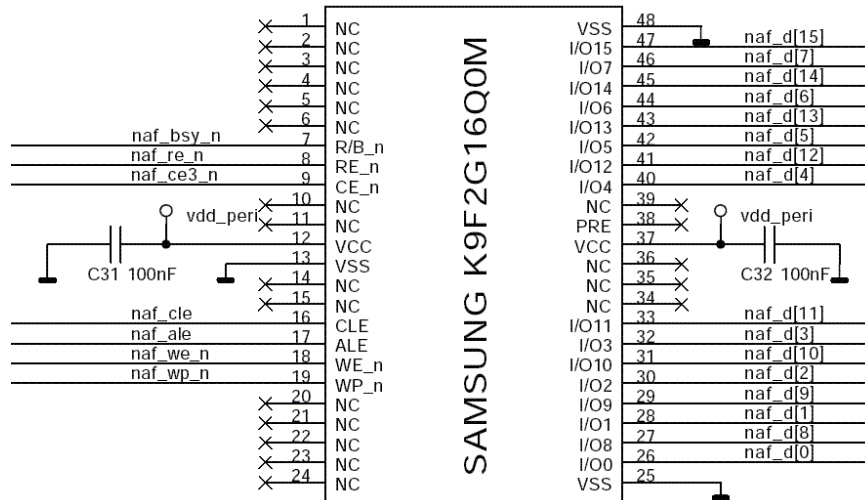


Figure 32 Connecting a NAND Flash



### 7.3.11.1 NandFlash Interface Registers

Table 55 NAF registers

| Register Name | Base Address           | Offset | Note                              |
|---------------|------------------------|--------|-----------------------------------|
| NAFCONFIG     | AS3525_NAND_FLASH_BASE | 0x00   | Configuration register            |
| NAFCONTROL    | AS3525_NAND_FLASH_BASE | 0x04   | Control register                  |
| NAFECC        | AS3525_NAND_FLASH_BASE | 0x08   | Error correction code reg         |
| NAFDATA       | AS3525_NAND_FLASH_BASE | 0x0C   | Data register                     |
| NAFMODE       | AS3525_NAND_FLASH_BASE | 0x10   | Mode register                     |
| NAFSTATUS     | AS3525_NAND_FLASH_BASE | 0x14   | Status register                   |
| NAFMASK       | AS3525_NAND_FLASH_BASE | 0x18   | Interrupt mask register           |
| NAFFIFODATA   | AS3525_NAND_FLASH_BASE | 0x1C   | buffered read/write data register |
| NAFWORDS      | AS3525_NAND_FLASH_BASE | 0x20   | Words register                    |
| NAFCLEAR      | AS3525_NAND_FLASH_BASE | 0x24   | Interrupt clear register          |
| NAFTEST       | AS3525_NAND_FLASH_BASE | 0x28   | Test register                     |

Table 56 NAF configuration register

| Name          |                         | Base                                                                                                                                                                                                  |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFConfig     |                         | AS3525_NAND_FLASH_BASE                                                                                                                                                                                |        | 0x00                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Offset 0x0000 |                         | NAF Configuration Register                                                                                                                                                                            |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|               |                         | The register is used for basic setup. 8 or 16-bit data width, little or big endian can be selected. DMA and FIFO on/off can be controlled as well as duty cycle and duration of read & write signals. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Bit           | Bit Name                | Default                                                                                                                                                                                               | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 19:16         | write_strobe_low [3:0]  | 0x00                                                                                                                                                                                                  | R/W    | low time (# of PCLK cycles + 1) of the output 'naf_we_n' (e.g. a value of 1 will keep naf_we_n at '0' for 3 PCLK cycles during write)                                                                                                                                                                                                                                                                                                                               |
| 15:12         | write_strobe_high [3:0] | 0x00                                                                                                                                                                                                  | R/W    | high time (# of PCLK cycles + 2) of the output 'naf_we_n' (e.g. a value of 0 will keep naf_we_n at '1' for 2 PCLK cycles during write)                                                                                                                                                                                                                                                                                                                              |
| 11:8          | read_strobe_low [3:0]   | 0x00                                                                                                                                                                                                  | R/W    | low time (# of PCLK cycles + 1) of the output 'naf_re_n' (e.g. a value of 2 will keep naf_re_n at '0' for 3 PCLK cycles during read)                                                                                                                                                                                                                                                                                                                                |
| 7:4           | read_strobe_high [3:0]  | 0x00                                                                                                                                                                                                  | R/W    | high time (# of PCLK cycles + 2) of the output 'naf_re_n' (e.g. a value of 0 will keep naf_re_n at '1' for 2 PCLK cycles during read)                                                                                                                                                                                                                                                                                                                               |
| 3             | dma_on                  | 0x0                                                                                                                                                                                                   | R/W    | 0: DMA is disabled and all DMA request signals are tied to 1: DMA is enabled                                                                                                                                                                                                                                                                                                                                                                                        |
| 2             | fifo_staticreset_n      | 0x0                                                                                                                                                                                                   | R/W    | 0: FIFO is reset<br>1: FIFO is enabled                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1             | big_endian              | 0x0                                                                                                                                                                                                   | R/W    | 0: little endian (FIFO data word will be processed in the order word(7:0), word(15:8), word(23:16) and word(31:24) when x16_device is 0; word(15:0) and word(31:16) when x16_device is 1<br>1: big endian (FIFO data word will be processed in the order word(31:24), word(23:16), word(15:8) and word(7:0) when x16_device is 0; word(31:16) and word(15:0) when x16_device is 1<br>Note: big_endian is only supported for r/w access through register NAFFifodata |
| 0             | x16_device              | 0x0                                                                                                                                                                                                   | R/W    | 0: X8 Device (for NAND flash with 8-bit data bus)<br>1: X16 Device (for NAND flash with 16-bit data bus)                                                                                                                                                                                                                                                                                                                                                            |

Table 57 NAF control register

| Name          |                   | Base                                                                 |        | Default                                                                                                                                |
|---------------|-------------------|----------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------|
| NAFControl    |                   | AS3525_NAND_FLASH_BASE                                               |        | 0x2                                                                                                                                    |
| Offset 0x0004 |                   | NAFControl Register                                                  |        |                                                                                                                                        |
|               |                   | The NAFControl register controls read access and FIFO dynamic reset. |        |                                                                                                                                        |
| Bit           | Bit Name          | Default                                                              | Access | Bit Description                                                                                                                        |
| 1             | read_strobe       | 0x1                                                                  | W      | 1: triggers a FIFO reset pulse (when NAFConfig bit 'fifo_staticreset_n' is 1) The bit is cleared automatically in the next PCLK cycle. |
| 0             | fifo_reset_strobe | 0x1                                                                  | W      | 1: triggers one single read cycle on output 'naf_re_n'. The bit is cleared automatically in the next PCLK cycle.                       |

Table 58 NAF error correction register

| Name          |               | Base                                                                      |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------|---------------|---------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFEcc        |               | AS3525_NAND_FLASH_BASE                                                    |        | 0x2                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Offset 0x0008 |               | NAF Error correction code register                                        |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|               |               | The NAFEcc register offers access to the error correction code registers. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Bit           | Bit Name      | Default                                                                   | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 32:0          | Nafecc [32:0] | 0x0001                                                                    | R      | <p>This register can be accessed up to 8 times and contains the following data:</p> <p>1.access =&gt; Line Parity Block1<br/> 2.access =&gt; Column Parity Block1**<br/> 3.access =&gt; Line Parity Block2<br/> 4.access =&gt; Column Parity Block2**<br/> 5.access =&gt; Line Parity Block3<br/> 6.access =&gt; Column Parity Block3**<br/> 7.access =&gt; Line Parity Block4<br/> 8.access =&gt; Column Parity Block4**<br/> (9.access =&gt; same as 1.access)</p> |

Note: \* Before access to NAFEcc registers is possible, NAFMode register has to be set to 0xd4 (after page write operation) or to 0x54 (after page read operation). NAFEcc register contents will be cleared if NAFMode register bits 6 and 5 are both '1'.

\*\* Only bits 11 to 0 are relevant for column parity, other bits are '0';

The content of NAFEcc depends on the device type.

#### X8 (8-bit data bus) devices:

|                      |                           |                                                     |
|----------------------|---------------------------|-----------------------------------------------------|
| Line Parity Block1   | : will contain the line   | parity of byte 1 to 512 (after 512 r/w cycles)      |
| Column Parity Block1 | : will contain the column | parity of byte 1 to 512 (after 512 r/w cycles)      |
| Line Parity Block2   | : will contain the line   | parity of byte 513 to 1024 (after 1024 r/w cycles)  |
| Column Parity Block2 | : will contain the column | parity of byte 513 to 1024 (after 1024 r/w cycles)  |
| Line Parity Block3   | : will contain the line   | parity of byte 1025 to 1536 (after 1536 r/w cycles) |
| Column Parity Block3 | : will contain the column | parity of byte 1025 to 1536 (after 1536 r/w cycles) |
| Line Parity Block4   | : will contain the line   | parity of byte 1537 to 2048 (after 2048 r/w cycles) |
| Column Parity Block4 | : will contain the column | parity of byte 1537 to 2048 (after 2048 r/w cycles) |

#### X16 (16-bit data bus) devices:

|                      |                           |                                                              |
|----------------------|---------------------------|--------------------------------------------------------------|
| Line Parity Block1   | : will contain the line   | parity of halfword(7:0) 1 to 512 (after 512 r/w cycles)      |
| Column Parity Block1 | : will contain the column | parity of halfword(7:0) 1 to 512 (after 512 r/w cycles)      |
| Line Parity Block2   | : will contain the line   | parity of halfword(15:8) 1 to 512 (after 512 r/w cycles)     |
| Column Parity Block2 | : will contain the column | parity of halfword(15:8) 1 to 512 (after 512 r/w cycles)     |
| Line Parity Block3   | : will contain the line   | parity of halfword(7:0) 513 to 1024 (after 1024 r/w cycles)  |
| Column Parity Block3 | : will contain the column | parity of halfword(7:0) 513 to 1024 (after 1024 r/w cycles)  |
| Line Parity Block4   | : will contain the line   | parity of halfword(15:8) 513 to 1024 (after 1024 r/w cycles) |
| Column Parity Block4 | : will contain the column | parity of halfword(15:8) 513 to 1024 (after 1024 r/w cycles) |

**Note: Read ECC is not performed in unbuffered READ mode (this means when CPU accesses the Nand Flash through the NAF\_DATA registers)**

Table 59 NAF data register

| Name          |          | Base                                                                                    |        | Default                                                                                                                                  |
|---------------|----------|-----------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------|
| NAFData       |          | AS3525_NAND_FLASH_BASE                                                                  |        | 0x0000                                                                                                                                   |
| Offset 0x000C |          | Data Register                                                                           |        |                                                                                                                                          |
|               |          | The NAFData register offers unbuffered access to the data bus of the NAND flash device. |        |                                                                                                                                          |
| Bit           | Bit Name | Default                                                                                 | Access | Bit Description                                                                                                                          |
| 15:0          | NAFData  | 0x01                                                                                    | R/W    | For X8 devices (8-bit data bus) only bits 7:0 are relevant, other bits are ignored<br>For X16 devices (16-bit data bus) all are relevant |

Table 60 NAF mode register

| Name          |                  | Base                                                                  |        | Default                                                                                                                                                                                                                                                                                                                                                        |
|---------------|------------------|-----------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFMode       |                  | AS3525_NAND_FLASH_BASE                                                |        | 0x00                                                                                                                                                                                                                                                                                                                                                           |
| Offset 0x0010 |                  | Mode register                                                         |        |                                                                                                                                                                                                                                                                                                                                                                |
|               |                  | The NAFMode register controls NAND flash read/write/erase procedures. |        |                                                                                                                                                                                                                                                                                                                                                                |
| Bit           | Bit Name         | Default                                                               | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                |
| 7             | write protection | 0x0                                                                   | R/W    | 0: write protection is on<br>1: write protection is off (when 'power_on' is 1)                                                                                                                                                                                                                                                                                 |
| 6:5           | ecc [1:0]        | 0x0                                                                   | R/W    | 0: error code correction disabled<br>1: error code correction enabled (when 'ce' is 1)<br>2: stop error code correction, disable read/write strobes and disable 'naf_do' (when 'ce' is 1). Use this mode when reading the NAFEcc register<br>3: Reset NAFEcc register contents, 'ecc' changes to value 1 (enable mode) automatically after the next PCLK cycle |
| 4             | ce               | 0x0                                                                   | R/W    | controls 'chip enable'<br>0: output 'naf_ce_n' is set to '1' (device is disabled)<br>1: output 'naf_ce_n' is set to '0' (device is enabled)                                                                                                                                                                                                                    |
| 3             | -                | 0x0                                                                   | R      | always '0'                                                                                                                                                                                                                                                                                                                                                     |
| 2             | power_on         | 0x0                                                                   | R/W    | 0: power off (all output enable signals are turned off)<br>1: power on                                                                                                                                                                                                                                                                                         |
| 1             | ale              | 0x0                                                                   | R/W    | controls 'address latch enable'<br>0: output 'naf_ale' is set to '0'<br>1: output 'naf_ale' is set to '1' (Address Latch Cycle)                                                                                                                                                                                                                                |
| 0             | cle              | 0x0                                                                   | R/W    | controls 'command latch enable'<br>0: output 'naf_cle' is set to '0'<br>1: output 'naf_cle' is set to '1' (Command Latch Cycle)                                                                                                                                                                                                                                |

Table 61 NAF status register

| Name          |                   | Base                                                                |        | Default                                                                                                                                                                                                                                                                                                                            |
|---------------|-------------------|---------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFStatus     |                   | AS3525_NAND_FLASH_BASE                                              |        | -                                                                                                                                                                                                                                                                                                                                  |
| Offset 0x0014 |                   | Status Register                                                     |        |                                                                                                                                                                                                                                                                                                                                    |
|               |                   | The NAFStatus register contains information on the internal status. |        |                                                                                                                                                                                                                                                                                                                                    |
| Bit           | Bit Name          | Default                                                             | Access | Bit Description                                                                                                                                                                                                                                                                                                                    |
| 13            | fifo_error        | 0x0                                                                 | R      | FIFO error signal<br>0: if FIFO is reset<br>1: if FIFO contains 36 words and FIFO push(write) has occurred or when FIFO contains 0 words and a FIFO pop(read) has occurred. The FIFO error will lock the FIFO and has to be reset by a reset of the FIFO (by setting NAFControl register bit 1 to '1')                             |
| 12            | fifo_full         | 0x0                                                                 | R      | FIFO full signal<br>0: if FIFO contains less than 36 words<br>1: if FIFO contains 36 words                                                                                                                                                                                                                                         |
| 11            | fifo_almost_full  | 0x0                                                                 | R      | FIFO almost_full signal<br>0: if FIFO contains less than 32 words<br>1: if FIFO contains more than or equal 32 words                                                                                                                                                                                                               |
| 10            | fifo_almost_empty | 0x0                                                                 | R      | FIFO almost_empty signal<br>0: if FIFO contains more than 4 words<br>1: if FIFO contains less than or equal 4 words                                                                                                                                                                                                                |
| 9             | fifo_empty        | 0x0                                                                 | R      | FIFO empty signal<br>0: if FIFO contains more than 0 words<br>1: = when FIFO contains 0 words                                                                                                                                                                                                                                      |
| 8             | strobe_ready      | 0x0                                                                 | R      | read/write strobe ready signal<br>0: if read/write strobe '0' (strobe active)<br>1: if read/write strobe '1' (strobe inactive)                                                                                                                                                                                                     |
| 7             | flash_ready       | 0x0                                                                 | R      | synchronised NAND flash ready signal<br>0: if synchronised input 'naf_busy_in_n' is '0' (busy)<br>1: if synchronised input 'naf_busy_in_n' is '1' (ready)                                                                                                                                                                          |
| 6             | got_fifo_error    | 0x0                                                                 | R      | FIFO error indication (edge triggered)<br>0: if bit 6 of NAFClear register is set to '1'<br>1: if FIFO contains 36 words and FIFO push(write) occurs or when FIFO contains 0 words and a FIFO pop(read) occurs.                                                                                                                    |
| 5             | got_fifo_full     | 0x0                                                                 | R      | FIFO full indication (edge triggered)<br>0: if bit 5 of NAFClear register is set to '1'<br>1: if FIFO contains 36.                                                                                                                                                                                                                 |
| 4             | got_fifo_high     | 0x0                                                                 | R      | FIFO high indication (edge triggered)<br>0: if bit 4 of NAFClear register is set to '1'<br>1: if FIFO gets full (36 words) or changes from 31 to 32 words (and when the NAFWords register is greater than 32).<br>Note: When this bit gets '1' during 'Page Read' mode, a new FIFO burst read of up to 32 words is possible.       |
| 3             | got_fifo_low      | 0x0                                                                 | R      | FIFO low indication (edge triggered)<br>0: if bit 3 of NAFClear register is set to '1'<br>1: if FIFO gets empty or changes from 5 to 4 words (and when the NAND Flash requires more than 32 bytes/halfwords).<br>Note: When this bit gets '1' during 'Page Programming' mode, a new FIFO burst write of up to 32 words is possible |

| Name          |                   | Base                                                                |        | Default                                                                                                                                                                                                                                                                                                                 |
|---------------|-------------------|---------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFStatus     |                   | AS3525_NAND_FLASH_BASE                                              |        | -                                                                                                                                                                                                                                                                                                                       |
| Offset 0x0014 |                   | Status Register                                                     |        |                                                                                                                                                                                                                                                                                                                         |
|               |                   | The NAFStatus register contains information on the internal status. |        |                                                                                                                                                                                                                                                                                                                         |
| Bit           | Bit Name          | Default                                                             | Access | Bit Description                                                                                                                                                                                                                                                                                                         |
| 2             | got_empty_and_rdy | 0x0                                                                 | R      | NAFWords empty and Controller ready indication (edge triggered)<br>0: when bit 2 of NAFClear register is set to '1'<br>1: when read/write strobe changes from '0' to '1' (end of strobe) and NAFWords register has become empty.<br>Note: This bit is used to detect the end of a multiple read/write burst transaction |
| 1             | got_strobe_ready  | 0x0                                                                 | R      | Read/write strobe ready indication (edge triggered)<br>0: when bit 1 of NAFClear register is set to '1'<br>1: when read/write strobe changes from '0' to '1' (end of strobe)<br>Note: read/write strobes can last from 3 to 33 PCLK cycles depending on NAFConfig settings.                                             |
| 0             | got_flash_ready   | 0x0                                                                 | R      | NAFWords empty and Controller ready indication (edge triggered)<br>0: when bit 2 of NAFClear register is set to '1'<br>1: when read/write strobe changes from '0' to '1' (end of strobe) and NAFWords register has become empty.<br>Note: This bit is used to detect the end of a multiple read/write burst transaction |

Table 62 NAF interrupt mask register

| Name          |          | Base                                                                         |        | Default                                                                                           |
|---------------|----------|------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------|
| NAFMask       |          | AS3525_NAND_FLASH_BASE                                                       |        | 0x0018                                                                                            |
| Offset 0x0018 |          | Interrupt Mask Register                                                      |        |                                                                                                   |
|               |          | The NAFMask register is used to mask/enable the internal interrupt requests. |        |                                                                                                   |
| Bit           | Bit Name | Default                                                                      | Access | Bit Description                                                                                   |
| 6             | mask6    | 0x1                                                                          | R/W    | Mask 'FIFO error indication' interrupt request<br>0: enable<br>1: masked                          |
| 5             | mask5    | 0x1                                                                          | R/W    | Mask 'FIFO full indication' interrupt request<br>0: enable<br>1: masked                           |
| 4             | mask4    | 0x1                                                                          | R/W    | Mask 'FIFO high indication' interrupt request<br>0: enable<br>1: masked                           |
| 3             | mask3    | 0x1                                                                          | R/W    | Mask 'FIFO low indication' interrupt request<br>0: enable<br>1: masked                            |
| 2             | mask2    | 0x1                                                                          | R/W    | Mask 'NAFWords empty and Controller ready indication' interrupt request<br>0: enable<br>1: masked |
| 1             | mask1    | 0x1                                                                          | R/W    | Mask 'Read/write strobe ready indication' interrupt request<br>0: enable<br>1: masked             |
| 0             | mask0    | 0x1                                                                          | R/W    | Mask 'NAND flash ready indication' interrupt request<br>0: enable<br>1: masked                    |

Table 63 NAF FiFo Data register

| Name          |                 | Base                                                         |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|-----------------|--------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFFifodata   |                 | AS3525_NAND_FLASH_BASE                                       |        | 0x0000                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Offset 0x001c |                 | FIFO Data Register                                           |        |                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|               |                 | The NAFFifodata register offers access to the internal FIFO. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Bit           | Bit Name        | Default                                                      | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 32:0          | Fifodata [32:0] | -                                                            | R/W    | Writing this register will push a word on the FIFO and the write address will be incremented by 1. When the FIFO is full (36 words) then a write access on the register is ignored and the FIFO ERROR status bit is set.<br>Reading on this register will pop a word from the FIFO and the read address will be incremented by 1. When the FIFO is empty then a read access on the register is ignored and the FIFO ERROR status bit is set. |

Table 64 NAF interrupt mask register

| Name          |              | Base                                                                                                                                                  |        | Default                                                                        |
|---------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------|
| NAFWords      |              | AS3525_NAND_FLASH_BASE                                                                                                                                |        | 0x0000                                                                         |
| Offset 0x0020 |              | Interrupt Mask Register                                                                                                                               |        |                                                                                |
|               |              | The NAFWords register informs the controller about the maximum words to be transferred and controls the FIFO transfer both in interrupt and DMA mode. |        |                                                                                |
| Bit           | Bit Name     | Default                                                                                                                                               | Access | Bit Description                                                                |
| 32:0          | Words [32:0] | 0x0000                                                                                                                                                | R/W    | 0: FIFO based data transfer is disabled<br>not 0: FIFO transfer is in progress |

Note: For page transfers (program or read) the initial number of words depends on the NAND flash device. For a page size of 512 bytes, an initial word value of  $512/4 = 128$  has to be written. For a page size of 2k bytes, an initial word value of 512 has to be used.

Table 65 NAF interrupt clear register

| Name          |          | Base                                                                                          |        | Default                                                                                                                                                     |
|---------------|----------|-----------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAFClear      |          | AS3525_NAND_FLASH_BASE                                                                        |        | 0x0018                                                                                                                                                      |
| Offset 0x0024 |          | Clear Register                                                                                |        |                                                                                                                                                             |
|               |          | The NAFClear register clears interrupt status information and re-enables interrupt detection. |        |                                                                                                                                                             |
| Bit           | Bit Name | Default                                                                                       | Access | Bit Description                                                                                                                                             |
| 6             | clear6   | -                                                                                             | W      | Reset of 'FIFO error indication' status bit<br>0: no action<br>1: bit 6 of NAFStatus is reset and interrupt 6 detection is enabled                          |
| 5             | clear5   | -                                                                                             | W      | Reset of 'FIFO full indication' status bit<br>0: no action<br>1: bit 5 of NAFStatus is reset and interrupt 5 detection is enabled                           |
| 4             | clear4   | -                                                                                             | W      | Reset of 'FIFO high indication' status bit<br>0: no action<br>1: bit 4 of NAFStatus is reset and interrupt 4 detection is enabled                           |
| 3             | clear3   | -                                                                                             | W      | Reset of 'FIFO low indication' status bit<br>0: no action<br>1: bit 3 of NAFStatus is reset and interrupt 3 detection is enabled                            |
| 2             | clear2   | -                                                                                             | W      | Reset of 'NAFWords empty and Controller ready indication' status bit<br>0: no action<br>1: bit 2 of NAFStatus is reset and interrupt 2 detection is enabled |
| 1             | clear1   | -                                                                                             | W      | Reset of 'Read/write strobe ready indication' status bit<br>0: no action<br>1: bit 1 of NAFStatus is reset and interrupt 1 detection is enabled             |
| 0             | clear0   | -                                                                                             | W      | Reset of 'Read/write strobe ready indication' status bit<br>0: no action<br>1: bit 0 of NAFStatus is reset and interrupt 0 detection is enabled             |

Table 66 NAF test register

| Name          |            | Base                                                           |        | Default                                                                                                         |
|---------------|------------|----------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------|
| NAFTest       |            | AS3525_NAND_FLASH_BASE                                         |        | 0x0000                                                                                                          |
| Offset 0x0028 |            | Test Register                                                  |        |                                                                                                                 |
|               |            | The NAFTest register is used for functional tests of the FIFO. |        |                                                                                                                 |
| Bit           | Bit Name   | Default                                                        | Access | Bit Description                                                                                                 |
| 1             | datainvert |                                                                | W      | 0: default mode<br>1: disables FIFO access by the internal controller => FIFO is accessed by APB interface only |
| 0             | fifotest   | -                                                              | W      | 0: default mode<br>1: data word both on FIFO input and output is inverted                                       |

### 7.3.12 DBOP - Data Block Output Port

Purpose of this ARM APB peripheral module is a high-speed data output port that can support data transfer to various display controllers based on synchronous control interfaces. Programmability of polarity and timing of the generated control signals makes it possible to support various kinds of displays. Example of a supported display controller is the Hitachi HD77766R LCDE controller.

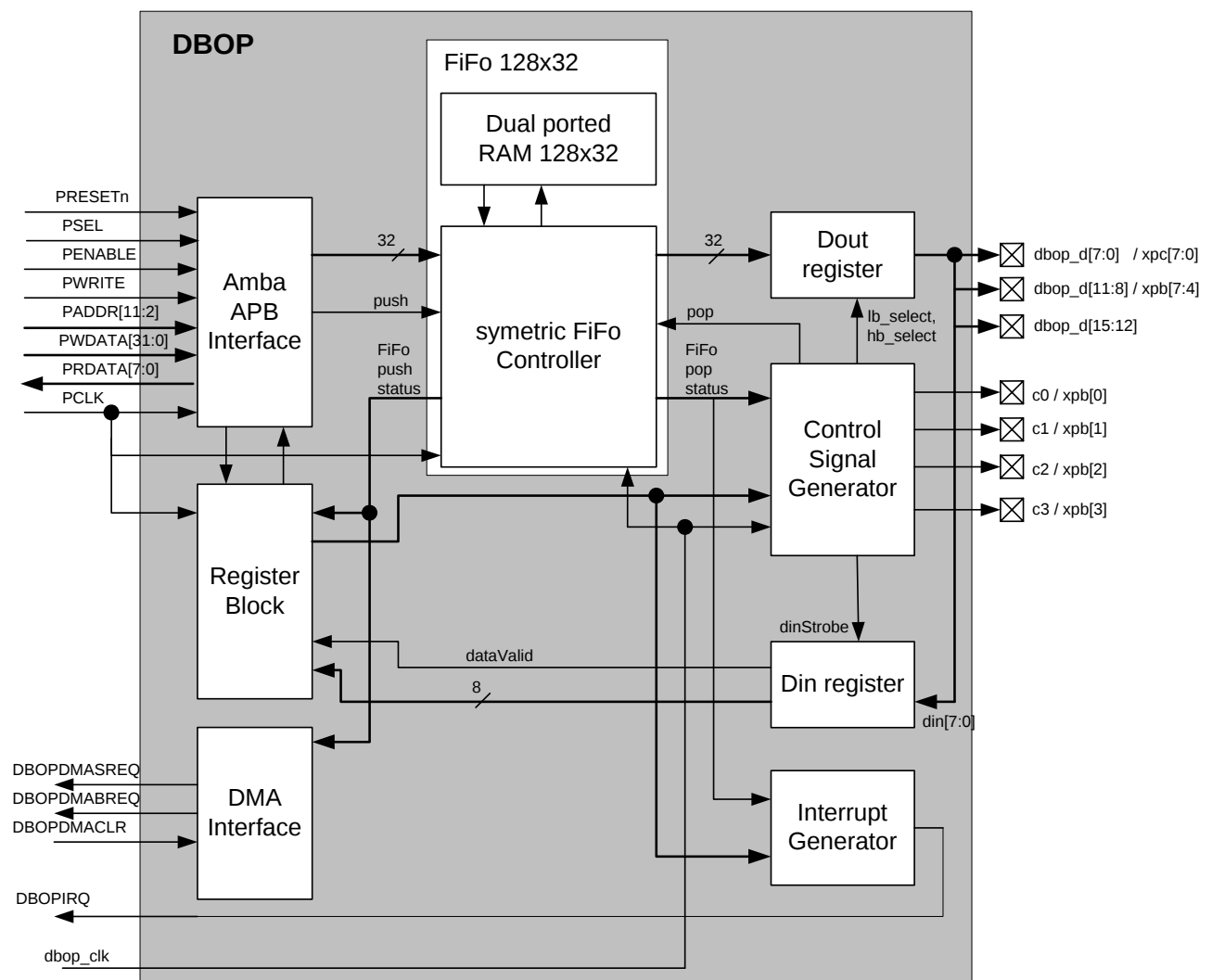
From the programmers point of view the DBOP module can be serviced by DMA accesses. With the large size of the data FIFO and the programmable interrupt request conditions the overhead for SW is minimised. Simple read instructions to read for example a status register of the LCD controller are also supported.

The usage of this cell results in a great performance boost compared to the standard ARM GPIO PrimeCell™ architecture.

#### Features

- APB bus interface
- support for direct memory access (DMA)
- data output FIFO with 128 words (32 bit wide)
- 8 or 16 bit parallel data output (configurable)
- 4 control outputs - flexible programming of the signal waveforms with respect to polarity and timing
- programmable even/odd control output generation
- 8 or 16 bit parallel data input register with programmable read strobe
- programmable conditions for interrupt generation based on FIFO flags
- usage of FIFO for simple division of APB clock domain and output clock domain
- programmable data output rate in range of 0.05 to 4 MHz
- APB Clock & DBOP Clocks are synchronous.

Figure 33 DBOP Block Diagram



## 7.3.12.1 DBOP register definitions

Table 67 DBOP Registers

| Register Name  | Base Address     | Offset | Note                                    |
|----------------|------------------|--------|-----------------------------------------|
| DBOP_TIMPOL_01 | AS3525_DBOP_BASE | 0x00   | Timing and polarity for control 0 and 1 |
| DBOP_TIMPOL_23 | AS3525_DBOP_BASE | 0x04   | Timing and polarity for control 1 and 2 |
| DBOP_CTRL_REG  | AS3525_DBOP_BASE | 0x08   | Control Register                        |
| DBOP_STAT_REG  | AS3525_DBOP_BASE | 0x0C   | Status Register                         |
| DBOP_DOUT_REG  | AS3525_DBOP_BASE | 0x10   | Data output register                    |
| DBOP_DIN_REG   | AS3525_DBOP_BASE | 0x14   | Data input register                     |

## Timing &amp; Polarity Control register TPC01

This register contains all information necessary for definition of control signals C0 and C1.

Table 68 DBOP control registers C0 and C1

| Register bits | Name  | type | function        | default value |  |
|---------------|-------|------|-----------------|---------------|--|
| 31            | c1_p0 | r/w  | polarity 1      | 0             |  |
| 30            | c1_p1 | r/w  | polarity 2      | 1             |  |
| 29            | c1_p2 | r/w  | polarity 3      | 0             |  |
| 28:24         | c1_t1 | r/w  | Time 1          | 0xA           |  |
| 23:19         | c1_t2 | r/w  | Time 2          | 0x14          |  |
| 18            | c1_ev | r/w  | even enable     | 1             |  |
| 17            | c1_od | r/w  | odd enable      | 1             |  |
| 16            | c1_qs | r/w  | quiescent state | 0             |  |
| 15            | c0_p0 | r/w  | polarity 1      | 0             |  |
| 14            | c0_p1 | r/w  | polarity 2      | 1             |  |
| 13            | c0_p2 | r/w  | polarity 3      | 0             |  |
| 12:8          | c0_t1 | r/w  | Time 1          | 0xA           |  |
| 7:3           | c0_t2 | r/w  | Time 2          | 0x14          |  |
| 2             | c0_ev | r/w  | even enable     | 1             |  |
| 1             | c0_od | r/w  | odd enable      | 1             |  |
| 0             | c0_qs | r/w  | quiescent state | 0             |  |

## Timing &amp; Polarity Control register TPC23

This register contains all information necessary for definition of control signals C2 and C3.

Table 69 DBOP control registers C2 and C3

| Register bits | Name  | type | function        | default value |  |
|---------------|-------|------|-----------------|---------------|--|
| 31            | c3_p0 | r/w  | polarity 1      | 0             |  |
| 30            | c3_p1 | r/w  | polarity 2      | 1             |  |
| 29            | c3_p2 | r/w  | polarity 3      | 0             |  |
| 28:24         | c3_t1 | r/w  | Time 1          | 0xA           |  |
| 23:19         | c3_t2 | r/w  | Time 2          | 0x14          |  |
| 18            | c3_ev | r/w  | even enable     | 1             |  |
| 17            | c3_od | r/w  | odd enable      | 1             |  |
| 16            | c3_qs | r/w  | quiescent state | 0             |  |
| 15            | c2_p0 | r/w  | polarity 1      | 0             |  |
| 14            | c2_p1 | r/w  | polarity 2      | 1             |  |
| 13            | c2_p2 | r/w  | polarity 3      | 0             |  |
| 12:8          | c2_t1 | r/w  | Time 1          | 0xA           |  |
| 7:3           | c2_t2 | r/w  | Time 2          | 0x14          |  |
| 2             | c2_ev | r/w  | even enable     | 1             |  |
| 1             | c2_od | r/w  | odd enable      | 1             |  |

|   |       |     |                 |   |  |
|---|-------|-----|-----------------|---|--|
| 0 | c2_qs | r/w | quiescent state | 0 |  |
|---|-------|-----|-----------------|---|--|

Table 70 DBOP control register

| Register bits | Name         | type | function                                               | default value |                                                                                     |
|---------------|--------------|------|--------------------------------------------------------|---------------|-------------------------------------------------------------------------------------|
| 31:22         |              |      | <i>reserved</i>                                        |               |                                                                                     |
| 21            | clr_pop_err  | W    | <i>Interrupt clear signal for pop error interrupt</i>  | 0             | Writing 1 to this bit will clear the pop error interrupt. Writing 0 has no effect.  |
| 20            | clr_push_err | W    | <i>Interrupt clear signal for push error interrupt</i> | 0             | Writing 1 to this bit will clear the push error interrupt. Writing 0 has no effect. |
| 19            | en_data      | r/w  | <i>Tri-state enable for dout bus</i>                   | 0             | When set, dout bus is tri-stated when there is no active write on the bus.          |
| 18            | sdsc         | r/w  | <i>short count bit</i>                                 | 0             |                                                                                     |
| 17            | res_even     | r/w  | reset to even cycle                                    | 0             | when set, next output cycle is even                                                 |
| 16            | enw          | r/w  | enable write                                           | 0             | 0: write disabled<br>1: write enabled                                               |
| 15            | strd         | r/w  | start read                                             | 0             |                                                                                     |
| 14:13         | osm          | r/w  | output serial mode                                     | 0             | 0: single word out<br>1: 2 serial words out<br>2: 4 serial words out                |
| 12            | ow           | r/w  | output data width                                      | 0             | 0: 8 bit data width<br>1: 16 bit data width                                         |
| 11            | ir_enable    | r/w  | IR enable                                              |               | 0: all IR disabled<br>1: IR enabled                                                 |
| 10            | ir_po_err    | r/w  | IR enable on pop error                                 | 0             |                                                                                     |
| 9             | ir_pu_err    | r/w  | IR enable on push error                                | 0             |                                                                                     |
| 8             | ir_e_en      | r/w  | IR enable set on push empty                            | 0             |                                                                                     |
| 7             | ir_ae_en     | r/w  | IR enable set on push almost empty                     | 0             |                                                                                     |
| 6             | ir_af_en     | r/w  | IR enable set on push almost full                      | 0             |                                                                                     |
| 5             | ir_f_en      | r/w  | IR enable set on push full                             | 0             |                                                                                     |
| 4:0           | rs_t         | r/w  | read strobe time                                       | 0x1F          |                                                                                     |

## Notes:

- If the start read bit is issued by setting the strd bit to 1, a single read cycle is generated. After this read cycle the strd bit is set to 0 again by HW.
- If write is enabled by setting enw=1, no read is possible (strd does not cause any action).
- res\_even is a reset bit that defines the start of even/odd generated signals. With res\_even bit set, the next output cycle is a even cycle. Within this first even output cycle the res\_even bit is set to 0 by the SW.
- sdsc selects the counter length for the timing generator. Default is end value of 31. With sdsc set to 1, the count end value is 15.
- en\_data is used as a tri-state enable for the dout bus . When set as 1, dout is tri-stated if there is no active write on the bus . When this bit is set as 0, dout is bus is tri-stated only during the read cycle.

Table 71: DBOP status register

| Register bits | Name       | type | function               | default value |  |
|---------------|------------|------|------------------------|---------------|--|
| 31:17         |            |      | <i>reserved</i>        |               |  |
| 16            | rd_d_valid | r    | read data valid        |               |  |
| 15:12         | Reserved   |      |                        |               |  |
| 11            | fi_pu_err  | f    | push error             |               |  |
| 10            | fi_pu_e    | r    | push fifo empty        |               |  |
| 9             | fi_pu_ae   | r    | push fifo almost empty |               |  |
| 8             | fi_pu_hf   | r    | push fifo half full    |               |  |
| 7             | fi_pu_af   | r    | push fifo almost full  |               |  |
| 6             | fi_pu_f    | r    | push fifo full         |               |  |
| 5             | fi_po_err  | r    | pop error              |               |  |
| 4             | fi_po_e    | r    | pop fifo empty         |               |  |
| 3             | fi_po_ae   | r    | pop fifo almost empty  |               |  |
| 2             | fi_po_hf   | r    | pop fifo half full     |               |  |
| 1             | fi_po_af   | r    | pop fifo almost full   |               |  |
| 0             | fi_po_f    | r    | pop fifo full          |               |  |

The read data valid flag is cleared with every start read and set after read data strobe is issued (at read data valid 1 the data can be readout by SW).

### Data Output Register

32 bit register for data output - the data written to this register are directly written to the FiFo. Depending on the serial output mode and the output data width, the effective register width of this register is 8, 16 or 32 bits.

Following table shows the effective data width for this register:

|         | osm=0     | osm=1             | osm=2                           |
|---------|-----------|-------------------|---------------------------------|
| odw = 0 | 8 (byte0) | 16 (byte0, byte1) | 32 (byte0, byte1, byte2, byte3) |
| odw = 1 | 16 (HW0)  | 32 (HW0, HW1)     | 32 (HW0, HW1)                   |

Depending on odw,

- either one, two or four bytes are transmitted serially for odw=0
  - or one or two half words (HW = 16 bits) are transmitted serially for odw=1.
- Note that for the 8 or 16 bit width only a part of the FiFo memory is used (to keep HW design simple).

### Data Input Register

16 bit data input register that holds the value of the last read cycle. It is only valid if the data valid flag is set in the status register. No interrupt support is given, for data input the read data valid flag must be polled.

## Dbop Integration Test Registers

The Dbop module is programmed to integration test mode using test control register. The integration test mode enables the user to access all the input/output pins through the APB bus interface.

| Name      | Offset | R/W | Reset Value | Description                            |
|-----------|--------|-----|-------------|----------------------------------------|
| DBOPITC   | 0x18   | R/W | 0x00000000  | DBOP integration test control register |
| DBOPITIP1 | 0x1C   | R/W | 0x00        | DBOP integration test input register   |
| DBOPITOP1 | 0x20   | R   | 0x0         | DBOP integration test output register  |

Table 72 DBOPITC test register

| Register bits | Name | type | function                | default value |                                         |
|---------------|------|------|-------------------------|---------------|-----------------------------------------|
| 31:1          |      |      | <i>reserved</i>         |               |                                         |
| 0             | iten | r/w  | Integration test enable |               | 1 will enable the integration test mode |

Table 73 DBOPITIP1 test register

| Register bits | Name        | type | function                       | default value |                                                            |
|---------------|-------------|------|--------------------------------|---------------|------------------------------------------------------------|
| 31:5          |             |      | <i>reserved</i>                |               |                                                            |
| 4             | Testctrloen | r/w  | Test value for out_enControl_n | 0             | The value on this bit will be reflected in out_enControl_n |
| 3             | Testdataoen | r/w  | Test value for out_enData_n    | 0             | The value on this bit will be reflected in out_enData_n    |
| 2             | Testdmasreq | r/w  | Test value for DMASREQ         | 0             | The value on this bit will be reflected in DBOPDMACSREQ    |
| 1             | Testdmabreq | r/w  | Test value for DMABREQ         | 0             | The value on this bit will be reflected in DBOPDMACBREQ    |
| 0             | testirq     | r/w  | Test value for interrupt       | 0             | The value on this bit will be reflected in DBOPIRQ         |

Table 74 DBOPITOP1 test register

| Register bits | Name       | type | function                   | default value |                                                                       |
|---------------|------------|------|----------------------------|---------------|-----------------------------------------------------------------------|
| 31:1          |            |      | <i>reserved</i>            |               |                                                                       |
| 0             | Testdmaclr | r    | DBOPDMACCLR test register. | 0             | Read of this register will return the value on the DBOPDMACCLR input. |

## 7.3.12.2 DBOP DMA Interface

This block generates all necessary interface signals with the DMAC primecell for DMA transfer. Following table gives a description of these signals.

|                    |                                                                                                                                                                                                    |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DBOPDMASREQ</b> | single word request, asserted by DBOP. This signal is asserted when there is at least one empty location in the FiFo                                                                               |
| <b>DBOPDMABREQ</b> | burst DMA transfer request, asserted by DBOP. This signal is asserted when there are at least four empty locations in the FiFo                                                                     |
| <b>DBOPDMACLR</b>  | DMA request clear, asserted by DMA controller to clear the DMA request signals. If DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst |

Symmetric FiFo

The FiFo buffer has two main purposes:

- data buffering: the FiFo contains 128 locations with 32 bits for data storage: with according DMA transfer, the data can be transferred in short time without need for any SW control

- clock domain crossing: the FiFo is at the boarder of clock domain PCLK and DBOPCLK. All necessary synchronisation is done internally. All flags are available as push flags (synchronised to the push clock PCLK) and pop flags (synchronised to the POP clk, which is synchronous to DBOPCLK).

The FiFo controller gives empty, almost empty, half full, almost full and full flags which are available in two fashions: synchronous to the push or the pop side (pop\_empty, push\_empty, ...).

### 7.3.12.3 Control Signal Generator

Four independent control signals can be generated: typical application for such signals is a 80xx interface with RS, RD\*, WR\* and E or a 68xx interface with RS, E, RWN. The idea of this control signal generator is a general-purpose block, which generates any signal timing/waveform that is necessary to transfer the data to any specific display.

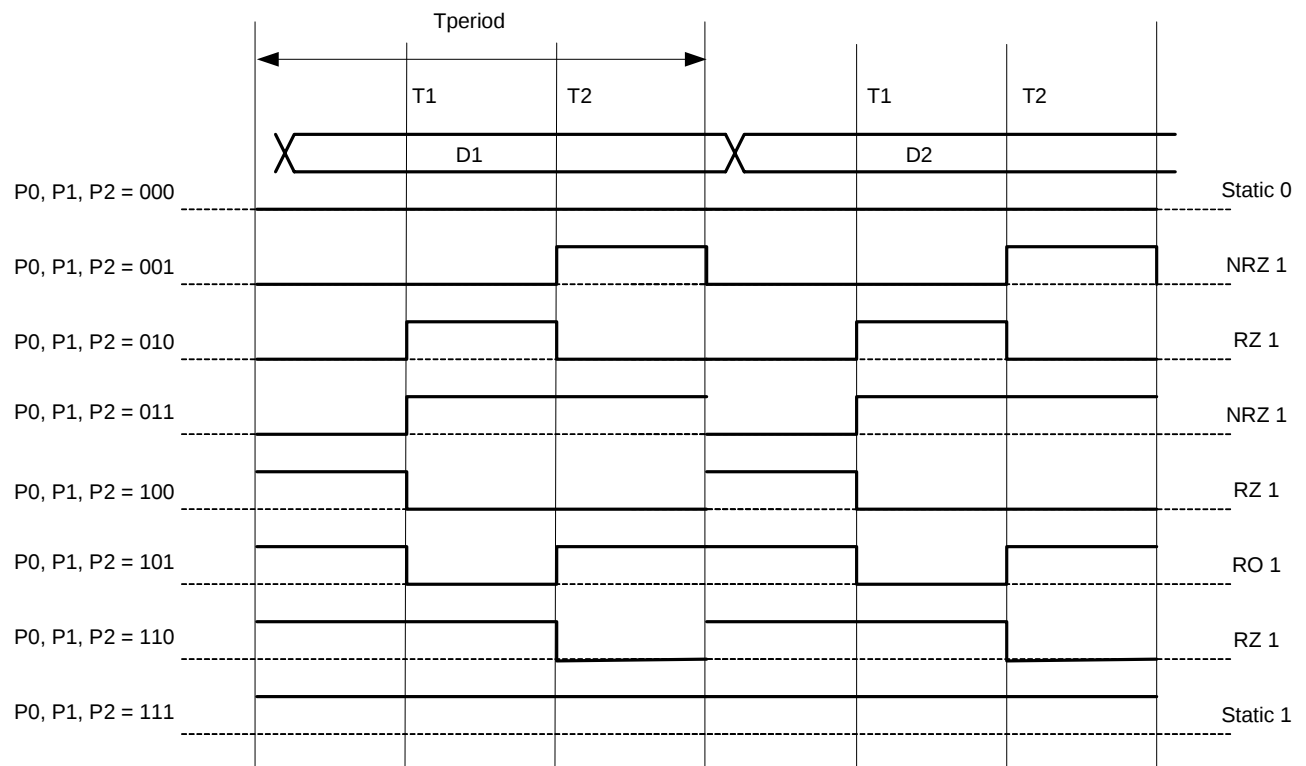
#### Polarity Parameters

For each of the control signals c0 - c3 following polarity parameters are defined:

- p0 ... polarity 0 at start of cycle
- p1 ... polarity 1 following polarity 0
- p2 ... polarity 2 following polarity 1

Following figure shows an example for timing waveforms defined with these control parameters.

Figure 34 DBOP timing waveform



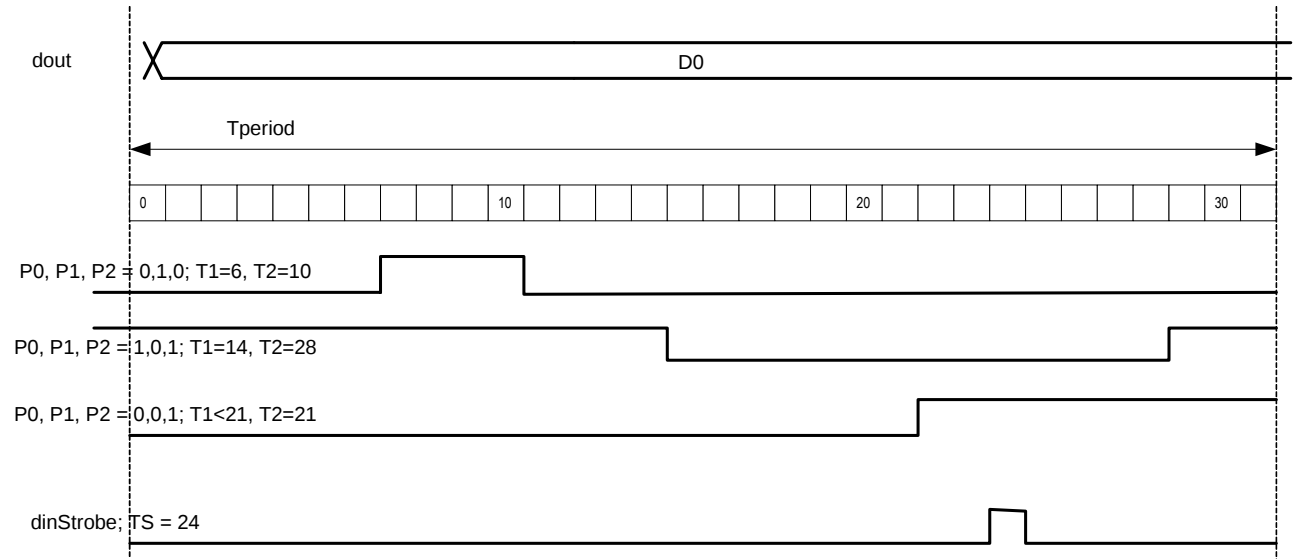
#### Quiescent State

The control signals are only generated with each data output cycle (data output cycles are generated as long as the FiFo is not empty). With FiFo empty and in the absence of a read cycle, all control signals are set to a quiescent state. For each control signal, this quiescent state can be programmed either to 1 or 0.

## Timing Parameters

Also the time points for change from p0-p1 (t1) and p1-p2 (t2) can be programmed. For these programmable timing parameters each data output cycle is divided into 32 steps. Both T1 and T2 can be in the range of 0 to 31. For short count bit set (sdc bit in control register), T1 and T2 must be in the range of 0 to 15.

Figure 35 DBOP timing parameters



### Even/odd generated signals

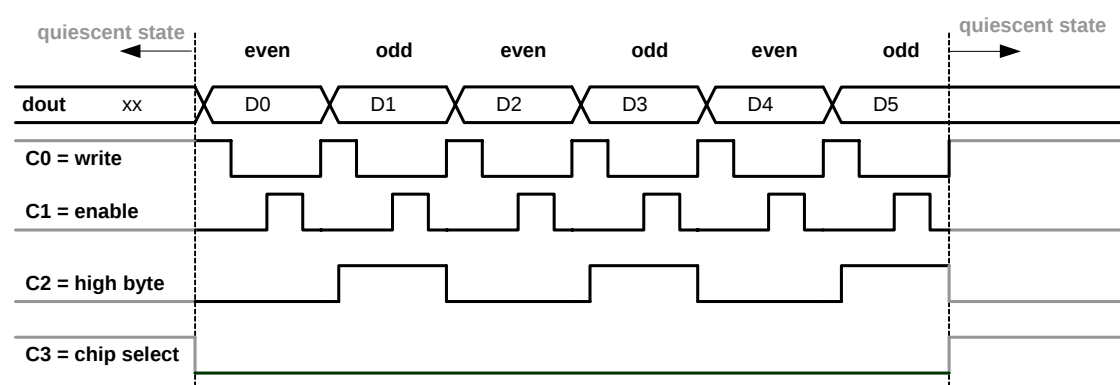
In addition to these timing parameters, signals can also be programmed to go active only during the even (0, 2, 4, ...) or the odd cycles (1, 3, 5, ...). For example the indication of even/odd bytes for the case that two bytes in serial are transmitted can be used.

Two control bits are used to set this signal behaviour:

evenEnable, oddEnable. For default, both are set to 1 and both cycles will appear. For cases where even or odd should be omitted, set according evenEnable/oddEnable to 0. With both set to 0, no cycles will appear at the output!

Following example illustrates a typical waveform for an output interface where the evenEnable=0 and oddEnable=1 for control signal C2. In this example, C2 is an active high indication of the high byte (D1, D3, D5, ...).

Figure 36 DBOP even/odd generated signals waveforms



Normally the even/odd cycles are toggling all the time, also if there are quiescent states in between. To have the possibility of defining a new start, reset of this even/odd counter can be done via the res\_even bit inside of the control register. With res\_even set, the counter starts with an even cycle. Res\_even is then set to 0 again by SW at the new start.

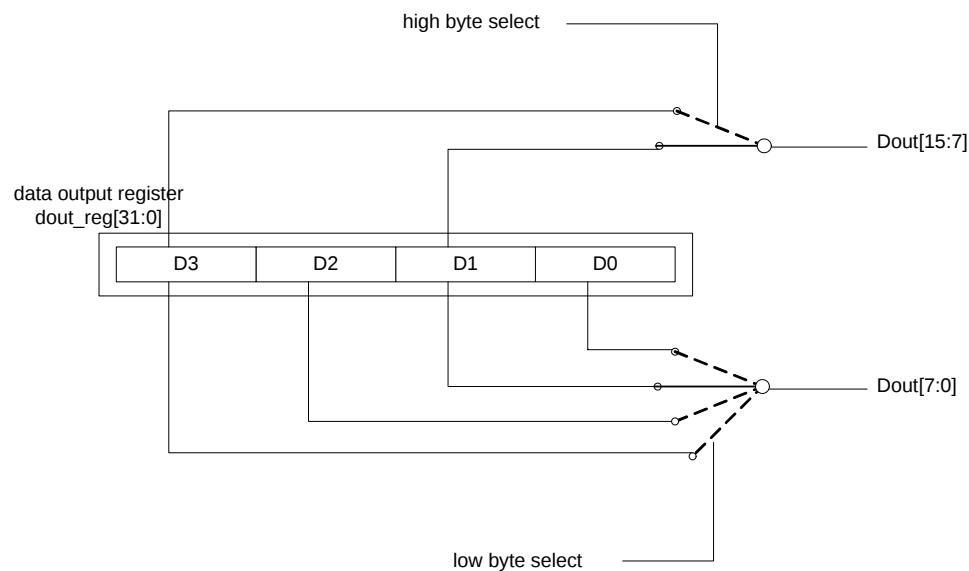
## Input strobe generation

In addition to the generation of the control signals, also an input strobe signal `dinStrobe` is generated within the control signal generator. With active `dinStrobe`, the input data are strobed with rising clock edge (see DIN register).

## 7.3.12.4 Data Output Register

The data output register handles different output widths and serial output mode (selected by parameters `osm` and `odw`). Following diagram illustrates the function of the data output register.

Table 75 DBOP data output register



The control part generates the according signals for low byte select and high byte select.

### 7.3.12.5 DIN register

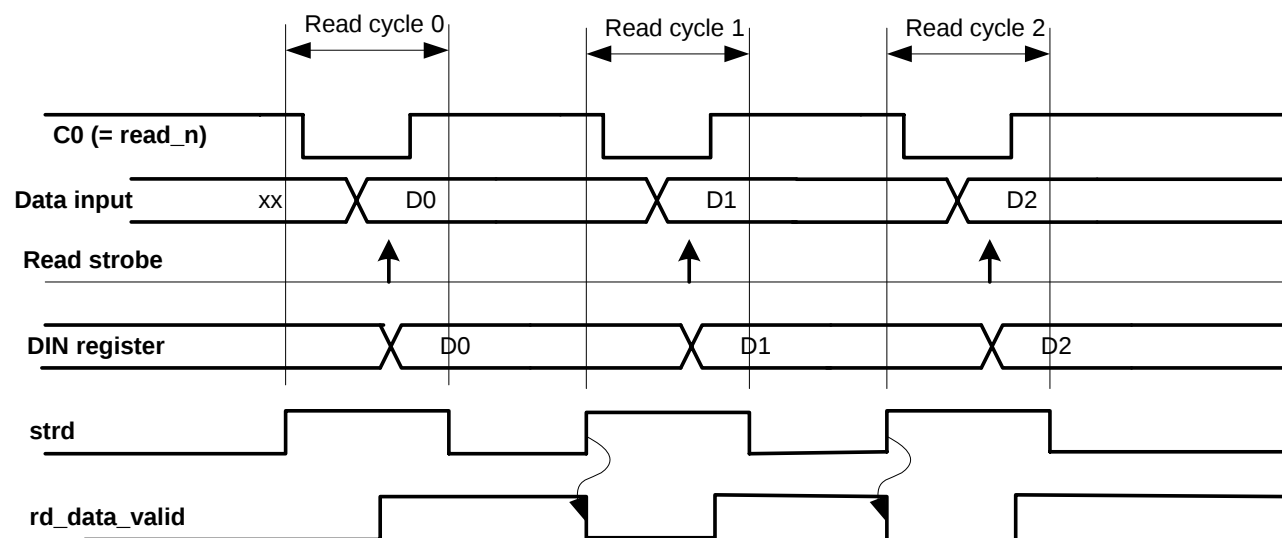
With the `dinStrobe`, data are written to the DIN register. This gives a simple mechanism, in which for example the status data can be read from a LCD display interface.

To do a data read, first the START READ (`strd`) bit is programmed into the control register. With START READ, the control signal generator starts to generate one cycle with the according control signals. Data are strobed by the programmed strobe time into the `din` register. After the cycle is completed the HW resets the `strd` bit to 0. With set of the `strd` bit, the `rd_data_valid` bit is also reset.

The SW just has to poll the `rd_data_valid` bit, when the bit gets set the input data can be read from the `din` register. After read cycle, the control signal generator returns to the quiescent state.

Following timing diagram shows an example of three read cycles.

Figure 37 DBOP read cycle example



Note: Be aware that the read cycle should only be activated when there is no active write cycle (FiFo is empty). Otherwise the results of such action get unpredictable.

For any read cycle, the write enable bit must be set to 0 (write disabled).

| start read<br>( <code>strd</code> ) | write enable<br>( <code>wen</code> ) | FiFo empty<br>Status | DBOP function |
|-------------------------------------|--------------------------------------|----------------------|---------------|
| 0                                   | 0                                    | 0                    | quiescent     |
| 0                                   | 0                                    | 1                    | quiescent     |
| 0                                   | 1                                    | 0                    | valid write   |
| 0                                   | 1                                    | 1                    | quiescent     |
| 1                                   | 0                                    | 0                    | valid read    |
| 1                                   | 0                                    | 1                    | valid read    |
| 1                                   | 1                                    | 0                    | valid write   |
| 1                                   | 1                                    | 1                    | quiescent     |

### 7.3.12.6 Interrupt Generator

Depending on the FiFo Status, an interrupt request can be generated. The conditions that cause an interrupt are set within the control register.

The interrupt output `DBOPIRQ` is active high.

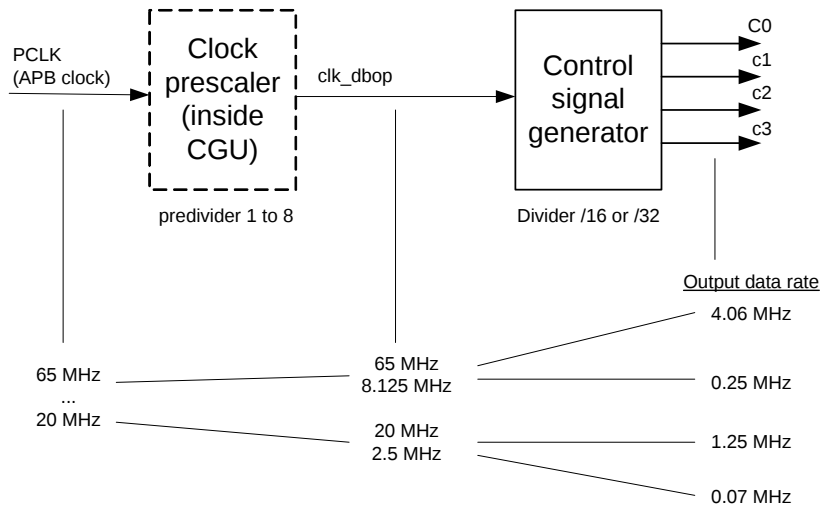
### 7.3.12.7 Clock frequencies

The input clock is directly taken from the PCLK clock. A programmable prescaler is implemented within the CGU. Input clock for the prescaler is in the range of 20 - 60 MHz.

Programmable division factors for the prescaler in the range of 1 to 8. Input clock to the module is in the range of 2.5 to 60 MHz.

Within the module the control signal generator is doing a division by 16 or 32 (selectable). So the effective output data rates are in the range of 1.25 to 4 MHz for maximum performance and can be scaled down in the range of 0.07 to 0.25 MHz.

Figure 38 DBOP data rate



Time constraining for the module should be done with 65 MHz, if there is a demand the time constraints for the output pads can be reduced.

### 7.3.12.8 Interface with GPIO PINs / additional PINs

For the SW, the usage of either ARM primecell GPIO ports or DBOP port can be configured with the GPIOAFSEL registers.

Following IO ports are used for the basic 8 bit interface

**xpc[7:0]** for dout[7:0] and din[7:0]  
**xpb[3:0]** for {C3, C2, C1, C0}

Following IO ports are used for the optional 16 bit interface

**xpb[7:4]** for dout[11:8] and din[11:8]  
**dbop\_d[15:12]** for dout[15:12] and din[15:12]

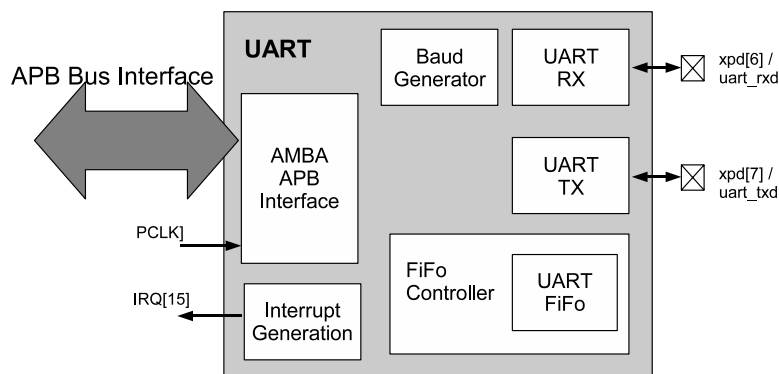
### 7.3.13 UART – Universal Asynchronous Receiver/Transmitter

The UART is a Universal Asynchronous Receiver Transmitter compatible to industry standard 16550 with APB slave interface. This UART provides FIFO based transmitter-receiver pair with programmable Baud-rate, character widths and parity encoding. Status and error information is also provided by the design. Maximum baud rate supported by this UART is 1Mbps for input clock of 16MHz.

#### Features

- Compliance to Industry Standard 16550 UART.
- APB slave interface.
- Separate 16x8 Transmit and 16x11 Receive FIFOs.
- Programmable FIFO disabling for 1-byte depth.
- Programmable Baud rate Generator.
- Independent masking for transmit, receive and Error interrupts.
- False Start bit detection.
- Line Break generation and detection.
- Fully programmable serial interface characteristics:
  - Supports 5,6,7 and 8 bits.
  - even, odd, stick and no parity generation and detection.
  - 1, 11/2 and 2 stop bits.

Figure 39 UART Block Diagram



### 7.3.13.1 UART Baud Generator and Clock Divider Settings

The internal baud generator module generates the required baud clock using the divisor register value. To achieve correct synchronization incoming bits are over sampled by a factor of 16x. Software should program the divisor value by which the system clock has to be divided to achieve the required baud clock frequency.

The equation to calculate baud divisor is

$$\text{Baud Divisor} = (\text{input frequency}) \div (\text{baud rate} \times 16)$$

**Important: the internal clock divider must be set to a value of 2 or higher. Setting the value to 1 (no division) is not allowed!**

For example, for 16 MHz PCLK clock following table gives the list of settings for different BAUD rates.

| Baud Rate | Required Baud clock frequency | Decimal divisor value |
|-----------|-------------------------------|-----------------------|
| 50        | 800                           | 20000                 |
| 75        | 1200                          | 13333                 |
| 110       | 1760                          | 9091                  |
| 134.5     | 2152                          | 7435                  |
| 150       | 2400                          | 6667                  |
| 300       | 4800                          | 3333                  |
| 600       | 9600                          | 1667                  |
| 1200      | 19200                         | 833                   |
| 1800      | 28800                         | 556                   |
| 2000      | 32000                         | 500                   |
| 4800      | 76800                         | 208                   |
| 7200      | 115200                        | 139                   |
| 9600      | 153600                        | 104                   |
| 19200     | 307200                        | 52                    |
| 38400     | 614400                        | 26                    |
| 56000     | 896000                        | 18                    |
| 128000    | 2048000                       | 8                     |
| 250000    | 4000000                       | 4                     |
| 300000    | 4800000                       | 3                     |
| 500000    | 8000000                       | 2                     |

### 7.3.13.2 UART Register Descriptions

All registers are 8 bits wide. Registers are selected based on the address and the value of Divisor Latch Select (DLS) bit in the line control register (UART\_LNCTR\_REG).

Table 76 UART registers

| Register Name      | Base Address     | Offset | DLS | Note                               |
|--------------------|------------------|--------|-----|------------------------------------|
| UART_DATA_REG      | AS3525_UART_BASE | 0x00   | 0   | Data register (Rx / Tx)            |
| UART_DLO_REG       | AS3525_UART_BASE | 0x00   | 1   | Clock divider lower byte register  |
| UART_DHI_REG       | AS3525_UART_BASE | 0x04   | 1   | Clock divider higher byte register |
| UART_INTEN_REG     | AS3525_UART_BASE | 0x04   | 0   | Interrupt enable register          |
| UART_INTSTATUS_REG | AS3525_UART_BASE | 0x08   |     | Interrupt status register          |
| UART_FCTL_REG      | AS3525_UART_BASE | 0x0C   |     | FIFO control register              |
| UART_LNCTL_REG     | AS3525_UART_BASE | 0x10   |     | Line control register              |
| UART_LNSTATUS_REG  | AS3525_UART_BASE | 0x14   |     | Line status register               |

Table 77 UART Data Register

| Name                                           |               | Base                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        | Default                                                                       |
|------------------------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------|
| UART_DATA_REG                                  |               | AS3525_UART_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |        | 0xC8110000                                                                    |
| <b>Offset: 0x00</b><br><b>DLS bit set to 0</b> |               | <b>Data register</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |                                                                               |
|                                                |               | Holds the data byte received or the data byte to be transmitted respectively.<br>RX:<br>This register holds the received data byte.<br>In FIFO mode, this byte will be the top byte of the 16-byte FIFO.<br>If FIFO mode is disabled, it will be the content of the receive shift register after a byte has been shifted in.<br>A read to the address value 3b000 with Divisor Latch Select (DLS) bit 1'b0 will give the content of this register.<br>If a character less than 8 bits is received, extra zero bits will be padded to this register.<br>TX:<br>This register contains the data to be transmitted. This register will be written by the processor.<br>In FIFO mode, a write to this address will write data into the FIFO.<br>In FIFO mode, top byte of txFIFO is passed on to transmitter shift register.<br>If FIFO is disabled, a write to the address 3'b000 with DLS bit 1'b0 will write into this register.<br>If FIFO is disabled, this register will be overwritten with new data.<br>If FIFO is disabled, data in this register will be passed on to transmitter shift register. |        |                                                                               |
| Bit                                            | Bit Name      | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Access | Bit Description                                                               |
| 7:0                                            | UART_DATA_REG | 00000000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | RW     | Holds the data byte received or the data byte to be transmitted respectively. |

Table 78 UART Clock divider lower byte register

| Name                                       |              | Base                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        | Default                                                                                  |
|--------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------|
| UART_DLO_REG                               |              | AS3525_UART_BASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | 0xC8110000                                                                               |
| <b>Offset: 0x00</b><br><b>DLS set to 1</b> |              | <b>Clock divider lower byte register</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |        |                                                                                          |
|                                            |              | This register holds the clock divider value (decimal) which is used to derive the baud clock. To achieve a desired baud rate, the baud clock should be 16-times higher than the baud rate. To derive this clock the ratio of the system clock and the required baud clock should be calculated and the value should be programmed into the clock divider lower byte and higher byte registers (UART_DLO_REG and UART_DHI_REG).<br>Clock divider value = (input frequency) / (baud rate x 16) |        |                                                                                          |
| Bit                                        | Bit Name     | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Access | Bit Description                                                                          |
| 7:0                                        | UART_DLO_REG | 00000000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | W      | This register holds the lower byte of the decimal divisor value to calculate baud clock. |

Table 79 UART Clock divider higher byte register

| Name                         |              | Base                                                                                      |        | Default                                                                                   |
|------------------------------|--------------|-------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------|
| UART_DHI_REG                 |              | AS3525_UART_BASE                                                                          |        | 0xC8110000                                                                                |
| Offset: 0x04<br>DLS set to 1 |              | Clock divider higher byte register                                                        |        |                                                                                           |
|                              |              | This register holds the higher byte of the decimal divisor value to calculate baud clock. |        |                                                                                           |
| Bit                          | Bit Name     | Default                                                                                   | Access | Bit Description                                                                           |
| 7:0                          | UART_DHI_REG | 00000000                                                                                  | W      | This register holds the higher byte of the decimal divisor value to calculate baud clock. |

Table 80 UART Interrupt enable register

| Name                         |               | Base                                                                                                                                  |        | Default                                        |
|------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------|
| UART_INTEN_REG               |               | AS3525_UART_BASE                                                                                                                      |        | 0xC8110000                                     |
| Offset: 0x04<br>DLS set to 0 |               | Interrupt enable register                                                                                                             |        |                                                |
|                              |               | This register will enable the three types of interrupts. Setting the bits of this register to logic 1 enables the selected interrupt. |        |                                                |
| Bit                          | Bit Name      | Default                                                                                                                               | Access | Bit Description                                |
| 7:3                          | Reserved      | 00000                                                                                                                                 |        | These bits are reserved for future use.        |
| 2                            | InStatusEn    | 0                                                                                                                                     | W      | This bit enables the "rxLineStatus" interrupt. |
| 1                            | txDataEmptyEn | 0                                                                                                                                     | W      | This bit enables the "txDataEmpty" interrupt.  |
| 0                            | rxDataRdyEn   | 0                                                                                                                                     | W      | This bit enables the "rxDataRdy" interrupt.    |

Table 81 UART Interrupt status register

| Name               |              | Base                                                                                                                                                                                                                                                                                                                                      |        | Default                                                                                                                                                                                                                                                                                 |
|--------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_INTSTATUS_REG |              | AS3525_UART_BASE                                                                                                                                                                                                                                                                                                                          |        | 0xC8110000                                                                                                                                                                                                                                                                              |
| Offset: 0x08       |              | Interrupt status register                                                                                                                                                                                                                                                                                                                 |        |                                                                                                                                                                                                                                                                                         |
|                    |              | This register will give the status of the interrupt. Depending on the enabled interrupt bits in the interrupt enable register (UART_INTEN_REG) different interrupts will be generated and the status will be updated in this register. On sensing an interrupt the software should read this register to get the status of the interrupt. |        |                                                                                                                                                                                                                                                                                         |
| Bit                | Bit Name     | Default                                                                                                                                                                                                                                                                                                                                   | Access | Bit Description                                                                                                                                                                                                                                                                         |
| 7:3                | Reserved     | 00000                                                                                                                                                                                                                                                                                                                                     |        | These bits are reserved for future use.                                                                                                                                                                                                                                                 |
| 2                  | rxLineStatus | 0                                                                                                                                                                                                                                                                                                                                         | RU     | This interrupt is set on any error condition on the receive line. There are four types of error possibilities. These error conditions are set in bits 4:1 of the line status register (UART_LNSTATUS_REG). This bit is reset on a read of the line status register (UART_LNSTATUS_REG). |
| 1                  | txDataEmpty  | 0                                                                                                                                                                                                                                                                                                                                         | RU     | In FIFO mode this bit is set when txFIFO is empty. If FIFO mode is disabled this interrupt is set if the data register (UART_DATA_REG (Tx)) is empty. This bit will be reset on write to the data register (UART_DATA_REG (Tx)).                                                        |

| Name               |           | Base                                                                                                                                                                                                                                                                                                                                      |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_INTSTATUS_REG |           | AS3525_UART_BASE                                                                                                                                                                                                                                                                                                                          |        | 0xC8110000                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Offset: 0x08       |           | Interrupt status register                                                                                                                                                                                                                                                                                                                 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                    |           | This register will give the status of the interrupt. Depending on the enabled interrupt bits in the interrupt enable register (UART_INTEN_REG) different interrupts will be generated and the status will be updated in this register. On sensing an interrupt the software should read this register to get the status of the interrupt. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Bit                | Bit Name  | Default                                                                                                                                                                                                                                                                                                                                   | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0                  | rxDataRdy | 0                                                                                                                                                                                                                                                                                                                                         | RU     | <p>This is the data ready interrupt.</p> <p>In FIFO mode this bit is set when the number of bytes in the FIFO reaches the trigger level. This bit is also set in FIFO mode when a timeout occurs in the reception, i.e. Rx line idle for more than 4 char times and there is data in the FIFO.</p> <p>If FIFO mode is disabled this bit is set when one full byte is received.</p> <p>This bit is cleared when the FIFO is empty or the data register (UART_DATA_REG (Rx)) is read.</p> |

Table 82 UART FIFO control register

| Name          |            | Base                                                                                                                                                                  |        | Default                                                                                                                                                                                                             |
|---------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_FCTL_REG |            | AS3525_UART_BASE                                                                                                                                                      |        | 0xC8110000                                                                                                                                                                                                          |
| Offset: 0x0C  |            | FIFO control register                                                                                                                                                 |        |                                                                                                                                                                                                                     |
|               |            | This register holds the control parameters to control receive (rx) and transmit (tx) FIFO. The parameters will enable the FIFOs, set the receiver trigger level, etc. |        |                                                                                                                                                                                                                     |
| Bit           | Bit Name   | Default                                                                                                                                                               | Access | Bit Description                                                                                                                                                                                                     |
| 7:5           | Reserved   | 000                                                                                                                                                                   |        | These bits are reserved for future use.                                                                                                                                                                             |
| 4:3           | trigLevel  | 00                                                                                                                                                                    | W      | <p>These two bits will select the trigger level for the rxFIFO. Once the FIFO pointer reaches this level rxDataRdy interrupt is asserted.</p> <p>00: 01 byte<br/>01: 04 bytes<br/>10: 08 bytes<br/>11: 14 bytes</p> |
| 2             | rxFIFORst  | 0                                                                                                                                                                     | W      | <p>This bit will reset rxFIFO pointers and clear all the bytes in the rxFIFO.</p> <p>This bit is self clearing, i.e. after resetting FIFO this bit will become zero.</p>                                            |
| 1             | txFIFORst  | 0                                                                                                                                                                     | W      | <p>This bit will reset txFIFO pointers and clear all the bytes in the txFIFO.</p> <p>This bit is self clearing, i.e. after resetting FIFO this bit will become zero.</p>                                            |
| 0             | FIFOModeEn | 0                                                                                                                                                                     | W      | This bit will enable the FIFO mode. By default this will be reset.                                                                                                                                                  |

Table 83 UART Line control register

| Name           |          | Base                                                                                                                                                                        |        | Default         |
|----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------|
| UART_LNCTL_REG |          | AS3525_UART_BASE                                                                                                                                                            |        | 0xC8110000      |
| Offset: 0x10   |          | Line control register                                                                                                                                                       |        |                 |
|                |          | This register controls the asynchronous data. Parameters in this register set the transmit and receive character format, the data length, parity bit, stop bit length, etc. |        |                 |
| Bit            | Bit Name | Default                                                                                                                                                                     | Access | Bit Description |

| Name           |             | Base                                                                                                                                                                        |        | Default                                                                                                                                                                                                                                                               |
|----------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_LNCTL_REG |             | AS3525_UART_BASE                                                                                                                                                            |        | 0xC8110000                                                                                                                                                                                                                                                            |
| Offset: 0x10   |             | Line control register                                                                                                                                                       |        |                                                                                                                                                                                                                                                                       |
|                |             | This register controls the asynchronous data. Parameters in this register set the transmit and receive character format, the data length, parity bit, stop bit length, etc. |        |                                                                                                                                                                                                                                                                       |
| Bit            | Bit Name    | Default                                                                                                                                                                     | Access | Bit Description                                                                                                                                                                                                                                                       |
| 7              | DLS         | 0                                                                                                                                                                           | RW     | Divisor Latch Select Bit. This bit is used to select Divisor Latch registers.<br>1: Divisor Latch registers can be accessed. To access other registers this bit should be zero.                                                                                       |
| 6              | breakCntl   | 0                                                                                                                                                                           | RW     | 1: Will cause a break condition to be transmitted, i.e. TX line is pulled low. Normal transmission can be recovered once this bit is cleared. Transmitter logic can be used as break timer.                                                                           |
| 5              | stickParity | 0                                                                                                                                                                           | RW     | 1: If this bit is set, along with parityEn a fixed parity bit will be transmitted and expected. This fixed parity bit will be the complement of the bit 4.                                                                                                            |
| 4              | evenParity  | 0                                                                                                                                                                           | RW     | 0: Data byte along with parity bit will be sent and expected to be odd parity.<br>1: Data byte along with the parity bit will be even parity.                                                                                                                         |
| 3              | parityEn    | 0                                                                                                                                                                           | RW     | Enable parity bit.<br>0: Data byte will be transmitted and received without parity bit.<br>1: Will enable the parity bit at the end of the data byte.                                                                                                                 |
| 2              | stopBits    | 0                                                                                                                                                                           | RW     | This bit decides how many stop bits should be sent along with a data byte.<br>0: 1 stop bit transmitted<br>1: 2 stop bits transmitted if 6, 7 or 8 bit wordLenSel<br>1: 1.5 stop bits transmitted if 5 bit wordLenSel<br>Receiver will always check for one stop bit. |
| 1:0            | wordLenSel  | 00                                                                                                                                                                          | RW     | These bits will select the number of data bits to be transmitted and received.<br>00: 5 bits<br>01: 6 bits<br>10: 7 bits<br>11: 8 bits                                                                                                                                |

Table 84 UART Line status register

| Name              |                | Base                                                                                                           |        | Default                                                                                                                                                                                                                                                                                   |
|-------------------|----------------|----------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_LNSTATUS_REG |                | AS3525_UART_BASE                                                                                               |        | 0xC8110000                                                                                                                                                                                                                                                                                |
| Offset: 0x14      |                | Line status register                                                                                           |        |                                                                                                                                                                                                                                                                                           |
|                   |                | This register holds the status information of the data transfer. It gives information about the received data. |        |                                                                                                                                                                                                                                                                                           |
| Bit               | Bit Name       | Default                                                                                                        | Access | Bit Description                                                                                                                                                                                                                                                                           |
| 7                 | FIFODataError  | 0                                                                                                              | RU     | 1: This bit is set when any data character in the FIFO has parity or framing error or break condition.<br>0: This bit is reset once the line status register (LINE_STATUS_REG) is read.                                                                                                   |
| 6                 | Reserved       | 0                                                                                                              |        | This bit is reserved for future use.                                                                                                                                                                                                                                                      |
| 5                 | txHoldRegEmpty | 0                                                                                                              | RU     | This bit is associated with the txDataEmpty interrupt.<br>1: Indicates that there is no data in txFIFO or the data register (UART_DATA_REG (Tx)). This bit is set once the data is shifted out.<br>0: This bit is reset once data is written into the data register (UART_DATA_REG (Tx)). |

| Name              |              | Base                                                                                                           |        | Default                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|--------------|----------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_LNSTATUS_REG |              | AS3525_UART_BASE                                                                                               |        | 0xC8110000                                                                                                                                                                                                                                                                                                                                                                 |
| Offset: 0x14      |              | Line status register                                                                                           |        |                                                                                                                                                                                                                                                                                                                                                                            |
|                   |              | This register holds the status information of the data transfer. It gives information about the received data. |        |                                                                                                                                                                                                                                                                                                                                                                            |
| Bit               | Bit Name     | Default                                                                                                        | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                            |
| 4                 | breakDetect  | 0                                                                                                              | RU     | This bit is associated with the rxLineStatus interrupt.<br>1: This bit is set if a break condition is detected, i.e. if a zero is detected on receive line for one full character duration. This condition will always cause framingError condition.                                                                                                                       |
| 3                 | framingError | 0                                                                                                              | RU     | This bit is associated with the rxLineStatus interrupt.<br>1: Indicates that the first stop bit of the received data byte is not valid, i.e. a zero is received in place of a one.<br>This error condition causes the receiver to re-synchronize.                                                                                                                          |
| 2                 | parityError  | 0                                                                                                              | RU     | This bit is associated with rxLineStatus interrupt.<br>1: Indicates that parity of the received data byte is different from the expected parity as set in the line control register (UART_LNCTL_REG).                                                                                                                                                                      |
| 1                 | overrunError | 0                                                                                                              | RU     | This bit is associated with the rxLineStatus interrupt.<br>1: Indicates an error condition which occurs when one character is fully assembled by the receiver but there is no space to write that byte.<br>In FIFO mode, the content of the FIFO remains unaffected.<br>If FIFO is disabled, the data register (UART_DATA_REG (Rx)) will be overwritten with the new data. |
| 0                 | dataReady    | 0                                                                                                              | RU     | 0: There is no data available.<br>1: There are one or more data bytes ready to be read by the processor.                                                                                                                                                                                                                                                                   |

### 7.3.14 CGU - Clock generation unit

The clock generation unit generates all clocks for all modules on the chip.

- Hardware programmable selection of clock input either from internal oscillator or external clock input
- Two on-chip PLL circuits for generation of internal clocks
- Programmable divider for generation of ARM922T clock (fclk)
- Programmable divider for generation of AMBA bus clock (pclk)
- Support of ARM922T fastbus, synchronous and asynchronous mode
- Included clock gating registers to optimise power consumption
- Three clock busses at input of all dividers (clk\_main, clk\_a, clk\_b) for utmost flexibility
- Spike-free switches between divider clock inputs (clk\_main, clk\_a, clk\_b)
- Independent clock dividers for peripheral modules

#### System startup

At startup, the system is configured in a way to run without the need of PLLs. PLLs are disabled and clk\_main is used for generation of the clock for the ARM controller (fclk) and ARM AMBA bus (pclk). Within the clock gating register, only the clocks that are really necessary for initial boot are enabled: clock for ARM, for the internal 1-TRAM memory, for the internal ROM and for the external memory. So the boot loader can start either from internal ROM or from the external MPMC.

#### Clock switching

The system can be reconfigured to run from PLLA or PLLB. Because the 1-TRAM is a dynamic memory that must always get the clock for the internal memory refresh, this switching must be implemented in a way that the PCLK clock is never stopped. The easiest solution to fulfil this requirement is always switching back to clk\_main for reconfiguring the PLLs. After reprogramming of the PLLs it must be checked that the PLLs are locked before the system is switched onto the PLL output frequency.

#### ARM922T and AMBA bus clock

The ARM processor can run in different modes. These modes can be set within the iA, nF bits of the ARM922T CP15 (coprocessor) register 1.

##### Fastbus mode

This is the default mode after startup. The ARM922T input clock frequency is the same as the AHB/APB bus frequency.

##### Synchronous mode

Within the synchronous mode, the ARM922T frequency must be higher than the AHB/APB bus frequency and it must be an integer multiple of the AHB/APB bus frequency. Advantage of the synchronous mode is a higher performance because of less synchronisation effort between the ARM922T and the AHB bus.

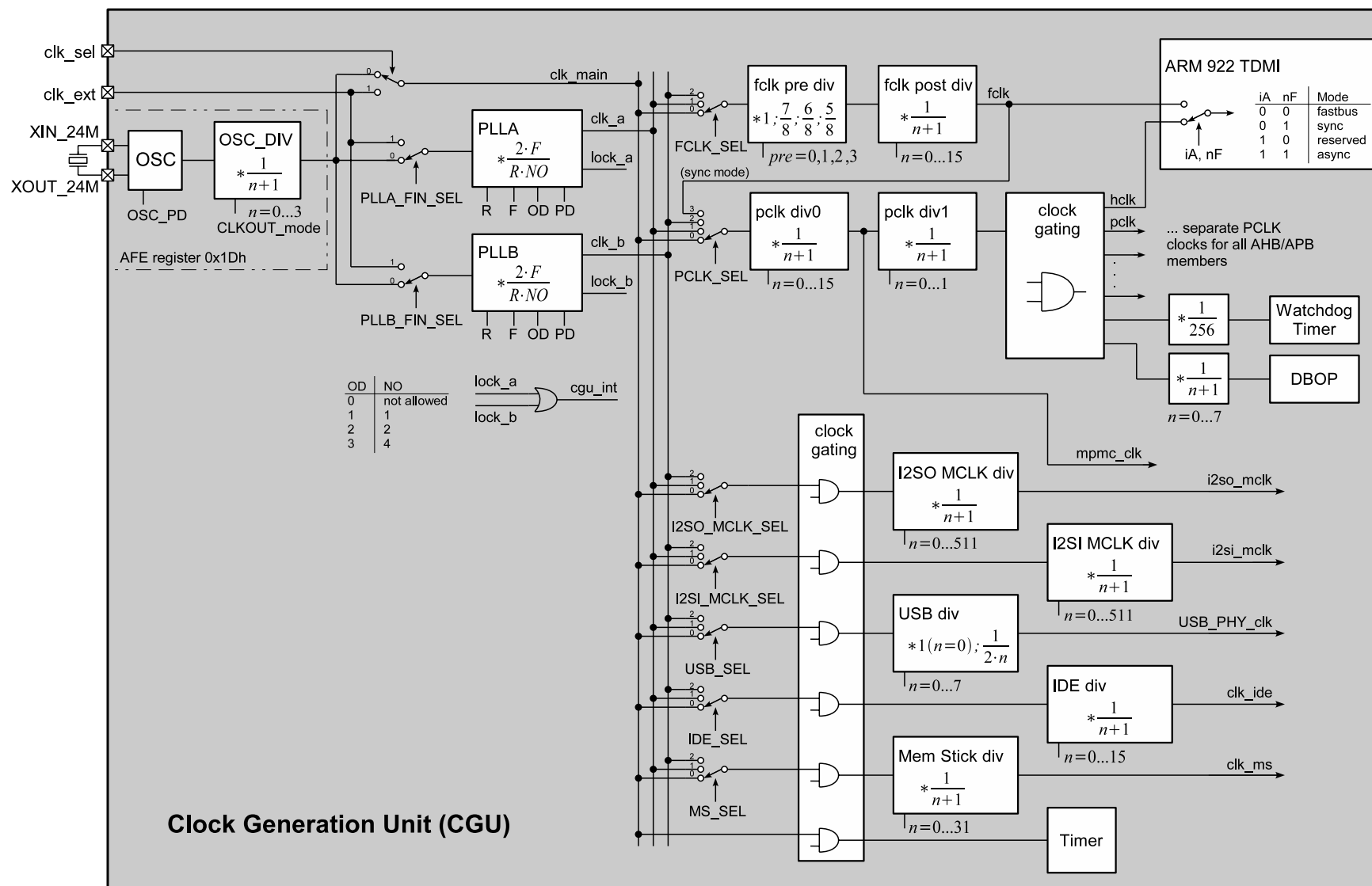
##### Asynchronous mode

Within asynchronous mode, the ARM922T frequency must be higher than the AHB bus frequency, but it can be completely asynchronous. Disadvantage is a slightly reduced performance of the system because of the higher effort for synchronisation between the ARM922T and AHB clock domains.

#### Block Diagram

The block diagram on the following page gives a detailed view of the structure of the CGU.

Figure 40 Clock generation unit block diagram



### 7.3.14.1 Input clock selection

Input clock is either coming directly from the clk\_ext pin or from the internal 24MHz crystal oscillator. Usage of external pin or internal oscillator is selected by the dedicated pin clk\_sel.

Table 85 Clock Selection

| Clk_sel | Description        |
|---------|--------------------|
| 0       | clk_main = clk_int |
| 1       | clk_main = clk_ext |

Three main internal clocks are generated as source for all clock dividers for all modules.

- clk\_a, clk\_b: the outputs of two independently configurable PLLs.
- clk\_main: this clock is always available without the need of configuring any internal PLL

An important constraint of the system is the memory type of the RAM: the internal 1-TRAM needs refresh cycles, with the following important restrictions:

- the free running AHB/APB clock (PCLK) for the 1-TRAM must always be present: also for changing frequency settings, this must be taken into account (e.g. switch from clk\_main to PLL output only after PLL is settled (start-up time)).
- the minimum frequency for the free running AHB/APB clock of the 1-TRAM is 20 MHz.

**Important note: Switching between the different frequencies must be done in a pre-defined order using the CGU-driver software.**

### 7.3.14.2 Clock Gating

For all peripheral clock domains clock gating is possible. Clock gating can be enabled/disabled by the corresponding bits within the clock control register CGU\_PERI. After start-up, only the modules, which are necessary for booting the device, are enabled. These enabled peripherals are

- 1-TRAM controller and 1-TRAM macros
- external memory interface MPMC
- internal ROM
- vectored IR controller (VIC)

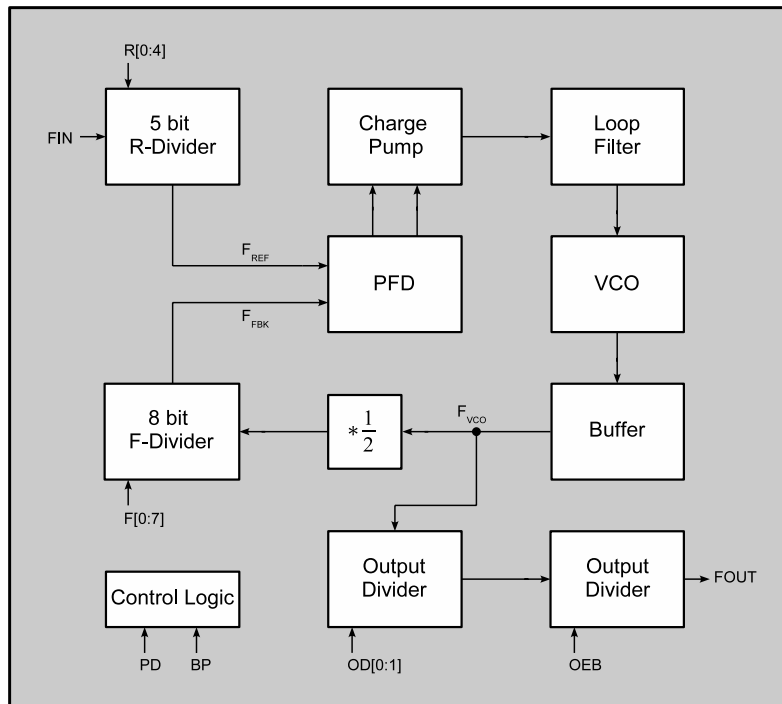
### 7.3.14.3 Interrupt generation

An interrupt can be generated after the PLL is locked.

#### 7.3.14.4 PLL description

- runs on single power supply at 1.2 V (special power PADs are used within the chip layout to guarantee lowest jitter: vddapll, vssapll which are connected to vdd\_core, vss\_core within the BGA substrate)
- fully integrated with internal loop filter
- VCO operating frequency from 200 - 400 MHz
- phase comparator input frequency from 2 - 8 MHz
- low power dissipation of typical 2.5 mW

Figure 41 PLL block diagram



#### Programming and calculation of the PLL output frequency

The output frequency is controlled by three programmable dividers within the PLL. These dividers are: the input divider NR, the feedback divider NF and the output divider NO. The divider settings are programmed by bits within CGU\_PLLA, CGU\_PLLB registers. The table on the following page gives the detailed formulas for setting the PLL output frequency.

Table 86 Setting the PLL output frequency

Input divider NR:

$$NR = 16 \cdot R4 + 8 \cdot R3 + 4 \cdot R2 + 2 \cdot R1 + R0$$

Feedback divider NF:

$$NF = 2 \cdot (128 \cdot F7 + 64 \cdot F6 + 32 \cdot F5 + 16 \cdot F4 + 8 \cdot F3 + 4 \cdot F2 + 2 \cdot F1 + F0)$$

Output divider NO:

| Output divider setting | NO (output divider value) |
|------------------------|---------------------------|
| OD0=0, OD1=0           | Not allowed               |
| OD0=1, OD1=0           | 1                         |
| OD0=0, OD1=1           | 2                         |
| OD0=1, OD1=1           | 4                         |

The PLL output frequency is calculated with following formula

$$\text{Output frequency} \quad f_{out} = \frac{NF}{NR \cdot NO} \cdot f_{in}$$

$$\text{Comparison frequency} \quad f_{ref} = \frac{f_{in}}{NR}$$

$$\text{VCO frequency} \quad f_{vco} = \frac{NF}{NR} \cdot f_{in}$$

Following constraints must be followed for the comparison and output frequency:

$$2 \text{ MHz} \leq f_{ref} \leq 8 \text{ MHz}$$

$$200 \text{ MHz} \leq f_{VCO} \leq 400 \text{ MHz}$$

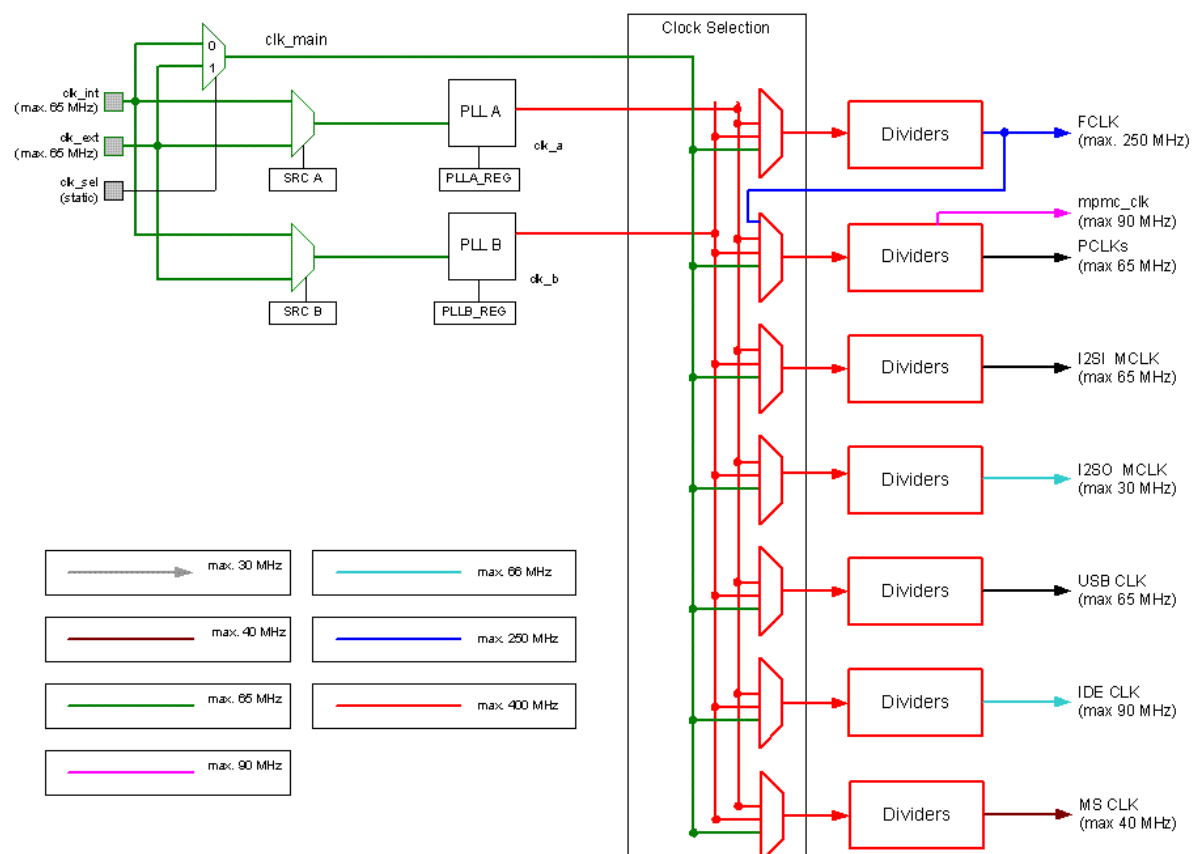
## Clock Constraining

Different clocks are constraint to different maximum clock speeds. As the clock frequencies can be set by software, care must be taken not to exceed these maximum clock frequencies.

Table 879 Clock Constraining

| Clock Domain | Max. Freq. [MHz] | Description                            |
|--------------|------------------|----------------------------------------|
| FCLK         | 250              | Processor Clock                        |
| PCLK         | 65               | AHB/APB bus clock                      |
| MPMC_CLK     | 90               | MPMC (external memory interface) clock |
| I2SI MCLK    | 65               | I2S input interface master clock       |
| I2SO MCLK    | 30               | I2S output interface master clock      |
| USB CLK      | 48               | USB interface clock                    |
| IDE CLK      | 90               | IDE interface clock                    |
| MS CLK       | 40               | Memory Stick Interface clock           |

Figure 42 Clock Generation Unit Block Diagram



## 7.3.14.5 Clock Generation Unit Registers

Table 20 CGU Registers

| Register Name | Base Address    | Offset | Note                                     |
|---------------|-----------------|--------|------------------------------------------|
| CGU_PLLA      | AS3525_CGU_BASE | 0x00   | PLLA configuration register              |
| CGU_PLLB      | AS3525_CGU_BASE | 0x04   | PLLB configuration register              |
| CGU_PLLASUP   | AS3525_CGU_BASE | 0x08   | PLLA supervisor register                 |
| CGU_PLLBSUP   | AS3525_CGU_BASE | 0x0C   | PLLB supervisor register                 |
| CGU_PROC      | AS3525_CGU_BASE | 0x10   | processor clock control register         |
| CGU_PERI      | AS3525_CGU_BASE | 0x14   | peripheral clock control register        |
| CGU_AUDIO     | AS3525_CGU_BASE | 0x18   | audio clock control register             |
| CGU_USB       | AS3525_CGU_BASE | 0x1C   | USB clock control register               |
| CGU_INTCTRL   | AS3525_CGU_BASE | 0x20   | CGU interrupt mask and enable register   |
| CGU_IRQ       | AS3525_CGU_BASE | 0x24   | interrupt clear and lock status register |
| CGU_COUNTA    | AS3525_CGU_BASE | 0x28   | PLLA lock counter register               |
| CGU_COUNTB    | AS3525_CGU_BASE | 0x2C   | PLLB lock counter register               |
| CGU_IDE       | AS3525_CGU_BASE | 0x30   | IDE clock control register               |
| CGU_MS        | AS3525_CGU_BASE | 0x34   | Memory Stick clock control register      |
| CGU_DBOP      | AS3525_CGU_BASE | 0x38   | DBOP clock controller register           |

Table 21 CGU\_PLLA Register

| Name       |               | Base                                                 |        | Default                              |
|------------|---------------|------------------------------------------------------|--------|--------------------------------------|
| CGU_PLLA   |               | AS3525_CGU_BASE                                      |        | 0x00                                 |
| Offset0x00 |               | PLLA Configuration Register                          |        |                                      |
|            |               | The CGU_PLLA register is used to configure the PLL A |        |                                      |
| Bit        | Bit Name      | Default                                              | Access | Bit Description                      |
| 14:13      | PLLA_OD [1:0] | 0x00                                                 | R/W    | PLLA output divider control, 2 bit   |
| 12:8       | PLLA_R [4:0]  | 0x00                                                 | R/W    | PLLA input divider control, 5-bit    |
| 7:0        | PLLA_F [7:0]  | 0x00                                                 | R/W    | PLLA feedback divider control, 8 bit |

Table 22 CGU\_PLLB Register

| Name       |               | Base                                                 |        | Default                              |
|------------|---------------|------------------------------------------------------|--------|--------------------------------------|
| CGU_PLLB   |               | AS3525_CGU_BASE                                      |        | 0x00                                 |
| Offset0x04 |               | PLLB Configuration Register                          |        |                                      |
|            |               | The CGU_PLLB register is used to configure the PLL B |        |                                      |
| Bit        | Bit Name      | Default                                              | Access | Bit Description                      |
| 14:13      | PLLB_OD [1:0] | 0x00                                                 | R/W    | PLLB output divider control, 2 bit   |
| 12:8       | PLLB_R [4:0]  | 0x00                                                 | R/W    | PLLB input divider control, 5-bit    |
| 7:0        | PLLB_F [7:0]  | 0x00                                                 | R/W    | PLLB feedback divider control, 8 bit |

Table 23 PLLA Supervisor Register

| Name        |              | Base                                                                                                                                  |        | Default                                                          |
|-------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------|
| CGU_PLLASUP |              | AS3525_CGU_BASE                                                                                                                       |        | 0x08                                                             |
| Offset0x08  |              | PLLA Supervisor Register                                                                                                              |        |                                                                  |
|             |              | This register contains control bits of the PLLA which are used very rarely, but have major impact on the functionality of the system. |        |                                                                  |
| Bit         | Bit Name     | Default                                                                                                                               | Access | Bit Description                                                  |
| 3           | PLLA_PD      | 0x00                                                                                                                                  | R/W    | PLLA power down if SET                                           |
| 2           | PLLA_OEB     | 0x00                                                                                                                                  | R/W    | PLLA output enable, active low                                   |
| 1           | PLLA_BP      | 0x00                                                                                                                                  | R/W    | PLLA bypass if SET                                               |
| 0           | PLLA_FIN_SEL | 0x00                                                                                                                                  | R/W    | PLLA clock source select<br>0: clk_int [PAD]<br>1: clk_ext [PAD] |

Table 24 PLBB Supervisor Register

| Name        |              | Base                                                                                                                                  |        | Default                                                          |
|-------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------|
| CGU_PLLBSUP |              | AS3525_CGU_BASE                                                                                                                       |        | 0x08                                                             |
| Offset0x0c  |              | PLLB Supervisor Register                                                                                                              |        |                                                                  |
|             |              | This register contains control bits of the PLLB which are used very rarely, but have major impact on the functionality of the system. |        |                                                                  |
| Bit         | Bit Name     | Default                                                                                                                               | Access | Bit Description                                                  |
| 3           | PLLB_PD      | 0x00                                                                                                                                  | R/W    | PLLB power down if SET                                           |
| 2           | PLLB_OEB     | 0x00                                                                                                                                  | R/W    | PLLB output enable, active low                                   |
| 1           | PLLB_BP      | 0x00                                                                                                                                  | R/W    | PLLB bypass if SET                                               |
| 0           | PLLB_FIN_SEL | 0x00                                                                                                                                  | R/W    | PLLB clock source select<br>0: clk_int [PAD]<br>1: clk_ext [PAD] |

Table 25 Processor Clock Controller Register

| Name       |                        | Base                                                                            |        | Default                                                                                                                     |
|------------|------------------------|---------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------|
| CGU_PROC   |                        | AS3525_CGU_BASE                                                                 |        | 0x00                                                                                                                        |
| Offset0x10 |                        | Processor Clock Controller Register                                             |        |                                                                                                                             |
|            |                        | This register contains control bits for ARM processor clock generation => FCLK. |        |                                                                                                                             |
| Bit        | Bit Name               | Default                                                                         | Access | Bit Description                                                                                                             |
| 7:4        | FCLK_POSTDIV_SEL [3:0] | 0x00                                                                            | R/W    | post divider division ratio => post_div = 1/(fclk_postdiv_sel + 1)                                                          |
| 3:2        | FCLK_PREDIV_SEL [1:0]  | 0x00                                                                            | R/W    | pre divider (fractional) division ratio<br>00: pre_div = 1/1<br>01: pre_div = 7/8<br>10: pre_div = 6/8<br>11: pre_div = 5/8 |
| 1:0        | FCLK_SEL[1:0]          | 0x00                                                                            | R/W    | clkin select<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main)                                 |

NOTE:  $f(\text{fclk}) := f(\text{clkin}) * \text{pred\_div} * \text{post\_div}$ ;

Table 26 Peripheral Clock Controller Register

| Name       |                     | Base                                                |        | Default                                                                               |
|------------|---------------------|-----------------------------------------------------|--------|---------------------------------------------------------------------------------------|
| CGU_PERI   |                     | AS3525_CGU_BASE                                     |        | 0x0F800000                                                                            |
| Offset0x14 |                     | Peripheral clock controller register                |        |                                                                                       |
|            |                     | This register allows setting the peripheral clocks. |        |                                                                                       |
| Bit        | Bit Name            | Default                                             | Access | Bit Description                                                                       |
| 28         | MBIST_EN            | 0                                                   | R/W    | memory bist manager clock enable                                                      |
| 27         | EXTMEM_EN           | 1                                                   | R/W    | external memory clock enable                                                          |
| 26         | EXTMEMIF_EN         | 1                                                   | R/W    | external memory AHB IF clock enable                                                   |
| 25         | 1TRAM_EN            | 1                                                   | R/W    | 1TRAM controller AHB IF clock enable                                                  |
| 24         | ROM_EN              | 1                                                   | R/W    | ROM AHB IF clock enable                                                               |
| 23         | VIC_EN              | 1                                                   | R/W    | vectored interrupt controller AHB IF clock enable                                     |
| 22         | DMAC_EN             | 0                                                   | R/W    | DMA controller AHB IF clock enable                                                    |
| 21         | USB_EN              | 0                                                   | R/W    | USB controller AHB IF clock enable                                                    |
| 20         | I2SO_APB_EN         | 0                                                   | R/W    | I2Sout APB IF clock enable                                                            |
| 19         | I2SI_APB_EN         | 0                                                   | R/W    | I2Sin APB IF clock enable                                                             |
| 18         | I2C_EN              | 0                                                   | R/W    | I2C master/slave APB IF clock enable                                                  |
| 17         | I2C_AUDIO_EN        | 0                                                   | R/W    | I2C audio APB IF clock enable                                                         |
| 16         | GPIO_EN             | 0                                                   | R/W    | general purpose IO APB IF clock enable                                                |
| 15         | SDMCI_EN            | 0                                                   | R/W    | secure digital/multimedia APB IF clock enable                                         |
| 14         | NANDFLASH_EN        | 0                                                   | R/W    | NAND flash/Smart Media APB IF clock enable                                            |
| 13         | UART_EN             | 0                                                   | R/W    | UART APB IF clock enable                                                              |
| 12         | WDOCNT_EN           | 0                                                   | R/W    | watchdog counter clock enable                                                         |
| 11         | WDOIF_EN            | 0                                                   | R/W    | watchdog timer module APB IF clock enable                                             |
| 10         | SSP_EN              | 0                                                   | R/W    | synchronous serial port APB IF clock enable                                           |
| 9          | TIMER1_EN           | 0                                                   | R/W    | timer module timer1 clock enable                                                      |
| 8          | TIMER2_EN           | 0                                                   | R/W    | timer module timer2 clock enable                                                      |
| 7          | TIMERIF_EN          | 0                                                   | R/W    | timer module APB IF clock enable                                                      |
| 6          | PCLK_DIV1_SEL       | 0                                                   | R/W    | division ratio div1 (AHB/APB clock) => div1 = 1/(pclk_div1_sel + 1)                   |
| 5:2        | PCLK_DIV0_SEL [3:0] | 0x0                                                 | R/W    | division ratio div0 (ext. memory clock) => div0 = 1/(pclk_div0_sel + 1)               |
| 1:0        | PCLK_SEL[1:0]       | 0x0                                                 | R/W    | clk in select<br>b'00: clk_main<br>b'01: pll_a_fout<br>b'10: pll_b_fout<br>b'11: fclk |

CAUTION: Clock gating takes effect immediately! Software must assure that all transactions to/from the module are finished before the clock is disabled.

CAUTION: The peripheral clock must not exceed 65 MHz. The software must assure that requirement.

Note:

$f(\text{clk\_extmem}) := f(\text{clk in}) * \text{div0};$

$f(\text{pclk}) := f(\text{clk in}) * \text{div0} * \text{div1};$

Table 27 Audio Clock Controller Register

| Name       |                         | Base                                                                            |        | Default                                                                                               |
|------------|-------------------------|---------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------|
| CGU_AUDIO  |                         | AS3525_CGU_BASE                                                                 |        | 0x00                                                                                                  |
| Offset0x18 |                         | Audio Clock Controller Register                                                 |        |                                                                                                       |
|            |                         | This register allows setting the audio clock to I2S input and output interface. |        |                                                                                                       |
| Bit        | Bit Name                | Default                                                                         | Access | Bit Description                                                                                       |
| 24         | I2SI_MCLK2PAD_EN        | 0                                                                               | R/W    | I2S audio input clock (I2SI_MCLK) to PAD connection enable                                            |
| 23         | I2SI_MCLK_EN            | 0                                                                               | R/W    | I2S audio input clock (I2SI_MCLK) enable                                                              |
| 22:14      | I2SI_MCLK_DIV_SEL [8:0] | 0x0                                                                             | R/W    | I2Sin audio IF clock division ratio => $div_i = 1/(i2si\_mclk\_div\_sel + 1)$                         |
| 13:12      | ISI_MCLK_SEL[1:0]       | 0x0                                                                             | R/W    | I2SI_MCLK clkin select<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main) |
| 11         | I2SO_MCLK_EN            | 0                                                                               | R/W    | I2S audio output clock (I2SO_MCLK) enable                                                             |
| 10:2       | I2SO_MCLK_DIV_SEL [8:0] | 0x0                                                                             | R/W    | I2Sout audio IF clock division ratio => $div_o = 1/(i2so\_mclk\_div\_sel + 1)$                        |
| 1:0        | ISO_MCLK_SEL[1:0]       | 0x0                                                                             | R/W    | I2SO_MCLK clkin select<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main) |

Note:

The clock gating bits in this register apply only to the audio clocks. To enable/disable the APB parts of the corresponding I2S IF CGU\_PERI has to be configured.

$f(i2si\_mclk) := f(i2si\_mclk\ clkin) * div_i;$

$f(i2so\_mclk) := f(i2so\_mclk\ clkin) * div_o;$

Table 28 Processor USB Clock Controller Register

| Name        |                   | Base                                                      |        | Default                                                                                      |
|-------------|-------------------|-----------------------------------------------------------|--------|----------------------------------------------------------------------------------------------|
| CGU_USB     |                   | AS3525_CGU_BASE                                           |        | 0x00                                                                                         |
| Offset 0x1c |                   | USB Clock Controller Register                             |        |                                                                                              |
|             |                   | This register allows setting the USB PHY interface clock. |        |                                                                                              |
| Bit         | Bit Name          | Default                                                   | Access | Bit Description                                                                              |
| 5           | USB_CLK_EN        | 0x00                                                      | R/W    | USB PHY clock enable => clk_usb                                                              |
| 4:2         | USB_DIV_SEL [2:0] | 0x00                                                      | R/W    | division ratio<br>0: div = 1/1<br>> 0: div = 1/(2*n); (even division factors only)           |
| 1:0         | USB_SEL[1:0]      | 0x00                                                      | R/W    | clk_in select<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main) |

Note:

The clock gating bit applies only to the USB PHY clock. To enable/disable the clock to the AHB part (USB CORE) CGU\_PERI has to be configured.

$$f(\text{clk\_usb}) = f(\text{clk\_core\_48m}) = f(\text{clk\_in}) * \text{div};$$

Table 29 Interrupt Mask and PLL Lock Status Register

| Name         |                  | Base                                        |        | Default                                               |
|--------------|------------------|---------------------------------------------|--------|-------------------------------------------------------|
| CGU_INTCTRL  |                  | AS3525_CGU_BASE                             |        | 0x00                                                  |
| Offset: 0x20 |                  | Interrupt Mask and PLL Lock Status Register |        |                                                       |
|              |                  |                                             |        |                                                       |
| Bit          | Bit Name         | Default                                     | Access | Bit Description                                       |
| 3            | INT_EN_PLLB_LOCK | 0x00                                        | R/W    | interrupt on PLLB lock enable (R/W)                   |
| 2            | INT_EN_PLLA_LOCK | 0x00                                        | R/W    | interrupt on PLLA lock enable (R/W)                   |
| 1            | PLLB_LOCK        | 0x00                                        | R      | PLLB lock status, locked if SET (not cleared on read) |
| 0            | PLLA_LOCK        |                                             | R      | PLLA lock status, locked if SET (not cleared on read) |

Table 30 Interrupt Clear Register

| Name         |           | Base                     |        | Default                                               |
|--------------|-----------|--------------------------|--------|-------------------------------------------------------|
| CGU_IRQ      |           | AS3525_CGU_BASE          |        | 0x00                                                  |
| Offset: 0x24 |           | Interrupt Clear Register |        |                                                       |
|              |           |                          |        |                                                       |
| Bit          | Bit Name  | Default                  | Access | Bit Description                                       |
| 1            | PLLB_LOCK | 0x00                     | R      | PLLB lock status, locked if SET (not cleared on read) |
| 0            | PLLA_LOCK | 0x00                     | R      | PLLA lock status, locked if SET (not cleared on read) |

Table 31 PLL A Lock Counter Register

| Name         |             | Base                        |        | Default                                                        |
|--------------|-------------|-----------------------------|--------|----------------------------------------------------------------|
| CGU_COUNTA   |             | AS3525_CGU_BASE             |        | 0x20                                                           |
| Offset: 0x28 |             | PLL A Lock Counter Register |        |                                                                |
|              |             |                             |        |                                                                |
| Bit          | Bit Name    | Default                     | Access | Bit Description                                                |
| 7:0          | COUNTA[7:0] | 0x00                        | R/W    | number of PLL A's four-clock cycles until the LOCKA bit is set |

Table 32 PLL B Lock Counter Register

| Name         |             | Base                        |        | Default                                                        |
|--------------|-------------|-----------------------------|--------|----------------------------------------------------------------|
| CGU_COUNTB   |             | AS3525_CGU_BASE             |        | 0x20                                                           |
| Offset: 0x2c |             | PLL B Lock Counter Register |        |                                                                |
|              |             |                             |        |                                                                |
| Bit          | Bit Name    | Default                     | Access | Bit Description                                                |
| 7:0          | COUNTB[7:0] | 0x00                        | R/W    | number of PLL B's four-clock cycles until the LOCKB bit is set |

Table 33 IDE Clock Controller Register

| Name         |                   | Base                                                   |        | Default                                                                                                |
|--------------|-------------------|--------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------|
| CGU_IDE      |                   | AS3525_CGU_BASE                                        |        | 0x20                                                                                                   |
| Offset: 0x30 |                   | IDE Clock Controller Register                          |        |                                                                                                        |
|              |                   | This register allows setting the IDE interface clocks. |        |                                                                                                        |
| Bit          | Bit Name          | Default                                                | Access | Bit Description                                                                                        |
| 7            | IDEIF_CLK_EN      | 0                                                      | R/W    | IDE AHB IF clock enable                                                                                |
| 6            | IDE_CLK_EN        | 0                                                      | R/W    | IDE IF clock enable (90MHz domain) => clk_ide                                                          |
| 5:2          | IDE_DIV_SEL [2:0] | 0x0                                                    | R/W    | division ratio => div = 1/(ide_div_sel + 1)                                                            |
| 1:0          | IDE_SEL[1:0]      | 0x0                                                    | R/W    | clk_in select (clk_ide)<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main) |

Note:  $f(\text{clk\_ide}) := f(\text{clk\_in}) * \text{div}$ ;

Table 34 Memory Stick (MS) Clock Controller Register

| Name         |                  | Base                                                  |        | Default                                                                                               |
|--------------|------------------|-------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------|
| CGU_MS       |                  | AS3525_CGU_BASE                                       |        | 0x00                                                                                                  |
| Offset: 0x34 |                  | MS Clock Controller Register                          |        |                                                                                                       |
|              |                  | This register allows setting the MS interface clocks. |        |                                                                                                       |
| Bit          | Bit Name         | Default                                               | Access | Bit Description                                                                                       |
| 8            | MSIF_CLK_EN      | 0                                                     | R/W    | MS APB IF clock enable                                                                                |
| 7            | MS_CLK_EN        | 0                                                     | R/W    | MS IF clock enable (20/40MHz domain) => clk_ms                                                        |
| 6:2          | MS_DIV_SEL [2:0] | 0x0                                                   | R/W    | division ratio => div = 1/(ms_div_sel + 1)                                                            |
| 1:0          | MS_SEL[1:0]      | 0x0                                                   | R/W    | clk_in select (clk_ms)<br>00: clk_main<br>01: pll_a_fout<br>10: pll_b_fout<br>11: reserved (clk_main) |

Note:  $f(\text{clk\_ms}) = f(\text{clk\_in}) * \text{div}$ ;

Table 35 Data Block Output Port (DBOP) Clock Controller Register

| Name         |                       | Base                                                    |        | Default                                         |
|--------------|-----------------------|---------------------------------------------------------|--------|-------------------------------------------------|
| CGU_DBOP     |                       | AS3525_CGU_BASE                                         |        | 0x00                                            |
| Offset: 0x38 |                       | DBOP Clock Controller Register                          |        |                                                 |
|              |                       | This register allows setting the DBOP interface clocks. |        |                                                 |
| Bit          | Bit Name              | Default                                                 | Access | Bit Description                                 |
| 3            | DBOP_EN               | 0                                                       | R/W    | DBOP APB IF clock enable                        |
| 2:0          | DBOP_PREDIV_SEL [2:0] | 0x0                                                     | R/W    | division ratio => div = 1/(dbop_prediv_sel + 1) |

Note: Setting DBOP\_EN will enable both clocks (push/APB and pop) immediately.  
clk\_dbop clock (pop clock) generation uses DBOP APB IF clock as input clock.

$f(\text{clk\_dbop}) = f(\text{PCLKDBOP}) * \text{div}$ ;

Figure 43 Table with verified CGU frequency settings for Audio and USB applications with 24MHz crystal

| PLL_F             | PLL_R | PLL_OD | fref [MHz] | fvco [MHz] | plla_fout [MHz] | fclk_pre | fclk_post | fclk [MHz] | pclk_div0 | pclk_div1 | pclk [MHz] | mclk_div | mclk [Hz] | fsaudio [Hz] | faudio error [%] | usb_div | fusbphy [Hz] | fusb error [%] | fsaudio target [Hz] | CPU clock mode |
|-------------------|-------|--------|------------|------------|-----------------|----------|-----------|------------|-----------|-----------|------------|----------|-----------|--------------|------------------|---------|--------------|----------------|---------------------|----------------|
| Target: 48.000 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0,00     | 5,00      | 64,000     | 0         | 0         | 64,000     | 61       | 6.193.548 | 48.387       | 0,806            | 3       | 48.000.000   | 0,000          | 48000               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0,00     | 1,00      | 48,000     | 0         | 0         | 48,000     | 15       | 6.000.000 | 46.875       | -2,344           | 1       | 48.000.000   | 0,000          | 48000               | fastbus        |
| 41                | 8     | 2      | 3,000      | 246,000    | 123,000         | 0,00     | 1,00      | 61,500     | 0         | 0         | 61,500     | 19       | 6.150.000 | 48.047       | 0,098            |         |              |                | 48000               | fastbus        |
| 23                | 5     | 3      | 4,800      | 220,800    | 55,200          | 0,00     | 0,00      | 55,200     | 0         | 0         | 55,200     | 8        | 6.133.333 | 47.917       | -0,174           |         |              |                | 48000               | fastbus        |
| Target: 44.100 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 67       | 5.647.059 | 44.118       | 0,040            | 3       | 48.000.000   | 0,000          | 44100               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 16       | 5.647.059 | 44.118       | 0,040            | 1       | 48.000.000   | 0,000          | 44100               | fastbus        |
| 47                | 10    | 2      | 2,400      | 225,600    | 112,800         | 0        | 1         | 56,400     | 0         | 0         | 56,400     | 19       | 5.640.000 | 44.063       | -0,085           |         |              |                | 44100               | fastbus        |
| 79                | 12    | 3      | 2,000      | 316,000    | 79,000          | 0        | 1         | 39,500     | 0         | 0         | 39,500     | 13       | 5.642.857 | 44.085       | -0,034           |         |              |                | 44100               | fastbus        |
| 47                | 10    | 3      | 2,400      | 225,600    | 56,400          | 0        | 1         | 28,200     | 0         | 0         | 28,200     | 9        | 5.640.000 | 44.063       | -0,085           |         |              |                | 44100               | fastbus        |
| Target: 32.000 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 93       | 4.085.106 | 31.915       | -0,266           | 3       | 48.000.000   | 0,000          | 32000               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 22       | 4.173.913 | 32.609       | 1,902            | 1       | 48.000.000   | 0,000          | 32000               | fastbus        |
| 41                | 6     | 3      | 4,000      | 328,000    | 82,000          | 0        | 1         | 41,000     | 0         | 0         | 41,000     | 19       | 4.100.000 | 32.031       | 0,098            |         |              |                | 32000               | fastbus        |
| 31                | 7     | 3      | 3,429      | 212,571    | 53,143          | 0        | 1         | 26,571     | 0         | 0         | 26,571     | 12       | 4.087.912 | 31.937       | -0,197           |         |              |                | 32000               | fastbus        |
| Target: 24.000 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 124      | 3.072.000 | 24.000       | 0,000            | 3       | 48.000.000   | 0,000          | 24000               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 30       | 3.096.774 | 24.194       | 0,806            | 1       | 48.000.000   | 0,000          | 24000               | fastbus        |
| 41                | 8     | 2      | 3,000      | 246,000    | 123,000         | 0        | 1         | 61,500     | 0         | 0         | 61,500     | 39       | 3.075.000 | 24.023       | 0,098            |         |              |                | 24000               | fastbus        |
| Target: 22.050 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 135      | 2.823.529 | 22.059       | 0,040            | 3       | 48.000.000   | 0,000          | 22050               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 33       | 2.823.529 | 22.059       | 0,040            | 1       | 48.000.000   | 0,000          | 22050               | fastbus        |
| 47                | 10    | 2      | 2,400      | 225,600    | 112,800         | 0        | 1         | 56,400     | 0         | 0         | 56,400     | 39       | 2.820.000 | 22.031       | -0,085           |         |              |                | 22050               | fastbus        |
| Target: 16.000 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 187      | 2.042.553 | 15.957       | -0,266           | 3       | 48.000.000   | 0,000          | 16000               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 46       | 2.042.553 | 15.957       | -0,266           | 1       | 48.000.000   | 0,000          | 16000               | fastbus        |
| 41                | 6     | 3      | 4,000      | 328,000    | 82,000          | 0        | 1         | 41,000     | 0         | 0         | 41,000     | 39       | 2.050.000 | 16.016       | 0,098            |         |              |                | 16000               | fastbus        |
| Target: 12.000 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 249      | 1.536.000 | 12.000       | 0,000            | 3       | 48.000.000   | 0,000          | 12000               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 62       | 1.523.810 | 11.905       | -0,794           | 1       | 48.000.000   | 0,000          | 12000               | fastbus        |
| 41                | 6     | 3      | 4,000      | 328,000    | 82,000          | 0        | 1         | 41,000     | 0         | 0         | 41,000     | 52       | 1.547.170 | 12.087       | 0,727            |         |              |                | 12000               | fastbus        |
| Target: 11.025 Hz |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 271      | 1.411.765 | 11.029       | 0,040            | 3       | 48.000.000   | 0,000          | 11025               | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 67       | 1.411.765 | 11.029       | 0,040            | 1       | 48.000.000   | 0,000          | 11025               | fastbus        |
| 41                | 6     | 3      | 4,000      | 328,000    | 82,000          | 0        | 1         | 41,000     | 0         | 0         | 41,000     | 57       | 1.413.793 | 11.045       | 0,184            |         |              |                | 11025               | fastbus        |
| Target: 8.000 Hz  |       |        |            |            |                 |          |           |            |           |           |            |          |           |              |                  |         |              |                |                     |                |
| 48                | 6     | 1      | 4,000      | 384,000    | 384,000         | 0        | 5         | 64,000     | 0         | 0         | 64,000     | 374      | 1.024.000 | 8.000        | 0,000            | 3       | 48.000.000   | 0,000          | 8000                | fastbus        |
| 24                | 3     | 3      | 8,000      | 384,000    | 96,000          | 0        | 1         | 48,000     | 0         | 0         | 48,000     | 93       | 1.021.277 | 7.979        | -0,266           | 1       | 48.000.000   | 0,000          | 8000                | fastbus        |
| 41                | 6     | 3      | 4,000      | 328,000    | 82,000          | 0        | 1         | 41,000     | 0         | 0         | 41,000     | 79       | 1.025.000 | 8.008        | 0,098            |         |              |                | 8000                | fastbus        |

### 7.3.15 CCU - Chip Control Unit

Following chapters describe the functions of the CCU.

Table 88 CCU Registers

| Register Name | Base Address    | Offset | Note                              |
|---------------|-----------------|--------|-----------------------------------|
| CCU_SRC       | AS3525_CCU_BASE | 0x0000 | Software reset control register   |
| CCU_SRL       | AS3525_CCU_BASE | 0x0004 | Software reset lock register      |
| CCU_MEMMAP    | AS3525_CCU_BASE | 0x0008 | Memory map register               |
| CCU_IO        | AS3525_CCU_BASE | 0x000C | IO configuration register         |
| CCU_SCON      | AS3525_CCU_BASE | 0x0010 | System configuration register     |
| CCU_VERS      | AS3525_CCU_BASE | 0x0014 | Chip version register             |
| CCU_SPARE1    | AS3525_CCU_BASE | 0x0018 | spare register 1 (for future use) |
| CCU_SPARE2    | AS3525_CCU_BASE | 0x001C | spare register 2 (for future use) |

#### 7.3.15.1 Reset Controller

- Generation of the internal reset: the external reset pin XRES is used to generate the internal global reset. This internal reset is synchronised to clk\_main and the active reset time is enlarged. This is necessary to wait for the startup of the DC/DC converter and LDO's that are generating the supplies of the digital chip. The time assumed for this startup is 10 ms, therefore 2<sup>18</sup> cycles of clk\_main are counted before the internal reset is released. This mechanism is also used for the WATCHDOG reset.
- Softreset: for each module, the reset can also be generated by SW control. For this purpose, the SW can write to the software reset control register (CCU\_SRC). To avoid unintended SW resets, the access to this control register is locked by the SW reset lock register (CCU\_SRL). So the correct usage is:
  - write CCU\_SRC
  - write CCU\_SRL (magic number 0x1A720212) to CCU\_LOCK to activate resets
  - write CCU\_SRL (0x00000000) to deactivate resets

Table 89 Software Reset Control Register

| Name            |            | Base                                                                                           |        | Default                                                                                                     |
|-----------------|------------|------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------|
| CCU_SRC         |            | AS3525_CCU_BASE                                                                                |        | 0x00                                                                                                        |
| Offset: 0x0000h |            | Software Reset Control Register                                                                |        |                                                                                                             |
|                 |            | Writing a logic 1 to the single bits in the read/write register enables resets to each module. |        |                                                                                                             |
| Bit             | Bit Name   | Default                                                                                        | Access | Bit Description                                                                                             |
| 24              | DBOP_EN    | 0                                                                                              | R/W    | 1: enable DBOP reset<br>0: disable DBOP reset                                                               |
| 23              | MBIST_EN   | 0                                                                                              | R/W    | 1: enable MBIST manager reset<br>0: disable MBIST manager reset                                             |
| 22              | SPDIF_EN   | 0                                                                                              | R/W    | 1: enable SPDIF reset<br>0: disable SPDIF reset                                                             |
| 21              | TIMER_EN   | 0                                                                                              | R/W    | 1: enable timer module reset<br>0: disable timer module reset                                               |
| 20              | SSP_EN     | 0                                                                                              | R/W    | 1: enable synchronous serial port reset<br>0: disable synchronous serial port reset                         |
| 19              | WDO_EN     | 0                                                                                              | R/W    | 1: enable watchdog timer module reset<br>0: disable watchdog timer module reset                             |
| 18              | IDE_EN     | 0                                                                                              | R/W    | 1: enable compact flash/IDE reset (except AHB part)<br>0: disable compact flash/IDE reset (except AHB part) |
| 17              | IDE_AHB_EN | 0                                                                                              | R/W    | 1: enable compact flash/IDE's AHB interface reset<br>0: disable compact flash/IDE's AHB interface reset     |

| Name            |              | Base                                                                                           |        | Default                                                                                                     |
|-----------------|--------------|------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------|
| CCU_SRC         |              | AS3525_CCU_BASE                                                                                |        | 0x00                                                                                                        |
| Offset: 0x0000h |              | Software Reset Control Register                                                                |        |                                                                                                             |
|                 |              | Writing a logic 1 to the single bits in the read/write register enables resets to each module. |        |                                                                                                             |
| Bit             | Bit Name     | Default                                                                                        | Access | Bit Description                                                                                             |
| 16              | UART_EN      | 0                                                                                              | R/W    | 1: enable UART interface reset<br>0: disable UART interface reset                                           |
| 15              | NAF_EN       | 0                                                                                              | R/W    | 1: enable NAND flash/Smart Media interface reset<br>0: disable NAND flash/Smart Media interface reset       |
| 14              | SDMCI_EN     | 0                                                                                              | R/W    | 1: enable secure digital/multimedia interface reset<br>0: disable secure digital/multimedia interface reset |
| 13              | GPIO_EN      | 0                                                                                              | R/W    | 1: enable general purpose IO reset<br>0: disable general purpose IO reset                                   |
| 12              | I2C_AUDIO_EN | 0                                                                                              | R/W    | 1: enable audio I2C interface reset<br>0: disable audio I2C interface reset                                 |
| 11              | I2C_EN       | 0                                                                                              | R/W    | 1: enable master/slave I2C interface reset<br>0: disable master/slave I2C interface reset                   |
| 10              | MMS_EN       | 0                                                                                              | R/W    | 1: enable memory stick interface reset<br>0: disable memory stick interface reset                           |
| 9               | I2SI_APB_EN  | 0                                                                                              | R/W    | 1: enable I2S input interface reset for APB part<br>0: disable I2S input interface reset for APB part       |
| 8               | I2SO_APB_EN  | 0                                                                                              | R/W    | 1: enable I2S output interface reset for APB part<br>0: disable I2S output interface reset for APB part     |
| 7               | USB_AHB_EN   | 0                                                                                              | R/W    | 1: enable USB AHB reset<br>0: disable USB AHB reset                                                         |
| 6               | USB_PHY_EN   | 0                                                                                              | R/W    | 1: enable USB PHY reset<br>0: disable USB PHY reset                                                         |
| 5               | DMAC_EN      | 0                                                                                              | R/W    | 1: enable DMA controller reset<br>0: disable DMA controller reset                                           |
| 4               | VIC_EN       | 0                                                                                              | R/W    | 1: enable vectored interrupt cell reset<br>0: disable vectored interrupt cell reset                         |
| 3               | RAMC_EN      | 0                                                                                              | R/W    | 1: enable RAMC reset<br>0: disable RAMC reset                                                               |
| 2               | 1TRAM_EN     | 0                                                                                              | R/W    | 1: enable 1TRAM reset<br>0: disable 1TRAM reset                                                             |
| 1               | MPMC_EN      | 0                                                                                              | R/W    | 1: enable external memory AHB reset<br>0: disable external memory AHB reset                                 |
| 0               | BRIDGE_EN    | 0                                                                                              | R/W    | 1: enable bridge reset<br>0: disable bridge reset                                                           |

Table 90 Software Reset Lock Register

| Name            |                     | Base                                                                                                                                                                                                                 |        | Default                                                       |
|-----------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------|
| CCU_SRL         |                     | AS3525_CCU_BASE                                                                                                                                                                                                      |        | 0x00                                                          |
| Offset: 0x0004h |                     | Software Reset Lock Register                                                                                                                                                                                         |        |                                                               |
|                 |                     | Use of this register enables the software reset selected with Software Reset Control Register. Writing a value of 0x1A720212 will enable the selected reset; writing any other value will not enable software reset. |        |                                                               |
| Bit             | Bit Name            | Default                                                                                                                                                                                                              | Access | Bit Description                                               |
| 0:31            | software_reset_lock | 0                                                                                                                                                                                                                    | R/W    | 0x1A720212: enables selected reset<br>Other values: no effect |

### 7.3.15.2 IO\_PADRING functions

Within the IO\_PADRING module all multiplexing for selecting alternative functions is implemented. The selection of active functions is chosen within the IO\_configuration\_register. Following table gives a description of the IO configurations:

Table 91 IO\_PADRING Configurations

| Name            |                   | Base                                                                                                              |        | Default                                                                                                                                                                              |
|-----------------|-------------------|-------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CCU_IO          |                   | AS3525_CCU_BASE                                                                                                   |        | 0x00                                                                                                                                                                                 |
| Offset: 0x000Ch |                   | IO Configuration Registers                                                                                        |        |                                                                                                                                                                                      |
|                 |                   | With this read/write registers the functionality of IOs are controlled which provides several different functions |        |                                                                                                                                                                                      |
| Bit             | Bit Name          | Default                                                                                                           | Access | Bit Description                                                                                                                                                                      |
| 8:7             | naf_ce_sel[1:0]   | 0                                                                                                                 | R/W    | these bits select which output is used for NAF ce_n.<br>0: naf_ce0_n<br>1: naf_ce1_n<br>2: naf_ce2_n<br>3: naf_ce3_n                                                                 |
| 6               | pll_probe_en      | 0                                                                                                                 | R/W    | test mode:<br>1: pll output clock is available at a GPIO Pin                                                                                                                         |
| 5               | ide_sel           | 0                                                                                                                 | R/W    | 1: the IDE input/output configuration is set                                                                                                                                         |
| 4               | spi_flash_mode    | 0                                                                                                                 | R/W    | SPI used in master mode:<br>1: pin SSP_FSSOUT always 0<br>0: pin SSP_FSSOUT generated by SSP hardware block<br>SPI used in slave mode:<br>spi_flash_mode has to be switched to 0     |
| 3:2             | xpd_func_sel(1:0) | 0                                                                                                                 | R/W    | 00: XPD works as general purpose IO<br>01: SD-MCI interface<br>10: the XPD[5:0] are configured to support MS, XPD[7:6] are general IO pins<br>11: reserved (XPD works as general IO) |
| 1               | i2c_ms_sel        | 0                                                                                                                 | R/W    | 1: the I2C master/slave IO configuration is set                                                                                                                                      |
| 0               | uart_sel          | 0                                                                                                                 | R/W    | 1: the uart IO configuration is set                                                                                                                                                  |

### 7.3.15.3 Other CCU functions

With the CCU\_MEMMAP register, the remap(r/w) and int\_boot\_sel (read only) bits are accessible.

Table 92 Memory Map Register

| Name            |              | Base                                                                            |        | Default                                                           |
|-----------------|--------------|---------------------------------------------------------------------------------|--------|-------------------------------------------------------------------|
| CCU_MEMMAP      |              | AS3525_CCU_BASE                                                                 |        | N/A                                                               |
| Offset: 0x0008h |              | Memory Map Register                                                             |        |                                                                   |
|                 |              | With the register the remap(r/w) and int_boot_sel (r only) bits are accessible. |        |                                                                   |
| Bit             | Bit Name     | Default                                                                         | Access | Bit Description                                                   |
| 1               | INT_BOOT_SEL | external pin XPC[0]                                                             | R      | Boot selection<br>1: internal ROM<br>0: external memory interface |
| 0               | REMAP        | 0                                                                               | R/W    | Defines memory mapping<br>1: RAM<br>0: ROM                        |

If the INIT\_BOOT\_SEL is 0 (boot from external memory interface), following pins will be latched at startup to define the MPMC interface settings:

|                   |                   |
|-------------------|-------------------|
| • mpmc_stcs1mw[0] | • mpmc_stcs1pb    |
| • mpmc_stcs1pol   | • mpmc_rel1config |

## 7.3.15.4 Additional Chip Control Unit Registers

Table 93 System Configuration Register

| Name            |                 | Base                                                 |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------|-----------------|------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CCU_SCON        |                 | AS3525_CCU_BASE                                      |        | 0x00                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Offset: 0x0010h |                 | System Configuration Register                        |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                 |                 | This read/write register controls system parameters. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Bit             | Bit Name        | Default                                              | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 0               | priority_config | 0                                                    | R/W    | AHB master's priority configuration:<br>0: Configuration A (default)<br>Highest priority: TIC (Test Interface Controller) – for production test only<br>2 <sup>nd</sup> highest priority: ARM922T<br>3 <sup>rd</sup> highest priority: DMA<br>4 <sup>th</sup> highest priority: USB<br>lowest priority: IDE<br>1: Configuration B<br>Highest priority: TIC (Test Interface Controller) – for production test only<br>2 <sup>nd</sup> highest priority: DMA<br>3 <sup>rd</sup> highest priority: USB<br>4 <sup>th</sup> highest priority: IDE<br>lowest priority: ARM922T |

Table 94 Chip Version Register

| Name            |                       | Base                                                |        | Default         |
|-----------------|-----------------------|-----------------------------------------------------|--------|-----------------|
| CCU_VERS        |                       | AS3525_CCU_BASE                                     |        | 0x09            |
| Offset: 0x0014h |                       | Chip Version Register                               |        |                 |
|                 |                       | Version information can be read from this register. |        |                 |
| Bit             | Bit Name              | Default                                             | Access | Bit Description |
| 31:12           | main_version_id(19:0) | 0x2                                                 | R      | main version ID |
| 11:0            | sub_version_id(11:0)  | 0x1                                                 | R      | sub version ID  |

Table 95 Spare Register 1

| Name            |                     | Base                                                                   |        | Default                                                      |
|-----------------|---------------------|------------------------------------------------------------------------|--------|--------------------------------------------------------------|
| CCU_SPARE1      |                     | AS3525_CCU_BASE                                                        |        | 0x00                                                         |
| Offset: 0x0018h |                     | Metal ECO Spare Register                                               |        |                                                              |
|                 |                     | This register implements 32bit spare FF's. Use for metal ECO redesign. |        |                                                              |
| Bit             | Bit Name            | Default                                                                | Access | Bit Description                                              |
| 31:9            | spare               | 0x00                                                                   | R/W    | spare bits to be used for metal ECO redesign if SET          |
| 8               | dma_sreq_SSPRX_off  | 0x00                                                                   | R/W    | disableDMA single request of SSPRX module if SET             |
| 7               | dma_sreq_SSPTX_off  | 0x00                                                                   | R/W    | disable DMA single request of SSPTX module if SET            |
| 6               | dma_sreq_DBOP_off   | 0x00                                                                   | R/W    | disable DMA single request of DBOP module if SET             |
| 5               | dma_sreq_I2Sin_off  | 0x00                                                                   | R/W    | disable DMA single request of I2Sin module if SET            |
| 4               | dma_sreq_I2Sout_off | 0x00                                                                   | R/W    | disable DMA single request of I2Sout module if SET           |
| 3:2             | spare               | 0x00                                                                   | R/W    | spare bits to be used for metal ECO redesign if SET          |
| 1:0             | mpmc_clk_inv        | 0x00                                                                   | R/W    | spare bits used to invert output clocks mpmc_clk(1:0) if SET |

Table 96 Spare Register 2

| Name            |                      | Base                                                                   |        | Default                                                                                                                                                                                    |
|-----------------|----------------------|------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CCU_SPARE2      |                      | AS3525_CCU_BASE                                                        |        | 0x00                                                                                                                                                                                       |
| Offset: 0x001Ch |                      | Metal ECO Spare Register                                               |        |                                                                                                                                                                                            |
|                 |                      | This register implements 32bit spare FF's. Use for metal ECO redesign. |        |                                                                                                                                                                                            |
| Bit             | Bit Name             | Default                                                                | Access | Bit Description                                                                                                                                                                            |
| 31:3            | spare                | 0x00                                                                   | R/W    | spare bits to be used for metal ECO redesign if SET                                                                                                                                        |
| 2:0             | bist_idle_cycle_ctrl | 0x00                                                                   | R/W    | internal RAM refresh cycle control bits of BIST_MGR module<br>000: idle every 32nd cycle (default)<br>100: idle every 16th cycle<br>110: idle every 8th cycle<br>111: idle every 4th cycle |

## 7.4 Audio and Power Management functions

### 7.4.1 SYSTEM

#### 7.4.1.1 General

The system block handles the power up, power down and regulator voltage settings of the AFE.

#### 7.4.1.2 Power Up

The chip powers up when on of the following condition is true:

- High signal on the PWR\_UP pin (>80ms, >1V & >1/3 BVDD)
- Input voltage on the UVDD pin (USB plug in: >80ms, BVDD>1.5V, UVDD>4.5V)
- Input voltage on the CHG\_IN pin (charger plug in: >80ms, BVDD>1.5V, CHG\_IN>4.0V)
- Input voltage on BVDD pin (battery change: >1.35V)

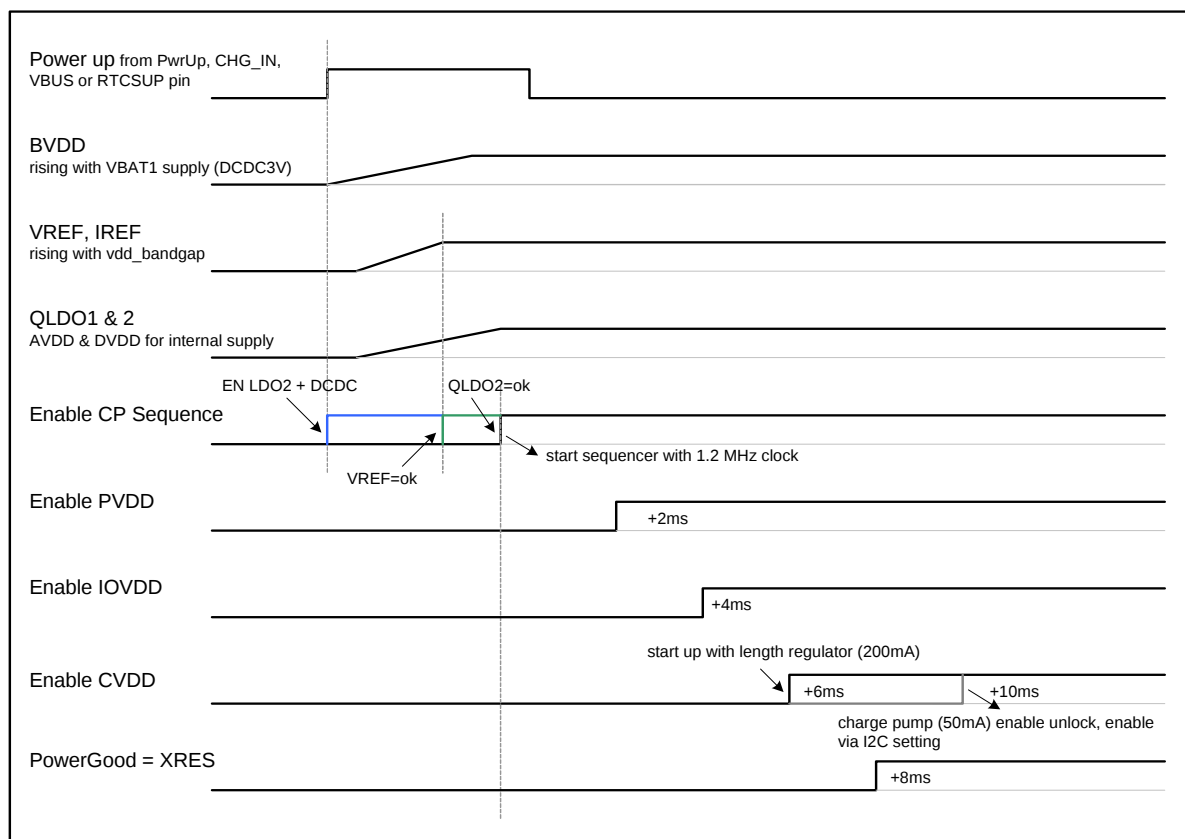
To hold the chip in power up mode the PwrUpHld bit in the SYSTEM register (0x20h) is set.

#### 7.4.1.3 Power Down

The chip automatically shuts off if one of the following conditions arises:

1. Clearing the PwrUpHld bit in SYSTEM register (0x20h)
2. I2C watchdog power down if enabled (no serial reading for >1s, has to be enabled)
3. BVDD drops below the minimum threshold voltage (<2.7V)
4. Junction temperature reaches maximum threshold, set in SUPERVISOR register (0x24h)
5. High signal on the PWR\_UP pin for more than (>6s, >1V & >1/3 BVDD).

Figure 44 Power Up Timing



## 7.4.1.4 Parameter

Table 97 Supply Regulator Block Characteristics

| Symbol               | Parameter       | Notes | Min | Typ  | Max | Unit |
|----------------------|-----------------|-------|-----|------|-----|------|
|                      | DVDD_POR_OFF    |       |     | 2.15 |     | V    |
|                      | DVDD_POR_ON     |       |     | 2.0  |     | V    |
|                      | POR_ON/OFF_HYST |       |     | 100  |     | mV   |
| <b>LRCK WATCHDOG</b> |                 |       |     |      |     |      |
|                      | F(LRCK)_WD_OFF  |       |     | 4.1  | 8   | kHz  |
|                      | ON_Delay        |       |     | 50   |     | us   |

DVDD=2.9V; T<sub>amb</sub>=25°C; unless otherwise specified

## 7.4.1.5 Register Description

Table 98 System Register

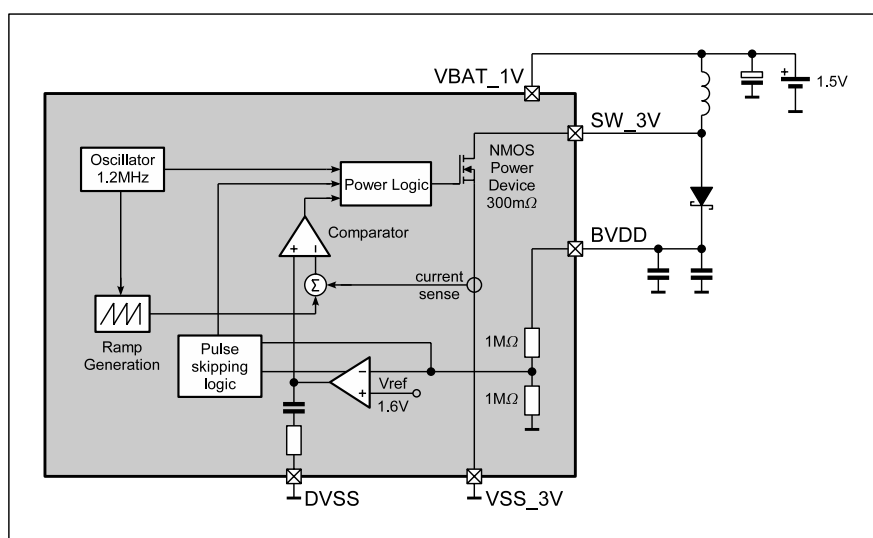
| Name         |               | Base                                  |        | Default                                                                                                                                              |
|--------------|---------------|---------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| System       |               | I2C audio master                      |        | 0x21                                                                                                                                                 |
| Offset: 0x20 |               | System Settings Register              |        |                                                                                                                                                      |
|              |               | This register is reset at a DVDD-POR. |        |                                                                                                                                                      |
| Bit          | Bit Name      | Default                               | Access | Bit Description                                                                                                                                      |
| 7:4          | Version <3:0> | 0010                                  | R      | AFE number to identify the design version<br><b>0010: revision 2</b>                                                                                 |
| 3            | PVDDp         | 0                                     | R/W    | PVDD trimming:<br><b>0: Vnom</b><br>1: Vnom *17/18                                                                                                   |
| 2            | IOVDDp        | 0                                     | R/W    | IOVDD trimming:<br><b>0: IOVDD = 3.11V (nominal)</b><br>1: IOVDD = 2.94V                                                                             |
| 1            | EnWDogPwn     | 0                                     | R/W    | <b>0: forced power down through watchdog is disabled</b><br>1: forced power down through watchdog is enabled (no serial interface reading within 1s) |
| 0            | PwrUpHld      | 1                                     | R/W    | 0: power up hold is cleared and supply is switched off<br><b>1: set to on after power on</b>                                                         |

## 7.4.2 3V Step-Up Converter

### 7.4.2.1 General

- Output voltage 3V to 3.6V (BVDD) programmable in 4 steps via DCDC3p bit to save power
- Input voltage 1V (1.2V) to 3V, voltages higher than that can be connected to BVDD directly
- Maximum output current to BVDD: 150mA
- Current mode operation
- On-chip compensation and feedback network
- On chip 300mΩ NMOS switch
- PWM mode with 1.2MHz switching frequency
- Inductor current limitation 850mA
- Pulse skipping capability
- Low quiescent current: 40μA in PFM-mode, 300μA in PWM mode
- ≤1μA shutdown current
- uses external coil (6.8μH) and Schottky diode (500mA)

Figure 45 DCDC 3V Block Diagram



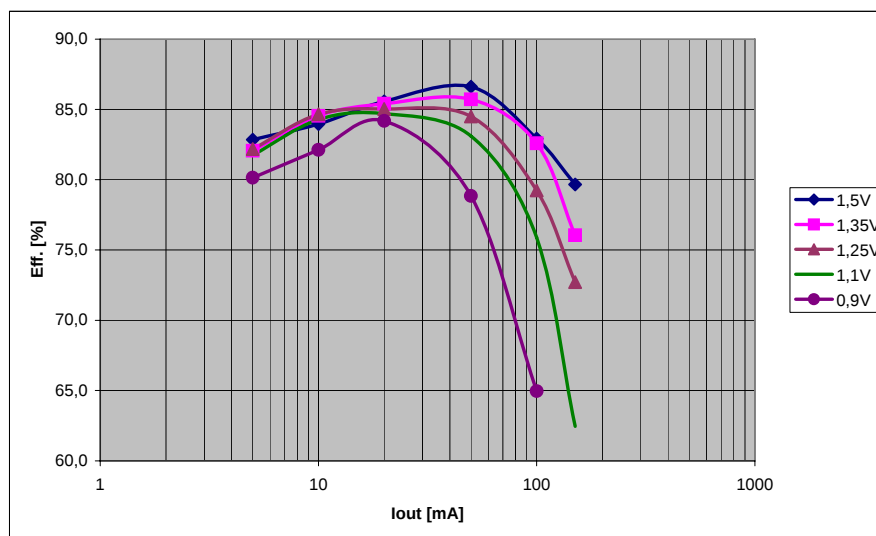
### 7.4.2.2 Parameter

Table 99 DCDC Boost Parameter

| Symbol               | Parameter                          | Notes                                              | Min  | Typ  | Max  | Unit |
|----------------------|------------------------------------|----------------------------------------------------|------|------|------|------|
| I <sub>VDD2.9</sub>  | Supply Current                     | Power down mode                                    |      |      | 5    | μA   |
|                      |                                    | PFM mode operation                                 |      | 40   |      | μA   |
|                      |                                    | PWM mode (low output load)                         |      | 300  |      | μA   |
| V <sub>STARTUP</sub> | Startup Voltage                    | R <sub>Load</sub> >220Ω                            | 1.0  |      |      | V    |
| V <sub>HOLD</sub>    | Hold-on Voltage                    | I <sub>OUT</sub> =1mA, VBAT falling from 1.5 to 0V |      | 0.5  |      | V    |
| R <sub>SW_on</sub>   | Internal Switch R <sub>DS_ON</sub> |                                                    |      |      | 300  | mΩ   |
| f <sub>SW</sub>      | Switching Frequency                | Start-up, X3VOK=1                                  | 100  | 250  | 500  | kHz  |
|                      |                                    | PWM mode operation, X3VOK=0                        |      | 1.2  |      | MHz  |
| t <sub>ON_min</sub>  | Minimum On-time                    |                                                    |      | 100  |      | ns   |
| t <sub>OFF_min</sub> | Minimum Off-time                   |                                                    |      | 100  |      | ns   |
| η <sub>eff</sub>     | Efficiency                         | I <sub>OUT</sub> =20mA, Vin=1.35                   |      | 85   |      | %    |
|                      |                                    | I <sub>OUT</sub> =50mA, Vin=1.5                    |      | 87   |      | %    |
| I <sub>SW_LIM</sub>  | Current Limit                      | 1.0V ≤ VB1V ≤ 3.0V                                 | 0.60 | 0.85 | 1.10 | A    |
| I <sub>OUT</sub>     | Load Current                       | VB1V=1.0V                                          |      |      | 150  | mA   |

Vin=1.0..2.0V, C(VBAT\_1V) = 2.2μF ceramic || 2000μF Elko, C(BVDD) = 3 x 2.2μF ceramic, L=DS1608 6.8μH, Temp = 25deg

Figure 46 DCDC Boost Typical Performance Characteristics



BVDD=3.1V, L=DS1608 6.8μH, Temp = 25deg

### 7.4.2.3 Register Description

Table 100 CVDD / DCDC3 Register

| Name          |            | Base                                  |        | Default                                                                                                                                                                                                             |
|---------------|------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CVDD / DCDC 3 |            | I2C audio master                      |        | 0x00                                                                                                                                                                                                                |
| Offset: 0x21  |            | Charge Pump and 3V DCDC Register      |        |                                                                                                                                                                                                                     |
|               |            | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                     |
| Bit           | Bit Name   | Default                               | Access | Bit Description                                                                                                                                                                                                     |
| 7             | CP_SW      | 0                                     | R/W    | charge pump / length regulator switch margin reduction<br><b>0: margin set to 200/300 mV</b><br>1: margin reduced to 150/225 mV (automatic switching to length regulator is done “later”, at a lower input voltage) |
| 6             | CP_on      | 0                                     | R/W    | <b>0: normal operation</b><br>1: keeps Mode 3 charge pump always on<br>Please note that bit 2 = “0”, overrides bit 6.                                                                                               |
| 5             | LREG_CPnot | 0                                     | R      | Core voltage generation mode<br><b>0: CP is working</b><br>1: LREG is working                                                                                                                                       |
|               |            |                                       | W      | For production testing purpose only, in normal application mode this bit must always be written with “0”.                                                                                                           |
| 4:3           | DCDC3p     | 00                                    | R/W    | DCDC3 Vout programming (BVDD)<br><b>00: 3.6V</b><br>01: 3.2V<br>10: 3.1V<br>11: 3.0V                                                                                                                                |
| 2             | LREG_off   | 0                                     | R/W    | <b>0: keeps Mode2 (length regulator always on)</b><br>1: normal operation                                                                                                                                           |
| 1:0           | CVDDp      | 00                                    | R/W    | CVDD trimming:<br><b>00: 1.2V</b><br>01: 1.15V<br>10: 1.10V<br>11: 1.05V                                                                                                                                            |

## 7.4.3 Low Drop Out Regulators

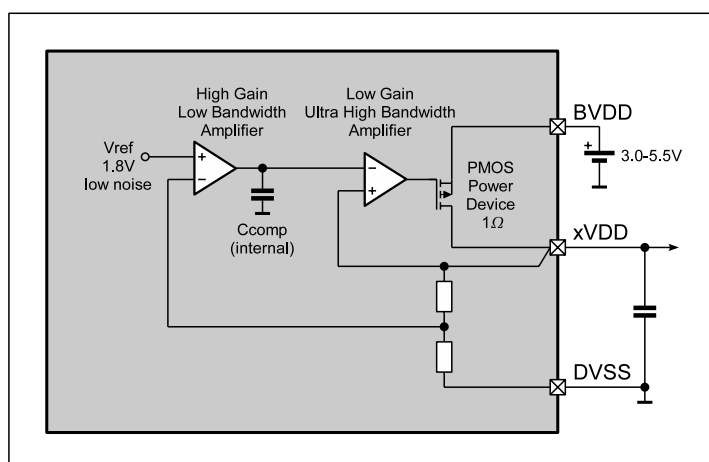
### 7.4.3.1 General

These LDO's are designed to supply sensitive analogue circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices.

The design is optimised to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of  $1\mu\text{F} \pm 20\%$  (X5R) or  $2.2\mu\text{F} \pm 100/-50\%$  (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 47 LDO Block Diagram



### 7.4.3.2 LDO1

This LDO generates the analog supply voltage used for the AFE itself.

- Input voltage is BVDD
- Output voltage is AVDD (typ. 2.9V)

### 7.4.3.3 LDO2

This LDO generates the digital supply voltage used for the AFE itself.

- Input Voltage is BVDD
- Output Voltage is DVDD (typ. 2.9V)
- Driver strength: 200mA

### 7.4.3.4 LDO3

This LDO can be used to generate the periphery voltage for the digital processor (e.g. vdd\_mem for MPMC interface)

- Input Voltage BVDD
- Output Voltage is PVDD 1.7 to 3.3V
- Driver strength: 200mA
- Programmable via P\_PVDD pin and PVDDp bit in 8 steps

Table 101 PVDD programming

| P_PVDD       | PVDDp=0 | PVDDp=1 |
|--------------|---------|---------|
| VSS          | OFF     | OFF     |
| 150k to VSS  | 2.50V   | 2.36V   |
| Open         | 3.33V   | 3.15V   |
| 150k to DVDD | 2.90V   | 2.74V   |
| DVDD         | 1.80V   | 1.70V   |

### 7.4.3.5 LDO4

This LDO will be used to supply the digital processor periphery (vdd\_peri). Default value is 3.11V, but it can be manually programmed to 2.94V if needed.

- Input Voltage BVDD
- Output Voltage is IOVDD (3.11 or 2.94)
- Programmable via IOVDDp bit.
- Driver strength: 200mA

### 7.4.3.6 LDO6

This LDO will be used to supply the USB 2.0 OTG interface block.

- Input Voltage BVDD
- Output Voltage is UVDD (3.26V)
- separate enable bit in USB\_UTIL register (0x17)
- Driver strength: 200mA

### 7.4.3.7 Parameter

Table 102 LDOs Block Characteristics

| Symbol               | Parameter                    | Notes                                        | Min | Typ | Max  | Unit              |
|----------------------|------------------------------|----------------------------------------------|-----|-----|------|-------------------|
| R <sub>ON</sub>      | On resistance                |                                              |     |     | 1    | Ω                 |
| PSRR                 | Power supply rejection ratio | f=1kHz                                       | 70  |     |      | dB                |
|                      |                              | f=100kHz                                     | 40  |     |      |                   |
| I <sub>OFF</sub>     | Shut down current            |                                              |     |     | 100  | nA                |
| I <sub>VDD</sub>     | Supply current               | without load                                 |     |     | 50   | μA                |
| Noise                | Output noise                 | 10Hz < f < 100kHz                            |     |     | 50   | μV <sub>rms</sub> |
| t <sub>start</sub>   | Startup time                 |                                              |     |     | 200  | μs                |
| V <sub>out</sub>     | Output voltage               | V <sub>bat</sub> >3.0V                       | 1.7 |     | 2.85 | V                 |
|                      |                              | full prog. range                             | 1.7 |     | 3.56 | V                 |
|                      |                              | LDO1, LDO2                                   |     | 2.9 |      | V                 |
| V <sub>out_tol</sub> | Output voltage tolerance     |                                              | -50 |     | 50   | mV                |
| V <sub>LineReg</sub> | Line regulation              | LDO1, Static                                 | -1  |     | 1    | mV                |
|                      |                              | LDO1, Transient; Slope: t <sub>r</sub> =10μs | -10 |     | 10   |                   |
| V <sub>LoadReg</sub> | Load regulation              | LDO1, Static                                 | -1  |     | 1    | mV                |
|                      |                              | LDO1, Transient; Slope: t <sub>r</sub> =10μs | -10 |     | 10   |                   |
| I <sub>LIMIT</sub>   | Current limitation           | LDO1, LDO2, LDO3, LDO4                       |     | 400 |      | mA                |

BVDD=4V; I<sub>LOAD</sub>=150mA; T<sub>amb</sub>=25°C; C<sub>LOAD</sub> =2.2μF (Ceramic); unless otherwise specified

## 7.4.3.8 Register Description

Table 103 System Register

| Name         |               | Base                                  |        | Default                                                                                                                                              |
|--------------|---------------|---------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| System       |               | I2C audio master                      |        | 0x21                                                                                                                                                 |
| Offset: 0x20 |               | System Settings Register              |        |                                                                                                                                                      |
|              |               | This register is reset at a DVDD-POR. |        |                                                                                                                                                      |
| Bit          | Bit Name      | Default                               | Access | Bit Description                                                                                                                                      |
| 7:4          | Version <3:0> | 0010                                  | R      | AFE number to identify the design version<br><b>0010: revision 2</b>                                                                                 |
| 3            | PVDDp         | 0                                     | R/W    | PVDD trimming:<br><b>0: Vnom</b><br>1: Vnom *17/18                                                                                                   |
| 2            | IOVDDp        | 0                                     | R/W    | IOVDD trimming:<br><b>0: IOVDD = 3.11V (nominal)</b><br>1: IOVDD = 2.94V                                                                             |
| 1            | EnWDogPwDn    | 0                                     | R/W    | <b>0: forced power down through watchdog is disabled</b><br>1: forced power down through watchdog is enabled (no serial interface reading within 1s) |
| 0            | PwrUpHld      | 1                                     | R/W    | 0: power up hold is cleared and supply is switched off<br><b>1: set to on after power on</b>                                                         |

Table 104 USB\_UTIL Register

| Name         |              | Base                                  |        | Default                                                                                                                                                                   |
|--------------|--------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB_UTIL     |              | I2C audio master                      |        | 0x00                                                                                                                                                                      |
| Offset: 0x17 |              | USB Utility Register                  |        |                                                                                                                                                                           |
|              |              | This register is reset at a DVDD-POR. |        |                                                                                                                                                                           |
| Bit          | Bit Name     | Default                               | Access | Bit Description                                                                                                                                                           |
| 7..5         |              | 000                                   | n/a    |                                                                                                                                                                           |
| 4            | LDO6_on      | 0                                     | R/W    | <b>0: UVDD generation disabled</b><br>1: LDO6 for generating UVDD enabled.                                                                                                |
| 3:2          | COMP_TH<1:0> | 0                                     | R/W    | Sets the threshold for the VBUS comparator<br><b>00: 4.5V</b><br>01: 3.18V<br>10: 1.5V<br>11: 0.6V                                                                        |
| 1            | SKIP_ENAB    | 0                                     | R/W    | <b>0: normal operation</b><br>1: enables the skip mode for the VBUS 1:2 charge pump. This is increasing the efficiency for smaller loads, but increasing the VBUS ripple. |
| 0            | CP_5V_on     | 0                                     | R/W    | <b>0: disables VBUS charge pump</b><br>1: enables VBUS charge pump                                                                                                        |

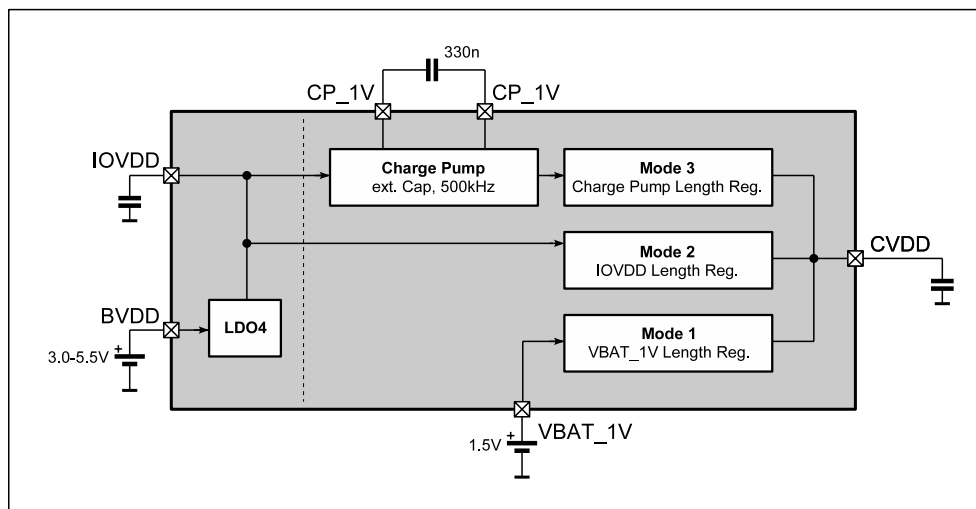
## 7.4.4 Charge-Pump Step-Down Converter

### 7.4.4.1 General

This converter will be used to supply the core voltage for a microprocessor.

- Input Voltage CPVDD
- Output Voltage 1.05 to 1.2 V
- Voltage setting via CVDDp<1:0> bits in 4 steps
- regulated 2:1 charge pump with pulse skipping
- scaleable switches according to BVDD
- Bypass LDO for higher currents or lower battery voltages respectively
- Driver strength: 50mA / 200mA with bypass LDO

Figure 48 CP Block Diagram



### 7.4.4.2 Mode Description

Three different functional parts generate core supply voltage CVDD. The switching between the modes is generally done automatically, but can also be manually overwritten by register settings.

Please observe that the charge pump block starts up in Mode 2 (IOVDD length regulator mode) to avoid a current limitation and has to be switched to automatic operation by register settings.

#### Direct length regulation from VBAT

Mode1=true IF  $((1.2V + V_{margin1}) < VBAT\_1V < (V_{TH1})) \&\& (NoUSB)$

- $V_{margin1} = 50mV / 150mV$  (100mV hysteric)
- $V_{TH1} = 1.7V / 1.8V$  (100mV hysteric)
- VBAT LDO is used when  $[1.8V > VBAT\_1V > 1.25V]$
- VBAT LDO is not used when there is high supply present from USB even when VBAT is in range.

#### Direct length regulation from IOVDD

Mode2=true IF  $((Not Mode1) \&\& (IOVDD/2 < (1.2 + V_{margin2})))$

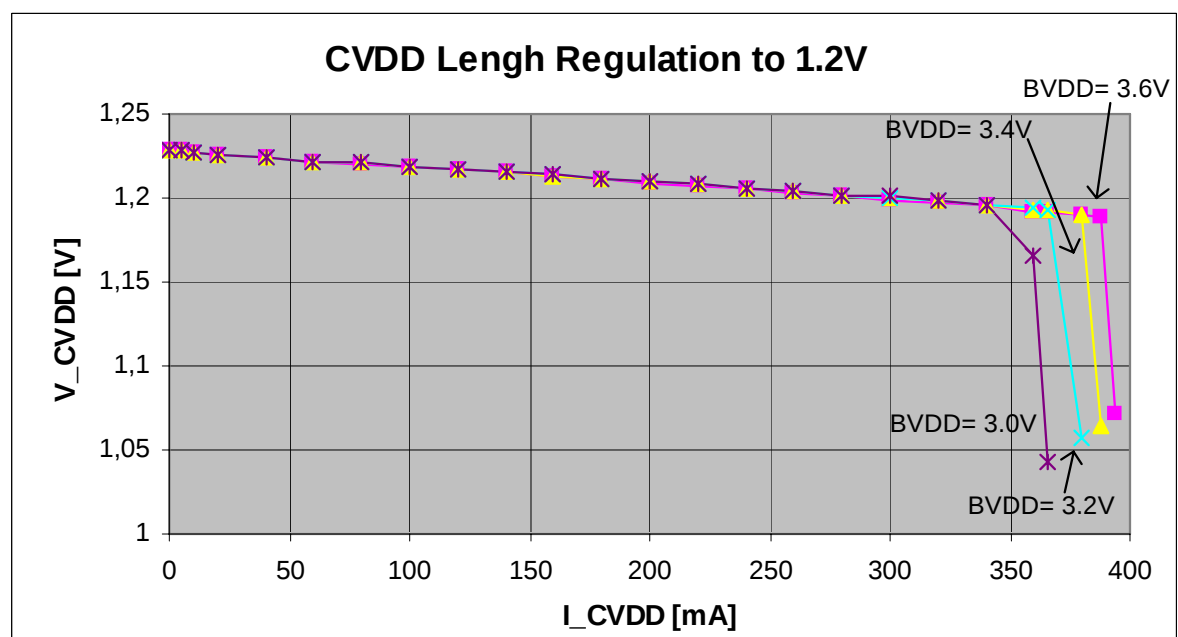
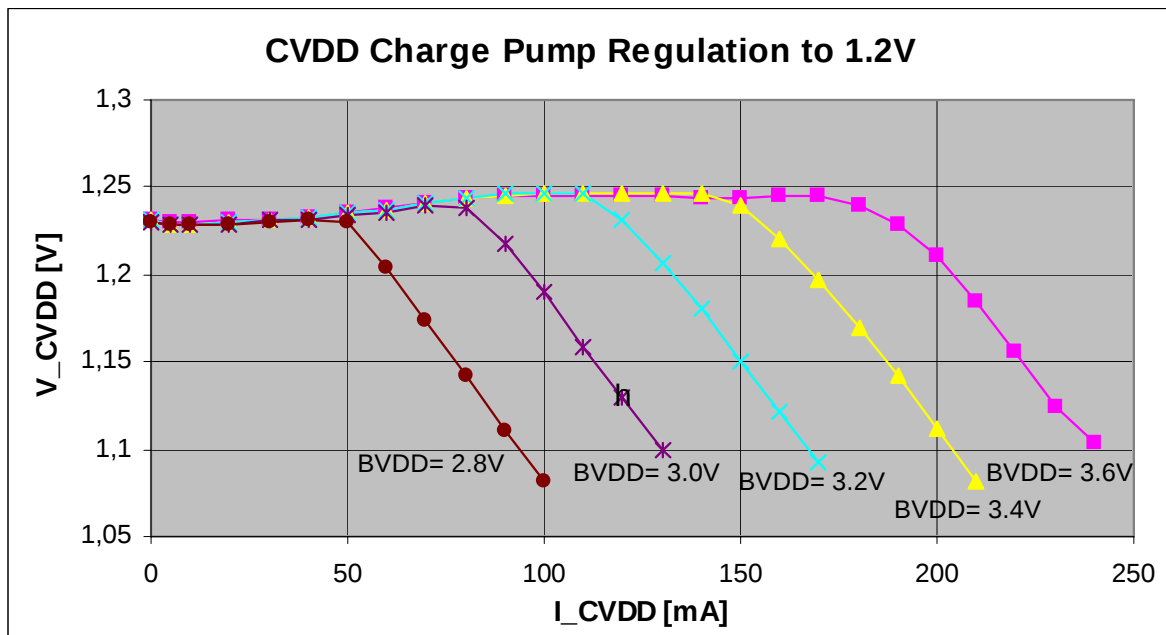
- $V_{margin2} = 200mV / 300mV$  (100mV hysteric)
- IOVDD LDO is used when VBAT LDO Mode1 is not entered and
- IOVDD is not high enough to do 2:1 charge-pump regulation.

#### Charge-Pump IOVDD division by 2 active plus length regulation

Mode3=true IF  $((Not Mode1) \&\& (Not Mode2))$

### 7.4.4.3 Parameter

Table 105 CP Typical Performance Parameter



## 7.4.4.4 Register Settings

Table 106 CVDD / DCDC3 Register

| Name         |            | Base                                  |        | Default                                                                                                                                                                                                             |
|--------------|------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CVDD / DCDC3 |            | I2C audio master                      |        | 0x00                                                                                                                                                                                                                |
| Offset: 0x21 |            | Charge Pump and 3V DCDC Register      |        |                                                                                                                                                                                                                     |
|              |            | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                     |
| Bit          | Bit Name   | Default                               | Access | Bit Description                                                                                                                                                                                                     |
| 7            | CP_SW      | 0                                     | R/W    | charge pump / length regulator switch margin reduction<br><b>0: margin set to 200/300 mV</b><br>1: margin reduced to 150/225 mV (automatic switching to length regulator is done "later", at a lower input voltage) |
| 6            | CP_on      | 0                                     | R/W    | <b>0: normal operation</b><br>1: keeps Mode 3 charge pump always on<br>Please note that bit 2 = "0", overrides bit 6.                                                                                               |
| 5            | LREG_CPnot | 0                                     | R      | Core voltage generation mode<br><b>0: CP is working</b><br>1: LREG is working                                                                                                                                       |
|              |            |                                       | W      | For production testing purpose only, in normal application mode this bit must always be written with "0".                                                                                                           |
| 4:3          | DCDC3p     | 00                                    | R/W    | DCDC3 Vout programming (BVDD)<br><b>00: 3.6V</b><br>01: 3.2V<br>10: 3.1V<br>11: 3.0V                                                                                                                                |
| 2            | LREG_off   | 0                                     | R/W    | <b>0: keeps Mode2 (length regulator always on)</b><br>1: normal operation                                                                                                                                           |
| 1:0          | CVDDp      | 00                                    | R/W    | CVDD trimming:<br><b>00: 1.2V</b><br>01: 1.15V<br>10: 1.10V<br>11: 1.05V                                                                                                                                            |

## 7.4.5 Audio Line Output

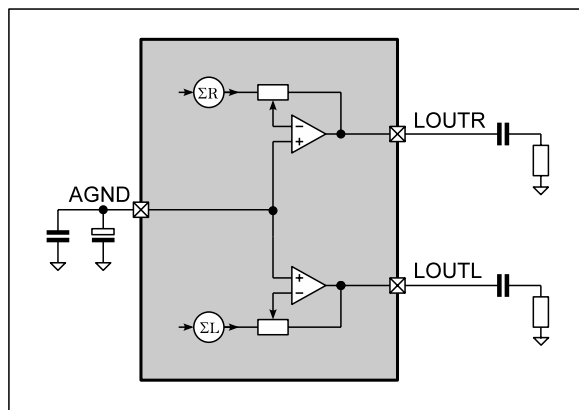
### 7.4.5.1 General

The line output is designed to provide the audio signal with typical 1Vp at a load of minimum 10k $\Omega$ , which is a minimum value for line inputs. Additional this output amplifier is capable to drive a 32 $\Omega$  load (e.g. an earpiece of a mobile phone). To achieve this operation mode can be switched from single ended stereo to mono differential.

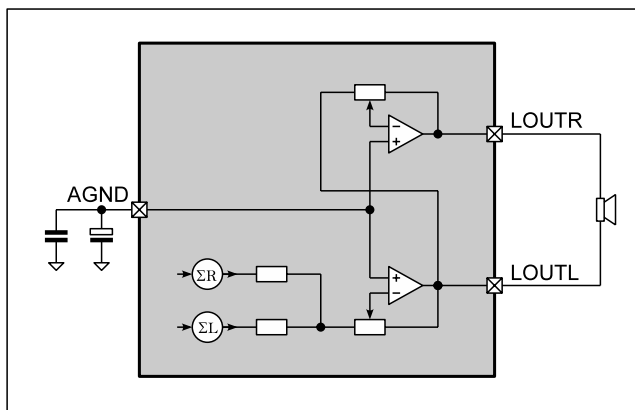
This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. Changing of volume and mute control can only be done after enabling the output.

If using the output in mono differential mode, the volume setting for the right channel should be set to 0dB.

Figure 49 Line Output



Stereo Mode



Mono Differential Mode (please observe that gain of right channel amplifier has to best to 0dB)

### 7.4.5.2 Parameter

Table 107 Line Output Characteristics

| Symbol          | Parameter             | Notes             | Min   | Typ | Max | Unit |
|-----------------|-----------------------|-------------------|-------|-----|-----|------|
| R <sub>L</sub>  | Output Load           | stereo mode       | 10k   |     |     | Ohm  |
|                 |                       | differential mode | 32    |     |     | Ohm  |
| A <sub>0</sub>  | Gain                  | programmable gain | -40.5 |     | 6   | dB   |
| ΔA <sub>x</sub> | Gain Step-Size        |                   |       | 1.5 |     | dB   |
| SNR             | Signal to Noise Ratio | stereo mode       | 90    |     |     | dB   |
|                 | Mute Attenuation      |                   | 120   |     |     | dB   |

BVDD = 3.3V, T<sub>A</sub> = 25°C unless otherwise mentioned

## 7.4.5.3 Register Description

Table 108 Line Output Related Register

| Name       | Base             | Offset | Description                 |
|------------|------------------|--------|-----------------------------|
| AudioSet_1 | I2C audio master | 0x14   | Enable/disable driver stage |

Table 109 LINE\_OUT\_R Register

| Name         |          | Base                                                                                                                                                        |        | Default                                                                                                                                                                       |
|--------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LINE_OUT_R   |          | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                          |
| Offset: 0x00 |          | Right Line Output Register                                                                                                                                  |        |                                                                                                                                                                               |
|              |          | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                               |
| Bit          | Bit Name | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                               |
| 7:5          |          | 000                                                                                                                                                         | n/a    | do not change                                                                                                                                                                 |
| 4:0          | LOR_VOL  | 00000                                                                                                                                                       | R/W    | volume settings for right line output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b> |

Table 110 LINE\_OUT\_L Register

| Name         |           | Base                                                                                                                                                        |        | Default                                                                                                                                                                                              |
|--------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LINE_OUT_L   |           | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                                                 |
| Offset: 0x01 |           | Left Line Output Register                                                                                                                                   |        |                                                                                                                                                                                                      |
|              |           | This register is reset when the stage is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                                                      |
| Bit          | Bit Name  | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                                                      |
| 7:6          | LO_SES_DM | 00                                                                                                                                                          | R/W    | Single ended stereo or differential mono selection<br>11: do not use<br>10: output switched to single ended stereo<br>01: output switched to differential mono<br><b>00: output switched to mute</b> |
| 5            |           | 0                                                                                                                                                           | n/a    | do not change                                                                                                                                                                                        |
| 4:0          | LOL_VOL   | 00000                                                                                                                                                       | R/W    | volume settings for right line output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b>                        |

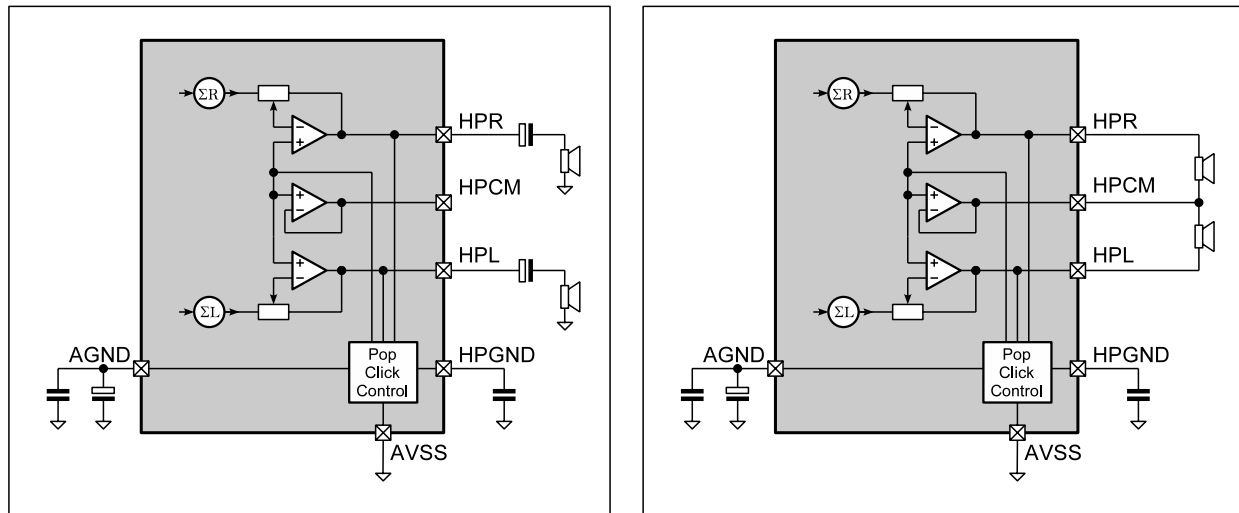
## 7.4.6 Headphone Output

### 7.4.6.1 General

The headphone output is designed to provide the audio signal with  $2 \times 40\text{mW}$  @  $16\Omega$  or  $2 \times 20\text{mW}$  @  $32\Omega$ , which are typical values for headphones.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from  $-43.43\text{dB}$  to  $+1.07\text{dB}$ . The maximum output power of  $40\text{mW}$  @  $16\Omega$  is achieved, by setting the mixer output to  $1\text{Vp}$  and using the gain of  $1.07\text{dB}$ .

Figure 50 Headphone Output



Headphones connected via decoupling capacitors

Headphones connected to Phantom Ground  
(Common Mode)

### 7.4.6.2 Phantom Ground

HPCM pin is the buffered HPGND output. It can be used to drive the loads without external blocking capacitors between HPL / HPR and HPCM. If the load is between HPR / HPL and BVSS,  $100\mu\text{F}$  of de-coupling capacitors are needed. The phantom ground can be switched off to save power if not needed.

### 7.4.6.3 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

HPGND pin, which needs a  $100\text{nF}$  capacitor outside, gets charged on power-up with  $2\mu\text{A}$  to  $\text{AGND}=1.45\text{V}$ . After start-up the DC level of the following pins are the same:  $\text{HPR}=\text{HPL}=\text{HPCM}=\text{HPGND}=\text{AGND}=1.45\text{V}$ . The Start-up time before releasing mute is about  $90\text{ms}$ . To avoid pop-noise  $150\text{ms}$  discharging time of HPGND after a shutdown, have to be waited before starting up again.

### 7.4.6.4 Over-current Protection

This output stage has an over-current protection, which disables the output for  $256\text{ms}$  or  $512\text{ms}$ . This value can be set in the headphone registers. The over-current protection limit of HPR and HPL pin is typical  $145\text{mA}$  while HPCM pin has a  $210\text{mA}$  threshold. If needed, the over-current condition can also be signalled via an interrupt to the controlling microprocessor.

### 7.4.6.5 Headphone Detection

With a control bit the headphone detection can be enabled. The detection is only working as long as the headphone stage is in power down mode and the load is applied between HPR / HPL and HPCM. The headphone detection can also trigger a corresponding interrupt.

### 7.4.6.6 Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected. Together with switching off the phantom ground this gives 4 possible operating modes.

Table 111 Headphone Power-Save Options

| HPCM_OFF | IBR_HPH | IDD_HPH (typ.) | Load   |
|----------|---------|----------------|--------|
| 0        | 0       | 2.2mA          | 16 Ohm |
| 1        | 0       | 1.5mA          | 16 Ohm |
| 0        | 1       | 1.5mA          | 32 Ohm |
| 1        | 1       | 1.0mA          | 32 Ohm |

BVDD = 3.3V, T<sub>A</sub> = 25°C unless otherwise mentioned

### 7.4.6.7 Parameter

Table 112 Power Amplifier Block Characteristics

| Symbol                | Parameter                      | Notes                                                   | Min    | Typ | Max  | Unit |
|-----------------------|--------------------------------|---------------------------------------------------------|--------|-----|------|------|
| R <sub>L</sub>        | Output Load                    | stereo mode                                             | 16     |     |      | Ohm  |
| P <sub>out</sub>      | Maximum Output Power           | R <sub>L</sub> = 32Ω                                    |        | 20  |      | mW   |
|                       |                                | R <sub>L</sub> = 16Ω                                    |        | 40  |      | mW   |
| A <sub>0</sub>        | Gain                           | programmable gain                                       | -43.43 |     | 1.07 | dB   |
| ΔA <sub>x</sub>       | Gain Step-Size                 |                                                         |        | 1.5 |      | dB   |
| PSRR                  | Power Supply Rejection Ratio   | 200Hz-20kHz, 720mV <sub>pp</sub> , R <sub>L</sub> = 16Ω | 60     | 90  |      | dB   |
|                       | Short Current Protection Level |                                                         |        | 145 |      | mA   |
| I <sub>OUT_pd</sub>   | I <sub>OUT</sub> power down    |                                                         | -20    |     | 20   | μA   |
| T <sub>power_up</sub> |                                |                                                         |        | 90  |      | ms   |
| SNR                   | Signal to Noise Ratio          |                                                         | 90     |     |      | dB   |
|                       | Mute Attenuation               |                                                         | 120    |     |      | dB   |

BVDD = 3.3V, T<sub>A</sub> = 25°C unless otherwise mentioned

## 7.4.6.8 Register Description

Table 113 Headphone Related Register

| Name       | Base             | Offset | Description                                          |
|------------|------------------|--------|------------------------------------------------------|
| AudioSet_3 | I2C audio master | 0x16   | Power save options, common mode buffer               |
| IRQ_ENRD_1 | I2C audio master | 0x26   | Interrupt settings for over current and HP detection |

Table 114 HPH\_OUT\_R Register

| Name         |           | Base                                  |        | Default                                                                                                                                                                                     |
|--------------|-----------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HPH_OUT_R    |           | I2C audio master                      |        | 0x00                                                                                                                                                                                        |
| Offset: 0x02 |           | Right Headphone Output Register       |        |                                                                                                                                                                                             |
|              |           | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                             |
| Bit          | Bit Name  | Default                               | Access | Bit Description                                                                                                                                                                             |
| 7:6          | HP_OVC_TO | 00                                    | R/W    | headphone over current time out:<br>11: 0 ms<br>10: 512 ms<br>01: 128 ms<br><b>00: 256 ms</b>                                                                                               |
| 5            |           | 0                                     | n/a    | do not change                                                                                                                                                                               |
| 4:0          | HPR_VOL   | 00000                                 | R/W    | volume settings for right headphone output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 1.07 dB gain<br>11110: -0.43 dB gain<br>..<br>00001: -43.93 dB gain<br><b>00000: -45.43 dB gain</b> |

Table 115 HPH\_OUT\_L Register

| Name         |            | Base                                  |        | Default                                                                                                                                                                                    |
|--------------|------------|---------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HPH_OUT_L    |            | I2C audio master                      |        | 0x00                                                                                                                                                                                       |
| Offset: 0x03 |            | Left Headphone Output Register        |        |                                                                                                                                                                                            |
|              |            | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                            |
| Bit          | Bit Name   | Default                               | Access | Bit Description                                                                                                                                                                            |
| 7            | HP_Mute_on | 0                                     | R/W    | <b>0: normal operation</b><br>1: headphone output set to mute (mute is on during power-up)                                                                                                 |
| 6            | HP_on      | 0                                     | R/W    | <b>0: headphone stage not powered</b><br>1: power up headphone stage                                                                                                                       |
| 5            | HPdet_on   | 0                                     | R/W    | <b>0: no headphone detection</b><br>1: enable headphone detection                                                                                                                          |
| 4:0          | HPL_VOL    | 00000                                 | R/W    | volume settings for left headphone output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 1.07 dB gain<br>11110: -0.43 dB gain<br>..<br>00001: -43.93 dB gain<br><b>00000: -45.43 dB gain</b> |

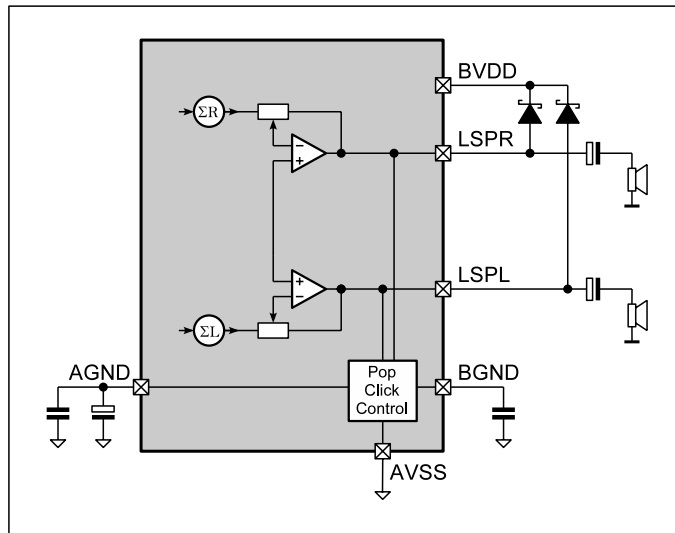
## 7.4.7 Speaker Output

### 7.4.7.1 General

The speaker output is designed to provide the stereo audio signal with 2x500mW @ 4Ω.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. The maximum output power of 500mW @ 4Ω is achieved, by setting the mixer output to 1Vp and using the gain of +6dB.

Figure 51 Speaker Output



Speaker connected via decoupling capacitors

### 7.4.7.2 Latchup Protection

For latchup protection of pins LSPL and LSPR, external schottky diodes must be implemented from LSPL to BVDD and LSPR to BVDD as drawn in the above diagram. These diodes protect pins LSPL and LSPR against the back-voltage induced by the inductance of the speaker in case of switching off the speaker. These diodes must be schottky type diodes with low forward voltages to prevent high current through the internal LSPR/LSPL ESD protection diodes that potentially would cause latchup for currents exceeding the maximum input current specifications given in chapter 6.1 Absolute Maximum Ratings.

These schottky diodes must be capable of surging maximum peak currents of up to 600 mA.

### 7.4.7.3 No-Pop Function

BGND pin, which needs a 100nF capacitor outside, gets charged on power-up to BVDD/2. To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

The Start-up time before releasing mute is about 100ms. To avoid pop-noise the 150ms discharging time of SPR / SPL after a shutdown (220μF capacitor in stereo single ended mode assumed), have to be waited before starting up again.

### 7.4.7.4 Over-current Protection

This output stage has an over-current protection, which disables the output for 0 to 512ms. This value can be set in the speaker registers. The over-current protection limit of SPR and SPL pin is typical 700mA. To get an interrupt on an over-current event, the corresponding bit in the IRQ\_ENRD1 register (0x26h) has to be set.

### 7.4.7.5 Power Save Options

When driving  $> 4\Omega$ , two power save options can be chosen.

The output driver stage can be set to only 25% drive capacity, which will reduce the maximum output power. Additionally the bias currents can be reduced to 50% in 3 steps.

Table 116 Speaker Power-Save Options

| LSP_LP | IBR_LSP | IDD_LSP (typ.) | Load      |
|--------|---------|----------------|-----------|
| 0      | 00      | 8mA            | 4 Ohm     |
| 1      | 00      | 2.8mA          | 16-32 Ohm |
| 1      | 01      | 2.4mA          | 16-32 Ohm |
| 1      | 10      | 1.9mA          | 16-32 Ohm |
| 1      | 11      | 1.5mA          | 16-32 Ohm |

BVDD = 3.3V,  $T_A = 25^\circ\text{C}$  unless otherwise mentioned

### 7.4.7.6 Parameter

Table 117 Speaker Amplifier Parameter

| Symbol          | Parameter                      | Notes                         | Min   | Typ | Max | Unit          |
|-----------------|--------------------------------|-------------------------------|-------|-----|-----|---------------|
| $R_L$           | Output Load                    | stereo mode                   | 4     |     |     | Ohm           |
|                 |                                | mono differential mode        | 8     |     |     | Ohm           |
| $P_{out}$       | Maximum Output Power           | $R_L = 8\Omega$               |       | 1   |     | W             |
| $A_0$           | Gain                           | programmable gain             | -40.5 |     | 6   | dB            |
| $\Delta A_x$    | Gain Step-Size                 |                               |       | 1.5 |     | dB            |
| PSRR            | Power Supply Rejection Ratio   | 200Hz-20kHz, 720mVpp, no load | 70    | 75  |     | dB            |
|                 | Short Current Protection Level |                               |       | 700 |     | mA            |
| $I_{OUT\_pd}$   | $I_{OUT}$ power down           |                               | -20   |     | 20  | $\mu\text{A}$ |
| $T_{power\_up}$ |                                |                               |       | 100 |     | ms            |
| SNR             | Signal to Noise Ratio          |                               | 90    |     |     | dB            |
|                 | Mute Attenuation               |                               | 120   |     |     | dB            |

BVDD = 5V,  $T_A = 25^\circ\text{C}$  unless otherwise mentioned

## 7.4.7.7 Register Description

Table 118 Speaker Related Register

| Name       | Base             | Offset | Description                                   |
|------------|------------------|--------|-----------------------------------------------|
| AudioSet_2 | I2C audio master | 0x15   | Power save options                            |
| IRQ_ENRD_1 | I2C audio master | 0x26   | Interrupt settings for over current detection |

## Right Speaker Register (04h)

Table 119 LSP\_OUT\_R Register

| Name         |           | Base                                  |        | Default                                                                                                                                                                          |
|--------------|-----------|---------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSP_OUT_R    |           | I2C audio master                      |        | 0x00                                                                                                                                                                             |
| Offset: 0x04 |           | Right Speaker Output Register         |        |                                                                                                                                                                                  |
|              |           | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                  |
| Bit          | Bit Name  | Default                               | Access | Bit Description                                                                                                                                                                  |
| 7:6          | SP_OVC_TO | 00                                    | R/W    | speaker over current time out:<br>11: 0 ms<br>10: 512 ms<br>01: 128 ms<br><b>00: 256 ms</b>                                                                                      |
| 5            |           | 0                                     | n/a    | do not change                                                                                                                                                                    |
| 4:0          | SPR_VOL   | 00000                                 | R/W    | volume settings for right speaker output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b> |

Table 120 LSP\_OUT\_L Register

| Name         |            | Base                                  |        | Default                                                                                                                                                                         |
|--------------|------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPH_OUT_L    |            | I2C audio master                      |        | 0x00                                                                                                                                                                            |
| Offset: 0x05 |            | Left Speaker Output Register          |        |                                                                                                                                                                                 |
|              |            | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                 |
| Bit          | Bit Name   | Default                               | Access | Bit Description                                                                                                                                                                 |
| 7            | SP_Mute_on | 0                                     | R/W    | <b>0: normal operation</b><br>1: speaker output set to mute (mute is on during power-up)                                                                                        |
| 6            | SP_on      | 0                                     | R/W    | <b>0: speaker stage not powered</b><br>1: power up speaker stage                                                                                                                |
| 5            |            | 0                                     | n/a    | do not change                                                                                                                                                                   |
| 4:0          | SPL_VOL    | 00000                                 | R/W    | volume settings for left speaker output,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b> |

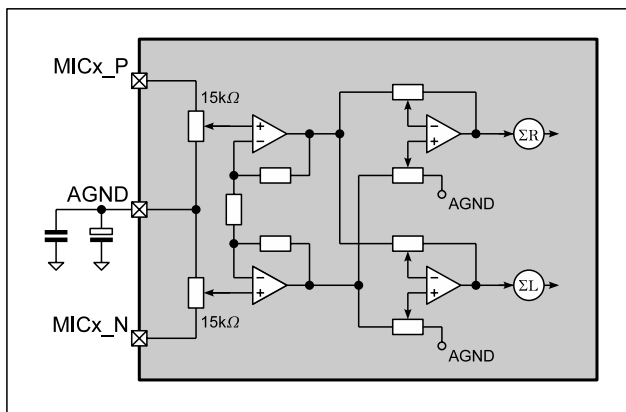
## 7.4.8 Microphone Inputs (2x)

### 7.4.8.1 General

The chip features two identical microphone inputs. The blocks have differential inputs to a microphone amplifier with adjustable gain. This stage also includes an AGC.

The following volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the input.

Figure 52 Microphone Input



Microphone Preamplifier and Gain Stage

### 7.4.8.2 AGC

The microphone amplifier includes an AGC, which is limiting the signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

### 7.4.8.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPHCM. The supply is designed for  $\leq 2\text{mA}$  and has a 10mA current limit. In OFF mode the MICSUP terminal is pulled to AVDD with 30kohm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPHCM as headset ground the HPH-stage gives the interrupt. After enabling the HPH-stage through the CPU the microphone detection interrupt will follow.

### 7.4.8.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

## 7.4.8.5 Parameter

Table 121 Microphone Inputs Parameter

| Symbol                   | Parameter                 | Notes                          | Min   | Typ    | Max | Unit |
|--------------------------|---------------------------|--------------------------------|-------|--------|-----|------|
| A0                       | Gain                      | programmable gain              | -40.5 |        | 6   | dB   |
| $\Delta Ax$              | Gain Step-Size            |                                |       | 1.5    |     | dB   |
| R <sub>inMIC</sub>       | Input Resistance          | differential                   |       | 15     |     | kOhm |
| A <sub>MIC0</sub>        | MicAmp_Gain0              |                                |       | 28     |     | dB   |
| A <sub>MIC1</sub>        | MicAmp_Gain1              |                                |       | 34     |     | dB   |
| A <sub>MIC2</sub>        | MicAmp_Gain2              |                                |       | 40     |     | dB   |
|                          | SoftClip_AGC_Range        |                                |       | 15*2.0 |     | dB   |
|                          | Attack_Time               |                                |       | 60     |     | us   |
|                          | Release_Time              |                                |       | 120    |     | ms   |
| V <sub>Innom0</sub>      | Nominal_Input_Voltage0    | MicInGain = 0dB, MicAmp_Gain0  |       | 40     |     | mVp  |
| V <sub>Innom1</sub>      | Nominal_Input_Voltage1    | MicInGain = 0dB, MicAmp_Gain1  |       | 20     |     | mVp  |
| V <sub>Innom2</sub>      | Nominal_Input_Voltage2    | MicInGain = 0dB, MicAmp_Gain2  |       | 10     |     | mVp  |
| SNR                      | Signal to Noise Ratio     |                                | 90    |        |     | dB   |
|                          | Mute Attenuation          |                                | 120   |        |     | dB   |
| <b>Microphone Supply</b> |                           |                                |       |        |     |      |
| V <sub>MICsup</sub>      | Microphone Supply Voltage | 0-4mA                          |       | 2.95   |     | V    |
| I <sub>MIClim</sub>      | Mic. Supply Current Limit |                                |       | 10     |     | mA   |
| I <sub>MICdet</sub>      | Mic. Detection Current    |                                |       | 50     |     | uA   |
| I <sub>REMdet</sub>      | Remote Detection Current  | microphone supply current step | 500   |        |     | uA   |
| V <sub>noise</sub>       | Voltage Noise             |                                |       | 5.7    |     | uV   |

BVDD = 3.3V, T<sub>A</sub> = 25°C unless otherwise mentioned

## 7.4.8.6 Register Description

Table 122 Microphone Related Register

| Name       | Base             | Offset | Description                                          |
|------------|------------------|--------|------------------------------------------------------|
| AudioSet_1 | I2C audio master | 0x14   | Enable/disable driver stage                          |
| IRQ_ENRD_1 | I2C audio master | 0x26   | Interrupt settings for microphone detection          |
| IRQ_ENRD_2 | I2C audio master | 0x27   | Interrupt settings for remote button press detection |

Table 123 MIC1\_R &amp; MIC2\_R Register

| Name               |                              | Base                                                                                                                                                        |        | Default                                                                                                                                                                     |
|--------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIC1_R, MIC2_R     |                              | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                        |
| Offset: 0x06, 0x08 |                              | Right Microphone Input Registers                                                                                                                            |        |                                                                                                                                                                             |
|                    |                              | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                             |
| Bit                | Bit Name                     | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                             |
| 7                  | Mic1_AGC_off<br>Mic2_AGC_off | 0                                                                                                                                                           | R/W    | 0: automatic gain control enabled<br>1: automatic gain control disabled                                                                                                     |
| 6:5                | Mic1_Gain<br>Mic2_Gain       | 00                                                                                                                                                          | R/W    | 00: gain set to 28 dB<br>01: gain set to 34 dB<br>10: gain set to 40 dB<br>11: reserved, do not use.                                                                        |
| 4:0                | Mic1R_VOL<br>Mic2R_VOL       | 00000                                                                                                                                                       | R/W    | volume settings for right microphone input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br>00000: -40.5 dB gain |

Table 124 MIC1\_L &amp; MIC2\_L Register

| Name               |                                | Base                                                                                                                                                        |        | Default                                                                                                                                                                    |
|--------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIC1_L, MIC2_L     |                                | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                       |
| Offset: 0x07, 0x09 |                                | Left Microphone Input Registers                                                                                                                             |        |                                                                                                                                                                            |
|                    |                                | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                            |
| Bit                | Bit Name                       | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                            |
| 7                  | Mic1_Sup_off<br>Mic2_Sup_off   | 0                                                                                                                                                           | R/W    | 0: microphone supply enabled<br>1: microphone supply disabled                                                                                                              |
| 6                  | Mic1_Mute_off<br>Mic2_Mute_off | 0                                                                                                                                                           | R/W    | 0: microphone input set to mute<br>1: normal operation                                                                                                                     |
| 5                  |                                | 0                                                                                                                                                           | n/a    |                                                                                                                                                                            |
| 4:0                | Mic1L_VOL<br>Mic2L_VOL         | 00000                                                                                                                                                       | R/W    | volume settings for left microphone input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br>00000: -40.5 dB gain |

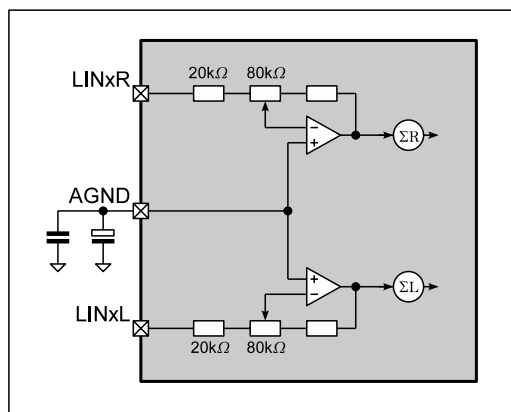
## 7.4.9 Audio Line Inputs (2x)

### 7.4.9.1 General

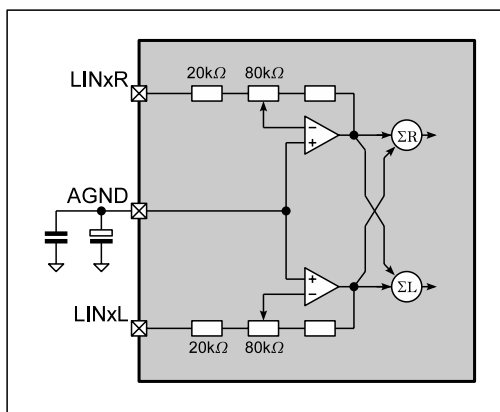
The chip features includes two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

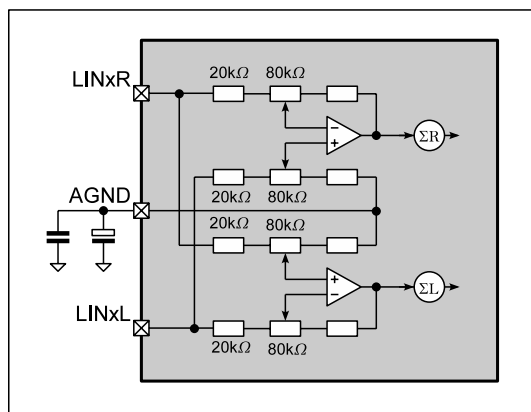
Figure 53 Line Inputs



Stereo Mode



Mono Single Ended Mode



Mono Differential Mode

### 7.4.9.2 Parameter

Figure 54 Line Input Parameter

| Symbol       | Parameter             | Notes                         | Min   | Typ | Max | Unit |
|--------------|-----------------------|-------------------------------|-------|-----|-----|------|
| A0           | Gain                  | programmable gain             | -34.5 |     | 12  | dB   |
| $\Delta A_x$ | Gain Step-Size        |                               |       | 1.5 |     | dB   |
| $R_{inLINE}$ | Input Resistance      | Mute                          |       | 49  |     | kOhm |
|              |                       | Min Gain, single ended stereo |       | 100 |     | kOhm |
| SNR          | Signal to Noise Ratio |                               | 90    |     |     | dB   |
|              | Mute Attenuation      |                               | 120   |     |     | dB   |

BVDD = 3.3V, T<sub>A</sub> = 25°C, f<sub>s</sub> = 48kHz unless otherwise mentioned

## 7.4.9.3 Register Description

Table 125 Line Input Related Register

| Name      | Base             | Offset | Description                 |
|-----------|------------------|--------|-----------------------------|
| AudioSet1 | I2C audio master | 0x14   | Enable/disable driver stage |

Table 126 LINE\_IN1\_R &amp; LINE\_IN2\_R Register

| Name                   |                                | Base                                                                                                                                                        |        | Default                                                                                                                                                                        |
|------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LINE_IN1_R, LINE_IN2_R |                                | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                           |
| Offset: 0x0A, 0x0C     |                                | Right Line Input Registers                                                                                                                                  |        |                                                                                                                                                                                |
|                        |                                | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                                |
| Bit                    | Bit Name                       | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                                |
| 7:6                    |                                | 00                                                                                                                                                          | n/a    | do not change                                                                                                                                                                  |
| 5                      | LI1R_Mute_off<br>LI2R_Mute_off | 0                                                                                                                                                           | R/W    | <b>0: right line input is set to mute</b><br>1: normal operation                                                                                                               |
| 4:0                    | LI1R_VOL<br>LI2R_VOL           | 00000                                                                                                                                                       | R/W    | volume settings for right line input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 12 dB gain<br>11110: 10.5 dB gain<br>..<br>00001: -33 dB gain<br><b>00000: -34.5 dB gain</b> |

Table 127 LINE\_IN1\_L &amp; LINE\_IN2\_L Register

| Name                   |                                | Base                                                                                                                                                        |        | Default                                                                                                                                                                                                  |
|------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LINE_IN1_L, LINE_IN2_L |                                | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                                                     |
| Offset: 0x0B, 0x0D     |                                | Right Line Input Registers                                                                                                                                  |        |                                                                                                                                                                                                          |
|                        |                                | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                                                          |
| Bit                    | Bit Name                       | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                                                          |
| 7:6                    | LI1L_Mode<br>LI2L_Mode         | 00                                                                                                                                                          | R/W    | Stereo or mono input selection<br><b>00: inputs switched to single ended stereo</b><br>01: inputs switched to differential mono<br>10: inputs switched to single ended mono<br>11: reserved, do not use. |
| 5                      | LI1L_Mute_off<br>LI2L_Mute_off | 0                                                                                                                                                           | R/W    | <b>0: left line input is set to mute</b><br>1: normal operation                                                                                                                                          |
| 4:0                    | LI1L_VOL<br>LI2L_VOL           | 00000                                                                                                                                                       | R/W    | volume settings for right line input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 12 dB gain<br>11110: 10.5 dB gain<br>..<br>00001: -33 dB gain<br><b>00000: -34.5 dB gain</b>                           |

## 7.4.10 I2S Digital Audio Interface

### 7.4.10.1 Input

Digital audio data can be fed into the AS3515A via the I2S interface. These input data are then used by the 18-bit DAC to generate the analog audio signal.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

### 7.4.10.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the 14 bit ADC. The digital output is done via an I2S interface.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

### 7.4.10.3 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up to 32 bits. When there are less than 18 bits sampled, the data sample is completed with "0"s. The ADC output is always 16 bits. If more SCLK pulses are provided, only the first 16 will be significant. All following bits will be "0".

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

The digital part has to provide MCLK (master clock) with  $128 \cdot f_s$  ( $f_s$  = audio sampling frequency) over-sampling to guarantee a proper DAC and ADC operation.

Figure 55 I2S Left Justified Mode

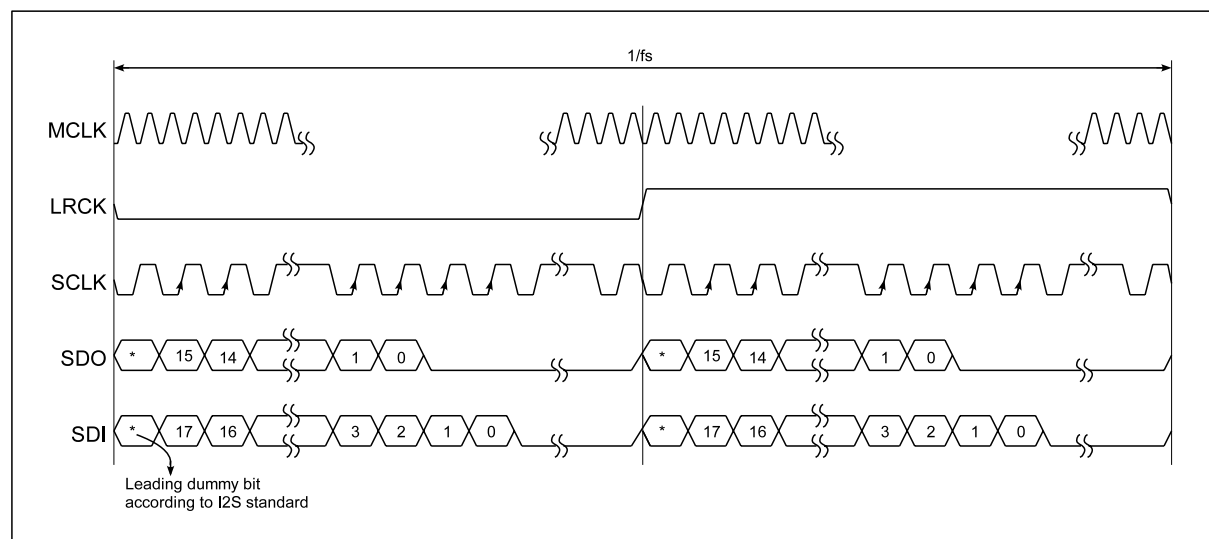
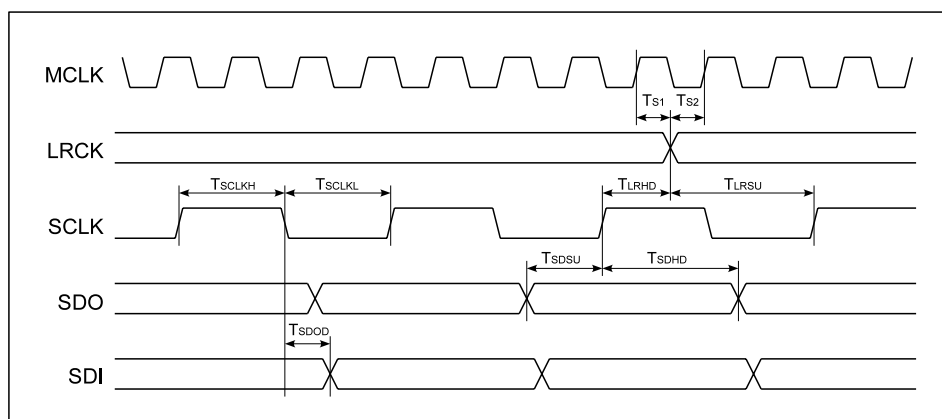


Figure 56 I2S Timing



#### 7.4.10.4 Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption.

#### 7.4.10.5 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

#### 7.4.10.6 Parameter

Table 128 Audio Converter Parameter

| Symbol                      | Parameter             | Notes                           | Min    | Typ | Max  | Unit |
|-----------------------------|-----------------------|---------------------------------|--------|-----|------|------|
| A0                          | Gain                  | programmable gain DAC input     | -43.43 |     | 1.07 | dB   |
|                             |                       | programmable gain ADC output    | -34.5  |     | 12   | dB   |
| $\Delta A_x$                | Gain Step-Size        |                                 |        | 1.5 |      | dB   |
|                             | Mute Attenuation      |                                 | 120    |     |      | dB   |
| <b>I2S inputs / outputs</b> |                       |                                 |        |     |      |      |
| $V_{IL}$                    |                       | SCLK, LRCK, SDI (30%DVDD/2)     | -      | -   | 0.42 | V    |
| $V_{IH}$                    |                       | SCLK, LRCK, SDI (70%DVDD/2)     | 1.02   | -   | DVDD | V    |
| $V_{OL}$                    |                       | SDO, IRQ @2mA                   | -      | -   | 0.3  | V    |
| $V_{OH}$                    |                       | SDO, IRQ @2mA                   | 2.6    | -   | -    | V    |
| $T_{SCLKH}$                 | SCLK clock high time  |                                 | 80     |     |      | ns   |
| $T_{SCLKL}$                 | SCLK clock low time   |                                 | 80     |     |      | ns   |
| $T_{SDSU}$                  | Data set-up time      | SDI versus rising edge of SCLK  | 80     |     |      | ns   |
| $T_{SDHD}$                  | Data hold time        | SDI versus rising edge of SCLK  | 80     |     |      | ns   |
| $T_{SDOD}$                  | Data Output Delay     | SDO versus falling edge of SCLK |        |     | 25   | ns   |
| $T_{LRSU}$                  | Clock set up time     | LRCK versus rising edge of SCLK | 80     |     |      | ns   |
| $T_{LRHD}$                  | Clock hold time       | LRCK versus rising edge of SCLK | 80     |     |      | ns   |
| $T_{S1}, T_{S2}$            | Clock separation time | MCLK rising edge versus LRCK    | 20     |     |      | ns   |
| $T_{JITTER}$                | clock Jitter          | LRCK                            | -20    |     | 20   | ns   |

BVDD = 3.3V, DVDD = 2.9V,  $T_A$  = 25°C unless otherwise mentioned

## 7.4.10.7 Register Description

Table 129 Audio Converter Related Register

| Name       | Base             | Offset | Description                           |
|------------|------------------|--------|---------------------------------------|
| AudioSet_1 | I2C audio master | 0x14   | Enable/disable DAC and ADC            |
| AudioSet_2 | I2C audio master | 0x15   | Power save options and dither control |
| IRQ_ENRD_1 | I2C audio master | 0x25   | Interrupt settings for LRCK changes   |

Table 130 DAC\_R Register

| Name         |          | Base                                                                                                                                                        |        | Default                                                                                                                                                                   |
|--------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DAC_R        |          | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                      |
| Offset: 0x0E |          | Right DAC output Registers                                                                                                                                  |        |                                                                                                                                                                           |
|              |          | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                           |
| Bit          | Bit Name | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                           |
| 7:5          |          | 000                                                                                                                                                         | n/a    | do not change                                                                                                                                                             |
| 4:0          | DAR_VOL  | 00000                                                                                                                                                       | R/W    | volume settings for right DAC output, adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b> |

Table 131 DAC\_L Register

| Name         |              | Base                                                                                                                                                        |        | Default                                                                                                                                                                  |
|--------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DAC_L        |              | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                     |
| Offset: 0x0F |              | Left DAC output Registers                                                                                                                                   |        |                                                                                                                                                                          |
|              |              | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                          |
| Bit          | Bit Name     | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                          |
| 7            |              | 0                                                                                                                                                           | n/a    |                                                                                                                                                                          |
| 6            | DAC_Mute_off | 0                                                                                                                                                           | R/W    | <b>0: DAC output is set to mute</b><br>1: normal operation                                                                                                               |
| 5            |              | 0                                                                                                                                                           | n/a    |                                                                                                                                                                          |
| 4:0          | DAL_VOL      | 00000                                                                                                                                                       | R/W    | volume settings for left DAC output, adjustable in 32 steps @ 1.5dB<br>11111: 6 dB gain<br>11110: 4.5 dB gain<br>..<br>00001: -39 dB gain<br><b>00000: -40.5 dB gain</b> |

Table 132 ADC\_R Register

| Name         |          | Base                                                                                                                                                        |        | Default                                                                                                                                                                |
|--------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC_R        |          | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                   |
| Offset: 0x10 |          | Right ADC input Registers                                                                                                                                   |        |                                                                                                                                                                        |
|              |          | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                        |
| Bit          | Bit Name | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                        |
| 7:6          | ADCmux   | 00                                                                                                                                                          | R/W    | 00: Stereo Microphone<br>01: Line_IN1<br>10: Line_IN2<br>11: Audio SUM                                                                                                 |
| 5            |          |                                                                                                                                                             |        |                                                                                                                                                                        |
| 4:0          | ADR_VOL  | 00000                                                                                                                                                       | R/W    | volume settings for right ADC input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 12 dB gain<br>11110: 10.5 dB gain<br>..<br>00001: -33 dB gain<br>00000: -34.5 dB gain |

Table 133 ADC\_L Register

| Name         |              | Base                                                                                                                                                        |        | Default                                                                                                                                                               |
|--------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC_L        |              | I2C audio master                                                                                                                                            |        | 0x00                                                                                                                                                                  |
| Offset: 0x11 |              | Left ADC input Registers                                                                                                                                    |        |                                                                                                                                                                       |
|              |              | This register is reset when the block is disabled in AudioSet1 register (0x14) or at a DVDD-POR. The register cannot be written when the block is disabled. |        |                                                                                                                                                                       |
| Bit          | Bit Name     | Default                                                                                                                                                     | Access | Bit Description                                                                                                                                                       |
| 7            | AD_FS_4      | 0                                                                                                                                                           | R/W    | Divider selection for ADC sampling clock<br>0: ADC sample clock is I2S LRCK / 2<br>1: ADC sample clock is I2S LRCK / 4                                                |
| 6            | ADC_Mute_off | 0                                                                                                                                                           | R/W    | 0: ADC output is set to mute<br>1: normal operation                                                                                                                   |
| 5            |              | 0                                                                                                                                                           | n/a    |                                                                                                                                                                       |
| 4:0          | ADL_VOL      | 00000                                                                                                                                                       | R/W    | volume settings for left ADC input,<br>adjustable in 32 steps @ 1.5dB<br>11111: 12 dB gain<br>11110: 10.5 dB gain<br>..<br>00001: -33 dB gain<br>00000: -34.5 dB gain |

## 7.4.11 Audio Output Mixer

### 7.4.11.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Microphone Input 2
- Line Input 1
- Line Input 2
- Digital Audio Input (DAC)

The mixing ratios have to be with the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

### 7.4.11.2 Register Description

*Audio Mixer Related Register*

| Name       | Base             | Offset | Description                |
|------------|------------------|--------|----------------------------|
| AudioSet_1 | I2C audio master | 0x14   | Enable/disable mixer stage |
| AudioSet_2 | I2C audio master | 0x15   | Enable/disable AGC         |

The mixer stage has no dedicated registers.

## 7.4.12 Audio Settings

### 7.4.12.1 Register Description

Table 134 AudioSet\_1 Register

| Name         |          | Base                                  |        | Default                                                                                                |
|--------------|----------|---------------------------------------|--------|--------------------------------------------------------------------------------------------------------|
| AudioSet_1   |          | I2C audio master                      |        | 0x00                                                                                                   |
| Offset: 0x14 |          | First Audio Set Register              |        |                                                                                                        |
|              |          | This register is reset at a DVDD-POR. |        |                                                                                                        |
| Bit          | Bit Name | Default                               | Access | Bit Description                                                                                        |
| 7            | ADC_on   | 0                                     | R/W    | <b>0: ADC disabled</b><br>1: ADC for recording is enabled                                              |
| 6            | SUM_on   | 0                                     | R/W    | <b>0: Summing / Mixing stage is disabled (no audio output)</b><br>1: Summing / Mixing stage is enabled |
| 5            | DAC_on   | 0                                     | R/W    | <b>0: DAC disabled</b><br>1: DAC enabled                                                               |
| 4            | LOUT_on  | 0                                     | R/W    | <b>0: Line output disabled</b><br>1: Line output enabled                                               |
| 3            | LIN2_on  | 0                                     | R/W    | <b>0: Line input 2 disabled</b><br>1: Line input 2 enabled                                             |
| 2            | LIN1_on  | 0                                     | R/W    | <b>0: Line input 1 disabled</b><br>1: Line input 1 enabled                                             |
| 1            | MIC2_on  | 0                                     | R/W    | <b>0: Microphone input 2 disabled</b><br>1: Microphone input 2 enabled                                 |
| 0            | MIC1_on  | 0                                     | R/W    | <b>0: Microphone input 1 disabled</b><br>1: Microphone input 1 enabled                                 |

Table 135 AudioSet\_2 Register

| Name         |              | Base                                  |        | Default                                                                                                                                                     |
|--------------|--------------|---------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AudioSet_2   |              | I2C audio master                      |        | 0x00                                                                                                                                                        |
| Offset: 0x15 |              | Second Audio Set Register             |        |                                                                                                                                                             |
|              |              | This register is reset at a DVDD-POR. |        |                                                                                                                                                             |
| Bit          | Bit Name     | Default                               | Access | Bit Description                                                                                                                                             |
| 7            | BIAS_off     | 0                                     | R/W    | <b>0: bias enabled</b><br>1: bias disabled, for power saving in non audio mode                                                                              |
| 6            | DITH_off     | 0                                     | R/W    | <b>0: add dither to the DAC audio stream</b><br>1: no dither added                                                                                          |
| 5            | AGC_off      | 0                                     | R/W    | <b>0: automatic gain control for summing stage enabled</b><br>1: automatic gain control for summing stage disabled                                          |
| 4:3          | IBR_DAC<1:0> | 00                                    | R/W    | Bias current reduction settings for DAC:<br><b>00: 0%</b><br>01: 25%<br>10: 40%<br>11: 50%                                                                  |
| 2            | LSP_LP       | 0                                     | R/W    | Low power mode for speaker output:<br><b>0: speaker output driver set for 40hm to 160hm loads</b><br>1: speaker output driver set for 160hm or larger loads |
| 1:0          | IBR_LSP<1:0> | 00                                    | R/W    | Bias current reduction settings for speaker output:<br><b>00: 0%</b><br>01: 17%<br>10: 34%<br>11: 50%                                                       |

Table 136 AudioSet\_3 Register

| Name         |          | Base                                  |        | Default                                                                                                                                                                |
|--------------|----------|---------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AudioSet_3   |          | I2C audio master                      |        | 0x00                                                                                                                                                                   |
| Offset: 0x16 |          | Third Audio Set Register              |        |                                                                                                                                                                        |
|              |          | This register is reset at a DVDD-POR. |        |                                                                                                                                                                        |
| Bit          | Bit Name | Default                               | Access | Bit Description                                                                                                                                                        |
| 7:3          |          | 00000                                 | n/a    | do not change                                                                                                                                                          |
| 2            | ZCU_off  | 0                                     | R/W    | Zero cross gain update of audio outputs<br><b>0: zero cross update enabled</b><br>1: zero cross update disabled<br>should be disabled for C21020                       |
| 1            | IBR_HPH  | 0                                     | R/W    | Bias current reduction settings for headphone output:<br><b>0: headphone output driver set for 16Ohm load</b><br>1: headphone output driver set for 32Ohm load or more |
| 0            | HPCM_off | 00                                    | R/W    | Headphone common mode buffer settings:<br><b>0: headphone CM buffer is switched on</b><br>1: headphone CM buffer is switched off                                       |

## 7.4.13 VBUS CP & Comparator

### 7.4.13.1 General

This block will be used to generate VBUS for USB OTG host operation and to read back VBUS voltage levels to support USB OTG protocols.

- Input Voltage DVDD
- Output Voltage 5V (VBUS)
- regulated 1:2 charge pump with pulse skipping
- Driver strength: 10mA

### 7.4.13.2 Register Description

Table 137 USB\_UTIL Register

| Name         |              | Base                                  |        | Default                                                                                                                                                            |
|--------------|--------------|---------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB_UTIL     |              | I2C audio master                      |        | 0x00                                                                                                                                                               |
| Offset: 0x17 |              | USB Utility Register                  |        |                                                                                                                                                                    |
|              |              | This register is reset at a DVDD-POR. |        |                                                                                                                                                                    |
| Bit          | Bit Name     | Default                               | Access | Bit Description                                                                                                                                                    |
| 7..5         |              | 000                                   | n/a    |                                                                                                                                                                    |
| 4            | LDO6_on      | 0                                     | R/W    | 0: UVDD generation disabled<br>1: LDO6 for generating UVDD enabled.                                                                                                |
| 3:2          | COMP_TH<1:0> | 0                                     | R/W    | Sets the threshold for the VBUS comparator<br>00: 4.5V<br>01: 3.18V<br>10: 1.5V<br>11: 0.6V                                                                        |
| 1            | SKIP_ENAB    | 0                                     | R/W    | 0: normal operation<br>1: enables the skip mode for the VBUS 1:2 charge pump. This is increasing the efficiency for smaller loads, but increasing the VBUS ripple. |
| 0            | CP_5V_on     | 0                                     | R/W    | 0: disables VBUS charge pump<br>1: enables VBUS charge pump                                                                                                        |

## 7.4.14 Auxiliary Oscillator

### 7.4.14.1 General

This block is a low power oscillator, which can provide a clock to the digital core. CLK\_OUT pad of the AFE is connected to clk\_int pad of the digital die.

### 7.4.14.2 Register Description

Table 138 CLOCK\_OUT Register

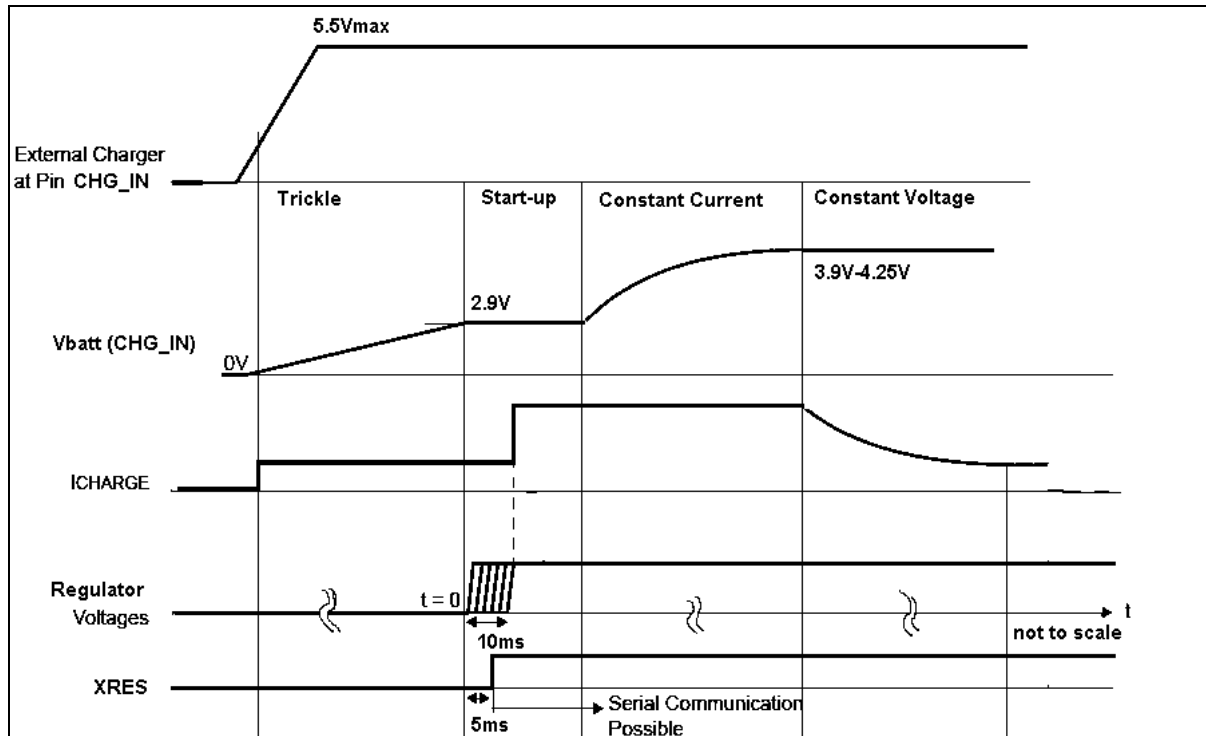
| Name         |                   | Base                                  |        | Default                                                                                                                                          |
|--------------|-------------------|---------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| CLOCK_OUT    |                   | I2C audio master                      |        | 0x00                                                                                                                                             |
| Offset: 0x1D |                   | Clock Output Register                 |        |                                                                                                                                                  |
|              |                   | This register is reset at a DVDD-POR. |        |                                                                                                                                                  |
| Bit          | Bit Name          | Default                               | Access | Bit Description                                                                                                                                  |
| 7..5         |                   | 000                                   | n/a    |                                                                                                                                                  |
| 4:3          | CLKOUT_mode<1:0>  | 00                                    | R/W    | CLKOUT pin frequency divider<br><b>00: oscillator frequency direct mode</b><br>01: osc freq. divide by 2<br>10: osc freq. divide by 4<br>11: OFF |
| 2:1          | CLKOUT_drive<1:0> | 00                                    | R/W    | CLKOUT pin driver strength adjustment<br><b>00: 4mA PushPull</b><br>01: 2mA PushPull<br>10: 1mA PushPull<br>11: 0.5mA PushPull                   |
| 0            | OSC_pd            | 0                                     | R/W    | <b>0: 24MHz oscillator enabled</b><br>1: 24MHz oscillator in power down                                                                          |

## 7.4.15 Charger

### 7.4.15.1 General

This block can be used to charge a 4V Li-Io accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (50 to 400mA) and maximum charging voltage (3.9 to 4.25V).

Figure 57 Charger States



### 7.4.15.2 Trickle Charge

If the battery voltage is below 3V, the charger goes automatically in trickle charge mode with 50mA charging current and 3.9V endpoint voltage. In this mode charging current and voltage are not precise, but provide a charger function also for deep discharged batteries. The temperature supervision is not enabled in trickle charge mode.

### 7.4.15.3 Temperature Supervision

This charger block also features a 15uA supply for an external 100k NTC resistor to measure the battery temperature while charging. If the temperature is too high, an interrupt can be generated.

## 7.4.15.4 Parameter

Table 139 Charger Parameter

| Symbol                  | Parameter                                 | Notes                            | Min                       | Typ                     | Max                       | Unit |
|-------------------------|-------------------------------------------|----------------------------------|---------------------------|-------------------------|---------------------------|------|
| I <sub>CHG_trick</sub>  | Charging Current (trickle charge)         | BVDD ≤ 3V, CHG_IN = 5.5V         | 37                        | 68                      | 111                       | mA   |
|                         |                                           | BVDD ≤ 3V, CHG_IN = 4.0V         | 17                        | 32                      | 55                        | mA   |
| V <sub>CHG_trick</sub>  | Charger Endpoint Voltage (trickle charge) | BVDD ≤ 3V, CHG_IN = 4.4V         | 0.70*<br>CHG_IN           | 0.72*<br>CHG_IN         | 0.74*<br>CHG_IN           | V    |
| I <sub>CHG</sub> (0-7)  | Charging Current                          | BVDD > 3V                        | I <sub>NOM</sub><br>-20%  | I <sub>NOM</sub>        | I <sub>NOM</sub><br>+20%  | mA   |
| V <sub>CHG</sub> (0-7)  | Charging Voltage                          | BVDD > 3V, end of charge is true | V <sub>NOM</sub><br>-50mV | V <sub>NOM</sub>        | V <sub>NOM</sub><br>+30mV | V    |
| V <sub>ON_ABS</sub>     | Charger On Voltage IRQ                    | BVDD = 3V                        |                           | 3.1                     | 4.0                       | V    |
| V <sub>ON_REL</sub>     | Charger On Voltage IRQ                    | CHG_IN-CHG_OUT                   |                           | 170                     | 240                       | mV   |
| V <sub>OFF_REL</sub>    | Charger Off Voltage IRQ                   | CHG_IN-CHG_OUT                   | 40                        | 77                      |                           | mV   |
| V <sub>BATEMP_ON</sub>  | Battery Temp. high level (55°C)           | BVDD > 3V                        | 380                       | 400                     | 420                       | mV   |
| V <sub>BATEMP_OFF</sub> | Battery Temp. low level (50°C)            | BVDD > 3V                        | 480                       | 500                     | 520                       | mV   |
| I <sub>CHG_OFF</sub>    | End Of Charge current level               | BVDD > 3V                        | 5%<br>I <sub>NOM</sub>    | 10%<br>I <sub>NOM</sub> | 15%<br>I <sub>NOM</sub>   | mA   |
| I <sub>REV_OFF</sub>    | Reverse current shut down                 | BVDD = 5V, CHG_IN open           | 160                       | 336                     | 420                       | nA   |

BVDD=3.6V; T<sub>amb</sub>=25°C; unless otherwise specified

## 7.4.15.5 Register Description

Charger Related Register

| Name       | Base             | Offset | Description                                                                          |
|------------|------------------|--------|--------------------------------------------------------------------------------------|
| IRQ_ENRD_0 | I2C audio master | 0x25   | Enable/disable EOC and battery over-temperature interrupt<br>Read out charger status |

Table 140 Charger Register

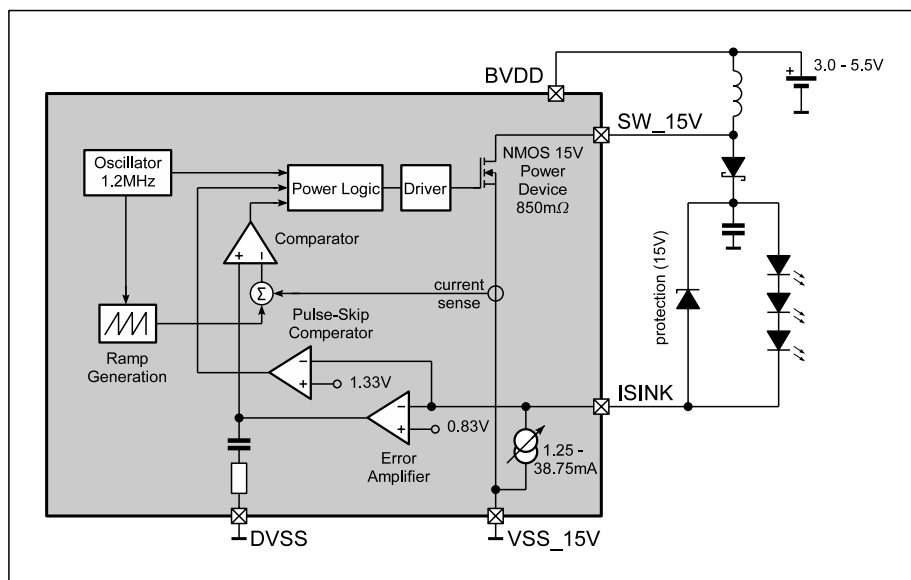
| Name         |            | Base                                  |        | Default                                                                                       |
|--------------|------------|---------------------------------------|--------|-----------------------------------------------------------------------------------------------|
| Charger      |            | I2C audio master                      |        | 0x00                                                                                          |
| Offset: 0x22 |            | Charger Register                      |        |                                                                                               |
|              |            | This register is reset at a DVDD-POR. |        |                                                                                               |
| Bit          | Bit Name   | Default                               | Access | Bit Description                                                                               |
| 7            | TMPSup_off | 0                                     | R/W    | 0: enables 15uA supply for external 100k NTC resistor<br>1: disables supply                   |
| 6:4          | CHG_I      | 000                                   | R/W    | set maximum charging current<br>111: 400 mA<br>110: 350 mA<br>..<br>001: 100 mA<br>000: 50 mA |
| 3:1          | CHG_V      | 000                                   | R/W    | set maximum charger voltage<br>111: 4.25 V<br>110: 4.2 V<br>..<br>001: 3.95 V<br>000: 3.9 V   |
| 0            | CHG_OFF    | 0                                     | R/W    | 0: enables Charger<br>1: disables Charger                                                     |

## 7.4.16 15V Step-Up Converter

### 7.4.16.1 General

The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 15V. A constant switching-frequency results in a low noise on supply and output voltages. When using an additional transistor the output voltage can be up to 25V to drive 6 white LED in series.

It has an adjustable sink current (1.25 to 38.75mA) to provide e.g. dimming function when driving white LEDs as back-light.



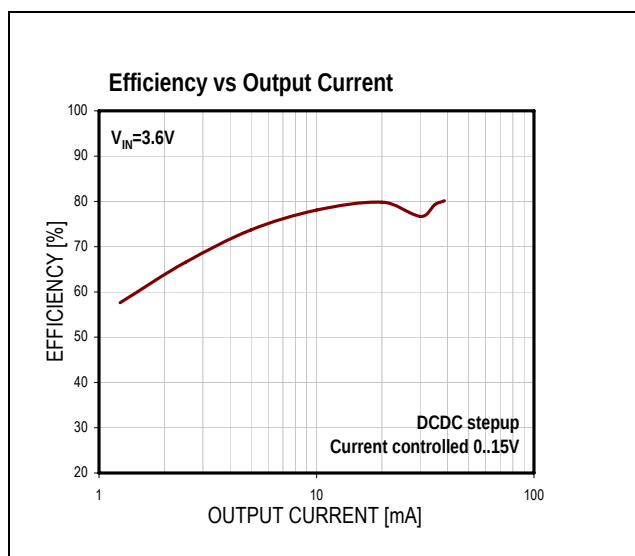
### 7.4.16.2 Parameter

Table 141 15V Step-Up Converter Parameter

| Symbol                 | Parameter                           | Notes                                                                               | Min  | Typ  | Max  | Unit |
|------------------------|-------------------------------------|-------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>SW</sub>        | High Voltage Pin                    | Pin SW15                                                                            | 0    |      | 15   | V    |
| I <sub>VDD</sub>       | Quiescent Current                   | Pulse Skipping mode                                                                 |      | 140  |      | μA   |
| V <sub>FB</sub>        | Feedback Voltage, Transient         | Pin ISINK                                                                           | 0    |      | 5.5  | V    |
| V <sub>FB</sub>        | Feedback Voltage, during Regulation | Pin ISINK                                                                           | 0.65 | 0.83 | 1.0  | V    |
| I <sub>SW_MAX</sub>    | Current Limit                       | V15_ON = 1                                                                          | 350  | 510  | 750  | mA   |
| R <sub>SW</sub>        | Switch Resistance                   | V15_ON = 0                                                                          |      | 0.85 | 1.54 | Ω    |
| I <sub>LOAD</sub>      | Load Current                        | @ 15V output voltage                                                                | 0    |      | 45   | mA   |
| V <sub>PULSESKIP</sub> | Pulse-skip Threshold                | Voltage at pin ISINK, pulse skips are introduces when load current becomes too low. | 1.2  | 1.33 | 1.5  | V    |
| F <sub>IN</sub>        | Fixed Switching Frequency           |                                                                                     | 0.5  | 0.55 | 0.6  | MHz  |
| C <sub>OUT</sub>       | Output Capacitor                    | Ceramic                                                                             |      | 1    |      | μF   |
| L (Inductor)           | I <sub>LOAD</sub> > 20mA            | Use inductors with small C <sub>PARASITIC</sub> (<100pF) for high efficiency        | 17   | 22   | 27   | μH   |
|                        | I <sub>LOAD</sub> < 20mA            |                                                                                     | 8    | 10   | 27   |      |
| t <sub>MIN_ON</sub>    | Minimum On-Time                     |                                                                                     | 90   |      | 180  | ns   |
| MDC                    | Maximum Duty Cycle                  | Guaranteed per design                                                               | 88   | 91   | 94   | %    |

BVDD=3.6V; T<sub>amb</sub>=25°C; unless otherwise specified

Figure 58 15V Step-Up Performance Characteristics



### 7.4.16.3 Register Description

Table 142 DCDC15 Register

| Name         |             | Base                                  |        | Default                                                                                                                                                             |
|--------------|-------------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DCDC15       |             | I2C audio master                      |        | 0x00                                                                                                                                                                |
| Offset: 0x23 |             | 15V DCDC Register                     |        |                                                                                                                                                                     |
|              |             | This register is reset at a DVDD-POR. |        |                                                                                                                                                                     |
| Bit          | Bit Name    | Default                               | Access | Bit Description                                                                                                                                                     |
| 7:5          |             | 000                                   | n/a    |                                                                                                                                                                     |
| 4:0          | I_V15<4..0> | 00000                                 | R/W    | defines the current through the LED = 1.25mA * I_V15<br><b>00000: DCDC15 switched off</b><br>00001: 1.25mA<br>00010: 2.5mA<br>..<br>11110: 37.5mA<br>11111: 38.75mA |

## 7.4.17 Supervisor

### 7.4.17.1 General

This supervisor function can be used for automatic detection of BVDD brown out or junction over-temperature condition.

### 7.4.17.2 BVDD Supervision

The supervision level can be set in 8 steps @ 60mV from 2.74 to 3.16V. If the level is reached an interrupt can be generated. If BVDD reaches 2.6V the AFE shuts down automatically.

### 7.4.17.3 Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to -15°C). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20°C higher. If the IRQ level is set to 120°C the shutdown is disabled.

### 7.4.17.4 Register Description

Table 143 Supervisor Related Register

| Name       | Base             | Offset | Description                                   |
|------------|------------------|--------|-----------------------------------------------|
| IRQ_ENRD_0 | I2C audio master | 0x25   | Enable/disable battery brown out interrupt    |
| IRQ_ENRD_1 | I2C audio master | 0x26   | Enable/disable junction temperature interrupt |

Table 144 Supervisor Register

| Name         |               | Base                                  |        | Default                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
|--------------|---------------|---------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|--------------|-------|-------|-------|---|---|---|---|---|---|-------|-------|-------|-------|-------|-------|
| Supervisor   |               | I2C audio master                      |        | 0x00                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| Offset: 0x24 |               | Supervisor Register                   |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
|              |               | This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| Bit          | Bit Name      | Default                               | Access | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| 7:5          | BVDD_Sup<2:0> | 000                                   | R/W    | supervision of BVDD brown out<br>V_BrownOut=2.74+x*60mV<br><b>000: 2.74V</b><br>001: 2.80V<br>...<br>110: 3.10V<br>111: 3.16V                                                                                                                                                                                                                                                                                                                                           |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| 4:0          | JT_Sup<4:0>   | 00000                                 | R/W    | junction temperature supervision:<br>Temp_ShutDown=140-x*5°C<br>Temp_IRQ=120-x*5°C<br>JT_Sup   IRQ   Shutdown<br><table><tr><td><b>00000</b></td><td><b>120°C</b></td><td><b>140°C</b></td></tr><tr><td>00001</td><td>115°C</td><td>135°C</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td><td>.</td></tr><tr><td>11110</td><td>-30°C</td><td>-10°C</td></tr><tr><td>11111</td><td>-35°C</td><td>-15°C</td></tr></table> <b>(Off for C21020)</b> | <b>00000</b> | <b>120°C</b> | <b>140°C</b> | 00001 | 115°C | 135°C | . | . | . | . | . | . | 11110 | -30°C | -10°C | 11111 | -35°C | -15°C |
| <b>00000</b> | <b>120°C</b>  | <b>140°C</b>                          |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| 00001        | 115°C         | 135°C                                 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| .            | .             | .                                     |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| .            | .             | .                                     |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| 11110        | -30°C         | -10°C                                 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |
| 11111        | -35°C         | -15°C                                 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |              |              |              |       |       |       |   |   |   |   |   |   |       |       |       |       |       |       |

## 7.4.18 Interrupt Generation

### 7.4.18.1 General

All interrupt sources can get enabled or disabled by corresponding bits in the 3 IRQ-bytes. By default no IRQ source is enabled.

The IRQ output can get configured to be PUSH/PULL or OPEN\_DRAIN and ACTIVE\_HIGH or ACTIVE\_LOW with 2 bits in IRQ\_ENRD\_2 register (0x27). Default state is open drain and active\_low.

### 7.4.18.2 IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

#### 7.4.18.3 LEVEL

The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled

#### 7.4.18.4 EDGE

The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

### 7.4.18.5 STATUS CHANGE

The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.

#### 7.4.18.6 De-bouncer

There is a de-bounc function implemented for USB and CHARGER. Since these 2 signals can be unstable for the phase of plug-in or unplug, a de-bounce time of 512ms/256ms/128ms can be selected by 2 bits in the IRQ\_ENRD2 register (0x27h).

Table 145 First Interrupt Register

| Name         |                     | Base                                                                                                                                                                                                                                                                                                              |        | Default                                                                                                                                                                                                                          |
|--------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IRQ_ENRD_0   |                     | I2C audio master                                                                                                                                                                                                                                                                                                  |        | 0x00                                                                                                                                                                                                                             |
| Offset: 0x25 |                     | First Interrupt Register                                                                                                                                                                                                                                                                                          |        |                                                                                                                                                                                                                                  |
|              |                     | Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                                  |
| Bit          | Bit Name            | Default                                                                                                                                                                                                                                                                                                           | Access | Bit Description                                                                                                                                                                                                                  |
| 7            | CHG_tmphigh (level) | 0                                                                                                                                                                                                                                                                                                                 | W      | battery over-temperature interrupt setting<br><b>0: disable</b><br>1: enable<br>The interrupt must not be enabled if the charger block and battery temperature supervision is disabled                                           |
|              |                     | x                                                                                                                                                                                                                                                                                                                 | R      | Battery over-temperature interrupt reading<br>0: battery temperature below 55°C<br>1: battery temperature was too high and the charger was turned off. The charger will be turned on again, when the temperature gets below 50°C |
| 6            | CHG_endofch (edge)  | 0                                                                                                                                                                                                                                                                                                                 | W      | Battery end of charge interrupt setting<br><b>0: disable</b><br>1: enable<br>The interrupt must not be enabled if the charger block is disabled                                                                                  |
|              |                     | x                                                                                                                                                                                                                                                                                                                 | R      | Battery end of charge interrupt reading<br>0: battery charging in progress<br>1: charging is complete, turn charger off<br>To check end of charge again the charger has to be turned on.                                         |
| 5            | CHG_status          | x                                                                                                                                                                                                                                                                                                                 | R      | 0: no charger input source connected<br>1: charger input source connected, also valid if charger is connected during wakeup                                                                                                      |

| Name         |                                | Base                                                                                                                                                                                                                                                                                                              |        | Default                                                                                                                                                                                                                                                          |
|--------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IRQ_ENRD_0   |                                | I2C audio master                                                                                                                                                                                                                                                                                                  |        | 0x00                                                                                                                                                                                                                                                             |
| Offset: 0x25 |                                | First Interrupt Register                                                                                                                                                                                                                                                                                          |        |                                                                                                                                                                                                                                                                  |
|              |                                | Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                                                                  |
| Bit          | Bit Name                       | Default                                                                                                                                                                                                                                                                                                           | Access | Bit Description                                                                                                                                                                                                                                                  |
| 4            | CHG_changed<br>(status change) | 0                                                                                                                                                                                                                                                                                                                 | W      | Charger input status change interrupt setting<br><b>0: disable</b><br>1: enable enables an interrupt on a low to high or high to low change of CHG_IN pin. The thresholds are set in                                                                             |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Charger input status change interrupt reading<br>0: charger input status not changed<br>1: charger input status changed, check CHG_status                                                                                                                        |
| 3            | USB_status                     | x                                                                                                                                                                                                                                                                                                                 | R      | 0: no USB input connected<br>1: USB input connected, also valid if USB is connected during wakeup                                                                                                                                                                |
| 2            | USB_changed<br>(status change) | 0                                                                                                                                                                                                                                                                                                                 | W      | USB input status change interrupt setting<br><b>0: disable</b><br>1: enables an interrupt on a low to high or high to low change of VBUS pin. The threshold can be set in the USB_UTIL register (0x17)                                                           |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | USB input status change interrupt reading<br>0: USB input status not changed<br>1: USB input status changed, check USB_status                                                                                                                                    |
| 1            | RVDD_waslow<br>(level)         | 0                                                                                                                                                                                                                                                                                                                 | W      | Real time clock supply interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                       |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Real time clock supply interrupt reading<br><b>0: RTC supply o.k.</b><br>1: RTC supply was low, RTC not longer valid<br>The interrupt gets set during power-up even if the interrupt is not enabled. For a valid reading, the interrupt has to be enabled first. |
| 0            | BVDD_islow                     | 0                                                                                                                                                                                                                                                                                                                 | W      | Supervisor BVDD interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                              |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Supervisor BVDD interrupt setting<br>0: BVDD is above brown out level<br>1: BVDD has reached brown out level<br>The threshold can be set in the SUPERVISOR register (0x24)                                                                                       |

Table 146 Second Interrupt Register

| Name         |                                | Base                                                                                                                                                                                                                                                                                                              |        | Default                                                                                                                                                                                                                                                                                        |
|--------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IRQ_ENRD_1   |                                | I2C audio master                                                                                                                                                                                                                                                                                                  |        | 0x00                                                                                                                                                                                                                                                                                           |
| Offset: 0x26 |                                | Second Interrupt Register                                                                                                                                                                                                                                                                                         |        |                                                                                                                                                                                                                                                                                                |
|              |                                | Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                                                                                                                |
| Bit          | Bit Name                       | Default                                                                                                                                                                                                                                                                                                           | Access | Bit Description                                                                                                                                                                                                                                                                                |
| 7            | JTEMP_high<br>(level)          | 0                                                                                                                                                                                                                                                                                                                 | W      | Supervisor junction over-temperature interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                                       |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Supervisor junction over-temperature interrupt reading<br>0: chip temperature below threshold<br>1: chip temperature has reached the threshold<br>The threshold can be set in the SUPERVISOR register (0x24)                                                                                   |
| 6            | LSP_overcurr<br>(level)        | 0                                                                                                                                                                                                                                                                                                                 | W      | Speaker over-current interrupt setting<br><b>0: disable</b><br>1: enable<br>The interrupt must not be enabled if the speaker block is disabled                                                                                                                                                 |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Speaker over-current interrupt reading<br>0: no over-current detected<br>1: speaker over-current detected, speaker amplifier was shut down. The shut-down time can be set in LSP_OUT_R register (0x04)                                                                                         |
| 5            | HPH_overcurr<br>(level)        | 0                                                                                                                                                                                                                                                                                                                 | W      | Headphone over-current interrupt setting<br><b>0: disable</b><br>1: enable<br>The interrupt must not be enabled if the headphone block is disabled                                                                                                                                             |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Headphone over-current interrupt reading<br>0: no over-current detected<br>1: headphone over-current detected, headphone amplifier was shut down. The shut-down time can be set in HPH_OUT_R register (0x02)                                                                                   |
| 4            | I2S_status                     | x                                                                                                                                                                                                                                                                                                                 | R      | 0: no LRCK on I2S interface detected<br>1: LRCK on I2S interface present                                                                                                                                                                                                                       |
| 3            | I2S_changed<br>(status change) | 0                                                                                                                                                                                                                                                                                                                 | W      | I2S input status change interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                                                    |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | I2S input status change interrupt reading<br>0: I2S input status not changed<br>1: I2S input status changed, check I2S_status                                                                                                                                                                  |
| 2            | MIC2_connect<br>(level)        | 0                                                                                                                                                                                                                                                                                                                 | W      | Microphone 2 connect detection interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                                             |
|              |                                | x                                                                                                                                                                                                                                                                                                                 | R      | Microphone 2 connect detection interrupt reading<br>0: no microphone connected to MIC2 input<br>1: microphone connected at MIC2 input.<br>IRQ will be released after enabling the microphone stage.<br>Detecting a microphone during operation has to be done by measuring the supply current. |

|   |                         |   |   |                                                                                                                                                                                                                                                                                                |
|---|-------------------------|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | MIC1_connect<br>(level) | 0 | W | Microphone 1 connect detection interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                                             |
|   |                         | x | R | Microphone 1 connect detection interrupt reading<br>0: no microphone connected to MIC1 input<br>1: microphone connected at MIC1 input.<br>IRQ will be released after enabling the microphone stage.<br>Detecting a microphone during operation has to be done by measuring the supply current. |
| 0 | HPH_connect<br>(level)  | 0 | W | Headphone connect detection interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                                                                                                |
|   |                         | x | R | Headphone connect detection interrupt reading<br>0: no headphone connected<br>1: headphone connected<br>IRQ will be released after enabling the headphone stage.<br>Detecting a headphone during operation is not possible.                                                                    |

Table 147 Third Interrupt Register

| Name         |                       | Base                                                                                                                                                                                                                                                                                                              |        | Default                                                                                                                                                                                                 |
|--------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IRQ_ENRD_2   |                       | I2C audio master                                                                                                                                                                                                                                                                                                  |        | 0x00                                                                                                                                                                                                    |
| Offset: 0x27 |                       | Third Interrupt Register                                                                                                                                                                                                                                                                                          |        |                                                                                                                                                                                                         |
|              |                       | Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR. |        |                                                                                                                                                                                                         |
| Bit          | Bit Name              | Default                                                                                                                                                                                                                                                                                                           | Access | Bit Description                                                                                                                                                                                         |
| 7:6          | T_deb<1:0>            | 00                                                                                                                                                                                                                                                                                                                | R/W    | Sets the USB and Charger connect de-bounce time:<br><b>00: 512ms</b><br>01: 256ms<br>10: 128ms<br>11: not defined                                                                                       |
| 5            | IRQ_Acthigh           | 0                                                                                                                                                                                                                                                                                                                 | R/W    | Sets the active output state of the INTRQ line:<br><b>0: IRQ is active low</b><br>1: IRQ is active high                                                                                                 |
| 4            | IRQ_PushPull          | 0                                                                                                                                                                                                                                                                                                                 | R/W    | Sets the INTRQ output buffer type:<br><b>0: IRQ output is open drain</b><br>1: IRQ output is push pull                                                                                                  |
| 3            | Remote_Det2<br>(edge) | 0                                                                                                                                                                                                                                                                                                                 | W      | Microphone 2 remote key press detection interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                             |
|              |                       | x                                                                                                                                                                                                                                                                                                                 | R      | Microphone 2 remote key press detection interrupt reading<br><b>0: no key press detected</b><br>1: Microphone 2 supply current got increased, remote key press detected -> measure MSUP2 supply current |
| 2            | Remote_Det1<br>(edge) | 0                                                                                                                                                                                                                                                                                                                 | W      | Microphone 1 remote key press detection interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                             |
|              |                       | x                                                                                                                                                                                                                                                                                                                 | R      | Microphone 1 remote key press detection interrupt reading<br>0: no key press detected<br>1: Microphone 1 supply current got increased, remote key press detected -> measure MSUP1 supply current        |
| 1            | RTC_update<br>(edge)  | 0                                                                                                                                                                                                                                                                                                                 | W      | RTC timer interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                                                           |

| Name         |                   | Base                                                                                                                                                                                                                                                                                                              |        | Default                                                                                                                                                                    |
|--------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IRQ_ENRD_2   |                   | I2C audio master                                                                                                                                                                                                                                                                                                  |        | 0x00                                                                                                                                                                       |
| Offset: 0x27 |                   | Third Interrupt Register                                                                                                                                                                                                                                                                                          |        |                                                                                                                                                                            |
|              |                   | Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a DVDD-POR. |        |                                                                                                                                                                            |
| Bit          | Bit Name          | Default                                                                                                                                                                                                                                                                                                           | Access | Bit Description                                                                                                                                                            |
|              |                   | x                                                                                                                                                                                                                                                                                                                 | R      | RTC timer interrupt reading<br>0: not RTC interrupt occurred<br>1: RTC timer interrupt occurred. Selecting minute or second interrupt can be done via RTCT register (0x29) |
| 0            | ADC_EndCon (edge) | 0                                                                                                                                                                                                                                                                                                                 | W      | ADC end of conversion interrupt setting<br><b>0: disable</b><br>1: enable                                                                                                  |
|              |                   | x                                                                                                                                                                                                                                                                                                                 | R      | ADC end of conversion interrupt reading<br>0: ADC conversion not finished<br>1: ADC conversion finished. Read out ADC_0 and ADC_1 register to get the result (0x2E & 0x2F) |

## 7.4.19 Real Time Clock

### 7.4.19.1 General

The real time clock block is an independent block, which is still working even when the chip is shut down. The only condition for this operation is that BVDD has a voltage of above 1.0V. The block uses a standard 32kHz crystal that is connected to a low power oscillator. An internal 32bit second register stores the current time.

The RTC block has special functions for trimming the time base and generating interrupts every second or minute.

### 7.4.19.2 RTC supply

The internal RTC is supplied via the BVDD pin. The block has an internal LDO to generate the RTC supply voltage on RVDD pin. This voltage can be programmed via the RTCV register (0x28h). If the internal RTC is not used, RVDD can be used to supply an external RTC block.

If the supply voltage on BVDD pin rises, the whole chip gets powered up. See also power-up conditions in chapter 7.4.1.2.

### 7.4.19.3 Register Description

Table 148 RTC Related Register

| Name       | Base             | Offset | Description                                                 |
|------------|------------------|--------|-------------------------------------------------------------|
| IRQ_ENRD_0 | I2C audio master | 0x25   | Interrupt settings for RVDD under-voltage detection         |
| IRQ_ENRD_2 | I2C audio master | 0x27   | Interrupt settings for getting a second or minute interrupt |

Table 149 RTCV Register

| Name         |            | Base                                                        |        | Default                                                                                                                                         |
|--------------|------------|-------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| RTCV         |            | I2C audio master                                            |        | 0x23                                                                                                                                            |
| Offset: 0x28 |            | RTC Voltage Register                                        |        |                                                                                                                                                 |
|              |            | This register is reset at a RVDD-POR. (DVDD_POR for C21020) |        |                                                                                                                                                 |
| Bit          | Bit Name   | Default                                                     | Access | Bit Description                                                                                                                                 |
| 7:4          | VRTC<3..0> | 0010                                                        | R/W    | Sets the RTC supply voltage, 16 steps @ 0.1V, default is 1.2V<br>0000: 1V<br>0001: 1.1V<br><b>0010: 1.2V</b><br>...<br>1110: 2.4V<br>1111: 2.5V |
| 3:2          | -          | 00                                                          | n/a    | do not change                                                                                                                                   |
| 1            | RTC_ON     | 1                                                           | R/W    | RTC clock control:<br>0: Disable clock for RTC<br><b>1: Enables clock for RTC</b>                                                               |
| 0            | OSC_ON     | 1                                                           | R/W    | RTC oscillator control:<br>0: Disables RTC oscillator<br><b>1: Enables RTC oscillator</b>                                                       |

Table 150 RTCV Register

| Name         |           | Base                                                        |        | Default                                                                                                                                                                                    |
|--------------|-----------|-------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RTCT         |           | I2C audio master                                            |        | 0x40                                                                                                                                                                                       |
| Offset: 0x29 |           | RTC Timing Register                                         |        |                                                                                                                                                                                            |
|              |           | This register is reset at a RVDD-POR. (DVDD_POR for C21O20) |        |                                                                                                                                                                                            |
| Bit          | Bit Name  | Default                                                     | Access | Bit Description                                                                                                                                                                            |
| 7            | IRQ_MIN   | 0                                                           | R/W    | 0: generates an interrupt every second<br>1: generates an interrupt every minute                                                                                                           |
| 6:0          | TRTC<6:0> | 1000000                                                     | R/W    | Trimming register for RTC, 128 steps @ 7.6ppm<br>000000: 1 (7.6ppm)<br>000001: 2 (15.2ppm)<br>...<br><b>100000: 64 (488ppm)</b><br>...<br>111110: 126 (960.8ppm)<br>111111: 127 (968.4ppm) |

Table 151 RTC\_0 to RTC\_3 Register

| Name                 |           | Base                                  |        | Default                               |
|----------------------|-----------|---------------------------------------|--------|---------------------------------------|
| RTC_0 to RTC_3       |           | I2C audio master                      |        | 0x00 00 00 00                         |
| Offset: 0x2A to 0x2D |           | Unique ID Register                    |        |                                       |
|                      |           | This register is reset at a RVDD-POR. |        |                                       |
| Adr.                 | Byte Name | Default                               | Access | Bit Description                       |
| 0x2A                 | RTC_0     | 0x00                                  | R/W    | RTC<7:0>; RTC seconds bits 0 to 7     |
| 0x2B                 | RTC_1     | 0x00                                  | R/W    | RTC<15:8>; RTC seconds bits 8 to 15   |
| 0x2C                 | RTC_2     | 0x00                                  | R/W    | RTC<23:9>; RTC seconds bits 9 to 23   |
| 0x2D                 | RTC_3     | 0x00                                  | R/W    | RTC<31:24>; RTC seconds bits 24 to 31 |

## 7.4.20 10-Bit ADC

### 7.4.20.1 General

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc... Please note that C21020 is measuring BVDD instead of CHG\_OUT

### 7.4.20.2 Input Sources

Table 152 ADC10 Input Sources

| Nr.    | Source    | Range        | LSB   | Description                                                                 |
|--------|-----------|--------------|-------|-----------------------------------------------------------------------------|
| 0      | CHG_OUT   | 5.120V       | 5mV   | check battery voltage of 4V Lilo accumulator                                |
| 1      | RTCSUP    | 5.120V       | 5mV   | check RTC backup battery voltage (connected to BVDD inside the package)     |
| 2      | VBUS      | 5.120V       | 5mV   | check USB host voltage                                                      |
| 3      | CHG_IN    | 5.120V       | 5mV   | check charger input voltage                                                 |
| 4      | CVDD      | 2.560V       | 2.5mV | check charge pump output voltage                                            |
| 5      | BatTemp   | 2.560V       | 2.5mV | check battery charging temperature                                          |
| 6      | MicSup1   | 2.560V       | 2.5mV | check voltage on MicSup1 for remote control or external voltage measurement |
| 7      | MicSup2   | 2.560V       | 2.5mV | check voltage on MicSup2 for remote control or external voltage measurement |
| 8      | VBE1      | 1.024        | 1mV   | measuring junction temperature                                              |
| 9      | VBE2      | 1.024        | 1mV   | measuring junction temperature                                              |
| 10     | I_MicSup1 | 1.024mA typ. | 1.0uA | check current of MicSup1 for remote control detection                       |
| 11     | I_MicSup2 | 1.024mA typ. | 1.0uA | check current of MicSup2 for remote control detection                       |
| 12     | VBAT      | 2.560V       | 2.5mV | check single cell battery voltage                                           |
| 13..15 | Reserved  | 1.024V       | 1mV   | for testing purpose only                                                    |

#### CHG\_OUT, RTCSUP, VBUS, CHG\_IN

These sources are fed into an 1/5 voltage divider (180kΩ typ.) and further amplified by 2.5.

#### CVDD, BatTemp, MicSup1, MicSup2

These sources are fed directly to the ADC input multiplexer.

#### VBE1, VBE2

These inputs are first amplified by 2.5 and then fed to the ADC input multiplexer.

#### I\_MicSup1, I\_MicSup2

The measurement of the microphone supply LDOs is not very accurate, as the current-voltage conversion is only done by a single resistor which shows wide process and temperature variations. These measurements should be only used for remote function detection.

#### VBAT

This source is divided by 2.5 with a voltage divider (180kΩ typ.) and then amplified by 2.5. This has to be done, as VBAT can represent voltages up to 3.6V. Please note, that the maximum measurement range will be still 2.560V

### 7.4.20.3 Reference

AVDD=2.9V is used as reference to the ADC. AVDD is trimmed to +/-20mV with over all precision of +/-29mV. So the absolute accuracy is +/-1%.

## 7.4.20.4 Parameter

Table 153 ADC10 Parameter

| Symbol             | Parameter                                | Notes                               | Min   | Typ  | Max   | Unit |
|--------------------|------------------------------------------|-------------------------------------|-------|------|-------|------|
| R <sub>DIV</sub>   | Input Divider Resistance                 | CHG_OUT, RTCSUP, VBUS, CHG_IN, VBAT | 138k  | 180k | 234k  | Ω    |
| ADC <sub>FS</sub>  | ADC Full Scale Range                     |                                     | 2.534 | 2.56 | 2.586 | V    |
| Ratio1             | Division Factor 1                        | CHG_OUT, RTCSUP, VBUS, CHG_IN       | 0.198 | 0.2  | 0.202 | 1    |
| Ratio2             | Division Factor 2                        | VBAT                                | 0.396 | 0.4  | 0.404 | 1    |
| Gain               | ADC Gain Stage                           |                                     | 2.475 | 2.5  | 2.525 | V    |
| T <sub>CON</sub>   | Conversion Time                          |                                     | -     | 34   | 50    | μs   |
| I <sub>MICFS</sub> | I <sub>MicSup</sub> 1/2 Full Scale Range |                                     | 0.7   | 1.0  | 1.4   | mA   |

BVDD=3.6V; T<sub>amb</sub>=25°C; unless otherwise specified

## 7.4.20.5 Register Description

Table 154 ADC10 Related Register

| Name       | Base             | Offset | Description                                        |
|------------|------------------|--------|----------------------------------------------------|
| IRQ_ENRD_2 | I2C audio master | 0x27   | Interrupt settings for end of conversion interrupt |

Table 155 ADC\_0 Register

| Name         |            | Base                                                                                                                                            |        | Default                                                                                                                                                                                                                                                                                                                             |
|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC_0        |            | I2C audio master                                                                                                                                |        | 0000 00xx                                                                                                                                                                                                                                                                                                                           |
| Offset: 0x2E |            | First 10-bit ADC Register                                                                                                                       |        |                                                                                                                                                                                                                                                                                                                                     |
|              |            | Writing to this register will start the measurement of the selected source.<br>This register is reset at a DVDD-POR, exception are bit 8 and 9. |        |                                                                                                                                                                                                                                                                                                                                     |
| Bit          | Bit Name   | Default                                                                                                                                         | Access | Bit Description                                                                                                                                                                                                                                                                                                                     |
| 7:4          | ADC_Source | 00000000                                                                                                                                        | R/W    | Selects ADC input source<br><b>0000: CHG_OUT</b><br>0001: RTCSUP<br>0010: VBUS<br>0011: CHG_IN<br>0100: CVDD<br>0101: BatTemp<br>0110: MicSup1<br>0111: MicSup2<br>1000: VBE_1uA<br>1001: VBE_2uA<br>1010: I <sub>MicSup</sub> 1<br>1011: I <sub>MicSup</sub> 2<br>1100: VBAT<br>1101: reserved<br>1110: reserved<br>1111: reserved |
| 3:2          | -          | 00                                                                                                                                              | n/a    | do not change                                                                                                                                                                                                                                                                                                                       |
| 1:0          | ADC<9:8>   | xx                                                                                                                                              | R/W    | ADC result bit 9 to 8                                                                                                                                                                                                                                                                                                               |

Table 156 ADC\_1 Register

| Name         |          | Base                        |        | Default               |
|--------------|----------|-----------------------------|--------|-----------------------|
| ADC_1        |          | I2C audio master            |        | xxxx xxxx             |
| Offset: 0x2F |          | Second 10-bit ADC Register  |        |                       |
|              |          | This register is not reset. |        |                       |
| Bit          | Bit Name | Default                     | Access | Bit Description       |
| 7:0          | ADC<7:0> | xxxx xxxx                   | R/W    | ADC result bit 7 to 0 |

## 7.4.21 128 bit OTP ROM

### 7.4.21.1 General

This fuse array is used to store a unique identification number, which can be used for DRM issues. The number is generated and programmed during the production process.

### 7.4.21.2 Register Description

Table 157 UID\_0 to UID\_15 Register

| Name                 |           | Base                                         |        | Default           |
|----------------------|-----------|----------------------------------------------|--------|-------------------|
| UID_0 to UID_15      |           | I2C audio master                             |        | n/a               |
| Offset: 0x30 to 0x3F |           | Unique ID Register                           |        |                   |
|                      |           | This register is read only and is not reset. |        |                   |
| Adr.                 | Byte Name | Default                                      | Access | Bit Description   |
| 0x30                 | UID_0     | 0x00                                         | R      | Unique ID byte 0  |
| 0x31                 | UID_1     | 0x00                                         | R      | Unique ID byte 1  |
| 0x32                 | UID_2     | 0x00                                         | R      | Unique ID byte 2  |
| 0x33                 | UID_3     | 0x00                                         | R      | Unique ID byte 3  |
| 0x34                 | UID_4     | 0x00                                         | R      | Unique ID byte 4  |
| 0x35                 | UID_5     | 0x00                                         | R      | Unique ID byte 5  |
| 0x36                 | UID_6     | 0x00                                         | R      | Unique ID byte 6  |
| 0x37                 | UID_7     | 0x00                                         | R      | Unique ID byte 7  |
| 0x38                 | UID_8     | n/a                                          | R      | Unique ID byte 8  |
| 0x39                 | UID_9     | n/a                                          | R      | Unique ID byte 9  |
| 0x3A                 | UID_10    | n/a                                          | R      | Unique ID byte 10 |
| 0x3B                 | UID_11    | n/a                                          | R      | Unique ID byte 11 |
| 0x3C                 | UID_12    | n/a                                          | R      | Unique ID byte 12 |
| 0x3D                 | UID_13    | n/a                                          | R      | Unique ID byte 13 |
| 0x3E                 | UID_14    | n/a                                          | R      | Unique ID byte 14 |
| 0x3F                 | UID_15    | n/a                                          | R      | Unique ID byte 15 |

## 7.4.22 2-Wire-Serial Control Interface

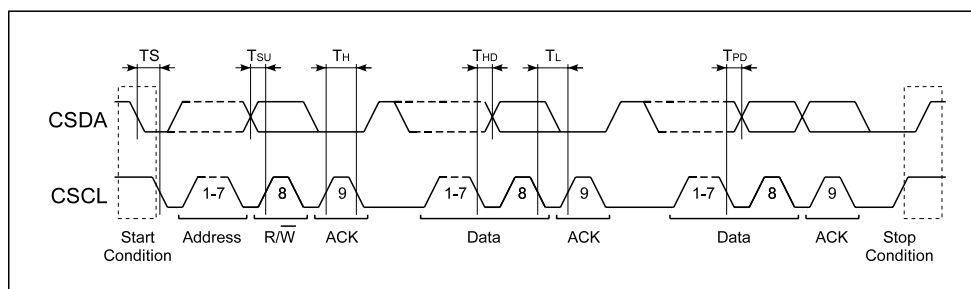
### 7.4.22.1 General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr\_Group8 - audio processors

- 8Ch\_write
- 8Dh\_read

Figure 59 I2C timing



### 7.4.22.2 Parameter

Table 158 I2C Operating Conditions

| Symbol          | Parameter                       | Notes                                                              | Min  | Typ | Max  | Unit |
|-----------------|---------------------------------|--------------------------------------------------------------------|------|-----|------|------|
| V <sub>IL</sub> | Input low voltage               | CSCL, CSDA (max 30%DVDD)                                           | 0    |     | 0.87 | V    |
| V <sub>IH</sub> | Input high voltage              | CSCL, CSDA (min 70%DVDD)                                           | 2.03 |     | 5.5  | V    |
| HYST            | Hysteretic                      | CSCL, CSDA                                                         | 200  | 450 | 800  | mV   |
| V <sub>OL</sub> | Output low voltage              | CSDA @3mA                                                          |      | -   | 0.4  | V    |
| T <sub>sp</sub> | Spike insensitivity             |                                                                    | 50   | 100 |      | ns   |
| T <sub>H</sub>  | Clock high time                 |                                                                    | 500  |     |      | ns   |
| T <sub>L</sub>  | Clock low time                  |                                                                    | 500  |     |      | ns   |
| T <sub>SU</sub> | Data setup time                 | CSDA has to change T <sub>SU</sub> before rising edge of CSCL      | 100  |     |      | ns   |
| T <sub>HD</sub> | Data hold time                  | No hold time needed for CSDA relative to rising edge of CSCL       | 0    |     |      | ns   |
| T <sub>S</sub>  | Clock start-condition hold time | CSCL HIGH hold time relative to CSDA edge for start/stop/rep_start | 200  |     |      | ns   |
| T <sub>PD</sub> | Output delay                    | CSDA propagation delay relative to low going edge of CSCL          | 24   | 50  | 80   | ns   |

DVDD = 2.9V, T<sub>amb</sub> = 25°C; unless otherwise specified

## 7.4.22.3 Register Description

## Registers Overview (00h to 3Fh)

Table 159 I2C Register Overview

| Addr | Name       | D<7>           | D<6>           | D<5>          | D<4>                                                                                          | D<3> | D<2> | D<1> | D<0> |
|------|------------|----------------|----------------|---------------|-----------------------------------------------------------------------------------------------|------|------|------|------|
| 00h  | LINE_OUT_R | reserved       |                | -             | LOR_Vol<4:0><br>Gain from Mixer_Out to Line_Out= (-40.5dB ... +6dB)                           |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 01h  | LINE_OUT_L | LO_SES_DM<1:0> |                | -             | LOL_Vol<4:0><br>Gain from Mixer_Out to Line_Out= (-40.5dB ... +6dB)                           |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 02h  | HPH_OUT_R  | HP_OVC_TO<1:0> |                | -             | HPR_Vol<4:0><br>Gain from Mixer_Out to HPH_Out= (-45.43dB ... +1.07dB)                        |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 03h  | HPH_OUT_L  | HP_Mute_on     | HP_on          | HPdet_on      | HPL_Vol<4:0><br>Gain from Mixer_Out to HPH_Out= (-45.43dB ... +1.07dB)                        |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 04h  | LSP_OUT_R  | SP_OVC_TO<1:0> |                | -             | SPR_Vol<4:0><br>Gain from Mixer_Out to LSP_Out= (-40.5dB ... +6.0dB)                          |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 05h  | LSP_OUT_L  | SP_Mute_on     | SP_on          | -             | SPL_Vol<4:0><br>Gain from Mixer_Out to LSP_Out= (-40.5dB ... +6.0dB)                          |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 06h  | MIC1_R     | Mic1_AGC_off   | Mic1_Gain<1:0> |               | Mic1R_Vol<4:0><br>Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)                      |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 07h  | MIC1_L     | Mic1_Sup_off   | Mic1_Mute_off  | -             | Mic1L_Vol<4:0><br>Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)                      |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 08h  | MIC2_R     | Mic2_AGC_off   | Mic2_Gain<1:0> |               | Mic2R_Vol<4:0><br>Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)                      |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 09h  | MIC2_L     | Mic2_Sup_off   | Mic2_Mute_off  | -             | Mic2L_Vol<4:0><br>Gain from MicAmp_Out to Mixer_In= (-40.5dB ... +6.0dB)                      |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 0Ah  | Line_IN1_R | -              | -              | LI1R_Mute_off | LI1R_Vol<4:0><br>Gain from LineIn_Pin to Mixer_In= -34.5dB+LI1R_VOL*1.5dB (-34.5dB ... +12dB) |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 0Bh  | Line_IN1_L | LI1_Mode<1:0>  |                | LI1L_Mute_off | LI1L_Vol<4:0><br>Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)                        |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 0Ch  | Line_IN2_R | -              | -              | LI2R_Mute_off | LI2R_Vol<4:0><br>Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)                        |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 0Dh  | Line_IN2_L | LI2_Mode<1:0>  |                | LI2L_Mute_off | LI2L_Vol<4:0><br>Gain from LineIn_Pin to Mixer_In= (-34.5dB ... +12dB)                        |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |
| 0Eh  | DAC_R      | -              | -              | -             | DAR_Vol<4:0><br>Gain from DAC_Out to Mixer_In= (-40.5dB ... +6dB)                             |      |      |      |      |
|      |            | 0              | 0              | 0             | 0                                                                                             | 0    | 0    | 0    | 0    |

| Addr | Name       | D<7>                | D<6>            | D<5>            | D<4>                                                                | D<3>            | D<2>              | D<1>            | D<0>              |
|------|------------|---------------------|-----------------|-----------------|---------------------------------------------------------------------|-----------------|-------------------|-----------------|-------------------|
| 0Fh  | DAC_L      | -                   | DAC_Mute_off    | -               | DAL_Vol<4:0><br>Gain from DAC_Out to Mixer_In= (-40.5dB ... +6dB)   |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 10h  | ADC_R      | ADCmux<1:0>         |                 | -               | ADR_Vol<4:0><br>Gain from ADCMux_Out to ADC_In= (-34.5dB ... +12dB) |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 11h  | ADC_L      | AD_FS2              | ADC_Mute_off    | -               | ADL_Vol<4:0><br>Gain from ADCMux_Out to ADC_In= (-34.5dB ... +12dB) |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 14h  | AudioSet1  | ADC_on              | SUM_on          | DAC_on          | LOUT_on                                                             | LIN2_on         | LIN1_on           | MIC2_on         | MIC1_on           |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 15h  | AudioSet2  | BIAS_off            | DITH_off        | AGC_off         | IBR_DAC<1:0>                                                        |                 | LSP_LP            | IBR_LSP<1:0>    |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 16h  | AudioSet3  | -                   | -               | -               | -                                                                   | -               | ZCU_OFF           | IBR_HPH         | HPCM_off          |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 17h  | USB_UTIL   | -                   | -               | -               | LDO6_on                                                             | COMP_TH<1:0>    |                   | SKIP_ENAB       | CP_5V_on          |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 1Dh  | CLOCK_OUT  | -                   | -               | -               | CLK_OUT_mode<1:0>                                                   |                 | CLKOUT_drive<1:0> |                 | OSC_pd            |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 20h  | SYSTEM     | Design_Version<3:0> |                 |                 |                                                                     | PVDDp           | IOVDDp            | EnWDogPw<br>dn  | PwrUPHId          |
|      |            | 0                   | 0               | 1               | 0                                                                   | 0               | 0                 | 0               | 1                 |
| 21h  | CVDD/DCDC3 | CP_SW               | CP_on           | LREG_C<br>P_not | DCDC3p<1:0>                                                         |                 | LREG_off          | CVDDp<1:0>      |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 22h  | CHARGER    | TmpSup_off          | CHGI<2:0>       |                 |                                                                     | CHGV<2:0>       |                   |                 | CHG_off           |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 23h  | DCDC15     | -                   | I_V15<4:0>      |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 24h  | SUPERVISOR | BVDD_Sup<2:0>       |                 |                 | JT_Sup<4:0>                                                         |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 25h  | IRQ_ENRD0  | CHG<br>tmphigh      | CHG<br>endofch  | CHG<br>status   | CHG<br>changed                                                      | USB<br>status   | USB<br>changed    | RVDD<br>was low | BVDD<br>Is low    |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 26h  | IRQ_ENRD1  | JTEMP<br>high       | LSP<br>overcurr | HPH<br>overcurr | I2S<br>status                                                       | I2S<br>changed  | Mic2<br>connect   | Mic1<br>connect | HeadPh<br>Connect |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 27h  | IRQ_ENRD2  | T_deb<1:0>          |                 | IRQ_ActH<br>igh | IRQ_PushP<br>ull                                                    | Remote_Det<br>2 | Remote_D<br>et1   | RTC_Updat<br>e  | ADC_EndCo<br>n    |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 28h  | RTCV       | VRTC<3:0>           |                 |                 |                                                                     | -               | RTC_ON            |                 | OSC_ON            |
|      |            | 0                   | 0               | 1               | 0                                                                   | 0               | 0                 | 1               | 1                 |
| 29h  | RTCT       | IRQ_MIN             | TRTC<6:0>       |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 1               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 2Ah  | RTC_0      | RTC<7:0>            |                 |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 2Bh  | RTC_1      | RTC<15:8>           |                 |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 2Ch  | RTC_2      | RTC<23:16>          |                 |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 2Dh  | RTC_3      | RTC<31:24>          |                 |                 |                                                                     |                 |                   |                 |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | 0               | 0                 |
| 2Eh  | ADC_0      | ADC_Source<3:0>     |                 |                 |                                                                     | -               | -                 | ADC<9:8>        |                   |
|      |            | 0                   | 0               | 0               | 0                                                                   | 0               | 0                 | X               | X                 |

| Addr  | Name        | D<7>        | D<6> | D<5> | D<4> | D<3> | D<2> | D<1> | D<0> |
|-------|-------------|-------------|------|------|------|------|------|------|------|
| 2Fh   | ADC_1       | ADC<7:0>    |      |      |      |      |      |      |      |
|       |             | X           | X    | X    | X    | X    | X    | X    | X    |
| 30-3F | UID_0 .. 15 | ID<7:0>     |      |      |      |      |      |      |      |
|       |             | ...         |      |      |      |      |      |      |      |
|       |             | ID<127:120> |      |      |      |      |      |      |      |

## 8 Pinout and Packaging

### 8.1 Package Variants

CTBGA (Thin ChipArray BGA) package technology is used for multi-chip-module (MCM) packaging. The following package variants are available for the product:

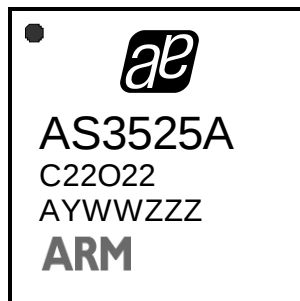
Table 160 Package Options

| Product Code | Package | Balls | Ball Matrix  | Pitch [mm] | Height [mm] | Size [mm] | Application                   |
|--------------|---------|-------|--------------|------------|-------------|-----------|-------------------------------|
| AS3525-A     | CTBGA   | 224   | 15x15, 7 Row | 0.8        | 1.2         | 13x13     | with external SDRAM interface |
| AS3525-B     | CTBGA   | 144   | 12x12, full  | 0.8        | 1.2         | 10x10     | w/o external SDRAM interface  |

### 8.2 CTBGA224 Package Drawings

#### 8.2.1 Marking

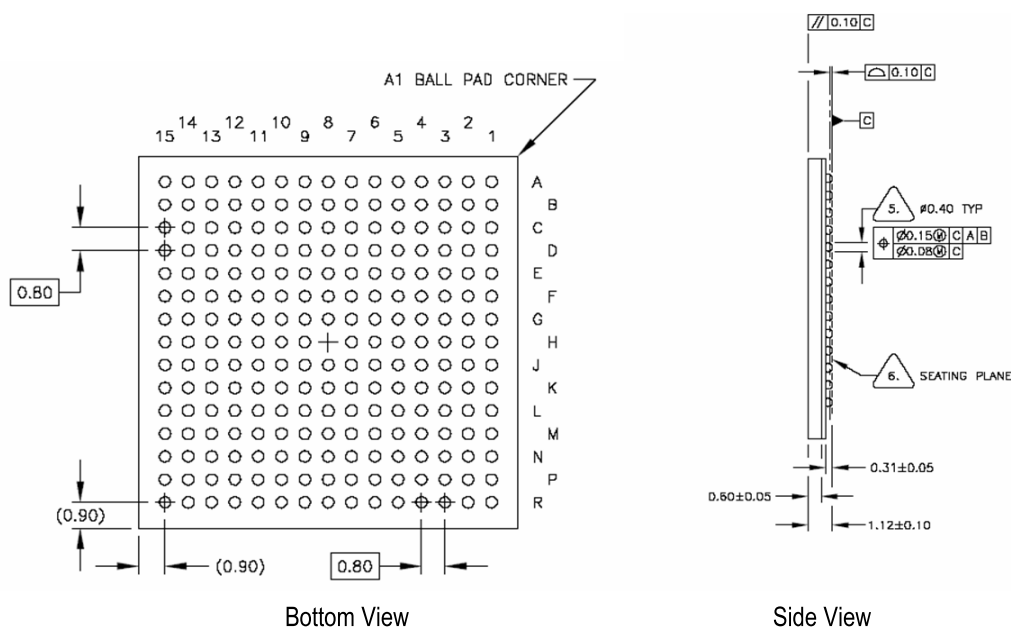
Figure 60 CTBGA224 Package Marking



Package Code AYYWWZZZ

| A                 | Y    | WW                              | ZZZ         |
|-------------------|------|---------------------------------|-------------|
| A ... for PB free | Year | working week assembly/packaging | Free choice |

Figure 61 CTBGA224 Package Drawing



## 8.2.2 CTBGA224 Package Ball-out

Figure 62 AS3525A Package Ball-out

|   | 1             | 2                | 3             | 4           | 5            | 6             | 7             | 8            | 9             | 10          | 11           | 12       | 13        | 14       | 15        |
|---|---------------|------------------|---------------|-------------|--------------|---------------|---------------|--------------|---------------|-------------|--------------|----------|-----------|----------|-----------|
| A | jtag_tms      | xpc_7            | xpc_3         | xpa_2       | mpmc_addr_3  | mpmc_addr_9   | mpmc_addr_17  | mpmc_cas_n   | mpmc_bls_n_0  | mpmc_data_5 | mpmc_data_13 | ide_ha_0 | naf_d_1   | dbop_d14 | vdd_peri  |
| B | jtag_tdi      | jtag_tck         | xpc_5         | xpa_0       | mpmc_addr_1  | mpmc_addr_11  | mpmc_addr_19  | vss_mem      | vdd_mem       | mpmc_data_7 | mpmc_data_15 | naf_d_7  | naf_d_4   | naf_d_2  | vss_peri  |
| C | i2si_sdata_in | jtag_trst_n      | xpc_6         | xpc_1       | xpa_6        | mpmc_addr_7   | mpmc_addr_15  | vss_mem      | vdd_mem       | mpmc_data_9 | ssp_issout   | naf_d_5  | naf_d_0   | naf_d_8  | dbop_d15  |
| D | i2si_lrck_out | tmsel            | jtag_tdo      | xpc_4       | xpa_4        | mpmc_addr_5   | mpmc_addr_13  | mpmc_dqm_0   | mpmc_stcs_n_0 | mpmc_oe_n   | ssp_rxd      | ide_ha_2 | naf_d_3   | naf_d_14 | naf_d_11  |
| E | clk_ext       | clk_sel          | i2si_sclk_out | i2si_mclk   | xpc_0        | mpmc_addr_8   | mpmc_addr_14  | mpmc_clk_0   | mpmc_dycs_n_1 | mpmc_data_1 | mpmc_data_11 | naf_d_9  | naf_d_13  | naf_d_15 | naf_oe0_n |
| F | id_dig        | usb_vdda33t      | VBUS          | xpc_2       | xpa_7        | mpmc_addr_6   | mpmc_addr_16  | mpmc_cke_0   | mpmc_we_n     | mpmc_data_3 | naf_d_10     | naf_d_12 | naf_ale   | naf_cle  | naf_bsy_n |
| G | usb_dp        | usb_vssa33t      | dbop_d12      | xpa_1       | mpmc_addr_0  | mpmc_addr_18  | mpmc_clk_1    | mpmc_data_10 | mpmc_data_12  | ide_reset_n | naf_d_6      | naf_wp_n | naf_oe3_n | naf_we_n | xpd_3     |
| H | usb_drm       | usb_vssa33t      | dbop_d13      | xpa_3       | mpmc_addr_10 | mpmc_addr_20  | mpmc_data_8   |              | ssp_clkout    | ide_ha_1    | naf_ce1_n    | naf_re_n | xpd_0     | xpd_4    | xpd_7     |
| J | usb_vssa33c   | usb_rkelvin_rext | usb_vdda33c   | xpa_5       | mpmc_addr_12 | mpmc_cke_1    | mpmc_ras_n    | mpmc_data_6  | mpmc_data_14  | ssp_bxd     | naf_ce2_n    | xpd_1    | xpd_2     | xpd_5    | xpd_6     |
| K | vdd_core      | nc               | DVDD          | nc          | mpmc_addr_4  | mpmc_dycs_n_0 | mpmc_bls_n_1  | mpmc_data_4  | xpb_4         | xpb_3       | xpb_2        | xpb_5    | xpb_7     | SW_15V   | SW_3V     |
| L | vss_core      | nc               | PwrUP         | mpmc_addr_2 | mpmc_fbclk_n | mpmc_dqm_1    | mpmc_stcs_n_1 | mpmc_data_0  | mpmc_data_2   | xpb_0       | xpb_1        | xpb_6    | CN_5V     | CP_5V    | VSS_3V    |
| M | CLK_OUT       | XRES             | CSDA          | CSCL        | MCLK         | SDI           | SDO           | VREF         | HPCM          | BATTEMP     | ISINK        | VSS_15V  | VBAT_1V   | QLDO2    | VSS_1V    |
| N | INTRQ         | P_PVDD           | MSUP2         | LOUTR       | LRCK         | SCLK          | LOUTL         | AVDD         | HPGND         | HPR         | BGND         | BVSS2    | HPL       | CHG_IN   | CN_1V     |
| P | DVSS          | LIN2R            | LIN1R         | MIC2_N      | MIC1_N       | MSUP1         | BVSS          | AGND         | BVDD          | BVDD        | BVDD         | IOVDD    | RVDD      | CHG_OUT  | CP_1V     |
| R | XIN_24M       | XOUT_24M         | LIN2L         | LIN1L       | MIC2_P       | MIC1_P        | AVSS          | BVSS         | LSPR          | LSPL        | UVDD         | PVDD     | XIN_32k   | XOUT_32k | CVDD      |

**Note:** PINs K2, L2 and K4 are reserved for production test purposes and must be left not connected for normal operation mode.

## 8.2.3 CTBGA224 Ball List

Table 161 CTBGA224 Ball List

| Ball Nr.<br>BGA224 | Ball Name          | PAD Type      | I/O    | Ball Description                                                                                            |
|--------------------|--------------------|---------------|--------|-------------------------------------------------------------------------------------------------------------|
| M2                 | XRES<br>resetext_n | DO<br>D IN ST | O<br>I | XRES is generated by the PMU subsystem and connected to reset input (active low) on the BGA                 |
| M1                 | CLK_OUT<br>clk_int | DO<br>D IN ST | O<br>I | CLK_OUT is output of 20-24MHz crystal oscillator clock and connected to clk_int on the BGA                  |
| E1                 | clk_ext            | D IN ST PD    | I      | external clock input (10-26MHz)                                                                             |
| E2                 | clk_sel            | D IN ST PD    | I      | clock select<br>0 (low): clock from internal oscillator is used<br>1 (high): clock from pad clk_ext is used |
| D2                 | tmsel              | D IN ST PD    | I      | test mode select<br>For testing purpose only, has to be set to "0".                                         |
| F1                 | id_dig             | D IN ST (PU)  | I      | USB mini receptacle identifier<br>Has to be connected to USB jack ID pin.                                   |

| Ball Nr.<br>BGA224 | Ball Name                        | PAD Type       | I/O | Ball Description                                                                                                                                                                                                                |
|--------------------|----------------------------------|----------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | Port A                           |                |     |                                                                                                                                                                                                                                 |
| B4                 | xpa[0]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| G4                 | xpa[1]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| A4                 | xpa[2]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| H4                 | xpa[3]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| D5                 | xpa[4]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| J4                 | xpa[5]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| C5                 | xpa[6]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
| F5                 | xpa[7]                           | D IO ST PD LSR | IO  | GPIO IO, Port A                                                                                                                                                                                                                 |
|                    | Port B / DISPLAY / UART          |                |     |                                                                                                                                                                                                                                 |
| L10                | xpb[0]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | mPMC_stcs1mw[0]*                 |                | I   | static memory chip memory width setting for boot loader<br>0: 8 bit data bus<br>1: 16 bit data bus<br>The value is latched at reset.                                                                                            |
|                    | dbop_c0                          |                | O   | DISPLAY control output                                                                                                                                                                                                          |
| L11                | xpb[1]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | mPMC_stcs1pol*                   |                | I   | static memory chip select polarity setting for boot loader<br>0: active LOW chip select<br>1: active high chip select<br>The value is latched at reset.                                                                         |
|                    | dbop_c1                          |                | O   | DISPLAY control output                                                                                                                                                                                                          |
| K11                | xpb[2]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | mPMC_stcs1pb*                    |                | I   | static memory byte lane polarity setting for boot loader<br>0: HIGH for reads, LOW for writes, used for we_n access<br>1: LOW for reads, LOW for writes, used for upper and lower byte access<br>The value is latched at reset. |
|                    | dbop_c2                          |                | O   | DISPLAY control output                                                                                                                                                                                                          |
| K10                | xpb[3]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | mPMC_rel1config*                 |                | I   | test mode configuration (for testing purpose only !!!)<br>The value is latched at reset.                                                                                                                                        |
|                    | dbop_c3                          |                | O   | DISPLAY control output                                                                                                                                                                                                          |
| K9                 | xpb[4]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | dbop_d[8]                        |                | IO  | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
| K12                | xpb[5]                           | D IO ST PD LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | dbop_d[9]                        |                | IO  | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
| L12                | xpb[6]                           | D IO ST PU LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | uart_rxd                         |                | I   | UART receive line                                                                                                                                                                                                               |
|                    | dbop_d[10]                       |                | IO  | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
| K13                | xpb[7]                           | D IO ST PU LSR | IO  | GPIO IO, Port B                                                                                                                                                                                                                 |
|                    | uart_txd                         |                | O   | UART transmit line                                                                                                                                                                                                              |
|                    | dbop_d[11]                       |                | IO  | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
|                    | Port C / DISPLAY / 2-WIRE SERIAL |                |     |                                                                                                                                                                                                                                 |
| E5                 | xpc[0]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                                                                                                                                                                 |
|                    | IntBootSel*                      |                | I   | BOOT LOADER source select input<br>1: internal ROM<br>0: external ROM/Flash                                                                                                                                                     |
|                    | dbop_d[0]                        |                | IO  | DISPLAY data input/output (low byte)                                                                                                                                                                                            |
| C4                 | xpc[1]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                                                                                                                                                                 |

| Ball Nr.<br>BGA224 | Ball Name                       | PAD Type       | I/O | Ball Description                                                                       |
|--------------------|---------------------------------|----------------|-----|----------------------------------------------------------------------------------------|
|                    | boot_sel[0]                     |                | I   | BOOT LOADER type select input                                                          |
|                    | dbop_d[1]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| F4                 | xpc[2]                          | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                        |
|                    | boot_sel[1]                     |                | I   | BOOT LOADER type select input                                                          |
|                    | dbop_d[2]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| A3                 | xpc[3]                          | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                        |
|                    | boot_sel[2]                     |                | I   | BOOT LOADER type select input                                                          |
|                    | dbop_d[3]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| D4                 | xpc[4]                          | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                        |
|                    | dbop_d[4]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| B3                 | xpc[5]                          | D IO ST PD LSR | IO  | GPIO IO, Port C                                                                        |
|                    | dbop_d[5]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| C3                 | xpc[6]                          | D IO ST PU LSR | IO  | GPIO IO, Port C                                                                        |
|                    | cmd_ms_sck                      |                | IO  | 2-WIRE SERIAL master/slave clock line                                                  |
|                    | dbop_d[6]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
| A2                 | xpc[7]                          | D IO ST PU LSR | IO  | GPIO IO, Port C                                                                        |
|                    | cmd_ms_sda                      |                | IO  | 2-WIRE SERIAL master/slave data line                                                   |
|                    | dbop_d[7]                       |                | IO  | DISPLAY data input/output (low byte)                                                   |
|                    | Port D / SD Card / Memory Stick |                |     |                                                                                        |
| H13                | xpd[0]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_dat[0]                      |                | IO  | MMC/SD data line                                                                       |
|                    | ms_sdio[0]                      |                | IO  | MEMORY STICK data line                                                                 |
| J12                | xpd[1]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_dat[1]                      |                | IO  | MMC/SD data line                                                                       |
|                    | ms_sdio[1]                      |                | IO  | MEMORY STICK data line                                                                 |
| J13                | xpd[2]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_dat[2]                      |                | IO  | MMC/SD data line                                                                       |
|                    | ms_sdio[2]                      |                | IO  | MEMORY STICK data line                                                                 |
| G15                | xpd[3]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_dat[3]                      |                | IO  | MMC/SD data line                                                                       |
|                    | ms_sdio[3]                      |                | IO  | MEMORY STICK data line                                                                 |
| H14                | xpd[4]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_cmd                         |                | O   | MMC/SD command line                                                                    |
|                    | ms_sclk                         |                | O   | MEMORY STICK clock line                                                                |
| J14                | xpd[5]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_clk                         |                | O   | MMC/SD clock line                                                                      |
|                    | ms_bs                           |                | O   | MEMORY STICK bus state                                                                 |
| J15                | xpd[6]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_fbclk                       |                | I   | MMC/SD feedback clock                                                                  |
|                    | ms_fbclk                        |                | I   | MEMORY STICK feedback clock                                                            |
| H15                | xpd[7]                          | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                    | mci_rod                         |                | O   | MMC/SD resistor open drain control                                                     |
|                    | 2-wire serial Audio Master      |                |     |                                                                                        |
| M4                 | CSCL                            | D IO ST PU LSR | O   | 2-wire serial audio master clock line<br>used for controlling the audio/PMU sub system |
| M3                 | CSDA                            | D IO ST PU LSR | O   | 2-wire serial audio master data line<br>used for controlling the audio/PMU sub system  |
|                    | Serial Synchronous Port         |                |     |                                                                                        |

| Ball Nr.<br>BGA224     | Ball Name  | PAD Type       | I/O | Ball Description                                                          |
|------------------------|------------|----------------|-----|---------------------------------------------------------------------------|
| C11                    | ssp_fssout | D IO ST PU LSR | O   | SSP master, frame or slave select                                         |
|                        | ssp_fssin  |                | I   | SSP slave, frame select                                                   |
| H9                     | ssp_clkout | D IO ST PU LSR | O   | SSP master, clock line                                                    |
|                        | ssp_clkin  |                | I   | SSP slave, clock line                                                     |
| D11                    | ssp_rxd    | D IO ST PU LSR | I   | SSP receive data input                                                    |
| J10                    | ssp_txd    | D IO ST PU LSR | O   | SSP transmit data output                                                  |
| <b>NandFlash / IDE</b> |            |                |     |                                                                           |
| C13                    | naf_d[0]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[0]  |                | IO  | IDE data line (low byte)                                                  |
| A13                    | naf_d[1]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[1]  |                | IO  | IDE data line (low byte)                                                  |
| B14                    | naf_d[2]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[2]  |                | IO  | IDE data line (low byte)                                                  |
| D13                    | naf_d[3]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[3]  |                | IO  | IDE data line (low byte)                                                  |
| B13                    | naf_d[4]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[4]  |                | IO  | IDE data line (low byte)                                                  |
| C12                    | naf_d[5]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[5]  |                | IO  | IDE data line (low byte)                                                  |
| G11                    | naf_d[6]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[6]  |                | IO  | IDE data line (low byte)                                                  |
| B12                    | naf_d[7]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                           |
|                        | ide_hd[7]  |                | IO  | IDE data line (low byte)                                                  |
| C14                    | naf_d[8]   | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[8]  |                | IO  | IDE data line (high byte)                                                 |
| E12                    | naf_d[9]   | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[9]  |                | IO  | IDE data line (high byte)                                                 |
| F11                    | naf_d[10]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[10] |                | IO  | IDE data line (high byte)                                                 |
| D15                    | naf_d[11]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[11] |                | IO  | IDE data line (high byte)                                                 |
| F12                    | naf_d[12]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[12] |                | IO  | IDE data line (high byte)                                                 |
| E13                    | naf_d[13]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[13] |                | IO  | IDE data line (high byte)                                                 |
| D14                    | naf_d[14]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[14] |                | IO  | IDE data line (high byte)                                                 |
| E14                    | naf_d[15]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                          |
|                        | ide_hd[15] |                | IO  | IDE data line (high byte)                                                 |
| F14                    | naf_cle    | D IO ST LSR    | O   | NAND FLASH command latch enable                                           |
|                        | ide_dmarq  |                | I   | IDE DMA request<br>used for DMA data transfers between host and device    |
| F13                    | naf_ale    | D IO ST LSR    | O   | NAND FLASH address latch enable                                           |
|                        | ide_iordy  |                | I   | IDE IO ready signal<br>used by device to extend host data transfer cycles |
| G12                    | naf_wp_n   | D IO ST PD LSR | O   | NAND FLASH write protect not                                              |
|                        | ide_intrq  |                | I   | IDE interrupt request<br>used by device to interrupt the host controller  |

| Ball Nr.<br>BGA224 | Ball Name                | PAD Type        | I/O    | Ball Description                                                                                                                      |
|--------------------|--------------------------|-----------------|--------|---------------------------------------------------------------------------------------------------------------------------------------|
| E15                | naf_ce0_n                | D IO ST LSR     | O      | NAND FLASH chip enable                                                                                                                |
|                    | ide_cs0_n                |                 | O      | IDE chip select 0<br>used by the host to select command block registers in the device                                                 |
| H11                | naf_ce1_n                | D IO ST LSR     | O      | NAND FLASH chip enable                                                                                                                |
|                    | ide_cs1_n                |                 | O      | IDE chip select 1<br>used by the host to select control block registers in the device                                                 |
| J11                | naf_ce2_n                | D IO ST LSR     | O      | NAND FLASH chip enable                                                                                                                |
|                    | ide_hiown                |                 | O      | IDE host IO write strobe                                                                                                              |
| G13                | naf_ce3_n                | D IO ST LSR     | O      | NAND FLASH chip enable                                                                                                                |
|                    | ide_hiorn                |                 | O      | IDE host IO read strobe                                                                                                               |
| G14                | naf_we_n                 | D IO ST LSR     | O      | NAND FLASH write enable not                                                                                                           |
|                    | ide_dackn                |                 | O      | IDE DMA acknowledge<br>used by the host to initiate DMA data transfers                                                                |
| H12                | naf_re_n                 | D IO ST LSR     | O      | NAND FLASH read enable not                                                                                                            |
|                    | ide_npcblid              |                 | I      | IDE primary channel cable ID detect                                                                                                   |
| F15                | naf_bsy_n                | D IO ST LSR     | I      | NAND FLASH ready / busy not                                                                                                           |
|                    | ide_nscblid              |                 | I      | IDE secondary channel cable ID select                                                                                                 |
| A12                | ide_ha[0]                | D OUT LSR       | O      | IDE host address                                                                                                                      |
| H10                | ide_ha[1]                | D OUT LSR       | O      | IDE host address                                                                                                                      |
| D12                | ide_ha[2]                | D OUT LSR       | O      | IDE host address                                                                                                                      |
| G10                | ide_reset_n              | D OUT LSR       | O      | IDE reset not,<br>used by the host to reset the device                                                                                |
| <b>I2S Output</b>  |                          |                 |        |                                                                                                                                       |
| M6                 | i2so_sdata<br><b>SDI</b> | D OUT LSR<br>DI | O<br>I | I2S data output<br>data output from digital core to audio sub system, <i>SDI</i> and <i>i2so_sdata</i> are connected on the BGA       |
| N6                 | i2so_sclk<br><b>SCLK</b> | D OUT LSR<br>DI | O<br>I | I2S serial clock<br>clock output from digital core to audio sub system, <i>SCLK</i> and <i>iso_sclk</i> are connected on the BGA      |
| N5                 | i2so_lrck<br><b>LRCK</b> | D OUT LSR<br>DI | O<br>I | I2S left/right clock<br>clock output from digital core to audio sub system, <i>LRCK</i> and <i>i2so_lrck</i> are connected on the BGA |
| M5                 | i2so_mclk<br><b>MCLK</b> | D OUT LSR<br>DI | O<br>I | I2S master clock<br>clock output from digital core to audio sub system, <i>MCLK</i> and <i>i2so_mclk</i> are connected on the BGA     |
| <b>I2S Input</b>   |                          |                 |        |                                                                                                                                       |
| M7                 | i2si_sdata<br><b>SDO</b> | D IN ST<br>DO   | I<br>O | I2S data input<br>data output from audio sub system to digital core, <i>SDO</i> and <i>i2si_sdata</i> are connected on the BGA        |
| E3                 | i2si_sclk_out            | D IO ST LSR     | O      | I2S master serial clock<br>serial clock output for external ADC if AS3525 is I2S master                                               |
|                    | i2si_sclk_in             |                 | I      | I2S slave serial clock<br>serial clock input for external ADC if AS3525 is I2S slave                                                  |
| D1                 | i2si_lrck_out            | D IO ST LSR     | O      | I2S master, left/right clock<br>left/right clock output for external ADC if AS3525 is I2S master                                      |
|                    | i2si_lrck_in             |                 | I      | I2S slave, left/right clock<br>left/right clock input for external ADC if AS3525 is I2S master                                        |
| E4                 | i2si_mclk                | D OUT LSR       | O      | I2S master, master clock                                                                                                              |
| C1                 | i2si_sdata_in            | D IN ST PD      | I      | I2S data input<br>data input from external audio ADC                                                                                  |

| Ball Nr.<br>BGA224         | Ball Name      | PAD Type          | I/O    | Ball Description                                                                                                      |
|----------------------------|----------------|-------------------|--------|-----------------------------------------------------------------------------------------------------------------------|
|                            | spdif_data_in  |                   | I      | SPDIF data input<br>data input for SPDIF to I2S conversion                                                            |
| <b>Audio Subsystem IRQ</b> |                |                   |        |                                                                                                                       |
| N1                         | INTRQ<br>intrq | DO<br>D IN ST     | O<br>I | used by the audio/PMU subsystem to interrupt the digital core, <i>INTRQ</i> and <i>intrq</i> are connected on the BGA |
| <b>JTAG Debugging IF</b>   |                |                   |        |                                                                                                                       |
| C2                         | jtag_trst_n    | D IN ST PD        | I      | JTAG reset not                                                                                                        |
| A1                         | jtag_tms       | D IN ST PU        | I      | JTAG mode select                                                                                                      |
| B2                         | jtag_tck       | D IN ST PU        | I      | JTAG clock                                                                                                            |
| B1                         | jtag_tdi       | D IN ST PU        | I      | JTAG data input                                                                                                       |
| D3                         | jtag_tdo       | D IO ST PU LSR    | O      | JTAG data output                                                                                                      |
| <b>External Memory IF</b>  |                |                   |        |                                                                                                                       |
| G5                         | mpmc_addr[0]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| B5                         | mpmc_addr[1]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| L4                         | mpmc_addr[2]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| A5                         | mpmc_addr[3]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| K5                         | mpmc_addr[4]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| D6                         | mpmc_addr[5]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| F6                         | mpmc_addr[6]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| C6                         | mpmc_addr[7]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| E6                         | mpmc_addr[8]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| A6                         | mpmc_addr[9]   | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| H5                         | mpmc_addr[10]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| B6                         | mpmc_addr[11]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| J5                         | mpmc_addr[12]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| D7                         | mpmc_addr[13]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| E7                         | mpmc_addr[14]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| C7                         | mpmc_addr[15]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| F7                         | mpmc_addr[16]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| A7                         | mpmc_addr[17]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| G6                         | mpmc_addr[18]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| B7                         | mpmc_addr[19]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| H6                         | mpmc_addr[20]  | D OUT LSR LV      | O      | EXT. MEMORY address line                                                                                              |
| F8                         | mpmc_cke[0]    | D OUT LSR LV      | O      | EXT. MEMORY clock enable0<br>used for SDRAM devices only                                                              |
| J6                         | mpmc_cke[1]    | D OUT LSR LV      | O      | EXT. MEMORY clock enable 1<br>used for SDRAM devices only                                                             |
| E8                         | mpmc_clk[0]    | D OUT LSR LV      | O      | EXT. MEMORY clock 0<br>used for SDRAM devices only                                                                    |
| G7                         | mpmc_clk[1]    | D OUT LSR LV      | O      | EXT. MEMORY clock 1<br>used for SDRAM devices only                                                                    |
| L5                         | mpmc_fbclk_in  | D IO ST PD LSR LV | O      | EXT. MEMORY feedback clock<br>used for SDRAM devices only                                                             |
| D8                         | mpmc_dqm[0]    | D OUT LSR LV      | O      | EXT. MEMORY data mask 0<br>used for SDRAM devices and static memories                                                 |
| L6                         | mpmc_dqm[1]    | D OUT LSR LV      | O      | EXT. MEMORY data mask 1<br>used for SDRAM devices and static memories                                                 |
| A8                         | mpmc_cas_n     | D OUT LSR LV      | O      | EXT. MEMORY column address strobe not<br>used for SDRAM devices only                                                  |
| K6                         | mpmc_dycs_n[0] | D OUT LSR LV      | O      | EXT. MEMORY dynamic memory chip select 0 not                                                                          |

| Ball Nr.<br>BGA224 | Ball Name      | PAD Type          | I/O | Ball Description                                                                          |
|--------------------|----------------|-------------------|-----|-------------------------------------------------------------------------------------------|
|                    |                |                   |     | used for SDRAM devices only                                                               |
| E9                 | mpmc_dycs_n[1] | D OUT LSR LV      | O   | EXT. MEMORY dynamic memory chip select 1 not used for SDRAM devices only                  |
| J7                 | mpmc_ras_n     | D OUT LSR LV      | O   | EXT. MEMORY row address strobe not used for SDRAM devices only                            |
| F9                 | mpmc_we_n      | D OUT LSR LV      | O   | EXT. MEMORY write enable not used for SDRAM devices and static memories                   |
| D9                 | mpmc_stcs_n[0] | D OUT LSR LV      | O   | EXT. MEMORY static memory chip select 0 not used for static memory devices only           |
| L7                 | mpmc_stcs_n[1] | D OUT LSR LV      | O   | EXT. MEMORY static memory chip select 0 not used for static memory devices only           |
| A9                 | mpmc_bls_n[0]  | D OUT LSR LV      | O   | EXT. MEMORY byte lane select 0 not used for static memory devices only                    |
| K7                 | mpmc_bls_n[1]  | D OUT LSR LV      | O   | EXT. MEMORY byte lane select 1 not used for static memory devices only                    |
| D10                | mpmc_oe_n      | D OUT LSR LV      | O   | EXT. MEMORY output enable not used for static memory devices only                         |
| L8                 | mpmc_data[0]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| E10                | mpmc_data[1]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| L9                 | mpmc_data[2]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| F10                | mpmc_data[3]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| K8                 | mpmc_data[4]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| A10                | mpmc_data[5]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| J8                 | mpmc_data[6]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| B10                | mpmc_data[7]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| H7                 | mpmc_data[8]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| C10                | mpmc_data[9]   | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| G8                 | mpmc_data[10]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| E11                | mpmc_data[11]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| G9                 | mpmc_data[12]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| A11                | mpmc_data[13]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| J9                 | mpmc_data[14]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| B11                | mpmc_data[15]  | D IO ST PD LSR LV | IO  | EXT. MEMORY data line                                                                     |
| <b>DBOP</b>        |                |                   |     |                                                                                           |
| G3                 | dbop_d[12]     | D IO ST PD LSR    | IO  | DISPLAY data input/output (high byte)                                                     |
| H3                 | dbop_d[13]     | D IO ST PD LSR    | IO  | DISPLAY data input/output (high byte)                                                     |
| A14                | dbop_d[14]     | D IO ST PD LSR    | IO  | DISPLAY data input/output (high byte)                                                     |
| C15                | dbop_d[15]     | D IO ST PD LSR    | IO  | DISPLAY data input/output (high byte)                                                     |
| <b>USB 2.0 OTG</b> |                |                   |     |                                                                                           |
| F2                 | vdda33t        | PWP_VD_RDO_3V     | P   | USB 3.3V analog power supply for OTG transceiver block                                    |
| J1                 | vssa33t        | PWP_VS_RDO_3V     | P   | USB 3.3V analog ground supply for OTG transceiver block                                   |
| H2                 | vssa33t        | PWP_VS_RDO_3V     | P   | USB 3.3V analog ground supply for OTG transceiver block                                   |
| G2                 | vssa33t        | PWP_VS_RDO_3V     | P   | USB 3.3V analog ground supply for OTG transceiver block                                   |
| G1                 | usb_dp         | USB_ESD_5VT       | A   | USB D+ signal from USB cable                                                              |
| H1                 | usb_dm         | USB_ESD_5VT       | A   | USB D- signal from USB cable                                                              |
| K4                 | NC             | -                 |     | test pin: <b>must stay unconnected for normal operation mode</b>                          |
| K2                 | NC             | -                 |     | test pin: <b>must stay unconnected for normal operation mode</b>                          |
| J2                 | usb_rext       | ANA_BI_RXT_3V     | A   | USB external resistor connect analog signal to the external resistor for setting the bias |

| Ball Nr.<br>BGA224  | Ball Name               | PAD Type           | I/O       | Ball Description                                                                                                         |
|---------------------|-------------------------|--------------------|-----------|--------------------------------------------------------------------------------------------------------------------------|
|                     |                         |                    |           | current of the USB 2.0 OTG PHY, voltage level is 1.1-1.3V                                                                |
| J3                  | vdda33c                 | PWP_VD_ANA_3V      | P         | USB 3.3V analog power supply for common block                                                                            |
| L2                  | NC                      | -                  |           | test pin: <b>must stay unconnected for normal operation mode</b>                                                         |
| F3                  | <b>VBUS</b><br>usb_vbus | USB20_VBUS_5VT_OTG | AO<br>AIO | <b>USB 5V supply generated by the PMU subsystem, VBUS and usb_vbus are connected on the BGA USB mini receptacle Vbus</b> |
| <b>Supply Balls</b> |                         |                    |           |                                                                                                                          |
| A15                 | vdd_peri                | P                  | P         | 3.3V peripheral power supply                                                                                             |
| B9                  | vdd_mem                 | P                  | P         | 3.3V (2.5V) external memory power supply                                                                                 |
| C9                  | vdd_mem                 | P                  | P         | 3.3V (2.5V) external memory power supply                                                                                 |
| B15                 | vss_peri                | P                  | P         | 3.3V peripheral ground supply                                                                                            |
| B8                  | vss_mem                 | P                  | P         | 3.3V (2.5V) external memory ground supply                                                                                |
| C8                  | vss_mem                 | P                  | P         | 3.3V (2.5V) external memory ground supply                                                                                |
| K1                  | vdd_core                | P                  | P         | 1.2V core power supply                                                                                                   |
| L1                  | vss_core                | P                  | P         | 1.2V core ground supply                                                                                                  |
| <b>AFE Balls</b>    |                         |                    |           |                                                                                                                          |
| K3                  | DVDD                    | P                  | P         | audio/PMU subsystem digital power supply to be connected to QLDO2 (2.9V)                                                 |
| L3                  | PwrUP                   | DI PD              | I         | power Up input                                                                                                           |
| N2                  | P_PVDD                  | AI                 | I         | 5 State program input of PVDD regulator                                                                                  |
| P1                  | DVSS                    | P                  | P         | audio/PMU subsystem digital ground supply                                                                                |
| R1                  | XIN_24M                 | AIO                | IO        | oscillator input 12-24MHz                                                                                                |
| R2                  | XOUT_24M                | AIO                | IO        | oscillator output 12-24MHz                                                                                               |
| P2                  | LIN2R                   | AI                 | I         | line input 2 right channel                                                                                               |
| R3                  | LIN2L                   | AI                 | I         | line input 2 left channel                                                                                                |
| P3                  | LIN1R                   | AI                 | I         | line input 1 right channel                                                                                               |
| R4                  | LIN1L                   | AI                 | I         | line input 1 left channel                                                                                                |
| N3                  | MSUP2                   | P                  | P         | microphone supply 2 (2.95V) / remote input 2                                                                             |
| P4                  | MIC2_N                  | AI                 | I         | microphone input 2N                                                                                                      |
| R5                  | MIC2_P                  | AI                 | I         | microphone input 2P                                                                                                      |
| R6                  | MIC1_P                  | AI                 | I         | microphone input 1P                                                                                                      |
| P5                  | MIC1_N                  | AI                 | I         | microphone input 1N                                                                                                      |
| P6                  | MSUP1                   | P                  | P         | microphone supply 1 (2.95V) / remote input 1                                                                             |
| N4                  | LOUTR                   | AO                 | O         | line output right channel / ear piece differential output N                                                              |
| N7                  | LOUTL                   | AO                 | O         | line output left channel / ear piece differential output P                                                               |
| N8                  | AVDD                    | P                  | P         | audio/PMU subsystem analog power supply                                                                                  |
| P8                  | AGND                    | AIO                | IO        | analog reference (AVDD/2) decoupling cap terminal (10uF)                                                                 |
| M8                  | VREF                    | AIO                | IO        | analog reference ( filtered AVDD) decoupling cap terminal (10uF)                                                         |
| R7                  | AVSS                    | P                  | P         | audio/PMU subsystem digital power supply                                                                                 |
| N9                  | HPGND                   | AIO                | IO        | headphone amplifier reference decoupling cap terminal (100nF)                                                            |
| M9                  | HPCM                    | AO                 | O         | headphone common GND output for DC-coupled speakers                                                                      |
| N10                 | HPR                     | AO                 | O         | headphone output right channel                                                                                           |
| N12                 | BVSS2                   | P                  | P         | headphone amplifier ground supply                                                                                        |
| N13                 | HPL                     | AO                 | O         | headphone output left channel                                                                                            |
| N11                 | BGND                    | P                  | P         | speaker amplifier reference decoupling cap terminal (100nF)                                                              |
| P9                  | BVDD                    | P                  | P         | audio/PMU subsystem power supply (max. 5.5V)                                                                             |

| Ball Nr.<br>BGA224 | Ball Name | PAD Type | I/O | Ball Description                                                                                        |
|--------------------|-----------|----------|-----|---------------------------------------------------------------------------------------------------------|
| R9                 | LSPR      | AO       | O   | speaker output right channel                                                                            |
| P7                 | BVSS      | P        | P   | speaker amplifier ground supply                                                                         |
| R8                 | BVSS      | P        | P   | speaker amplifier ground supply                                                                         |
| R10                | LSPL      | AO       | O   | speaker output left channel                                                                             |
| P10                | BVDD      | P        | P   | audio/PMU subsystem power supply (max. 5.5V)                                                            |
| R11                | UVDD      | AO       | O   | LDO6 Regulator Output fixed to 3.262V<br>to be used for USB transceiver supply                          |
| R12                | PVDD      | AO       | O   | LDO3 Regulator Output programmed to 1.7 - 3.33V                                                         |
| P11                | BVDD      | AO       | O   | audio/PMU subsystem power supply (max. 5.5V)                                                            |
| P12                | IOVDD     | AO       | O   | LDO4 Regulator Output fixed to 3.109V                                                                   |
| R15                | CVDD      | AO       | O   | charge pump output for digital core supply, programmed to<br>1.05 - 1.2V<br>to be connected to vdd_core |
| M13                | VBAT_1V   | P        | P   | battery supply input for single cell application                                                        |
| P15                | CP_1V     | AIO      | IO  | CVDD charge pump flying cap                                                                             |
| N15                | CN_1V     | AIO      | IO  | CVDD charge pump flying cap                                                                             |
| M15                | VSS_1V    | P        | P   | CVDD charge pump ground supply                                                                          |
| M14                | QLDO2     | AO       | O   | LDO2 regulator output fixed 2.9V<br>to be connected to DVDD                                             |
| L14                | CP_5V     | AIO      | IO  | VBUS charge pump flying cap                                                                             |
| L13                | CN_5V     | AIO      | IO  | VBUS charge pump flying cap                                                                             |
| L15                | VSS_3V    | P        | P   | DCDC3V ground supply                                                                                    |
| K15                | SW_3V     | AO       | O   | DCDC3V switch terminal                                                                                  |
| K14                | SW_15V    | AO       | O   | DCDC15V switch terminal                                                                                 |
| M12                | VSS_15V   | P        | P   | DCDC15V ground supply                                                                                   |
| M11                | ISINK     | AO       | O   | DCDC15V load current sink terminal                                                                      |
| N14                | CHG_IN    | AI       | I   | charger input                                                                                           |
| P14                | CHG_OUT   | AO       | O   | charger output<br>programmable current (50-400mA) and voltage ( 3.9-4.25V)                              |
| M10                | BATTEMP   | AIO      | IO  | charger battery temperature sensor input (RNTC 100k)                                                    |
| R14                | XOUT_32k  | AIO      | IO  | 32kHz RTC oscillator crystal terminal                                                                   |
| R13                | XIN_32k   | AIO      | IO  | 32kHz RTC oscillator crystal terminal                                                                   |
| P13                | RVDD      | AO       | O   | RTC supply regulator output<br>supplied via BVDD, programmed to 1.0-2.5V                                |

## 8.3 CTBGA144 Package Drawings

Figure 63 CTBGA144 Package Drawing



Package Code AYWZZZ

| A                 | Y    | WW                              | ZZZ         |
|-------------------|------|---------------------------------|-------------|
| A ... for PB free | Year | working week assembly/packaging | Free choice |

### 8.3.1 CTBGA144 Package Ball-out

Figure 64 AS3525B Package Ball-out

|   | 1           | 2          | 3             | 4      | 5        | 6         | 7          | 8          | 9         | 10       | 11       | 12       |
|---|-------------|------------|---------------|--------|----------|-----------|------------|------------|-----------|----------|----------|----------|
| A | dbop_d12    | dbop_d13   | i2si_sdata_in | xpc_2  | xpa_6    | xpa_7     | vdd_peri   | vss_peri   | dbop_d14  | naf_d_2  | naf_d_1  | naf_d_0  |
| B | jtag_tdi    | jtag_tck   | jtag_tdo      | xpc_3  | xpa_4    | xpa_5     | ssp_fssout | ssp_clkout | dbop_d15  | naf_d_3  | naf_d_9  | naf_d_8  |
| C | jtag_trst_n | clk_ext    | jtag_tms      | xpc_4  | xpa_2    | xpa_3     | ssp_rxd    | ssp_bxd    | naf_d_4   | naf_d_12 | naf_d_11 | naf_d_10 |
| D | usb_dp      | clk_sel    | xpc_7         | xpc_1  | xpa_0    | xpa_1     | naf_d_7    | naf_d_6    | naf_d_5   | naf_d_15 | naf_d_14 | naf_d_13 |
| E | usb_dm      | tmsel      | xpc_6         | xpc_0  | naf_we_n | naf_ce1_n | naf_ce0_n  | naf_wp_n   | naf_ale   | naf_cle  | naf_re_n | CHG_OUT  |
| F | usb_vssa33  | usb_vdda33 | xpc_5         | xpd_4  | xpd_3    | xpd_2     | xpd_1      | xpd_0      | naf_bsy_n | xpd_5    | ISINK    | SW_15V   |
| G | vss_core    | usb_rxtx   | id_dig        | xpb_2  | xpb_1    | xpb_0     | xpd_7      | xpd_6      | CHG_IN    | CP_5V    | CN_5V    | SW_3V    |
| H | XIN_32k     | vdd_core   | VBUS          | xpb_7  | xpb_6    | xpb_5     | xpb_4      | xpb_3      | QLD02     | VSS_3V   | CP_1V    | CN_1V    |
| J | XOUT_32k    | RVDD       | CSCL          | P_PVDD | INTRQ    | PwrUP     | naf_ce2_n  | naf_ce3_n  | VSS_15V   | VSS_1V   | PVDD     | CVDD     |
| K | DVDD        | CSDA       | XRES          | MSUP1  | MSUP2    | BATTEMP   | HPGND      | BGND       | BVSS2     | VBAT_1V  | BVDD     | BVDD     |
| L | XOUT_24M    | AVDD       | VREF          | MIC1_N | MIC2_N   | LIN2L     | LIN1L      | LOUTL      | BVSS      | HPR      | HPL      | IOVDD    |
| M | XIN_24M     | AVSS       | AGND          | MIC1_P | MIC2_P   | LIN2R     | LIN1R      | LOUTR      | HPCM      | LSPR     | LSPL     | UVDD     |

### 8.3.2 CTBGA144 Ball List

Table 162 CTBGA144 Ball List

| Ball Nr.<br>BGA144             | Ball Name             | PAD Type       | I/O    | Ball Description                                                                                                                                                                                                                |
|--------------------------------|-----------------------|----------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| K3                             | XRES<br>resetext_n    | DO<br>D IN ST  | O<br>I | <b>XRES is generated by the PMU subsystem</b> and connected to reset input (active low) on the BGA                                                                                                                              |
| C2                             | clk_ext               | D IN ST PD     | I      | external clock input (10-26MHz)                                                                                                                                                                                                 |
| D2                             | clk_sel               | D IN ST PD     | I      | clock select<br>0 (low): clock from internal oscillator is used<br>1 (high): clock from pad <i>clk_ext</i> is used                                                                                                              |
| E2                             | tmsel                 | D IN ST PD     | I      | test mode select<br>For testing purpose only, has to be set to "0".                                                                                                                                                             |
| G3                             | id_dig                | D IN ST (PU)   | I      | USB mini receptacle identifier<br>Has to be connected to USB jack ID pin.                                                                                                                                                       |
| <b>Port A</b>                  |                       |                |        |                                                                                                                                                                                                                                 |
| D5                             | xpa[0]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| D6                             | xpa[1]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| C5                             | xpa[2]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| C6                             | xpa[3]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| B5                             | xpa[4]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| B6                             | xpa[5]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| A5                             | xpa[6]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| A6                             | xpa[7]                | D IO ST PD LSR | IO     | GPIO IO, Port A                                                                                                                                                                                                                 |
| <b>Port B / DISPLAY / UART</b> |                       |                |        |                                                                                                                                                                                                                                 |
| G6                             | xpb[0]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | mpmc_stcs1mw[0]<br>]* |                | I      | static memory chip memory width setting for boot loader<br>0: 8 bit data bus<br>1: 16 bit data bus<br>The value is latched at reset.                                                                                            |
|                                | dbop_c0               |                | O      | DISPLAY control output                                                                                                                                                                                                          |
| G5                             | xpb[1]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | mpmc_stcs1pol*        |                | I      | static memory chip select polarity setting for boot loader<br>0: active LOW chip select<br>1: active high chip select<br>The value is latched at reset.                                                                         |
|                                | dbop_c1               |                | O      | DISPLAY control output                                                                                                                                                                                                          |
| G4                             | xpb[2]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | mpmc_stcs1pb*         |                | I      | static memory byte lane polarity setting for boot loader<br>0: HIGH for reads, LOW for writes, used for we_n access<br>1: LOW for reads, LOW for writes, used for upper and lower byte access<br>The value is latched at reset. |
|                                | dbop_c2               |                | O      | DISPLAY control output                                                                                                                                                                                                          |
| H8                             | xpb[3]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | mpmc_rel1config*      |                | I      | test mode configuration (for testing purpose only !!!)<br>The value is latched at reset.                                                                                                                                        |
|                                | dbop_c3               |                | O      | DISPLAY control output                                                                                                                                                                                                          |
| H7                             | xpb[4]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | dbop_d[8]             |                | IO     | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
| H6                             | xpb[5]                | D IO ST PD LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |
|                                | dbop_d[9]             |                | IO     | DISPLAY data input/output (high byte)                                                                                                                                                                                           |
| H5                             | xpb[6]                | D IO ST PU LSR | IO     | GPIO IO, Port B                                                                                                                                                                                                                 |

| Ball Nr.<br>BGA144 | Ball Name                        | PAD Type       | I/O | Ball Description                                                            |
|--------------------|----------------------------------|----------------|-----|-----------------------------------------------------------------------------|
|                    | uart_rxd                         |                | I   | UART receive line                                                           |
|                    | dbop_d[10]                       |                | IO  | DISPLAY data input/output (high byte)                                       |
| H4                 | xpb[7]                           | D IO ST PU LSR | IO  | GPIO IO, Port B                                                             |
|                    | uart_txd                         |                | O   | UART transmit line                                                          |
|                    | dbop_d[11]                       |                | IO  | DISPLAY data input/output (high byte)                                       |
|                    | Port C / DISPLAY / 2-WIRE SERIAL |                |     |                                                                             |
| E4                 | xpc[0]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | IntBootSel*                      |                | I   | BOOT LOADER source select input<br>1: internal ROM<br>0: external ROM/Flash |
|                    | dbop_d[0]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| D4                 | xpc[1]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | boot_sel[0]                      |                | I   | BOOT LOADER type select input                                               |
|                    | dbop_d[1]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| A4                 | xpc[2]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | boot_sel[1]                      |                | I   | BOOT LOADER type select input                                               |
|                    | dbop_d[2]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| B4                 | xpc[3]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | boot_sel[2]                      |                | I   | BOOT LOADER type select input                                               |
|                    | dbop_d[3]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| C4                 | xpc[4]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | dbop_d[4]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| F3                 | xpc[5]                           | D IO ST PD LSR | IO  | GPIO IO, Port C                                                             |
|                    | dbop_d[5]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| E3                 | xpc[6]                           | D IO ST PU LSR | IO  | GPIO IO, Port C                                                             |
|                    | cmd_ms_sck                       |                | IO  | 2-WIRE SERIAL master/slave clock line                                       |
|                    | dbop_d[6]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
| D3                 | xpc[7]                           | D IO ST PU LSR | IO  | GPIO IO, Port C                                                             |
|                    | cmd_ms_sda                       |                | IO  | 2-WIRE SERIAL master/slave data line                                        |
|                    | dbop_d[7]                        |                | IO  | DISPLAY data input/output (low byte)                                        |
|                    | Port D / SD Card / Memory Stick  |                |     |                                                                             |
| F8                 | xpd[0]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_dat[0]                       |                | IO  | MMC/SD data line                                                            |
|                    | ms_sdio[0]                       |                | IO  | MEMORY STICK data line                                                      |
| F7                 | xpd[1]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_dat[1]                       |                | IO  | MMC/SD data line                                                            |
|                    | ms_sdio[1]                       |                | IO  | MEMORY STICK data line                                                      |
| F6                 | xpd[2]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_dat[2]                       |                | IO  | MMC/SD data line                                                            |
|                    | ms_sdio[2]                       |                | IO  | MEMORY STICK data line                                                      |
| F5                 | xpd[3]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_dat[3]                       |                | IO  | MMC/SD data line                                                            |
|                    | ms_sdio[3]                       |                | IO  | MEMORY STICK data line                                                      |
| F4                 | xpd[4]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_cmd                          |                | O   | MMC/SD command line                                                         |
|                    | ms_sclk                          |                | O   | MEMORY STICK clock line                                                     |
| F10                | xpd[5]                           | D IO ST LSR    | IO  | GPIO IO, Port D                                                             |
|                    | mci_clk                          |                | O   | MMC/SD clock line                                                           |

| Ball Nr.<br>BGA144         | Ball Name  | PAD Type       | I/O | Ball Description                                                                       |
|----------------------------|------------|----------------|-----|----------------------------------------------------------------------------------------|
|                            | ms_bs      |                | O   | MEMORY STICK bus state                                                                 |
| G8                         | xpd[6]     | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                            | mci_fbclk  |                | I   | MMC/SD feedback clock                                                                  |
|                            | ms_fbclk   |                | I   | MEMORY STICK feedback clock                                                            |
| G7                         | xpd[7]     | D IO ST LSR    | IO  | GPIO IO, Port D                                                                        |
|                            | mci_rod    |                | O   | MMC/SD resistor open drain control                                                     |
| 2-WIRE SERIAL Audio Master |            |                |     |                                                                                        |
| J3                         | CSCL       | D IO ST PU LSR | O   | 2-WIRE SERIAL audio master clock line<br>used for controlling the audio/PMU sub system |
| K2                         | CSDA       | D IO ST PU LSR | O   | 2-WIRE SERIAL audio master data line<br>used for controlling the audio/PMU sub system  |
| Serial Synchronous Port    |            |                |     |                                                                                        |
| B7                         | ssp_fssout | D IO ST PU LSR | O   | SSP master, frame or slave select                                                      |
|                            | ssp_fssin  |                | I   | SSP slave, frame select                                                                |
| B8                         | ssp_clkout | D IO ST PU LSR | O   | SSP master, clock line                                                                 |
|                            | ssp_clkin  |                | I   | SSP slave, clock line                                                                  |
| C7                         | ssp_rxd    | D IO ST PU LSR | I   | SSP receive data input                                                                 |
| C8                         | ssp_txd    | D IO ST PU LSR | O   | SSP transmit data output                                                               |
| NandFlash / IDE            |            |                |     |                                                                                        |
| A12                        | naf_d[0]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| A11                        | naf_d[1]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| A10                        | naf_d[2]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| B10                        | naf_d[3]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| C9                         | naf_d[4]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| D9                         | naf_d[5]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| D8                         | naf_d[6]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| D7                         | naf_d[7]   | D IO ST PD LSR | IO  | NAND FLASH data line (low byte)                                                        |
|                            |            |                |     |                                                                                        |
| B12                        | naf_d[8]   | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |
| B11                        | naf_d[9]   | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |
| C12                        | naf_d[10]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |
| C11                        | naf_d[11]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |
| C10                        | naf_d[12]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |
| D12                        | naf_d[13]  | D IO ST PD LSR | IO  | NAND FLASH data line (high byte)                                                       |
|                            |            |                |     |                                                                                        |

| Ball Nr.<br>BGA144  | Ball Name      | PAD Type          | I/O    | Ball Description                                                                                           |
|---------------------|----------------|-------------------|--------|------------------------------------------------------------------------------------------------------------|
| D11                 | naf_d[14]      | D IO ST PD LSR    | IO     | NAND FLASH data line (high byte)                                                                           |
|                     |                |                   |        |                                                                                                            |
| D10                 | naf_d[15]      | D IO ST PD LSR    | IO     | NAND FLASH data line (high byte)                                                                           |
|                     |                |                   |        |                                                                                                            |
| E10                 | naf_cle        | D IO ST LSR       | O      | NAND FLASH command latch enable                                                                            |
|                     |                |                   |        |                                                                                                            |
| E9                  | naf_ale        | D IO ST LSR       | O      | NAND FLASH address latch enable                                                                            |
|                     |                |                   |        |                                                                                                            |
| E8                  | naf_wp_n       | D IO ST PD LSR    | O      | NAND FLASH write protect not                                                                               |
|                     |                |                   |        |                                                                                                            |
| E7                  | naf_ce0_n      | D IO ST LSR       | O      | NAND FLASH chip enable                                                                                     |
|                     |                |                   |        |                                                                                                            |
| E6                  | naf_ce1_n      | D IO ST LSR       | O      | NAND FLASH chip enable                                                                                     |
|                     |                |                   |        |                                                                                                            |
| J7                  | naf_ce2_n      | D IO ST LSR       | O      | NAND FLASH chip enable                                                                                     |
|                     |                |                   |        |                                                                                                            |
| J8                  | naf_ce3_n      | D IO ST LSR       | O      | NAND FLASH chip enable                                                                                     |
|                     |                |                   |        |                                                                                                            |
| E5                  | naf_we_n       | D IO ST LSR       | O      | NAND FLASH write enable not                                                                                |
|                     |                |                   |        |                                                                                                            |
| E11                 | naf_re_n       | D IO ST LSR       | O      | NAND FLASH read enable not                                                                                 |
|                     |                |                   |        |                                                                                                            |
| F9                  | naf_bsy_n      | D IO ST LSR       | I      | NAND FLASH ready / busy not                                                                                |
|                     |                |                   |        |                                                                                                            |
| I2S Input           |                |                   |        |                                                                                                            |
| A3                  | i2si_sdata_in  | D IN ST PD        | I      | I2S data input<br>data input from external audio ADC                                                       |
|                     | spdif_data_in  |                   | I      | SPDIF data input<br>data input for SPDIF to I2S conversion                                                 |
| Audio Subsystem IRQ |                |                   |        |                                                                                                            |
| J5                  | INTRQ<br>intrq | DO<br>D IN ST     | O<br>I | used by the audio/PMU subsystem to interrupt the digital core,<br>INTRQ and intrq are connected on the BGA |
| JTAG Debugging IF   |                |                   |        |                                                                                                            |
| C1                  | jtag_trst_n    | D IN ST PD        | I      | JTAG reset not                                                                                             |
| C3                  | jtag_tms       | D IN ST PU        | I      | JTAG mode select                                                                                           |
| B2                  | jtag_tck       | D IN ST PU        | I      | JTAG clock                                                                                                 |
| B1                  | jtag_tdi       | D IN ST PU        | I      | JTAG data input                                                                                            |
| B3                  | jtag_tdo       | D IO ST PU LSR    | O      | JTAG data output                                                                                           |
| DBOP                |                |                   |        |                                                                                                            |
| A1                  | dbop_d[12]     | D IO ST PD LSR    | IO     | DISPLAY data input/output (high byte)                                                                      |
| A2                  | dbop_d[13]     | D IO ST PD LSR    | IO     | DISPLAY data input/output (high byte)                                                                      |
| A9                  | dbop_d[14]     | D IO ST PD LSR    | IO     | DISPLAY data input/output (high byte)                                                                      |
| B9                  | dbop_d[15]     | D IO ST PD LSR    | IO     | DISPLAY data input/output (high byte)                                                                      |
| USB 2.0 OTG         |                |                   |        |                                                                                                            |
| F2                  | vdda33         | PWP_VD_<br>ANA_3V | P      | USB 3.3V analog power supply for common block                                                              |
| F1                  | vssa33         | PWP_VS_<br>ANA_3V | P      | USB 3.3V analog ground supply for common block                                                             |

| Ball Nr.<br>BGA144  | Ball Name               | PAD Type               | I/O       | Ball Description                                                                                                                                    |
|---------------------|-------------------------|------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| D1                  | usb_dp                  | USB_ESD_5VT            | A         | USB D+ signal from USB cable                                                                                                                        |
| E1                  | usb_dm                  | USB_ESD_5VT            | A         | USB D- signal from USB cable                                                                                                                        |
| G2                  | usb_rext                | ANA_BI_RXT_3V          | A         | USB external resistor connect analog signal to the external resistor for setting the bias current of the USB 2.0 OTG PHY, voltage level is 1.1-1.3V |
| H3                  | <b>VBUS</b><br>usb_vbus | USB20_VBUS_5V<br>T_OTG | AO<br>AIO | <b>USB 5V supply generated by the PMU subsystem,</b><br>VBUS and usb_vbus are connected on the BGA<br>USB mini receptacle Vbus                      |
| <b>Supply Balls</b> |                         |                        |           |                                                                                                                                                     |
| A7                  | vdd_peri                | P                      | P         | 3.3V peripheral power supply                                                                                                                        |
| A8                  | vss_peri                | P                      | P         | 3.3V peripheral ground supply                                                                                                                       |
| H2                  | vdd_core                | P                      | P         | 1.2V core power supply<br><b>Note: This PIN has to be connected to CVDD!</b>                                                                        |
| G1                  | vss_core                | P                      | P         | 1.2V core ground supply                                                                                                                             |
| <b>AFE Balls</b>    |                         |                        |           |                                                                                                                                                     |
| K1                  | DVDD                    | P                      | P         | audio/PMU subsystem digital power supply to be connected to QLDO2 (2.9V)                                                                            |
| J6                  | PwrUP                   | DI PD                  | I         | power Up input                                                                                                                                      |
| J4                  | P_PVDD                  | AI                     | I         | 5 State program input of PVDD regulator                                                                                                             |
| M1                  | XIN_24M                 | AIO                    | IO        | oscillator input 12-24MHz                                                                                                                           |
| L1                  | XOUT_24M                | AIO                    | IO        | oscillator output 12-24MHz                                                                                                                          |
| M6                  | LIN2R                   | AI                     | I         | line input 2 right channel                                                                                                                          |
| L6                  | LIN2L                   | AI                     | I         | line input 2 left channel                                                                                                                           |
| M7                  | LIN1R                   | AI                     | I         | line input 1 right channel                                                                                                                          |
| L7                  | LIN1L                   | AI                     | I         | line input 1 left channel                                                                                                                           |
| K5                  | MSUP2                   | P                      | P         | microphone supply 2 (2.95V) / remote input 2                                                                                                        |
| L5                  | MIC2_N                  | AI                     | I         | microphone input 2N                                                                                                                                 |
| M5                  | MIC2_P                  | AI                     | I         | microphone input 2P                                                                                                                                 |
| M4                  | MIC1_P                  | AI                     | I         | microphone input 1P                                                                                                                                 |
| L4                  | MIC1_N                  | AI                     | I         | microphone input 1N                                                                                                                                 |
| K4                  | MSUP1                   | P                      | P         | microphone supply 1 (2.95V) / remote input 1                                                                                                        |
| M8                  | LOUTR                   | AO                     | O         | line output right channel / ear piece differential output N                                                                                         |
| L8                  | LOUTL                   | AO                     | O         | line output left channel / ear piece differential output P                                                                                          |
| L2                  | AVDD                    | P                      | P         | audio/PMU subsystem analog power supply                                                                                                             |
| M3                  | AGND                    | AIO                    | IO        | analog reference (AVDD/2) decoupling cap terminal (10uF)                                                                                            |
| L3                  | VREF                    | AIO                    | IO        | analog reference ( filtered AVDD) decoupling cap terminal (10uF)                                                                                    |
| M2                  | AVSS                    | P                      | P         | audio/PMU subsystem digital power supply                                                                                                            |
| K7                  | HPGND                   | AIO                    | IO        | headphone amplifier reference decoupling cap terminal (100nF)                                                                                       |
| M9                  | HPCM                    | AO                     | O         | headphone common GND output for DC-coupled speakers                                                                                                 |
| L10                 | HPR                     | AO                     | O         | headphone output right channel                                                                                                                      |
| K9                  | BVSS2                   | P                      | P         | headphone amplifier ground supply                                                                                                                   |
| L11                 | HPL                     | AO                     | O         | headphone output left channel                                                                                                                       |
| K8                  | BGND                    | P                      | P         | speaker amplifier reference decoupling cap terminal (100nF)                                                                                         |
| K11                 | BVDD                    | P                      | P         | audio/PMU subsystem power supply (max. 5.5V)                                                                                                        |
| M10                 | LSPR                    | AO                     | O         | speaker output right channel                                                                                                                        |
| L9                  | BVSS                    | P                      | P         | speaker amplifier ground supply                                                                                                                     |
| M11                 | LSPL                    | AO                     | O         | speaker output left channel                                                                                                                         |
| K12                 | BVDD                    | P                      | P         | audio/PMU subsystem power supply (max. 5.5V)                                                                                                        |

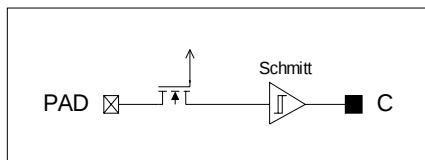
| Ball Nr.<br>BGA144 | Ball Name | PAD Type | I/O | Ball Description                                                                                                                |
|--------------------|-----------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------|
| M12                | UVDD      | AO       | O   | LDO6 Regulator Output fixed to 3.262V<br>to be used for USB transceiver supply                                                  |
| J11                | PVDD      | AO       | O   | LDO3 Regulator Output programmed to 1.7 - 3.33V                                                                                 |
| L12                | IOVDD     | AO       | O   | LDO4 Regulator Output fixed to 3.109V                                                                                           |
| J12                | CVDD      | AO       | O   | charge pump output for digital core supply, programmed to 1.05 - 1.2V<br><b>Note: This PIN has to be connected to vdd_core!</b> |
| K10                | VBAT_1V   | P        | P   | battery supply input for single cell application                                                                                |
| H11                | CP_1V     | AIO      | IO  | CVDD charge pump flying cap                                                                                                     |
| H12                | CN_1V     | AIO      | IO  | CVDD charge pump flying cap                                                                                                     |
| J10                | VSS_1V    | P        | P   | CVDD charge pump ground supply                                                                                                  |
| H9                 | QLDO2     | AO       | O   | LDO2 regulator output fixed 2.9V<br>to be connected to DVDD                                                                     |
| G10                | CP_5V     | AIO      | IO  | VBUS charge pump flying cap                                                                                                     |
| G11                | CN_5V     | AIO      | IO  | VBUS charge pump flying cap                                                                                                     |
| H10                | VSS_3V    | P        | P   | DCDC3V ground supply                                                                                                            |
| G12                | SW_3V     | AO       | O   | DCDC3V switch terminal                                                                                                          |
| F12                | SW_15V    | AO       | O   | DCDC15V switch terminal                                                                                                         |
| J9                 | VSS_15V   | P        | P   | DCDC15V ground supply                                                                                                           |
| F11                | ISINK     | AO       | O   | DCDC15V load current sink terminal                                                                                              |
| G9                 | CHG_IN    | AI       | I   | charger input                                                                                                                   |
| E12                | CHG_OUT   | AO       | O   | charger output<br>programmable current (50-400mA) and voltage ( 3.9-4.25V)                                                      |
| K6                 | BATTEMP   | AIO      | IO  | charger battery temperature sensor input (RNTC 100k)                                                                            |
| J1                 | XOUT_32k  | AIO      | IO  | 32kHz RTC oscillator crystal terminal                                                                                           |
| H1                 | XIN_32k   | AIO      | IO  | 32kHz RTC oscillator crystal terminal                                                                                           |
| J2                 | RVDD      | AO       | O   | RTC supply regulator output<br>supplied via BVDD, programmed to 1.0-2.5V                                                        |

## 8.4 Pad Cell Description

### 8.4.1 Digital Pads

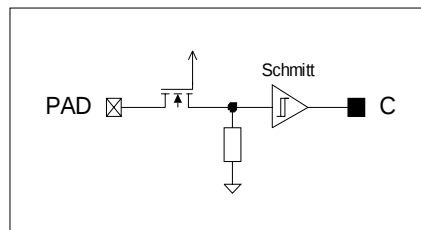
#### 8.4.1.1 D IN ST

Figure 65 Digital Input with Schmitt Trigger



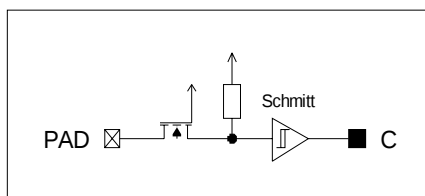
#### 8.4.1.2 D IN PD ST

Figure 66 Digital Input with Schmitt Trigger and Pull-Down



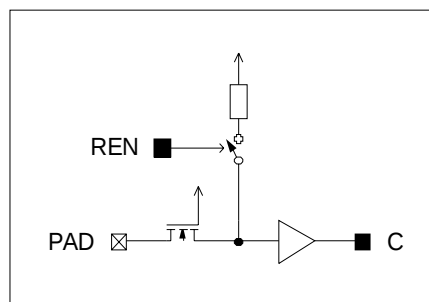
#### 8.4.1.3 D IN PU ST

Figure 67 Digital Input with Schmitt Trigger and Pull-Up



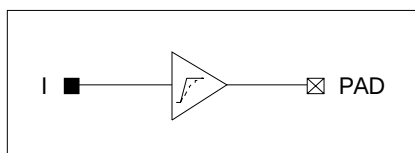
#### 8.4.1.4 D IN (PU)

Figure 68 Digital Input with enable controlled Pull-Up



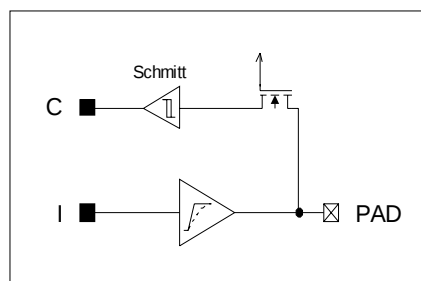
#### 8.4.1.5 D OUT LSR

Figure 69 Digital Output with Limited Slew Rate



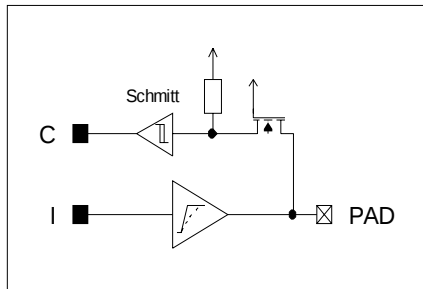
#### 8.4.1.6 D IO ST LSR

Figure 70 Digital Schmitt Trigger Input and Limited Slew Rate Output



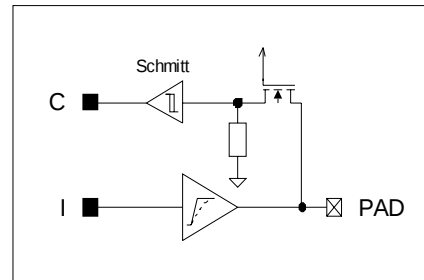
#### 8.4.1.7 D IO ST PU LSR

Figure 71 Digital Schmitt Trigger Input with Pull-Up and Limited Slew Rate Output



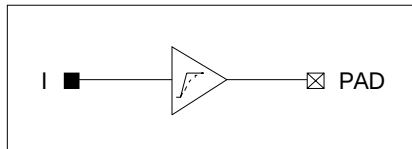
#### 8.4.1.8 D IO ST PD LSR

Figure 72 Digital Schmitt Trigger Input with Pull-Down and Limited Slew Rate Output



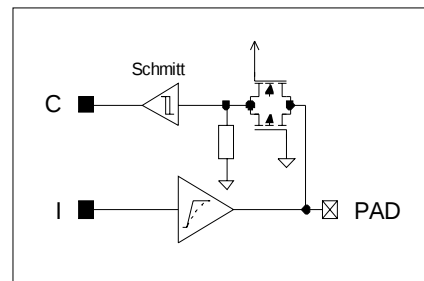
#### 8.4.1.9 D OUT LSR LV

Figure 73 Digital Output with Limited Slew Rate (low voltage)



#### 8.4.1.10 D IO ST PD LSR LV

Figure 74 Digital Schmitt Trigger Input with Pull-Down and Limited Slew Rate Output (low voltage)



## 9 Appendix

### 9.1 Memory MAP

ARM922T provides 32-bit address to access the peripherals and memory. With this 32-bit address ARM922T can access up to 4 Giga Bytes of memory. Cocoa does not use the complete 4 GB address space.

Address 0x0000\_0000 is mapped to internal ROM or External Memory interface based on the boot ROM selection by the external input pin (Port C, xpc[0] = intBootSel) Pin intBootSel=1 at startup selects the internal ROM, intBootSel = 0 selects the external memory.

The address range starting at 0x0000\_0000 is also mapped to internal RAM upon setting of the remap bit. This remap allows the user to select either RAM or ROM at 0x0000\_0000.

Table 163 Address Map

| S.No | Start (Base) Address | End Address | Actual Block Size | Peripheral                                             | Comment                      |
|------|----------------------|-------------|-------------------|--------------------------------------------------------|------------------------------|
|      |                      |             |                   | <b>AHB Blocks</b>                                      |                              |
|      | 0x0000_0000          | 0x0001_FFFF | 128 KByte         | Internal ROM                                           | Remap = 0 and IntBootSel = 1 |
|      | 0x0000_0000          | 0x003F_FFFF | 4 MB              | External Memory IF (MPMC Bank1 – Ext Flash or Ext ROM) | Remap = 0 and IntBootSel = 0 |
|      | 0x0000_0000          | 0x0004_FFFF | 320 KByte         | Embedded 1T-RAM                                        | Remap = 1                    |
|      | 0x0100_0000          | 0x0FFF_FFFF |                   | Reserved                                               |                              |
|      | 0x1000_0000          | 0x103F_FFFF | 4 MB              | External Memory IF (MPMC Bank1 – Ext Flash or Ext ROM) | Aliased                      |

| S.No | Start (Base) Address | End Address | Actual Block Size | Peripheral                                                | Comment |
|------|----------------------|-------------|-------------------|-----------------------------------------------------------|---------|
|      | 0x1100_0000          | 0x1FFF_FFFF |                   | Reserved                                                  |         |
|      | 0x2000_0000          | 0x203F_FFFF | 4 MB              | External Memory IF (MPMC Bank2 – External LCD Controller) |         |
|      | 0x2100_0000          | 0x2FFF_FFFF |                   | Reserved                                                  |         |
|      | 0x3000_0000          | 0x3FFF_FFFF | 256 MB            | External Memory IF (MPMC Bank 4 – SDRAM)                  |         |
|      | 0x4000_0000          | 0x4FFF_FFFF | 256 MB            | External Memory If (MPMC Bank5 – SDRAM)                   |         |
|      | 0x5000_0000          | 0x7FFF_FFFF |                   | Reserved                                                  |         |
|      | 0x8000_0000          | 0x8001_FFFF | 128 KByte         | Internal ROM                                              | Aliased |
|      | 0x8002_0000          | 0x80FF_FFFF |                   | Reserved                                                  |         |
|      | 0x8100_0000          | 0x8104_FFFF | 320 KByte         | Embedded 1T-RAM                                           | Aliased |
|      | 0x8105_0000          | 0xBFFF_FFFF |                   | Reserved                                                  |         |
|      | 0xC000_0000          | 0xC001_FFFF | 128 KByte         | Internal ROM                                              | Aliased |
|      | 0xC002_0000          | 0xC0FF_FFFF |                   | Reserved                                                  |         |
|      | 0xC100_0000          | 0xC104_FFFF | 320 KByte         | Embedded 1T-RAM                                           | Aliased |
|      | 0xC105_0000          | 0xC5FF_FFFF |                   | Reserved                                                  |         |
|      | 0xC600_0000          | 0xC600_FFFF | Few               | USB2.0 Slave                                              |         |
|      | 0xC601_0000          | 0xC601_FFFF | Few               | VIC                                                       |         |
|      | 0xC602_0000          | 0xC602_FFFF | Few               | DMAC Slave                                                |         |
|      | 0xC603_0000          | 0xC603_FFFF | Few               | ExtMemIFSlave                                             |         |
|      | 0xC604_0000          | 0xC604_FFFF | Few               | MemoryStick Slave                                         |         |
|      | 0xC605_0000          | 0xC605_FFFF | Few               | CompactFlash/IDE Slave                                    |         |
|      | 0xC606_0000          | 0xC606_FFFF | 4 KByte           | ARM922T Slave                                             |         |
|      | 0xC607_0000          | 0xC7FF_FFFF |                   | Reserved                                                  |         |
|      |                      |             |                   | <b>APB blocks</b>                                         |         |
|      | 0xC800_0000          | 0xC800_FFFF | Few               | Nand Flash / Smart Media Interface                        |         |
|      | 0xC801_0000          | 0xC801_FFFF | Few               | BistManager                                               |         |
|      | 0xC802_0000          | 0xC802_FFFF | Few               | SD-MCI                                                    |         |
|      | 0xC803_0000          | 0xC803_FFFF | Few               | Reserved                                                  |         |
|      | 0xC804_0000          | 0xC804_FFFF | Few               | Timer                                                     |         |
|      | 0xC805_0000          | 0xC805_FFFF | Few               | Watchdog Timer                                            |         |
|      | 0xC806_0000          | 0xC806_FFFF | Few               | I2C Master/Slave                                          |         |
|      | 0xC807_0000          | 0xC807_FFFF | Few               | I2C Audio Master                                          |         |
|      | 0xC808_0000          | 0xC808_FFFF | Few               | SSP                                                       |         |
|      | 0xC809_0000          | 0xC809_FFFF | Few               | I2S IN Interface                                          |         |
|      | 0xC80A_0000          | 0xC80A_FFFF | Few               | I2S OUT Interface                                         |         |
|      | 0xC80B_0000          | 0xC80B_FFFF | Few               | GPIO A                                                    |         |
|      | 0xC80C_0000          | 0xC80C_FFFF | Few               | GPIO B                                                    |         |
|      | 0xC80D_0000          | 0xC80D_FFFF | Few               | GPIO C                                                    |         |
|      | 0xC80E_0000          | 0xC80E_FFFF | Few               | GPIO D                                                    |         |
|      | 0xC80F_0000          | 0xC80F_FFFF | Few               | Clock Generation Unit                                     |         |
|      | 0xC810_0000          | 0xC810_FFFF | Few               | Chip Control Unit                                         |         |
|      | 0xC811_0000          | 0xC811_FFFF | Few               | Debug UART                                                |         |
|      | 0xC812_0000          | 0xC812_FFFF |                   | DBOP                                                      |         |
|      | 0xC813_0000          | 0xC813_FFFF |                   | reserved                                                  |         |

## 9.2 Register definitions

This section gives a short overview of all module registers.

### 9.2.1 Base Address definitions

Each module register block starts at a specific base address.

Table 164 Base Addresses

| REGISTER Name            | Register Address |
|--------------------------|------------------|
| AS3525_RAM_BASE          | 0x00000000       |
| AS3525_USB_BASE          | 0xC6000000       |
| AS3525_VIC_BASE          | 0xC6010000       |
| AS3525_DMACE_BASE        | 0xC6020000       |
| AS3525_EXTMEM_ITF_BASE   | 0xC6030000       |
| AS3525_MEMSTICK_BASE     | 0xC6040000       |
| AS3525_CF_IDE_BASE       | 0xC6050000       |
| AS3525_NAND_FLASH_BASE   | 0xC8000000       |
| AS3525_BIST_MANAGER_BASE | 0xC8010000       |
| AS3525_SD_MCI_BASE       | 0xC8020000       |
| AS3525_TIMER_BASE        | 0xC8040000       |
| AS3525_WDT_BASE          | 0xC8050000       |
| AS3525_I2C_MS_BASE       | 0xC8060000       |
| AS3525_I2C_AUDIO_BASE    | 0xC8070000       |
| AS3525_SSP_BASE          | 0xC8080000       |
| AS3525_I2SIN_BASE        | 0xC8090000       |
| AS3525_I2SOUT_BASE       | 0xC80A0000       |
| AS3525_GPIO1_BASE        | 0xC80B0000       |
| AS3525_GPIO2_BASE        | 0xC80C0000       |
| AS3525_GPIO3_BASE        | 0xC80D0000       |
| AS3525_GPIO4_BASE        | 0xC80E0000       |
| AS3525_CGU_BASE          | 0xC80F0000       |
| AS3525_CCU_BASE          | 0xC8100000       |
| AS3525_UART_BASE         | 0xC8110000       |
| AS3525_DBOP_BASE         | 0xC8120000       |

## 10 Ordering Information

Table 165 ordering information

| Number             | Package Type | Delivery Form | Description                            |
|--------------------|--------------|---------------|----------------------------------------|
| AS3525A C21O20 TRA | CTBGA 224    | Tray          | <u>don't use for new design starts</u> |
| AS3525A C21O20T&R  | CTBGA 224    | Tape and Reel | <u>don't use for new design starts</u> |
| AS3525B C21O20TRA  | CTBGA 144    | Tray          | <u>don't use for new design starts</u> |
| AS3525B C21O20T&R  | CTBGA 144    | Tape and Reel | <u>don't use for new design starts</u> |
| AS3525A C22O22 TRA | CTBGA 224    | Tray          |                                        |
| AS3525A C22O22T&R  | CTBGA 224    | Tape and Reel |                                        |
| AS3525B C22O22TRA  | CTBGA 144    | Tray          |                                        |
| AS3525B C22O22T&R  | CTBGA 144    | Tape and Reel |                                        |

AS3525P V D

Where

V = **Version**P = **Package Type:**

A: CTBGA 224, Thin ChipArray Ball Grid Array, 13x13mm package size, 0.8mm ball pitch

B: CTBGA 144, Thin ChipArray Ball Grid Array, 10x10mm package size, 0.8mm ball pitch

D = **Delivery Form:**

TRA = Tray

T&amp;R = Tape and Reel

All package variants are Pb-free/ RoHS package types.

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