EP312 & EP324
Classic EPLDs

April 1995, ver. 1 Data Sheet

Features

- High-performance EPLDs with 12 macrocells (EP312) or 24 macrocells (EP324)
  - Combinatorial speeds as fast as 25 ns
  - Counter frequencies of up to 33.3 MHz
  - Pipelined data rates of up to 66 MHz
- Multiple 20-pin PAL and GAL replacement and integration
- Device erasure and reprogramming with advanced, nonvolatile EPROM configuration elements
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear and Clock controls
- Dual feedback on all macrocells for implementing buried registers with bidirectional I/O
- Programmable-`AND`/allocatable-`OR` structure allowing up to 16 product terms per macrocell
- Two product terms on all macrocell control signals
- Programmable inputs (8 in EP312, 10 in EP324) configurable as latches, registers, or flow-through input
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages with 24 to 44 pins:
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)
  - 40-pin CerDIP and PDIP
  - 44-pin PLCC
- One global Clock pin; one global Input Latch Enable/Input Clock/Input (`ILE`/`ICLK`/`INPUT`) pin
- Programmable "standby" option for low-power operation
- Programmable Security Bit for total protection of proprietary designs
- 100% generically testable to provide 100% programming yield
- Software design support with the Altera PLDshell Plus software and a wide range of third-party tools; programming support through third-party vendors

General Description

The CMOS EPROM EP312 and EP324 devices have a versatile macrocell structure and I/O architecture, which allow them to implement high-performance logic functions effectively. The EP312 and EP324 input and macrocell features are a superset of features offered by PAL/GAL devices. Therefore, EP312 and EP324 devices can be used as an alternative to multiple PAL/GAL devices, SSI and MSI logic devices, or low-end gate arrays.

EP312 and EP324 devices operate in high-performance systems with low power consumption. The programmable standby function provides "zero" power consumption for applications where performance can be traded for power savings.

Functional Description

The EP312 and EP324 architecture is based on a sum-of-products programmable-AND/allocatable-OR structure. EP312 and EP324 devices can implement combinatorial and sequential logic functions, as well as combinatorial-register and register-combinatorial-register logic forms, to easily accommodate state machine designs.

Figure 1 and Figure 2 show block diagrams of the EP312 and EP324 architectures. The EP312 device contains 12 I/O macrocells and 8 programmable input structures; the EP324 device contains 24 I/O macrocells and 10 programmable input structures. EP312 and EP324 macrocells are divided into 2 rings for product-term allocation. Both devices have 2 additional inputs that can be programmed either as combinatorial inputs or Clock inputs. Each input structure can be individually configured as a latch, register, or flow-through input. Input latches and registers can be clocked synchronously or asynchronously.

Figure 1. EP312 Block Diagram

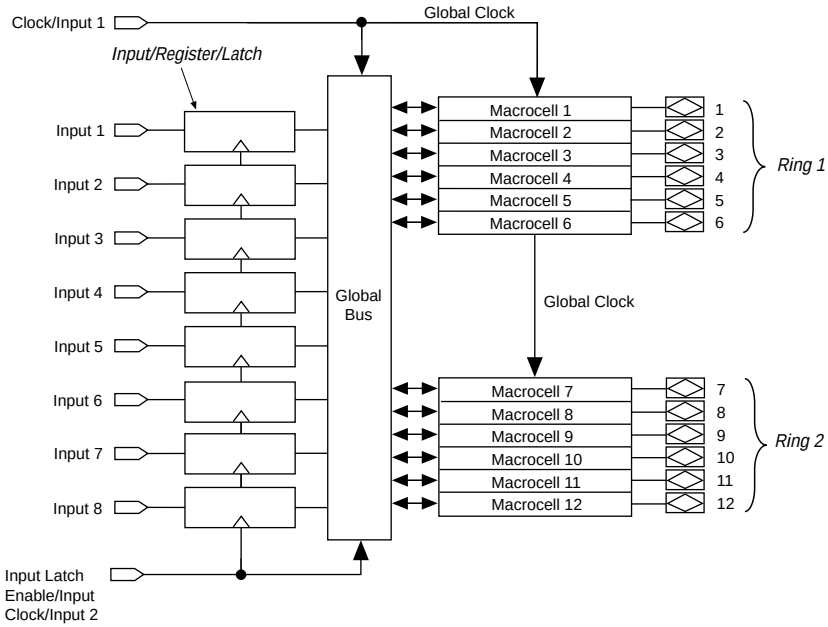
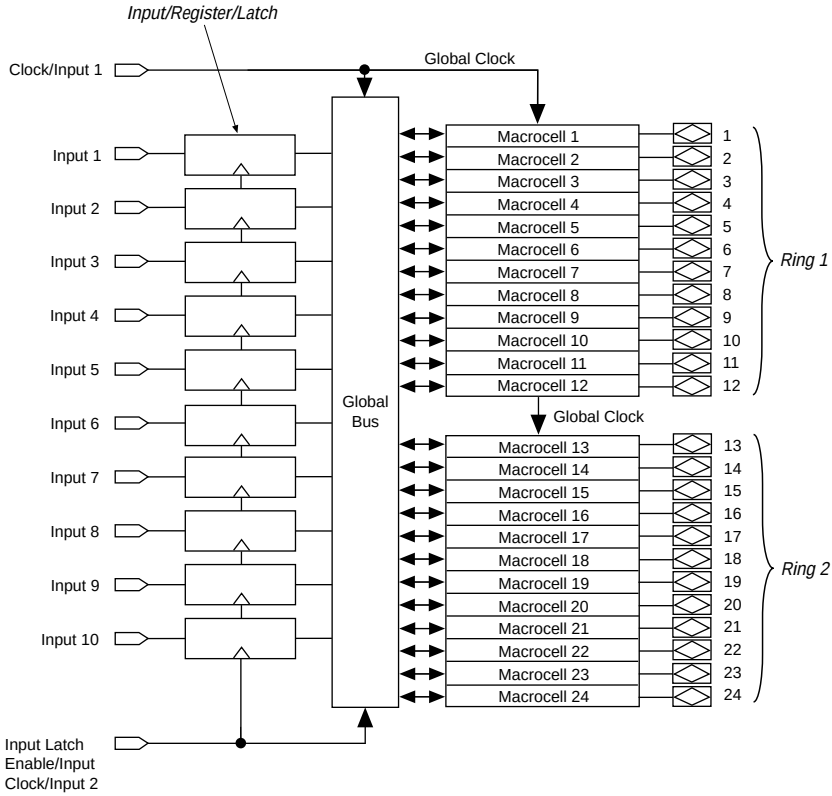


Figure 2. EP324 Block Diagram



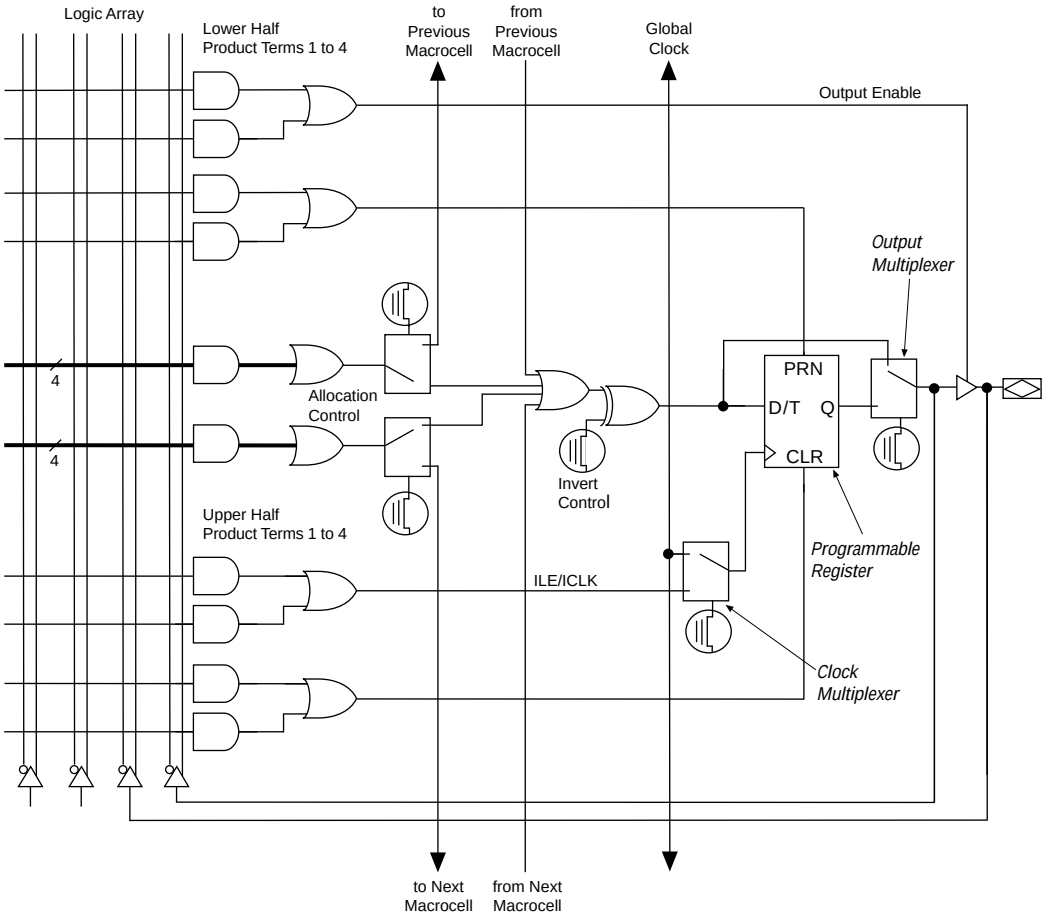
The EP312 and EP324 architectures include the following features:

- Macrocells
- Product-term allocation
- Programmable inputs
- Power-on characteristics

Macrocells

Each EP312 and EP324 macrocell contains 16 product terms (see Figure 3). Half of the product terms are available to support logic functions; half are dedicated to the macrocell control signals. The inputs to the AND array originate from the true and complement signals of the programmable input structure, the dedicated inputs, and the 2 feedback paths from each I/O macrocell to the global bus.

Figure 3. EP312 & EP324 Macrocell



The eight product terms available for implementing logic functions are divided into two equal groups, and can be used in other macrocells. Each macrocell provides a dual feedback to the logic array.

The eight product terms for control functions support the following four control signals, with two product terms each: Output Enable (OE), Preset, Clear, and asynchronous Clock. When the global Clock (CLK) signal synchronously clocks a macrocell register, it cannot function as an input to the logic array. However, the global Clock can simultaneously function as an input to the logic array and as an asynchronous, non-global Clock.

To implement registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation. If necessary, the register can be bypassed for combinatorial operation. The XOR gate can implement active-high or active-low logic, or use DeMorgan's inversion to reduce the number of product terms required to implement a function. Registers are cleared automatically during power-up.

The macrocell output can be fed back to the logic array via two paths. Pin feedback that is connected after the output buffer can be used to implement bidirectional I/O; if internal feedback is used for a buried register or logic function, the pin feedback can be used as an input.

Product-Term Allocation

In EP312 and EP324 devices, product-term resources can be taken from one macrocell and used in another. For product-term allocation, macrocells in both the EP312 and EP324 are divided into 2 rings. The EP312 has 6 macrocells per ring; the EP324 has 12 macrocells per ring. Product terms from one macrocell can be allocated to adjacent macrocells in the same ring. Product terms are allocated in groups of 4, and a macrocell can borrow up to 8 product terms (4 from each adjacent macrocell).

Table 1 and Table 2 show the product-term allocation rings for the EP312 and EP324 devices, respectively. The Altera PLDshell Plus design software automatically allocates product terms.

Table 1. EP312 Product-Term Allocation Rings

Ring 1			Ring 2		
Current Macrocell	Next Macrocell	Previous Macrocell	Current Macrocell	Next Macrocell	Previous Macrocell
1	2	6	7	8	12
2	3	1	8	9	7
3	4	2	9	10	8
4	5	3	10	11	9
5	6	4	11	12	10
6	1	5	12	7	11

Table 2. EP324 Product-Term Allocation Rings

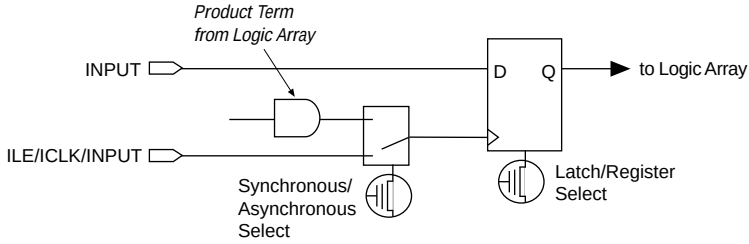
Ring 1			Ring 2		
Current Macrocell	Next Macrocell	Previous Macrocell	Current Macrocell	Next Macrocell	Previous Macrocell
1	7	2	13	19	14
2	1	3	14	13	15
3	2	4	15	14	16
4	3	5	16	15	17
5	4	6	17	16	18
6	5	12	18	17	24
7	8	1	19	20	13
8	9	7	20	21	19
9	10	8	21	22	20
10	11	9	22	23	21
11	12	10	23	24	22
12	6	11	24	18	23

Programmable Inputs

Figure 4 shows a block diagram of the EP312 and EP324 input structure. The user-programmable inputs can be individually configured to operate in the following modes:

- Input D register, synchronously clocked
- Input D register, asynchronously clocked
- Input D latch, synchronously clocked
- Input D latch, asynchronously clocked
- Flow-through input

Figure 4. EP312 & EP324 Input Structure



The ILE/ICLK/INPUT pin is a dedicated input to the logic array. For synchronous operation, the ILE/ICLK/INPUT pin becomes a global ILE/ICLK input to all latch/register/input structures; for asynchronous operation, a separate product term in the logic array is used to derive the ILE/ICLK signal for each input structure. Because the Clock signal for each programmable input can be selected individually, a combination of asynchronously and synchronously clocked inputs is available. Flow-through operation occurs when the ILE product term is tied to V_{CC}. Data is latched or clocked on the falling edge of ILE/ICLK in synchronous mode.

Power-On Characteristics

EP312 and EP324 inputs and outputs respond between 6 µs and 10 µs after power-up, or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low on power-up. Input registers are not reset on power-up and their values are indeterminate. Input latches reflect the state of the input pins on power-up.

Design Security

EP312 and EP324 devices contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM configuration elements is invisible. The Security Bit that controls this function, as well as all other program data, is reset when a device is erased.

Turbo Bit

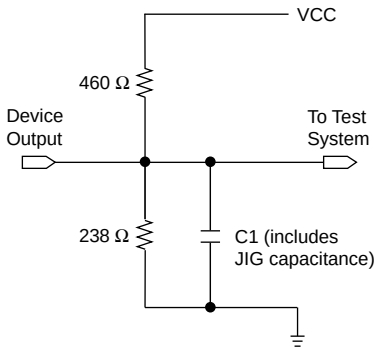
EP312 and EP324 devices contain a programmable Turbo Bit that controls the automatic power-down feature, which enables the low-standby-power mode (I_{CC1}). When the Turbo Bit is turned on, the low-standby-power mode is disabled. All AC parameters are tested with the Turbo Bit turned on. When the device is operating with the Turbo Bit turned off (non-turbo mode), a non-turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-turbo adder is specified in the "AC Operating Conditions" tables in this data sheet.

Generic Testing

EP312 and EP324 devices are fully functionally tested and guaranteed. Complete testing of each programmable EPROM configuration element and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 5.

Figure 5. EP312 & EP324 AC Test Circuits

Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test-system ground, significant reductions in observable noise immunity can result.



Test programs are used and then erased during the early stages of a device production flow. EPROM-based devices in one-time-programmable packages also contain on-board logic test circuitry to allow verification of function and AC specifications during production flow.

Software & Programming Support

The EP312 and EP324 are supported by the Altera PLDshell Plus design software and other industry-standard logic compilers (e.g., ABEL, CUPL, PLDesigner, LOG/IC, and iPLS II). The EP312 and EP324 are supported by third-party programming hardware.

For more information on software support with PLDshell Plus, go to the ***PLDshell Plus/PLDasm User's Guide***, which is available from the Altera Literature Department; refer to the *Programming Hardware Manufacturers Data Sheet* in the Altera ***Data Book*** for more information on third-party programming hardware support.

Figure 6 shows the typical supply current (I_{CC}) versus frequency for EP312 and EP324 devices.

Figure 6. EP312 & EP324 I_{CC} vs. Frequency

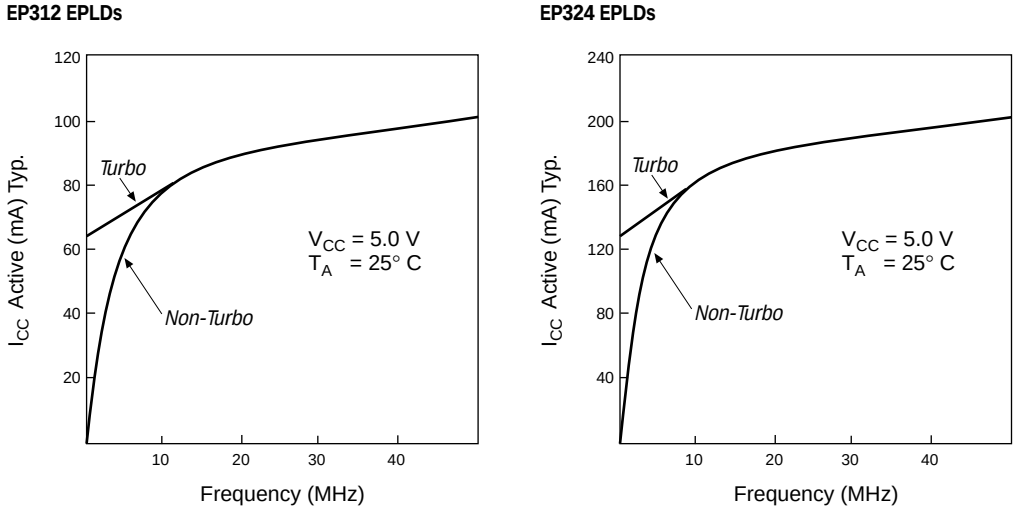
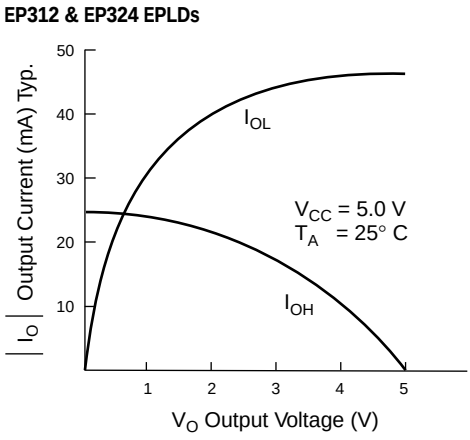


Figure 7 shows the maximum output drive characteristics of EP312 and EP324 I/O pins.

Figure 7. EP312 & EP324 Output Drive Characteristics



Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–10	85	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_{IN}	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			500	ns
t_F	Input fall time			500	ns

DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	*Note (2)*	–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4.0 mA DC, V_{CC} = min.	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, V_{CC} = min.	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC, V_{CC} = min.		0.45	V
I_I	Input leakage current	V_{CC} = max., GND < V_{IN} < V_{CC}		10	µA
I_{OZ}	Tri-state output leakage current	V_{CC} = max., GND < V_{OUT} < V_{CC}		10	µA
I_{SC}	Output short-circuit current	V_{CC} = max., V_{OUT} = 0.5 V, *Note (6)*	–30	–90	mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	I/O capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	EP312 `ILE/ICLK/INPUT` pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	EP324 `ILE/ICLK/INPUT` pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{VPP}	V_{PP} pin capacitance	*Note (7)*, f = 1.0 MHz		25	pF

I_{CC} Supply Current *Note (5)*

			EP312			EP324			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	Standby current	V_{CC} = max., V_{IN} = V_{CC} or GND, standby mode, *Note (8)*, *(9)*		100	300		150	500	µA
I_{CC3}	V_{CC} supply current	V_{CC} = max., V_{IN} = V_{CC} or GND, no load, f_{IN} = 1 MHz, *Note (9)*		10			20		mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in the current Altera ***Data Book***.
(2) Voltage with respect to ground; all over- and undershoots due to system or tester noise are included.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods of less than 20 ns under no-load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 80° C for industrial use.
(6) Test one output at a time; test duration should not exceed one second.
(7) For EP312 devices: DIP packages, V_{PP} is on pin 1
PLCC packages, V_{PP} is on pin 2
For EP324 devices: DIP packages, V_{PP} is on pin 18
PLCC packages, V_{PP} is on pin 20
(8) When the Turbo Bit is not set (non-turbo mode), an EP312 or EP324 device enters standby mode if no logic transitions occur for 100 ns after the last transition.
(9) For EP312 devices: parameter measured with device configured as one 12-bit counter.
For EP324 devices: parameter measured with device configured as two 12-bit counters.

AC Operating Conditions: EP312 *Note (1)*

Combinatorial Mode			EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
t_{PD1}	Input to non-registered output	C_1 = 35 pF		25		30	20	ns
t_{PD2}	I/O to non-registered output	C_1 = 35 pF		25		30	20	ns
t_{PZX}	Input or I/O to output enable, *Note (3)*	C_1 = 35 pF		25		30	20	ns
t_{PXZ}	Input or I/O to output disable, *Note (3)*	C_1 = 5 pF		25		30	20	ns
t_{PCLR}	Input or I/O to asynchronous reset	C_1 = 35 pF		25		30	20	ns
t_{PSET}	Input or I/O to asynchronous set	C_1 = 35 pF		25		30	20	ns

Synchronous Clock Mode (MacroCells)		EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{MAX}	Maximum frequency (pipelined), no feedback	66		50			MHz
f_{CNT1}	Maximum counter frequency, external feedback	33.3		26.3			MHz
f_{CNT2}	Maximum counter frequency, internal feedback	33.3		28.5			MHz
t_{SU1}	Input or I/O setup time to global clock	15		20		20	ns
t_{SU1}	Input or I/O setup time to global clock	15		20		20	ns
t_{H}	Input or I/O hold time from global clock	0		0		0	ns
t_{CO}	Global clock to output delay		15		18	0	ns
t_{CNT}	Minimum global clock period		30		35	20	ns
t_{CL}	Clock low time	7		9		0	ns
t_{CH}	Clock high time	7		9		0	ns
t_{CP}	Clock period	15		20		0	ns

Synchronous Clock (Input Structure)		EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{MAXI}	Maximum frequency input structure	66		50			MHz
t_{SUIR}	Input register/latch setup time to `ILE/ICLK`	5		5		0	ns
t_{ESUI}	Input latch setup time to `ILE`, *Note (4)*	5		5		0	ns
t_{COI}	`ICLK` to combinatorial output		35		40	20	ns
t_{EOI}	`ILE` up to combinatorial output		35		40	20	ns
t_{HI}	Input hold after falling edge of `ILE/ICLK`	7		10		0	ns
t_{EHI}	Input hold after falling edge of `ILE`	7		10		0	ns
t_{CHI}	`ILE/ICLK` high time	7		9		0	ns
t_{CLI}	`ILE/ICLK` low time	7		9		0	ns
t_{CPI}	Minimum `ICLK` period	15		20		0	ns

Asynchronous Clock Mode (Macrocells)		EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{AMAX}	Maximum frequency (pipelined), no feedback	66		50			MHz
f_{ACNT1}	Maximum counter frequency, external feedback	28.5		23.8			MHz
f_{ACNT2}	Maximum counter frequency, internal feedback	33.3		30			MHz
t_{ASU1}	Input or I/O setup time to asynchronous clock	10		12		20	ns
t_{ASU1}	Input or I/O setup time to asynchronous clock	10		12		20	ns
t_{AH}	Input or I/O hold time from asynchronous clock	5		5		0	ns
t_{ACO}	Asynchronous clock to output delay		25		30	20	ns
t_{ACNT}	Minimum global clock period		30		35	20	ns
t_{ACL}	Asynchronous clock low time	7		9		20	ns
t_{ACH}	Asynchronous clock high time	7		9		20	ns
t_{ACP}	Minimum asynchronous clock period	15		20		20	ns

Asynchronous Clock (Input Structure)		EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{AMAXI}	Maximum frequency input structure	66		50			MHz
t_{ASUIR}	Input register/latch setup time to asynchronous `ILE/ICLK`	0		0		0	ns
t_{AESUI}	Input latch setup time to asynchronous `ILE`, *Note (4)*	0		0		0	ns
t_{ACOI}	Asynchronous `ICLK` to combinatorial output		48		55	20	ns
t_{AEOI}	Asynchronous `ILE` up to combinatorial output		48		55	20	ns
t_{AHI}	Input hold after falling edge of asynchronous `ILE/ICLK`	20		25		20	ns
t_{AEHI}	Input hold after falling edge of asynchronous `ILE`	20		25		0	ns
t_{ACHI}	Asynchronous `ILE/ICLK` high time	7		9		20	ns
t_{ACLI}	Asynchronous `ILE/ICLK` low time	7		9		20	ns
t_{ACPI}	Minimum `ICLK` period	15		20		20	ns

Input Clock to Macrocell Clock		EP312-25		EP312-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
t_{C1C2}	Synchronous `ILE/ICLK` to synchronous macrocell `CLK`		25		30	20	ns
t_{C1C2}	Synchronous `ILE/ICLK` to asynchronous macrocell `CLK`		15		18	20	ns
t_{C1C2}	Asynchronous `ILE/ICLK` to synchronous macrocell `CLK`		35		40	20	ns
t_{C1C2}	Asynchronous `ILE/ICLK` to asynchronous macrocell `CLK`		25		35	20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°$ C to 85° C for industrial use.

(2) If the device is operating in standby mode, increase the time by the amount shown.

(3) The t_{PZX} and t_{PXZ} parameters are measured at ±0.5 V from steady-state voltage that is driven by the specified output load.

(4) This specification must be met to guarantee t_{EOI}. If `ILE` goes high before data is valid, use t_{PD} instead of t_{EOI}.

AC Operating Conditions: EP324 *Note (1)*

Combinatorial Mode			EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
t_{PD1}	Input to non-registered output	C_1 = 35 pF		25		30	20	ns
t_{PD2}	I/O to non-registered output,	C_1 = 35 pF		25		30	20	ns
t_{PZX}	Input or I/O to output enable, *Note (3)*	C_1 = 35 pF		25		30	20	ns
t_{PXZ}	Input or I/O to output disable, *Note (3)*	C_1 = 5 pF		25		30	20	ns
t_{PCLR}	Input or I/O to asynchronous reset	C_1 = 35 pF		25		30	20	ns
t_{PSET}	Input or I/O to asynchronous set	C_1 = 35 pF		25		30	20	ns

Synchronous Clock Mode (Macrocells)		EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{MAX}	Maximum frequency (pipelined), no feedback	66		50			MHz
f_{CNT1}	Maximum counter frequency, external feedback	33.3		25			MHz
f_{CNT2}	Maximum counter frequency, internal feedback	33.3		28.5			MHz
t_{SU1}	Input or I/O setup time to global clock	12.5		20		20	ns
t_{SU1}	Input or I/O setup time to global clock	12		20		20	ns
t_H	Input or I/O hold time from global clock	0		0		0	ns
t_{CO}	Global clock to output delay		17.8		20	0	ns
t_{CNT}	Minimum global clock period		30		35	20	ns
t_{CL}	Clock low time	7		9		0	ns
t_{CH}	Clock high time	7		9		0	ns
t_{CP}	Clock period	15		20		0	ns

Synchronous Clock Mode (Input Structure)		EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{MAXI}	Maximum frequency input structure	66		50			MHz
t_{SUIR}	Input register/latch setup time to `ILE/ICLK`	1		2.5		0	ns
t_{ESUI}	Input latch setup time to `ILE`, *Note (4)*	1		2.5		0	ns
t_{COI}	`ICLK` to combinatorial output		30		35	20	ns
t_{EOI}	`ILE` up to combinatorial output		30		35	20	ns
t_{HI}	Input hold after falling edge of `ILE/ICLK`	8		9		0	ns
t_{EHI}	Input hold after falling edge of `ILE`	7		8		0	ns
t_{CHI}	`ILE/ICLK` high time	7		9		0	ns
t_{CLI}	`ILE/ICLK` low time	7		9		0	ns
t_{CPI}	Minimum `ICLK` period	15		20		0	ns

Asynchronous Clock Mode (Macrocells)		EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{AMAX}	Maximum frequency (pipelined), no feedback	66		50			MHz
f_{ACNT1}	Maximum counter frequency, external feedback	27.7		23.8			MHz
f_{ACNT2}	Maximum counter frequency, internal feedback	33.3		28.5			MHz
t_{ASU1}	Input or I/O setup time to asynchronous clock	11		12		20	ns
t_{ASU1}	Input or I/O setup time to asynchronous clock	11		12		20	ns
t_{AH}	Input or I/O hold time from asynchronous clock	3		4		0	ns
t_{ACO}	Asynchronous clock to output delay		25		30	20	ns
t_{ACNT}	Minimum global clock period		30		35	20	ns
t_{ACL}	Asynchronous clock low time	7		9		20	ns
t_{ACH}	Asynchronous clock high time	7		9		20	ns
t_{ACP}	Minimum asynchronous clock period	15		20		20	ns

Asynchronous Clock Mode (Input Structure)		EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{AMAXI}	Maximum frequency input structure	66		50			MHz
t_{ASUIR}	Input register/latch setup time to asynchronous `ILE/ICLK`	–5		–5		0	ns
t_{AESUI}	Input latch setup time to asynchronous `ILE`, *Note (4)*	–5		–5		0	ns
t_{ACOI}	Asynchronous `ICLK` to combinatorial output		30		35	20	ns
t_{AEOI}	Asynchronous `ILE` up to combinatorial output		30		45	20	ns
t_{AHI}	Input hold after falling edge of asynchronous `ILE/ICLK`	15		18		20	ns
t_{AEHI}	Input hold after falling edge of asynchronous `ILE`	14		17		0	ns
t_{ACHI}	Asynchronous `ILE/ICLK` high time	7		9		20	ns
t_{ACLI}	Asynchronous `ILE/ICLK` low time	7		9		20	ns
t_{ACPI}	Minimum `ICLK` period	15		20		20	ns

Input Clock to Macrocell Clock		EP324-25		EP324-30		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
t_{C1C2}	Synchronous `ILE/ICLK` to synchronous macrocell `CLK`		20		25	20	ns
t_{C1C2}	Synchronous `ILE/ICLK` to asynchronous macrocell `CLK`		12.5		15	20	ns
t_{C1C2}	Asynchronous `ILE/ICLK` to synchronous macrocell `CLK`		40		45	20	ns
t_{C1C2}	Asynchronous `ILE/ICLK` to asynchronous macrocell `CLK`		20		25	20	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.

(2) If the device is operating in standby mode, increase the time by the amount shown.

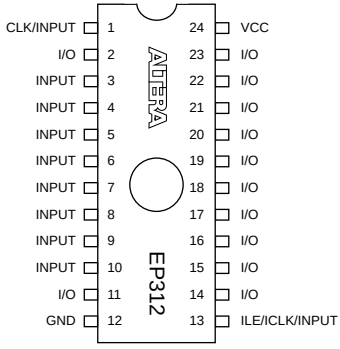
(3) The t_{PZX} and t_{PXZ} parameters are measured at ±0.5 V from steady-state voltage that is driven by the specified output load.

(4) This specification must be met to guarantee t_{EOI}. If `ILE` goes high before the data is valid, use t_{PD} instead of t_{EOI}.

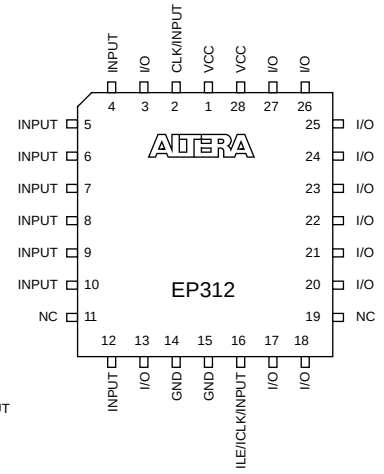
Figure 8 shows the package pin-outs for EP312 and EP324 devices.

Figure 8. EP312 & EP324 Package Pin-Outs

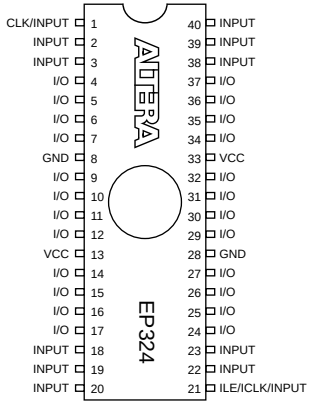
Package outlines not drawn to scale. Windows in ceramic packages only.



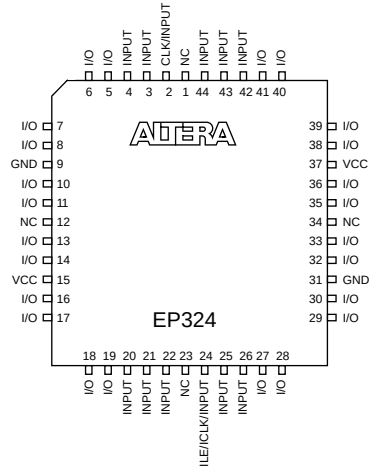
24-Pin DIP



28-Pin J-Lead



40-Pin DIP



44-Pin J-Lead

Package Outlines

Refer to "Altera Device Package Outlines" in the Altera ***Data Book*** for detailed information on packages outlines.

Product Availability

Table 3 gives the availability and ordering codes for EP312 and EP324 devices. Altera will accept Intel product names and ordering codes for Intel devices until June 30, 1995, after which only Altera product names and ordering codes will be accepted.

Table 3. EP312 & EP324 Availability

Device	Temperature Grade	Speed Grade	Package	Altera Ordering Code	Former Intel Ordering Code
EP312	Commercial temperature (0° C to 70° C)	-25	24-pin CerDIP	EP312DC-25	D5AC312-25
		-30	24-pin CerDIP	EP312DC-30	D5AC312-30
		-25	24-pin PDIP	EP312PC-25	P5AC312-25
		-30	24-pin PDIP	EP312PC-30	P5AC312-30
		-25	28-pin PLCC	EP312LC-25	N5AC312-25
	Industrial temperature (–40° C to 85° C)	-30	28-pin PLCC	EP312LI-30	TNAC312-30
EP324	Commercial temperature (0° C to 70° C)	-30	40-pin CerDIP	EP324DC-30	D5AC324-30
		-25	40-pin PDIP	EP324PC-25	P5AC324-25
		-30	40-pin PDIP	EP324PC-30	P5AC324-30
		-25	44-pin PLCC	EP324LC-25	N5AC324-25
		-30	44-pin PLCC	EP324LC-30	N5AC324-30

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