ADVANCED INFORMATION

CY7C1325

256K x 18 Synchronous 3.3V Cache RAM

Features

- Supports 117-MHz microprocessor cache systems with zero wait states
- 256K by 18 common I/O
- Low Standby Power (6.6 mW, L version)
- Fast clock-to-output times
  — 7.5 ns (117MHz version)
- Two-bit wrap-around counter supporting either interleaved or linear burst sequence
- Separate processor and controller address strobes provides direct interface with the processor and external cache controller
- Synchronous self-timed write
- Asynchronous output enable
- I/Os capable of 2.5–3.3V operation
- JEDEC-standard pinout
- 100-pin TQFP packaging
- ZZ "sleep" mode

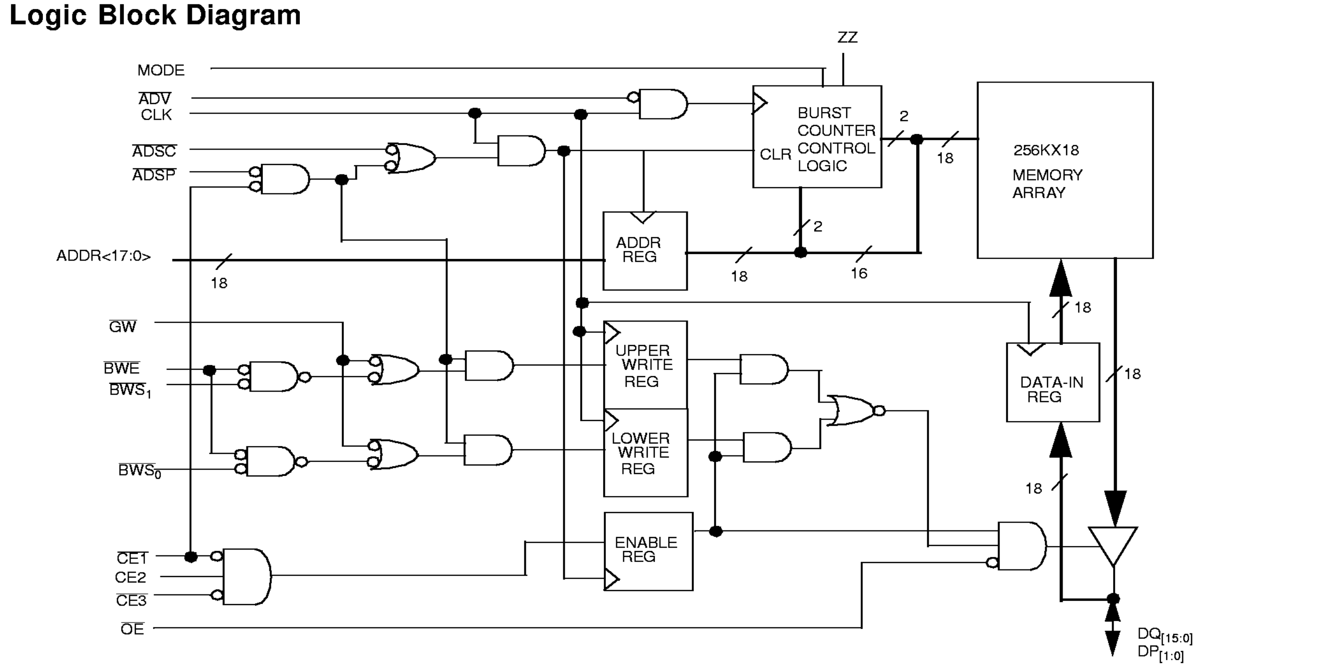
Functional Description

The CY7C1325 is a 3.3V 256K by 18 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 7.5 ns (117-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C1325 allows both an interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip enable input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Selection Guide

	7C1325–117	7C1325–100	7C1325–80	7C1325–50
Maximum Access Time (ns)	7.5	8.0	8.5	11.0
Maximum Operating Current (mA)	350	325	300	250
Maximum Standby Current (mA)	2.0	2.0	2.0	2.0

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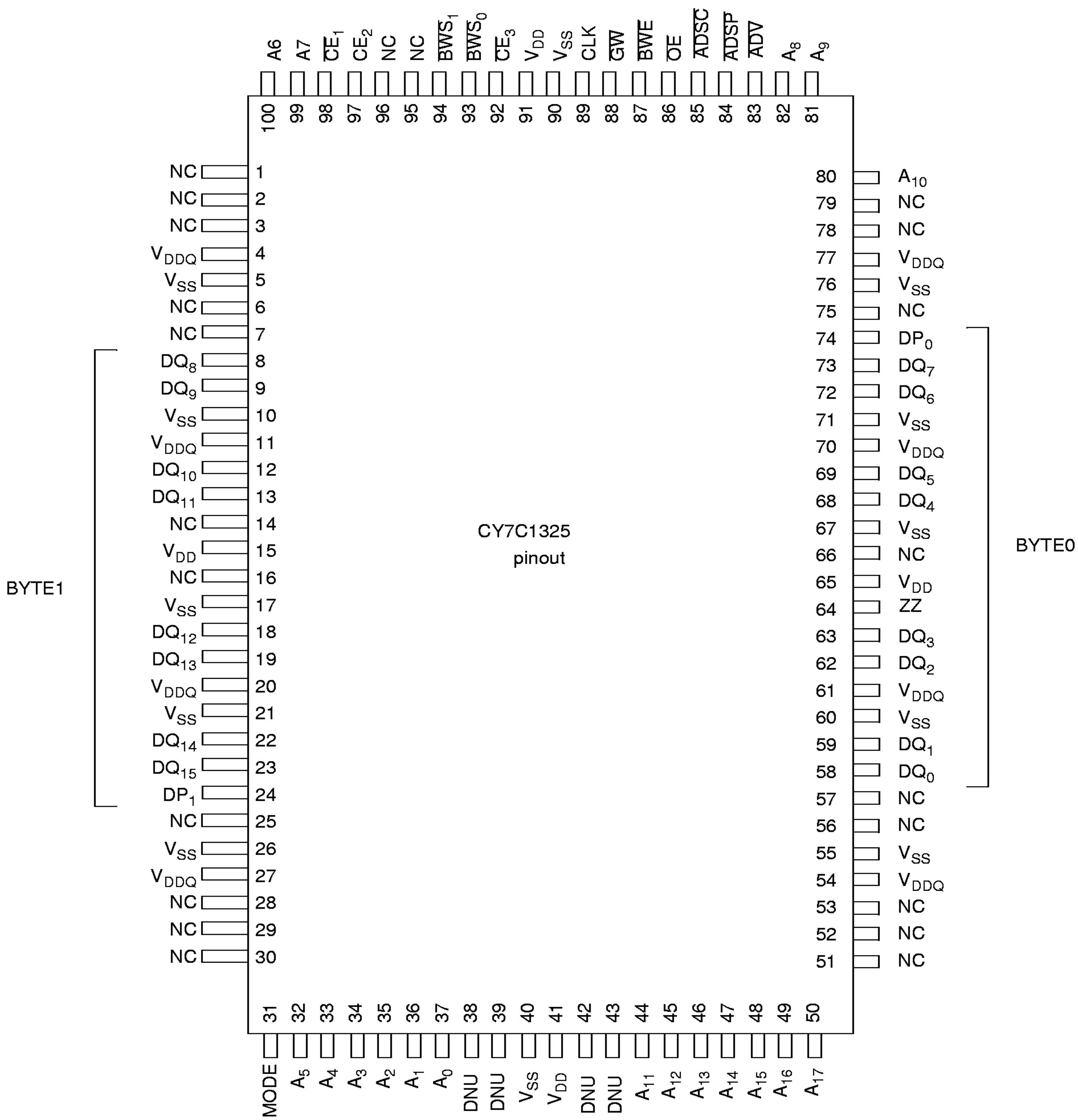
100-Lead TQFP



Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the RAM core. The write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BWS}_{[1:0]}$) are ignored during this first clock cycle. If the write inputs are asserted active (see write table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. Byte writes are allowed. During byte writes, $\overline{BWS}_0$ controls $DQ_{[7:0]}$ and DP_0 while $\overline{BWS}_1$ controls $DQ_{[15:8]}$ and DP_1. All I/Os are three-stated during a byte write. Since these are common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be three-stated prior to the presentation of data to $DQ_{[15:0]}$ and $DP_{[1:0]}$. As a safety precaution, the data lines are three-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) The write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BWS}_{[1:0]}$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register, burst counter/control logic and delivered to the RAM core. The information presented to $DQ_{[15:0]}$ and $DP_{[1:0]}$ will be written into the specified address location. Byte writes are allowed, with $\overline{BWS}_0$ controlling $DQ_{[7:0]}$ and DP_0 while $\overline{BWS}_1$ controlling $DQ_{[15:8]}$ and DP_1. All I/Os are three-stated when a write is detected, even a byte write. Since these are common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be three-stated prior to the presentation of data to $DQ_{[15:0]}$ and $DP_{[1:0]}$. As a safety precaution, the data lines are three-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the Address Register, burst counter /control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data will be available at the data outputs a maximum to T_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE1}$ is HIGH.

Burst Sequences

This family of devices provide a 2-bit wrap around burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

Table 1. Counter Implementation for the Intel Pentium®/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
A_{X+1}, A_x	A_{X+1}, A_x	A_{X+1}, A_x	A_{X+1}, A_x
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
A_{X+1}, A_x	A_{X+1}, A_x	A_{X+1}, A_x	A_{X+1}, A_x
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ HIGH places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Cycle Description Table[1, 2, 3]

Cycle Description	ADD Used	$\overline{CE}_1$	$\overline{CE}_3$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSP}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	HIGH-Z
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L-H	HIGH-Z
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L-H	HIGH-Z
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L-H	HIGH-Z
Deselected Cycle, Power-down	None	X	X	X	L	H	L	X	X	X	L-H	HIGH-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	HIGH-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	HIGH-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	HIGH-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	HIGH-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	HIGH-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	HIGH-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	HIGH-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:

1. X=Don't Care, 1=Logic HIGH, 0=Logic LOW.
2. The SRAM always initiates a read cycle when $\overline{ADSP}$ asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BWS}_{[1:0]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three– state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
3. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. During a read cycle DQ=HIGH–Z when $\overline{OE}$ is inactive, and DQ=data when $\overline{OE}$ is active

Pin Descriptions

TQFP Pin Number	Name	I/O	Description
85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[17:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, $A_{[17:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
36, 37	$A_{[1:0]}$	Input-Synchronous	A_1, A_0 address inputs, These inputs feed the on-chip burst counter as the LSBs as well as being used to access a particular memory location in the memory array.
50–44, 80–82, 99, 100, 32–35	$A_{[17:2]}$	Input-Synchronous	Address Inputs used in conjunction with $A_{[1:0]}$ to select one of the 256K address locations. Sampled at the rising edge of the CLK, if $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active, and $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW.

Pin Descriptions (continued)

94, 93	$\overline{BWS}_{[1:0]}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes. Sampled on the rising edge. $\overline{BWS}_0$ controls $DQ_{[7:0]}$ and DP_0, $\overline{BWS}_1$ controls $DQ_{[15:8]}$ and DP_1. See write table for further details.
83	$\overline{ADV}$	Input-Synchronous	Advance input used to advance the on-chip address counter. When LOW the internal burst counter is advanced in a burst sequence. The burst sequence is selected using the MODE input.
87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
88	$\overline{GW}$	Input-Synchronous	Global Write Input, active LOW. Sampled on the rising edge of CLK. This signal is used to conduct a global write, independent of the state of $\overline{BWE}$ and $\overline{BWS}_{[1:0]}$. Global writes override byte writes.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device.
98	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$, to select/deselect the device. $\overline{CE}_1$ gates $\overline{ADSP}$.
97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
64	ZZ	Input-Asynchronous	Snooze input. Active HIGH asynchronous. When HIGH, the device enters a low power standby mode in which all other inputs are ignored, but the data in the memory array is maintained.Leaving ZZ floating or NC will default the device into an active state.
31	MODE	-	Mode input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. When left floating or NC, defaults to interleaved burst order.
23, 22, 19, 18, 13, 12, 9, 8, 73, 72, 69, 68, 63, 62, 59, 58	$DQ_{[15:0]}$	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ in conjunction with the internal control logic. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $DQ_{[15:0]}$ and $DP_{[1:0]}$ are placed in a three-state condition. The outputs are automatically three-stated when a WRITE cycle is detected.
74, 24	$DP_{[1:0]}$	I/O-Synchronous	Bidirectional Data Parity lines. These behave identical to $DQ_{[15:0]}$ described above. These signals can be used as parity bits for bytes 0 and 1 respectively.
15, 41, 65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5 or 3.3V power supply.
1–3, 6, 7, 14, 16, 25, 28-30, 51–53, 56, 57, 66, 75, 78, 79, 95–96	NC	-	No connects.
38, 39, 42, 43	DNU	-	Do not use pins. Should be left unconnected or tied LOW.

Write Cycle Descriptions[1,2,3,4]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWS}_1$	$\overline{BWS}_0$
Read	1	1	X	X
Read	1	0	1	1
Write Byte 0-$DQ_{[7:0]}$ and DP_0	1	0	1	0
Write Byte 1-$DQ_{[15:8]}$ and DP_1	1	0	0	1
Write All Bytes	1	0	0	0
Write All Bytes	0	X	X	X

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		10	mA
I_{DDZZ} (L Version)	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		2	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied ....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND................–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[5]...–0.5V to V_{DD} + 0.5V

DC Input Voltage[5]..–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature[6]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.135V to 3.6V	2.375V to V_{DD}

Notes:
4. When a write cycle is detected, all I/Os are three-stated, even during byte writes.
5. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
6. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1325 Min.	7C1325 Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{DDQ} = 3.3V$, V_{DD} = Min., I_{OH}=–4.0 mA		2.4		V
		$V_{DDQ} = 2.5V$, V_{DD} = Min., I_{OH}=–2.0 mA		1.7		V
V_{OL}	Output LOW Voltage	$V_{DDQ} = 3.3V$, V_{DD} = Min., I_{OL}=8.0 mA			0.4	V
		$V_{DDQ} = 2.5V$, V_{DD} = Min., I_{OL}=2.0 mA			0.7	V
V_{IH}	Input HIGH Voltage			1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[5]			–0.3	0.8	V
I_X	Input Load Current (except ZZ and MODE)	GND ≤ V_I ≤ V_{DDQ}		–1	1	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DDQ}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DDQ}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DD,}$ Output Disabled		–5	5	µA
I_{OS}	Output Short Circuit Current[7]	V_{DD}=Max., V_{OUT}=GND			–300	mA
I_{DD}	V_{DD} Operating Supply Current	V_{DD}=Max., Iout=0mA, f=f_{MAX} =1/t_{CYC}.	8.5 ns cycle, 117 MHz		350	mA
			10 ns cycle, 100 MHz		325	mA
			11 ns cycle, 90 MHz		300	mA
			20 ns cycle,50 MHz		250	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs switching	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}, inputs switching	8.5 ns cycle, 117 MHz		125	mA
			10 ns cycle, 100 MHz		110	mA
			11 ns cycle, 90 MHz		100	mA
			20 ns cycle,50 MHz		75	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs static	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DD}$ –0.3V or V_{IN} ≤ 0.3V, f=0, inputs static	Std version -All speeds		10	mA
			L version -All speeds		2	mA
I_{SB3}	Automatic CE Power-Down Current—CMOS Inputs switching, F=Max	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DDQ}$– 0.3V or V_{IN} ≤ 0.3V, f=$f_{MAX,}$ inputs switching	8.5 ns cycle, 117 MHz		95	mA
			10 ns cycle, 100MHz		85	mA
			11 ns cycle, 90MHz		70	mA
			20 ns cycle,50MHz		60	mA
I_{SB4}	Automatic CE Power-Down Current — CMOS Inputs static, F=Max	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DD}$ –0.3V or V_{IN} ≤ 0.3V, f=f_{MAX}, inputs static	8.5 ns cycle, 117 MHz		60	mA
			10 ns cycle, 100MHz		50	mA
			11 ns cycle, 90MHz		40	mA
			20 ns cycle,50MHz		35	mA

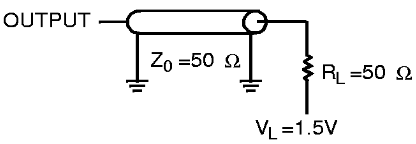
Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V	5.0	pF
$C_{I/O}$	I/O Capacitance		8.0	pF

Notes:

7. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms



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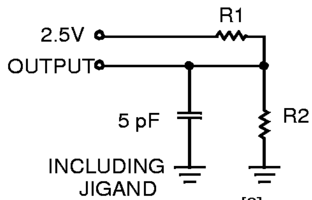

(b)[9]

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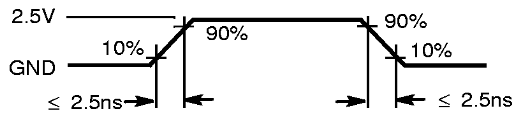

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Switching Characteristics Over the Operating Range[10]

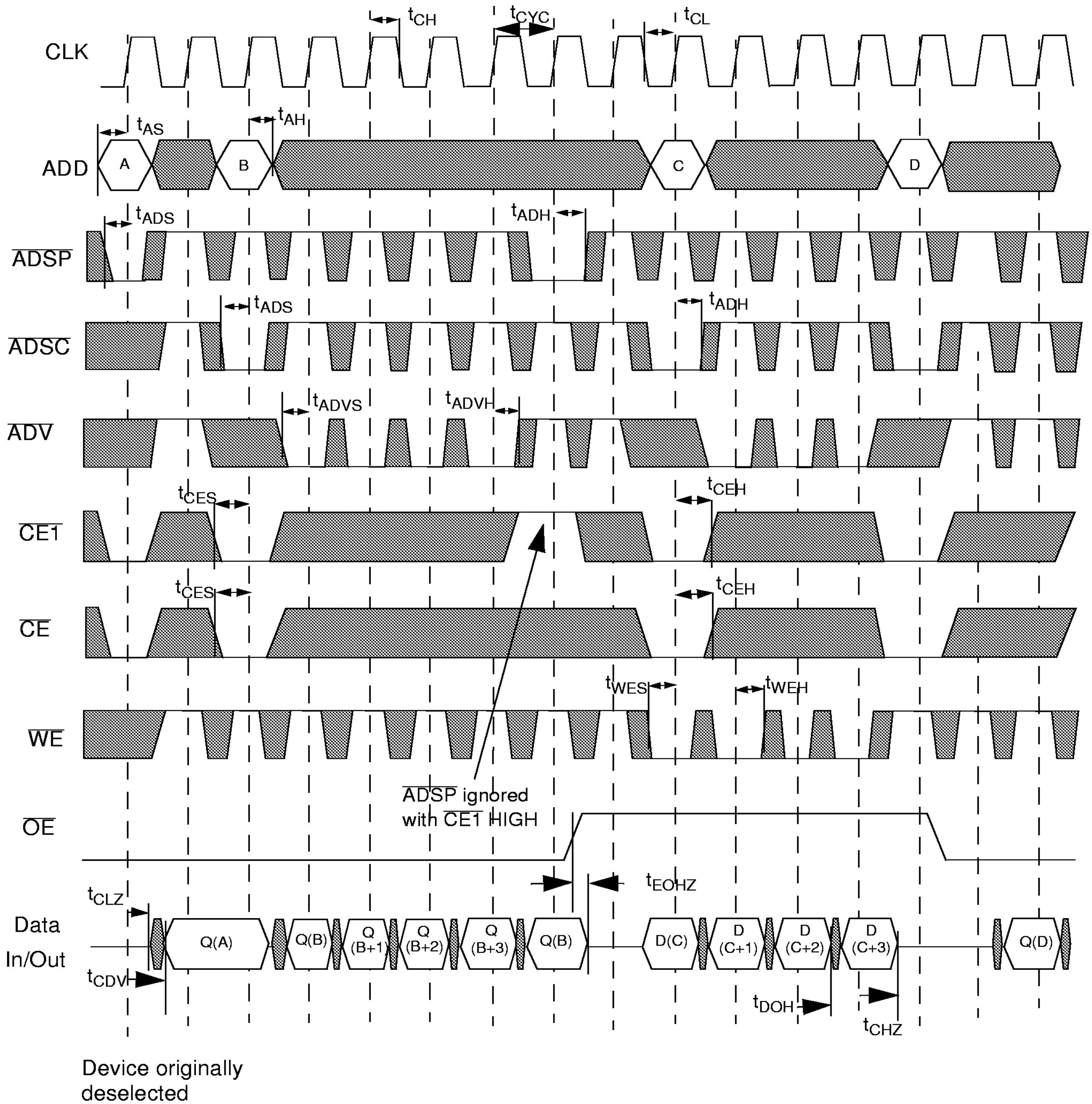
Parameter	Description	-117		-100		-90		-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	8.5		10		11		20		ns
t_{CH}	Clock HIGH	3.0		4.0		4.5		4.5		ns
t_{CL}	Clock LOW	3.0		4.0		4.5		4.5		ns
t_{AS}	Address Set-Up Before CLK Rise	2.0		2.0		2.0		2.0		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		7.5		8.0		8.5		11.0	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		2.0		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.0		2.0		2.0		2.0		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{WES}	$\overline{BWS}_{[1:0]}$, $\overline{GW}$,$\overline{BWE}$ Set-Up Before CLK Rise	2.0		2.0		2.0		2.0		ns
t_{WEH}	$\overline{BWS}_{[1:0]}$, $\overline{GW}$,$\overline{BWE}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.0		2.0		2.0		2.0		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.0		2.0		2.0		2.0		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CES}	Chip Enable Set-Up	2.0		2.0		2.0		2.0		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[11,12]		3.5		3.5		3.5		3.5	ns
t_{CLZ}	Clock to Low-Z[11,12]	0		0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[11,13]		3.5		3.5		3.5		3.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[11,13]	0		0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		3.5		3.5		3.5		3.5	ns

Notes:

9. R1=1667Ω and R2=1538Ω for IOH/IOL=–4/8mA, R1=521Ω and R2=481Ω for IOH/IOL=–2/2mA.
10. Unless otherwise noted, test conditions assume signal transition time of 2.5ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
11. t_{CHZ}, t_{CLZ}, t_{EOHZ}, and t_{EOLZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
12. At any given voltage and temperature, t_{CHZ} (max) is less than t_{CLZ} (min).
13. This parameter is sampled and not 100% tested.

Timing Diagrams

READ/WRITETiming

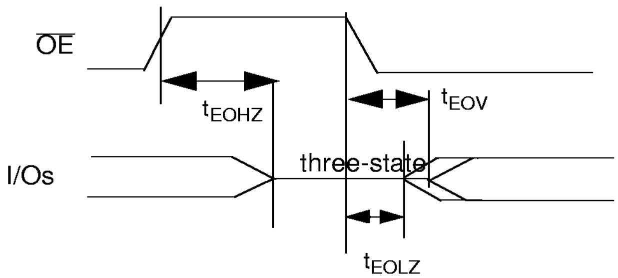


$\overline{WE}$ is the combination of $\overline{BWE}$, $\overline{BWS}_{[1:0]}$ and $\overline{GW}$ to define a write cycle (see write cycle definition table).
$\overline{CE}$ is the combination of CE_2 and $\overline{CE}_3$. All chip selects need to be active in order to select the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in X, Qx stands for Data-out X

= DON'T CARE = UNDEFINED

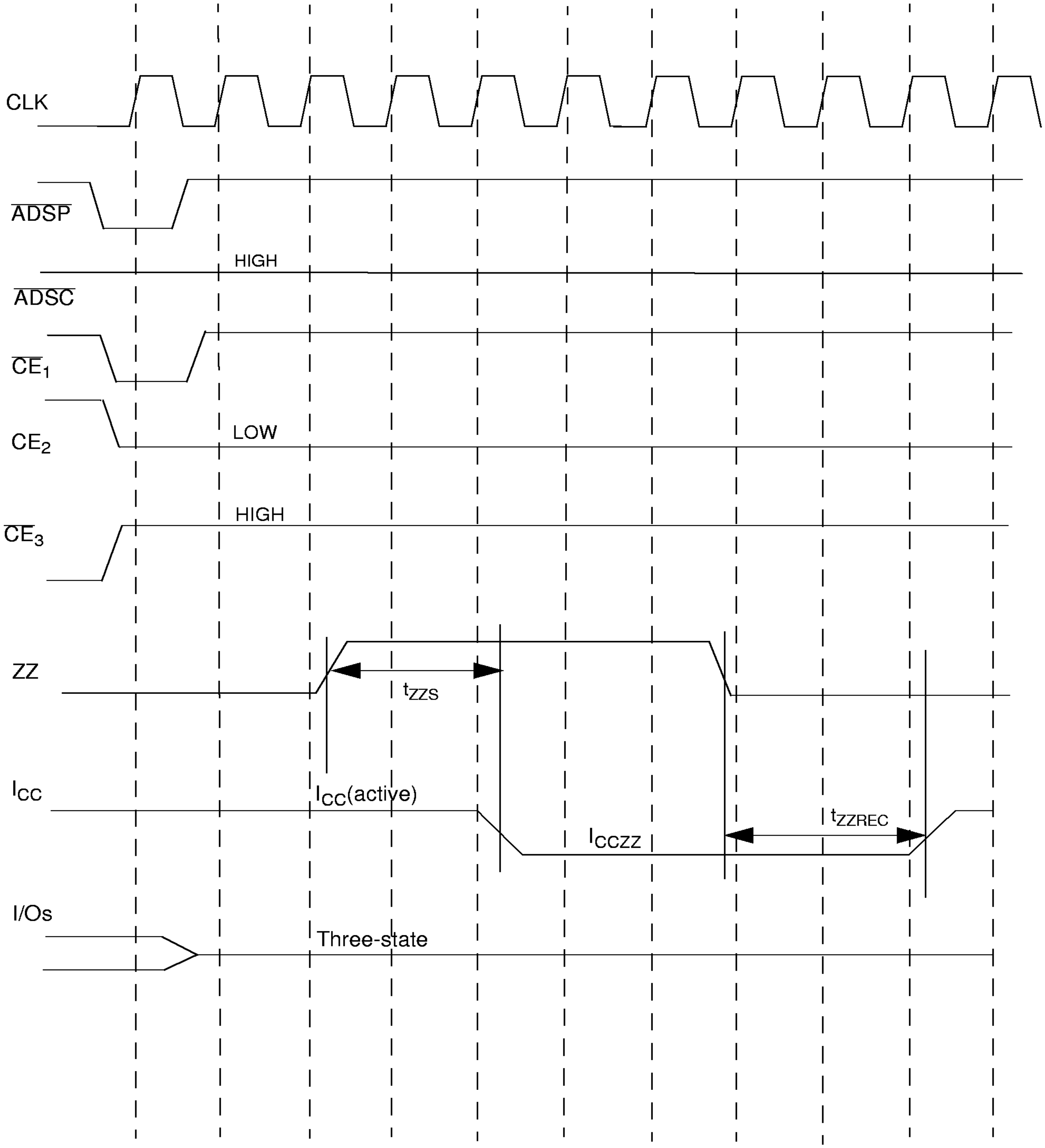
Timing Diagrams (continued)

$\overline{OE}$ Switching Waveforms



Timing Diagrams (continued)

ZZ Mode Timing [14,15]



Notes:

14. Device must be deselected when entering ZZ mode. See Cycle description for all possible signal conditions to deselect the device.
15. I/Os are in three-state when exiting ZZ sleep mode.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
117	CY7C1325–117AC	A101	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1325L–117AC	A101	100-Lead Thin Quad Flat Pack	Commercial
100	CY7C1325–100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
100	CY7C1325L–100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
80	CY7C1325–80AC	A101	100-Lead Thin Quad Flat Pack	Commercial
80	CY7C1325L–80AC	A101	100-Lead Thin Quad Flat Pack	Commercial
50	CY7C1325–50AC	A101	100-Lead Thin Quad Flat Pack	Commercial
50	CY7C1325L–50AC	A101	100-Lead Thin Quad Flat Pack	Commercial

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Package Diagram

100-Pin Plastic Thin Quad Flat Pack (TQFP) A101