National Semiconductor

DM77/87SR27
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR27 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

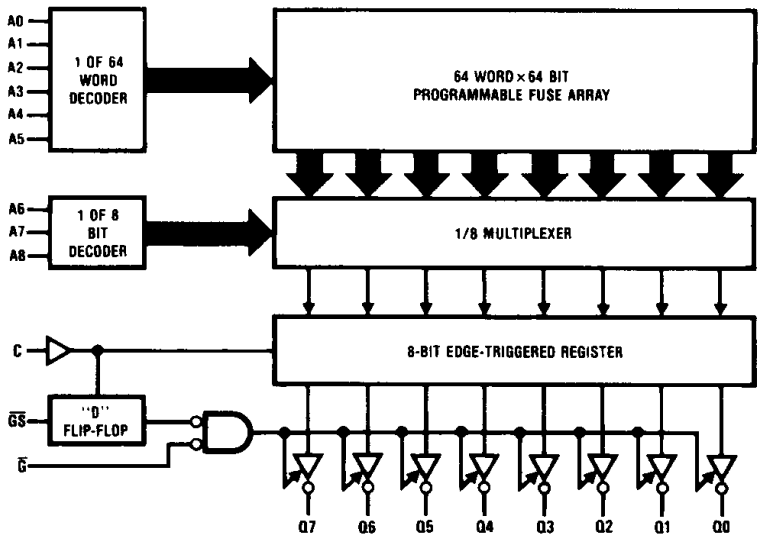
Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with Am27S27
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 22-pin 400-mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



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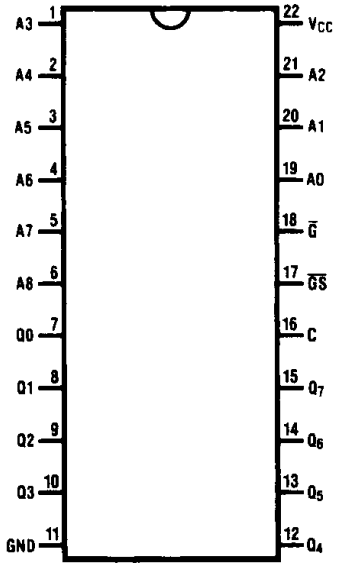
Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM77/87SR27J, DM77/87SR27BJ, DM87SR27N or DM87SR27BN
See NS Package Number J22A or N22A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM87SR27BJ	35
DM87SR27J	50
DM87SR27BN	35
DM87SR27N	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM77SR27BJ	40
DM77SR27J	55

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	−0.5V to +7.0V
Input Voltage (Note 1)	−1.2V to +5.5V
Output Voltage (Note 1)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operations should be limited to those conditions specified under DC Electrical Characteristics.

Operating Conditions

Supply Voltage (V_{CC})	
Military	4.5V to 5.5V
Commercial	4.75V to 5.25V
Ambient Temperature (T_A)	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Logical "0" Input Voltage	0V to 0.8V
Logical "1" Input Voltage	2.0V to 5.5V

DC Electrical Characteristics T_A = 25°C, V_{CC} = 5.0V unless otherwise specified

Symbol	Parameter	Test Conditions	DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR27	55	20		50	20		ns
		SR27B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR27		15	30		15	27	ns
		SR27B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		25	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Programming Parameters Do not test or you may program the device

Symbol	Parameter	Test Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current While Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4	4.2	V
V_{CCVH}	Required High V_{CC} for Verification		5.8	6	6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Functional Description

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

Functional Description (Continued)

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

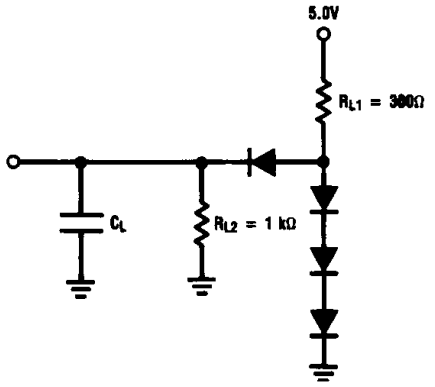
DM77/87SR27 Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at ambient temperatures between 15 and 30 degrees Celsius.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedures must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. Synchronous chip Enable $\overline{GS}$ should be held low throughout the entire programming procedure.
   b) Increase V_{CC} from nominal 10.5V (±0.5V) with a slew rate between 1.0 V/μs and 10 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 V/μs to 10 V/μs. This voltage may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time.)
   d) Enable the device by taking the chip Enable $\overline{G}$ to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through e for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enable device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

AC Test Load



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